



Exploring PADS PCB Design Solutions

PADS Tutorial with PADS Logic

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Table of Contents

| | | |
|-----------|--|-----------|
| 1 | Introduction | 3 |
| 2 | The PADS Evaluation Circuit | 4 |
| 3 | System Design with PADS Logic..... | 5 |
| 3.1 | PADS Logic Schematic Editor | 5 |
| 3.2 | Environment Options | 7 |
| 3.3 | Sheet Setup | 8 |
| 3.4 | Title Blocks | 9 |
| 3.5 | Hotkeys and Mouse Operation | 10 |
| 3.6 | Project Explorer | 10 |
| 3.7 | The Library Manager | 11 |
| 3.8 | Schematic Design Creation | 13 |
| 3.9 | Add Parts and Wire Schematic | 14 |
| 3.10 | Saving the Schematic..... | 17 |
| 4 | PADS Design Rules and Constraints..... | 18 |
| 4.1 | Assign Net Constraints | 21 |
| 4.2 | Intelligent PDF (option)..... | 23 |
| 5 | PCB Design with PADS Layout..... | 24 |
| 5.1 | Quick Filter | 26 |
| 5.2 | Project Explorer | 26 |
| 5.3 | Board Outline Creation | 27 |
| 5.4 | Footprint Creation using the Symbol Wizard..... | 28 |
| 5.5 | PADS Layout Link / PADS Router Link | 32 |
| 5.6 | Component placement | 34 |
| 5.7 | Vias..... | 35 |
| 5.8 | Layer Setup | 36 |
| 5.9 | Passing the Design to PADS Router..... | 38 |
| 6 | Introduction to PADS Routing Solutions..... | 39 |
| 6.1 | Constraint Assignment/Review | 40 |
| 6.2 | Interactive, high-speed routing environment | 41 |
| 6.3 | PADS AutoRouter..... | 45 |
| 6.4 | Create Copper Pour in PADS Layout..... | 48 |
| 6.5 | Design verification | 50 |
| 6.6 | CAM Outputs | 51 |
| 7 | Other PADS Layout Highlights | 56 |
| 7.1 | Automation | 56 |
| 7.2 | Attribute support | 56 |
| 8 | Other PADS Options | 57 |
| 8.1 | Design For Fabrication (DFF) Audit | 57 |
| 8.2 | Testpoint Creation and Checking (DFT Audit option) | 57 |
| 8.3 | Physical Design Reuse (PDR)..... | 58 |
| 8.4 | Advanced Packaging And COB Toolkit..... | 58 |
| 8.5 | Assembly Variants..... | 58 |
| 8.6 | Mechanical Data Import/Export | 59 |
| 9 | PADS Layout Keyboard Shortcut Commands | 60 |
| 10 | Default Non-Electrical Layer Assignment..... | 61 |

1 Introduction

Welcome to the *PADS Tutorial*. Using this tutorial, you can quickly and easily explore the PADS environment— from schematic capture to PCB layout, interactive and automatic routing, and CAM outputs.

This tour of the PADS products should take a morning or an afternoon, though you may want to spend more time to review other educational material available with PADS, and visit the PADS website at Mentor Graphics, <http://www.mentor.com/products/pcb/pads>.

In the PADS evaluation process, you can view any size file. However, the files you can save are limited to 30 components, 65 nets, and 150 connections.

To order PADS software or to find a distributor near you, please visit <http://www.mentor.com/products/pcb/pads/resellers/index.cfm>.

2 The PADS Evaluation Circuit

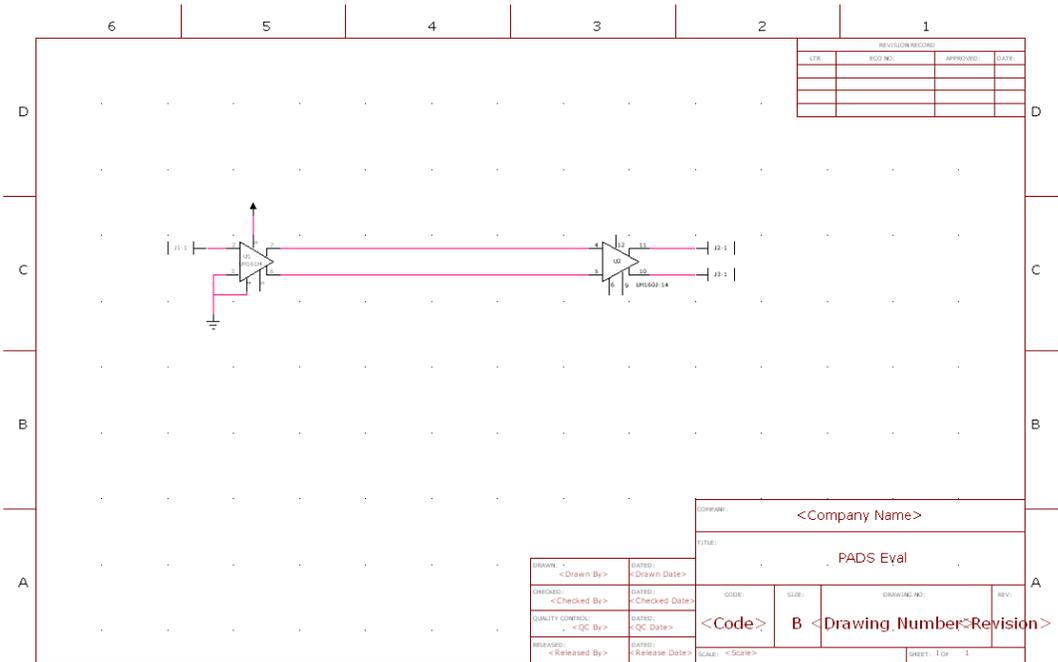
The circuit shown below will be used to introduce you to the PADS design flow. To save time, the design is available in various stages of development. If you find you are pressed for time, you can open one of the partially finished versions for usage with the exercises. The files can be found in C:\PADS Projects\Samples.

Schematic

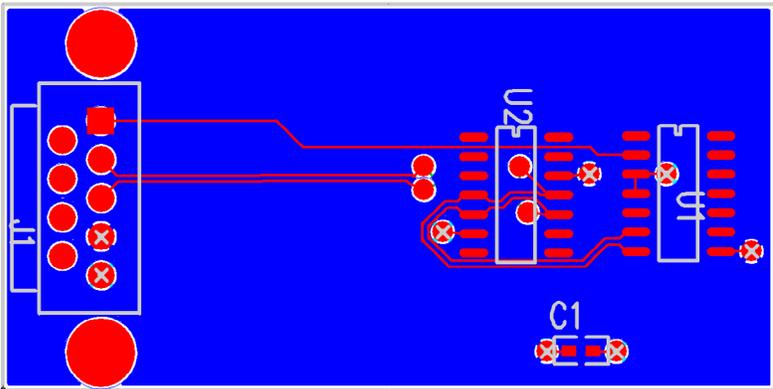
- Sch_Eval_Blank.sch
- Sch_Eval_Start.sch
- Sch_Eval_Partial.sch
- Sch_Eval_Done.sch

Layout

- Layout_Eval_Outline.pcb
- Layout_Eval_PrePlaced.pcb
- Layout_Eval_Placed.pcb
- Layout_Eval_Routed.pcb
- Layout_Eval_Done.pcb



Sch_Eval_Done.sch

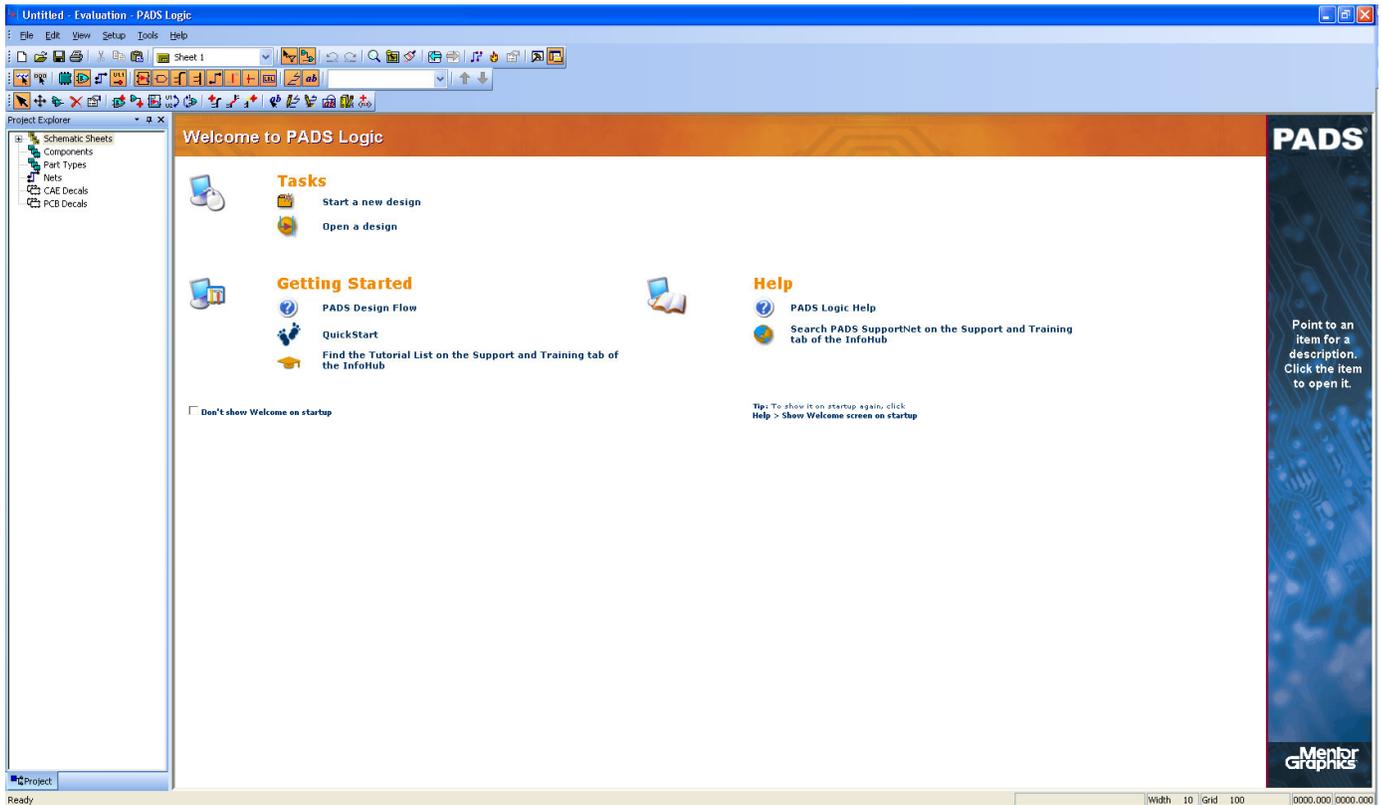


Layout_Eval_Done.pcb

Open a schematic.

1. Click **Start > Programs > Mentor Graphics SDD > <PADS_Release> > Design Entry > PADS Logic** to start PADS Logic.

The PADS Logic Welcome Screen opens.



2. Click **File > Open** or **Open a design** from the Welcome Screen.

Browse to **C:\PADS Projects\Samples** and double-click PREVIEW.SCH.

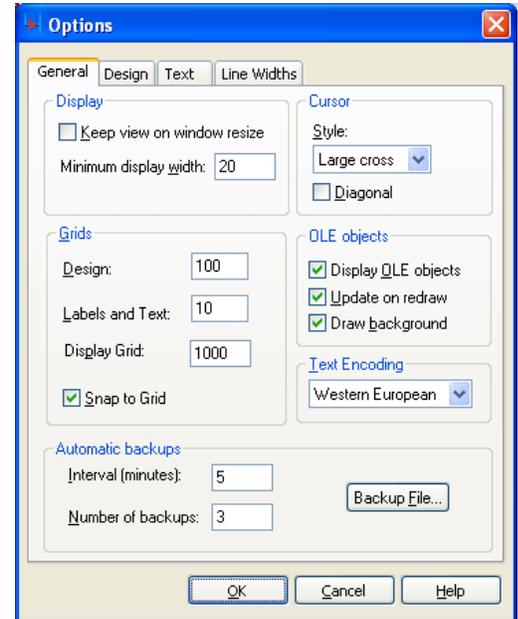
3.2 Environment Options

PADS Logic provides you with a number of default system options, including, among others:

- Sheet size
- Sheet backup/save interval
- Cursor size
- Text size

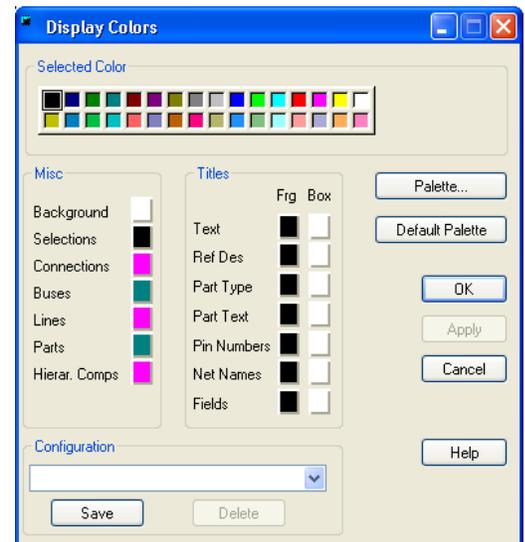
Explore environment settings.

1. Click **Tools > Options**.
Try changing cursor style.
Note various settings.
Click **OK** to exit.



Assign a different background color to sheet.

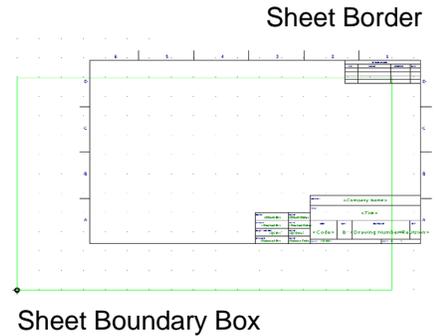
1. Click **Setup > Display Colors**. The Display Colors dialog box opens.
2. Click the color square you want.
3. Click the Background square in the Misc area.
4. Click **OK** when you are done.



3.3 Sheet Setup

PADS Logic uses a *boundary box* (working area displayed as a rectangular box) and a “sheet border”. Because the boundary box defines what will be printed, all sheet borders, title blocks, and parts must be within this space. To change the sheet size, you must change both the boundary box size and the sheet size.

- Sheet preferences are controlled within a single, intuitive menu.
- System sheet borders are stored in the “Common” library.

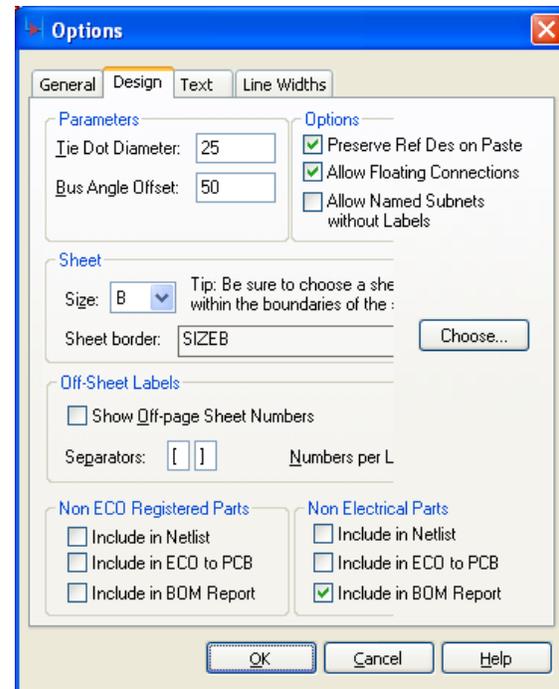


Selecting a B-size sheet border.

1. Click **Tools > Options**. The Options dialog box opens.
2. Select the **Design** tab.
3. Verify that **B** is selected from the Size list.
4. Click **Choose**. Scroll down to select the **common: SIZE B** sheet.

Click **OK**. The sheet border changes.

5. Click **OK** to close the Options dialog box.
6. Click the **Home <sheet >** button (or press **Home**) to zoom to the full sheet.



3.4 Title Blocks

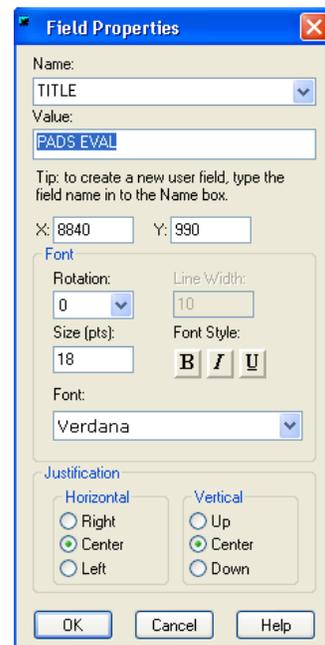
You can create and store title blocks as library elements with or without sheet borders. Within the title block, you also can automatically update and propagate text fields, such as sheet name, number, or customizable fields such as *Company Name*, and *Checked by*, which are propagated through the rest of the design.

Title blocks:

- Can be part of a sheet border or a separate library item.
- Contain “smart fields” which update name, page, and other information to all sheets in a design.

Select and modify any title block field.

1. Right-click anywhere on the sheet, and click **Select Drafting Items**.
2. Double-click any title block field to modify.
For example, double-click <Title >.



3.5 Hotkeys and Mouse Operation

PADS Logic offers several ways to pan, zoom, and scroll. You can use the menus, keyboard, mouse, or any combination of these to navigate through your schematics.

With the keyboard, you can:



- **Zoom In** (Page Up)
- **Zoom Out** (Page Down)
- **Zoom to Full sheet** (Home)
- **Center on cursor** (Insert)

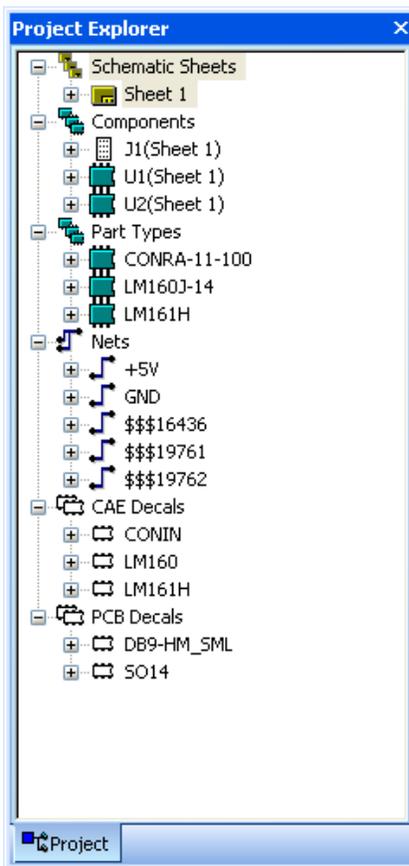
With the mouse, you can:



- **Pan Up/Down** (Mouse wheel)
- **Pan Left/Right** (SHIFT/Mouse wheel)
- **Zoom In/Out** (Ctrl/Mouse wheel)

3.6 Project Explorer

The Project Explorer enables you to use a familiar Windows style Explorer tree to browse through objects in the design project such as sheets, parts, pins, nets, and help.



3.7 The Library Manager

The Library Manager is the means to set up and use your libraries.

You can:

- View, add, edit, delete, libraries and library part attributes.
- Set a specific library search order.
- Filter items by name and type.
- View from both PADS Logic and PADS Layout.

PADS libraries:

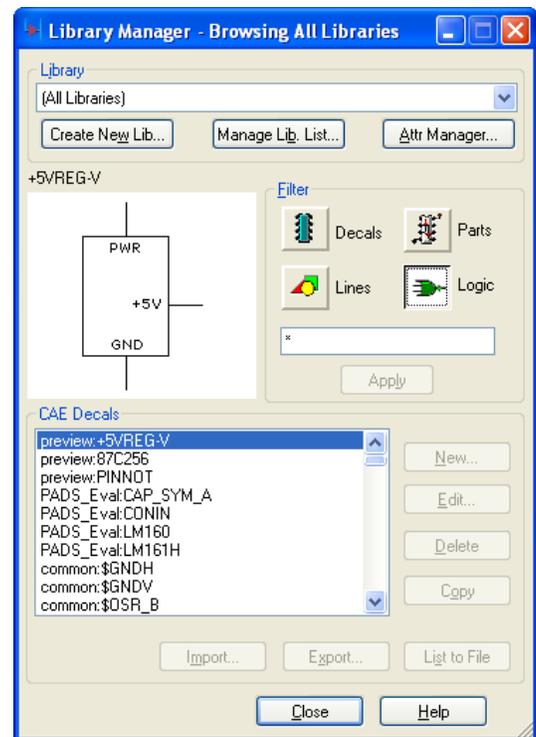
- Are shared by both PADS Logic and PADS Layout.
- Store parts with different information stored in 4 separate files.

The .pt file holds pointers to the schematic symbol and PCB footprint symbol information.

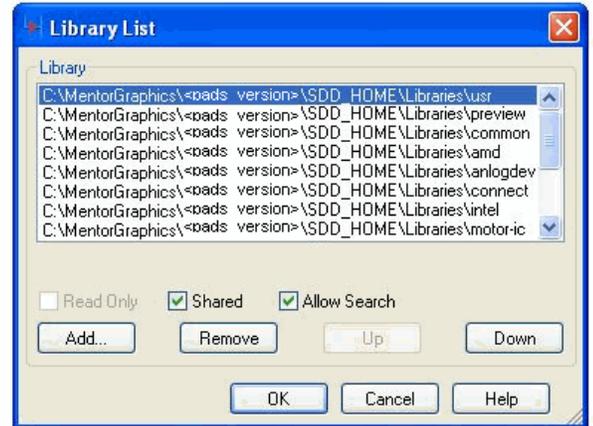
A part listed in the library contains information stored as attributes, and pointers to graphical elements such as schematic symbol(s) and library layout footprints. These are graphically represented in Logic or Layout respectively.

Add the PADS Eval library to the library list and view parts.

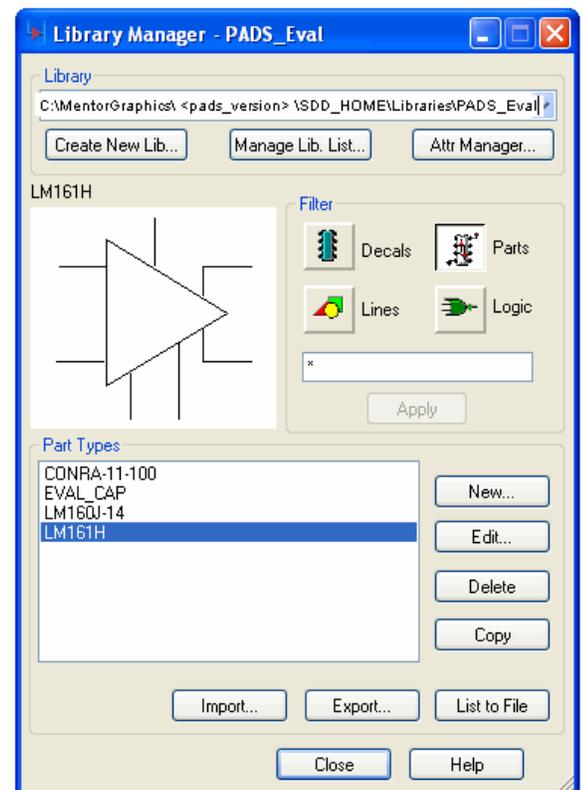
1. Click **File > Library** to open the Library Manager
2. Click **Manage Lib. List**.



- In the Library List dialog box, click **Add**.
- In the Add Library dialog box, browse to and select the **PADS_Eval.pt*** library in the following folder:
C:\MentorGraphics\9.0PADS\SDD_HOME\Libraries
- Click **Open** to add the library to the library list.
Tip: Any library can be re-positioned in the search order list using the Up or Down buttons.
- In the Library List dialog box, click **OK**.



- In the Library Manager dialog box, Select the PADS_Eval library from the **Library** list.
- Click the **Parts** button.
- Type * in the Filter box and click **Apply**
- Try partial names using *, ? characters
- The parts used for the evaluation design are listed here.



View a part's properties, including attributes, PCB decals, and Signal Pins.

- In the schematic, right-click in a blank area and click **Select Parts**.
- Select any part and click **Edit > Properties** from the main menu to view the part's properties.
- Click **Close** to exit the Part Properties dialog box
- Click **Close** to exit the Library Manager dialog box.

3.9 Add Parts and Wire Schematic

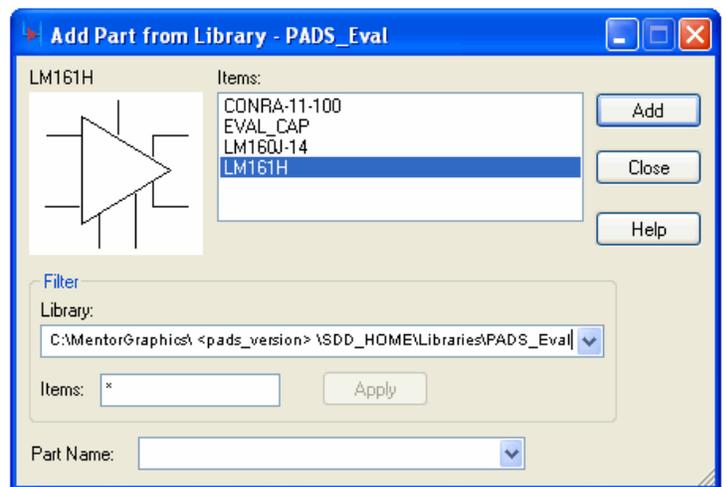
PADS Logic has remained very popular over the years thanks in part to its simplicity in operation. Here are some key editing features including some new functionality:

- Parts can be imported from library or copied/created from existing parts in the schematic.
- Reference Designators automatically assigned during placement.
- Net name visibility can be toggled on/off.
- Auto-wire feature (connection created by touching pins and dragging comps apart)
- Wires can be left terminated or un-terminated

Placing and wiring following parts from library: **CONRA-11-100, LM161H**



1. Click the **Add Part** button to open the Add Part from Library dialog box.
2. Select the PADS_Eval library from the Filter **Library** pulldown arrow.
3. Enter an asterisk into the Items box, click **Apply**
4. Select **LM161H**, click **Add**, then move cursor into the open sheet area. Click to place down on the sheet.
Tip: The reference designators are automatically assigned.
5. Repeat for the **CONRA-11-100**.
6. Press **Esc** to exit mode.
7. Select **Close** button.

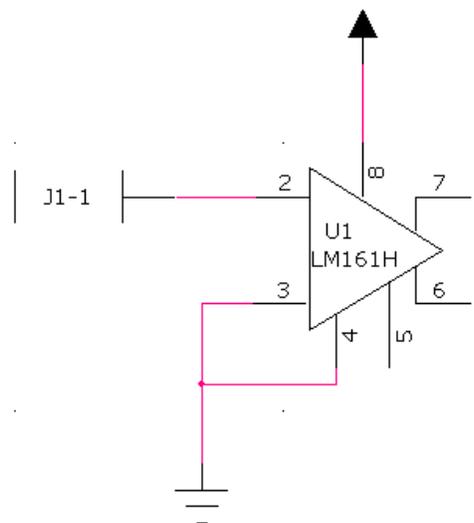


Tip: Press **Page Up** to zoom in at the cursor, and **Page Down** to zoom out at the cursor.

Wiring parts with power and ground connections.



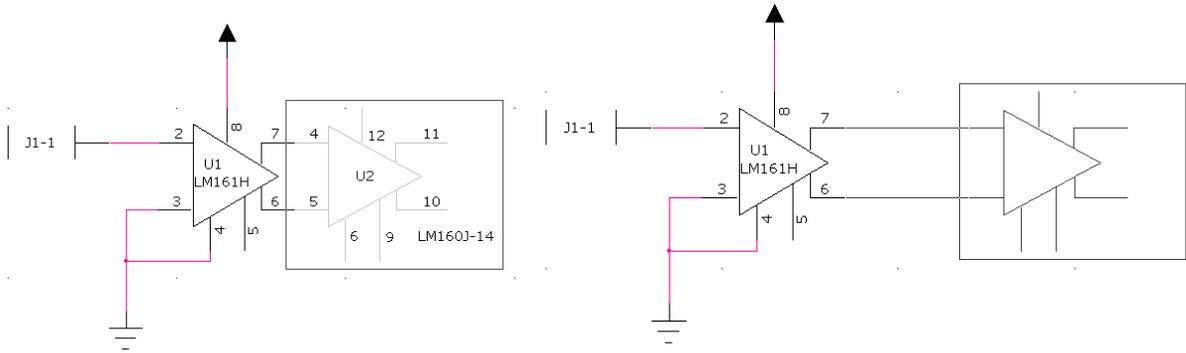
1. Wiring the connector to the input pin. Click the **Add Connection** button. Click to place a wire from J1-1 of **CONRA-11-100** to pin 2 of the **LM161H**
2. Wiring the power pin. Click to start the wire on pin 8, move upwards, then right-click and click **Power**. Click to place the symbol on sheet.
Tip: Click to add a corner to a connection you're making; Backspace to remove the last corner you made.
3. Repeat for **Ground** for pin 3 and 4 to ground net as shown.
Note that you may select alternate power and ground symbols using the **Alternate** command in the right click menu.



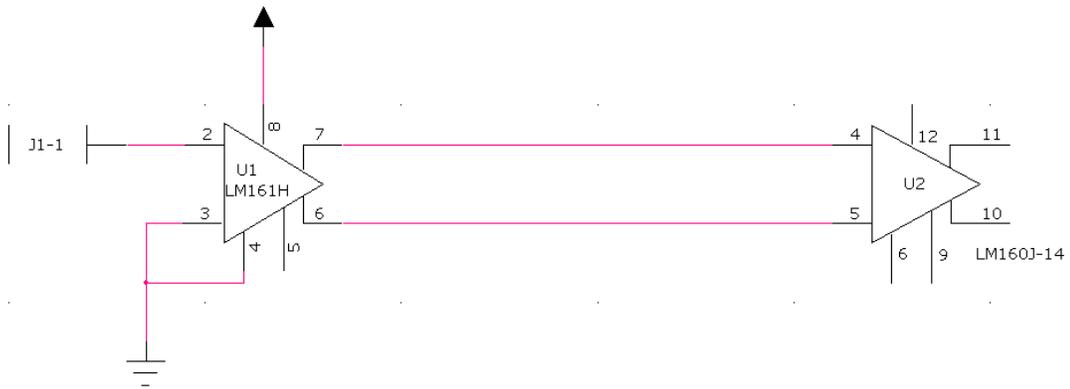
Using the automatic pin-wire feature.



1. Click the **Add Part** button to open the Add Part dialog box.
2. Fetch the **LM160J-14** from the library.
3. Using the **Selection** tool, position the **LM160J-14** input pins to touch the **LM161H** output pins as shown. Click to set down on the sheet. Press Esc to cancel the Add Part command.



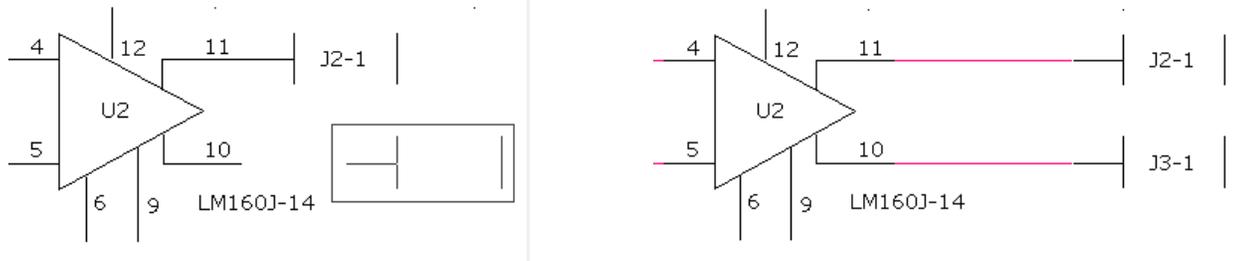
4. Now click and drag the **LM160J-14** to the right, and click again to locate the part. It will end up looking like this:



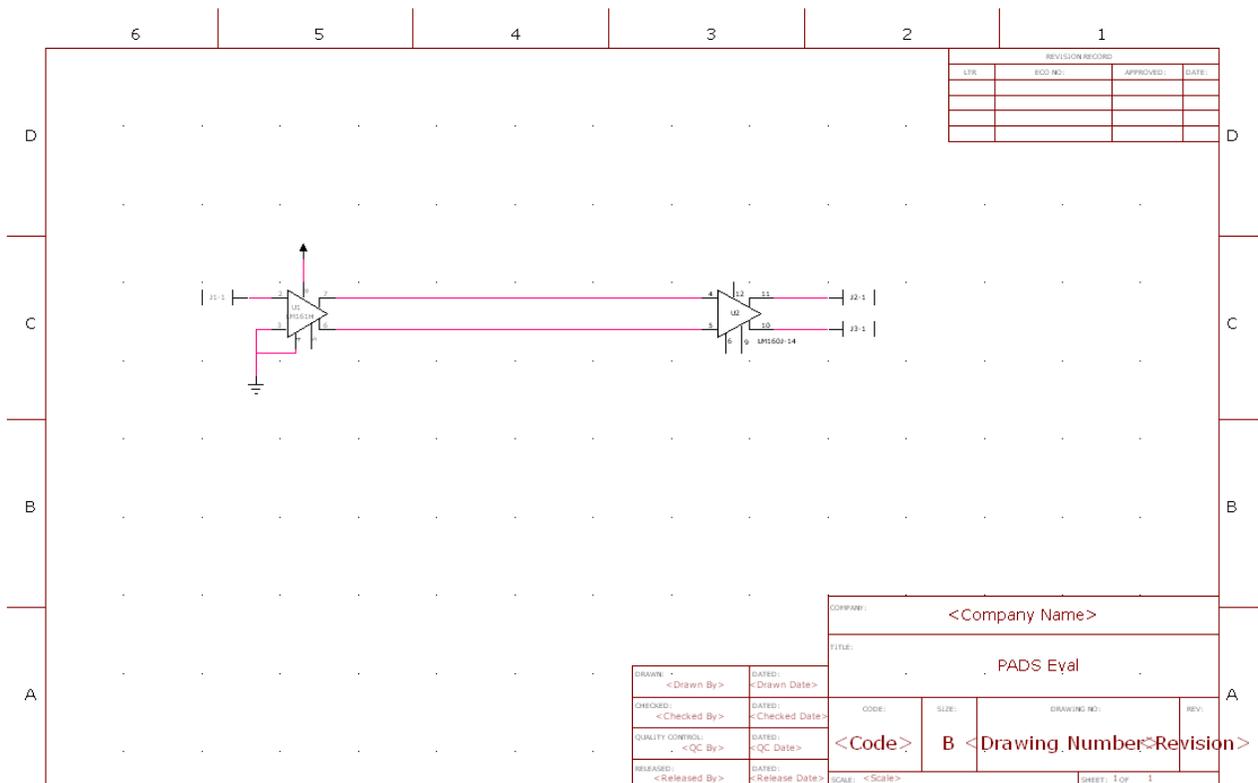
Creating parts from a part already on the sheet.



1. Click on an open space in the schematic to unselect the **LM160J-14**.
2. Right-click and click **Select Gates**.
3. Click the **Selection** button.
4. Click **J1-1 (CONTRA-11-100)**.
5. Right-click and click **Copy**.
6. Right-click and click **Paste**. A new connector snaps to your pointer.
7. Right-click and click **X Mirror**, then place the connector directly touching pin 11 of the **LM160J** as shown.
8. Press **Esc** to end mode.
9. Right-click and click **Paste** to attach another connector to the pin 10.
10. Now drag the components to the right.
11. Try creating a duplicate of U1 or U2. A new part is created, with a new reference designator assigned automatically. Select this part press **Delete** to delete it, as it is not needed.



Now the schematic will look like this:



Name nets:

1. Right-click and click **Connections**.
2. Click the connection between pin 11 of the **LM160J-14** and the **CONRA-11-100**.
3. Right-click and click **Properties**. The Net Properties dialog box opens.
4. Change the net name to **OUT_DATA_NEG**.
5. Click **Net Name Label**, then Click **OK**. The new name of the connection is visible on the schematic.
6. Repeat steps 2-4 to change the name of the connection between pin 10 of the **LM160J-14** and the **CONRA-11-100** to **OUT_DATA_POS**.

3.10 Saving the Schematic

Schematics are saved by default as binary files but can also be saved as ASCII.

Saved schematics are:

- Single, self-contained files – easy to transport, copy.
- Files that carry ALL part information/graphics.

Save schematic

1. Select **File > Save As ...**
2. Name it **Eval_1.sch** (or any name that you want).

4 PADS Design Rules and Constraints

PADS power and popularity owes in part to it's advanced, hierarchical design rule structure.

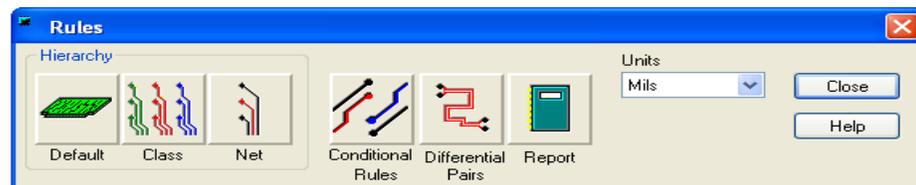
Design rules are stored in schematic and PCB design files. Design rules you setup in PADS Logic are automatically transferred when you import the netlist into PADS Layout. Design rules you setup in PADS Layout are automatically available when opening the design in PADS Router.

Design rules:

- Save time and virtually eliminate human error due to miscommunication between engineer and designer, i.e. they ...
- Allow the *engineer* to tag critical nets
- Allow the *designer* to maintain absolute design control
- Enable you to specify design rule priority
- Can be set so designs are not over-constrained, thus easier to route
- Can be assigned in either PADS Logic or PADS Layout
- Are carried in the design.
- *Extended* rules (high speed, e.g. differential pair rules) are optional.

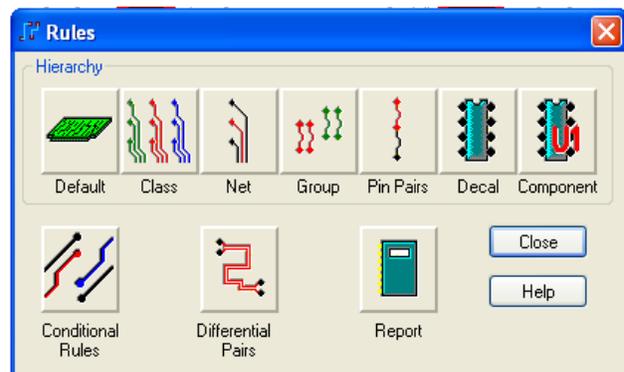
Review PADS Logic and PADS Layout design rules menus.

1. In PADS Logic, select **Setup > Design Rules**.
PADS Logic supports default, class, and net rules, as well as Conditional and Differential Pair rules can be assigned.



PADS Logic Rules Menu

2. In PADS Layout, select **Setup > Design Rules**.
PADS Layout provides *additional* rule control for Group, Pin Pairs, Decal, Component.



PADS Layout Rules Menu

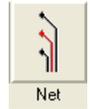
Rules Hierarchy



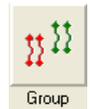
Rules apply to all objects in the design



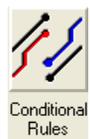
Overrides Default rules. Rules apply to groups of nets defined as a single constraint. Highly efficient method of defining constraints across similar nets. *(Optional)*



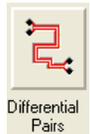
Overrides Class, Default rules. Rules apply to individual signals.



Overrides Class, Default, Net rules. Rules apply to a collection of pin pairs. *(Optional)*



Define “what If” rules between objects. Ex:
- Class A against class B
- Net(s) against a layer (force trace width to change automatically as a trace is routed from layer to layer)
(Optional)



Diff pair length, min/max, gap constraints. Can be assigned to nets, classes. *(Optional)*



Applies fanout/spacing/pad entry constraints to package types. Ex: Assigning smaller line widths on fine pitch parts so traces can exit the part without creating violations.



Applies packaging constraints for individual parts.

Rule Categories



Clearance

Clearances for trace, package body, drill;
Trace width settings



Routing

Trace topology, copper-sharing, protect/push and shove controls, layer biasing,
maximum # of vias



High
Speed

Min/max rules for parallelism, matched length, delay, capacitance which are
then viewed in a report.
(Optional)



Fanout

SMD pad patterns - alignment, direction, length, via spacing.



Pad Entry

Location and angles for pad-to-trace intersections. Placing vias on SMD pads.

4.1 Assign Net Constraints

A crucial element to PADS methodology is the concept of net *constraints*. Constraints are special conditional rules applied to objects such as critical traces, and are adhered to by the interactive or autorouter, as well as by the design rule checking routines.

Constraints can be crucial in the design of high speed PCBs.

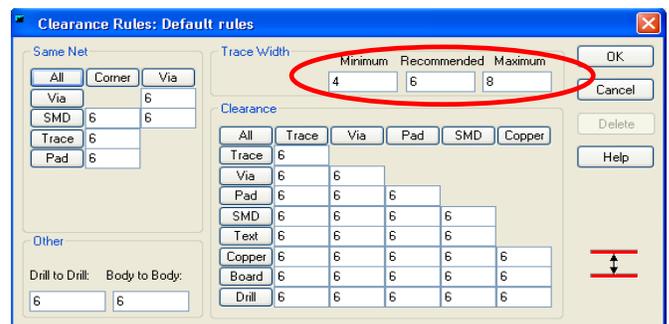
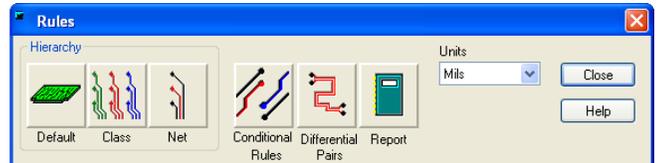
With constraints, you can:

- Apply design parameters to a hierarchy of design objects (default, class, group, etc.)
- Tag critical nets as differential pairs, min/max and matched lengths.
- Be sure constraints travel with the schematic database.
- Assign quickly through easy-to-use dialogs.

Assign default trace widths min/typ/max as 4/6/8 respectively. Also, assign two signals as differential pairs, with a min length of 1000 mils and a max length of 4000 mils. The signals are listed under **Nets** in **Project Explorer** as follows:

| Netnames | Constraints |
|-------------------------------|---|
| OUT_DATA_NEG, OUT_DATA_POS | Diff pair; min. length=1000 mils, max. length=4000 mils |

1. In Logic, click **Setup > Design Rules**.
2. Click the **Default** button, then the **Clearance** button.
3. Set trace widths as depicted.
4. Click **OK** to exit the Clearance Rules dialog box.
5. Click **Close** to exit Default Rules dialog box.



6. In the **Rules** dialog box, click **Differential Pairs**
7. Use the Select and Add buttons to select the **OUT_DATA_NEG** and **OUT_DATA_POS** nets in the **Available** list and move them to the **Pairs** list:
 - a. Select one of the nets and click a **Select >>** button.
 - b. Select the other net and click the other **Select >>** button.
 - c. Click the **Add >>** button.

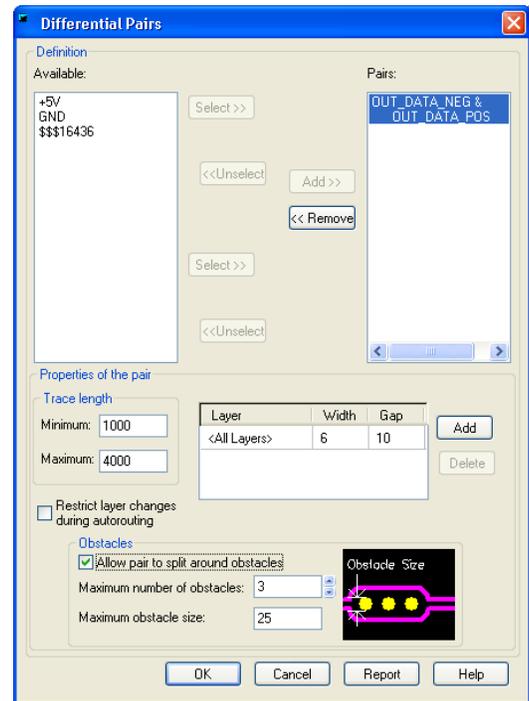
8. Set parameters as shown.

Trace length

Minimum **1000**
Maximum **4000**

Obstacles

Click **Allow pair to split around obstacles**
Type **3** in the Maximum number of obstacles box



9. Click **OK** to exit.
10. Click **Close** in the Rules dialog box.

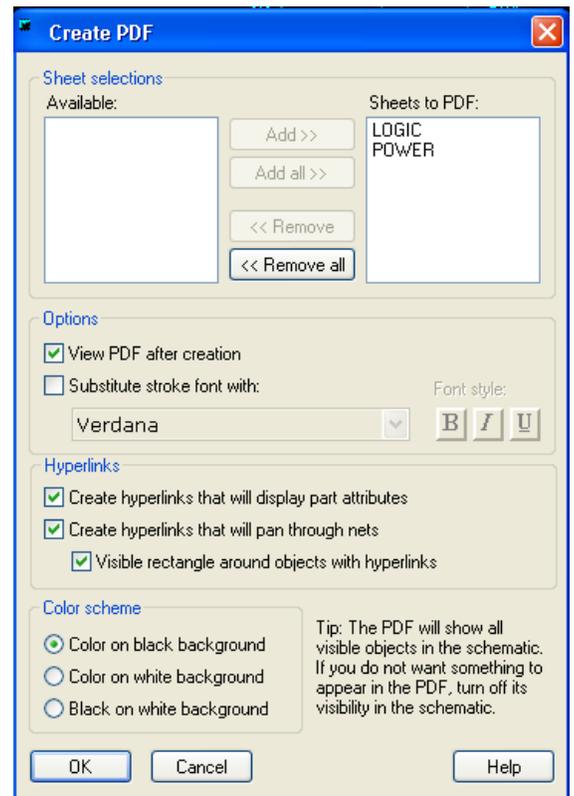
4.2 Intelligent PDF (option)

Intelligent PDF means the ability to view component and net information, even embedded objects right in the PDF document, without PADS Logic. PADS PDF files have significant advantages over standard PDFs:

- View component attribute information.
- Trace nets through the design.
- Great way to distribute read-only design information to non-PADS users.
- Allow embedded OLE objects (spreadsheets, notes).

Generate a PDF schematic.

1. Click **File > Create PDF** from the main menu.
2. Click the **Save** button when you are prompted with an output name.
3. In the Create PDF dialog box, review the available options and click **OK** to generate the PDFs.
4. View the PDFs. Select objects in the pdf file to view attribute information.



5 PCB Design with PADS Layout

Before continuing with the design, we will now review the highlights of PADS Layout – the most trusted name in PCB layout design since 1987 for digital, analog, mixed, RF, COB, MCM.

PADS Layout features:

- Easy-to-use design, placement, manual routing, CAM outputs
- Advanced constraint management
- Communications link between schematic and layout
- Full ECO forward/backward support
- Physical Design Reuse (PDR)
- Advanced Packaging and Chip-On-Board Toolkits
- Split/mixed planes support
- Fabrication Verification (DFF)
- Design For Test (DFT)

PADS Layout users are able to create wireless designs such as cell phones, cell repeater stations, satellite communication, automotive FOBS, and any other RF/Microwave application.

With every seat of PADS Layout you can now:

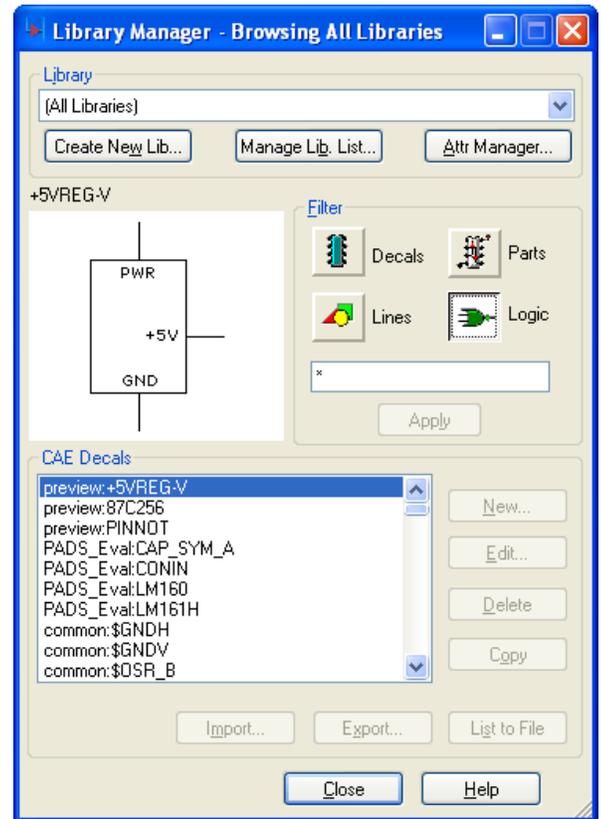
- Import complex copper shapes and line geometries into the Decal Editor
- Shield crucial traces for efficient channel/co-planar waveguide design
- Stitch area with Vias Arrays for complex copper-pour areas with specific pattern requirements
- Provide greater conductivity between planes on different layer
- Minimize noise susceptibility
- Create precise outlines and square & chamfered corner geometry and output them in Gerber

Getting familiar with the PADS Layout environment. Open PADS Layout and view a finished design.

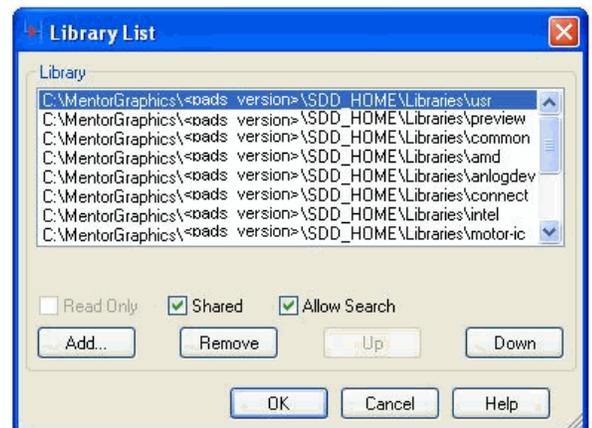
1. Click **Start > Programs > Mentor Graphics SDD > PADS 9.0 > Design Layout & Routing > PADS Layout.**
2. In the Welcome screen, click **Open a design.**
3. Browse to C:\PADS Projects\Samples\Layout_Eval_Done.pcb.

Add the PADS Eval library to the library list.

1. Click **File > Library** to open the Library Manager
2. Click the **Manage Lib. List** button



3. In the Library List dialog box, click the **Add Button**.
4. In the Add Library dialog, browse to and select the **PADS_Eval.pt*** library in the following folder.
C:\MentorGraphics\9.0PADS\SDD_HOME\Libraries
5. Click **Open** to add the library to the library list.
Tip: Any library can be re-positioned in the search order list using the Up or Down buttons.
6. In the Library List dialog box, click **OK**.
7. Click **Close** in the Library Manager.



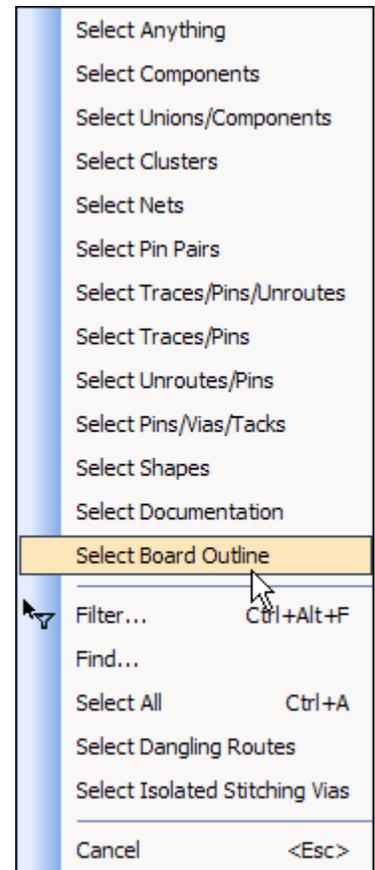
5.1 Quick Filter

The quick filter determines what objects can be selected. It allows selection of objects in very tight areas of overlap (pads, traces, text).

Quickly Filtering

At any time, with nothing selected in the design, you can right-click to show the filter and click to set the selection you want.

Tip: The top item, Select Anything, selects all objects *except* the Board Outline. You must specifically click Select Board Outline to select that object.



5.2 Project Explorer

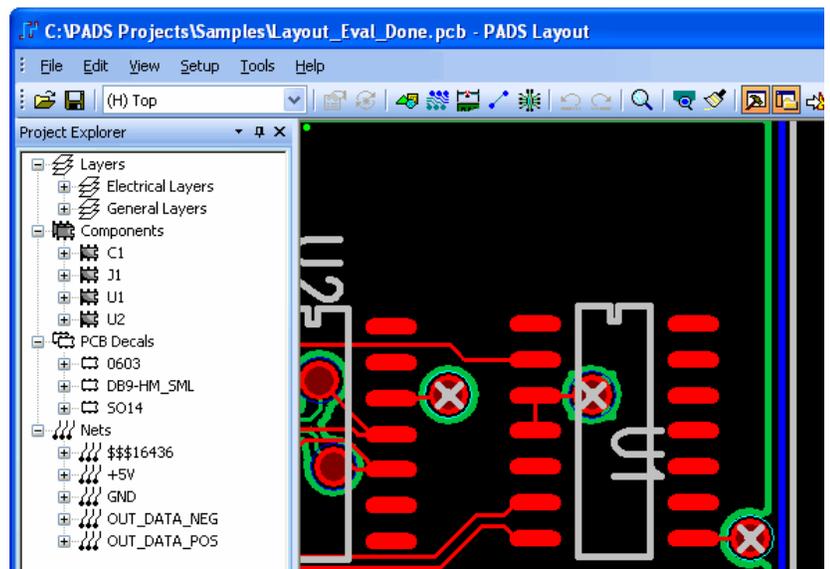
The Project Explorer makes it easy to navigate and query objects in your design. The Project Explorer allows you to:

- Browse layers, trace components, nets, and part decals.
- Zoom to selected objects
- Review design rules, constraints
- Autohide feature

Navigate using Project Explorer

Select an individual object such as a component or PCB decal.

The screen zooms to the first instance of the select object type.



5.3 Board Outline Creation

It is simple to create board outlines in PADS Layout, though you can also import outlines from other drafting packages such as AutoCAD via the DXF/IDF format.

Use the Board Outline and Cutout tool to:

- Create board outlines quickly and efficiently.
- Include board cutout areas, routing/part keepouts.

Tip: You can press the Page Up key to zoom in, the Page Down key to zoom out, or the Insert key to center the view on the cursor location.

Creating simple board outline

1. Click the **Drafting Toolbar** button, , to open the Drafting toolbar.
2. Click the **Board Outline and Cutout** button, .
3. Move the cursor to the design area, right-click and click **Rectangle**.
4. Type **S0 0** (S zero space zero) and press **Enter** to place the pointer at the origin.
5. Press the **Spacebar** to start the rectangle at the design origin.
6. Type **S2000 1000** and press **Enter** to place the pointer at X/Y 2000/1000.
7. Press the **Spacebar** to locate the corner and complete the board outline.
8. Press **Home** to zoom to the board outline.



The PADS Eval Board Outline

Optional: Select the board outline and try the Move and Split options.

Save the PCB Design

- Click the Save button, , and save the file as **Eval_outline.pcb**.

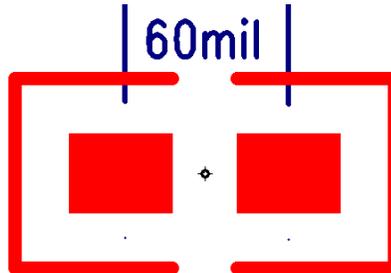
5.4 Footprint Creation using the Symbol Wizard

PADS Layout includes a part PCB decal editor as well as a symbol wizard. The symbol wizard allows you to:

- Create PCB decal (i.e. footprint, land pattern, etc.) quickly and efficiently.
- Automatically create/assign pin information.

Create a 2-pin 0603 CAP footprint, with rectangular pads 30 mil X 38 mils, spaced 60 mils apart center to center. Note that this capacitor will not be used in the evaluation circuit – one of these already exists.

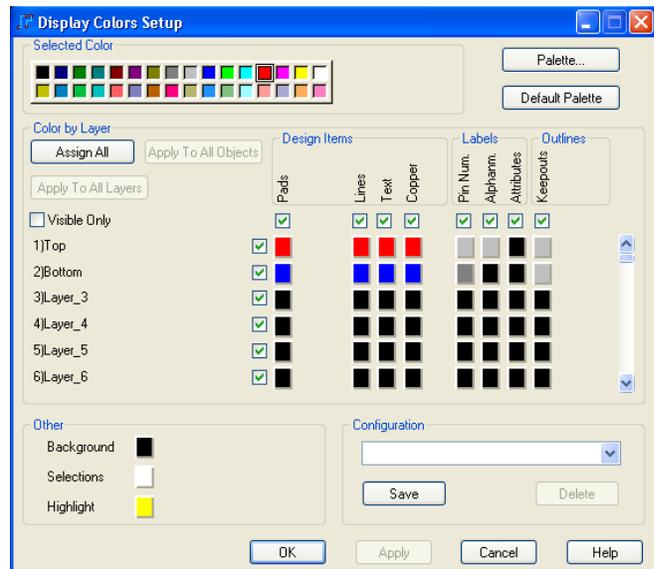
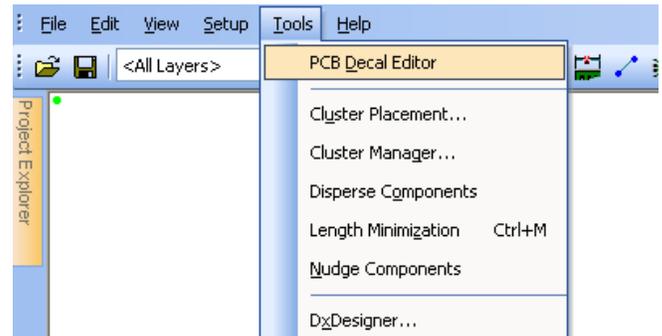
Pads are SMT, 30 X 38 mils rect.,
60 mils centers.



1. Invoke the PCB Decal Editor
Tools > PCB Decal Editor.
2. Review the color/layer scheme
Setup/Display Colors...

Note we will create a surface mount part with pads on the top layer (assigned color red).

Click **OK** to exit.



- In the Decal Editor, click the **Drafting Toolbar** icon.
Pass the cursor over the various tools; note the tooltip labels.



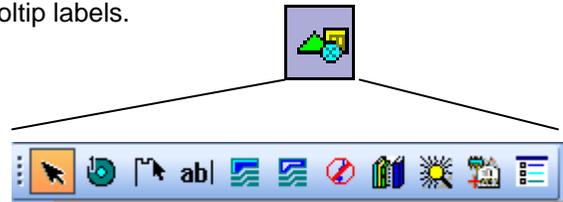
- The leftmost tool is the **Selector** tool.

Other tools/functions include creation of:

- Terminals (pads)
- 2D lines
- Text
- Copper
- Copper cut-out
- Keepouts

... as well as:

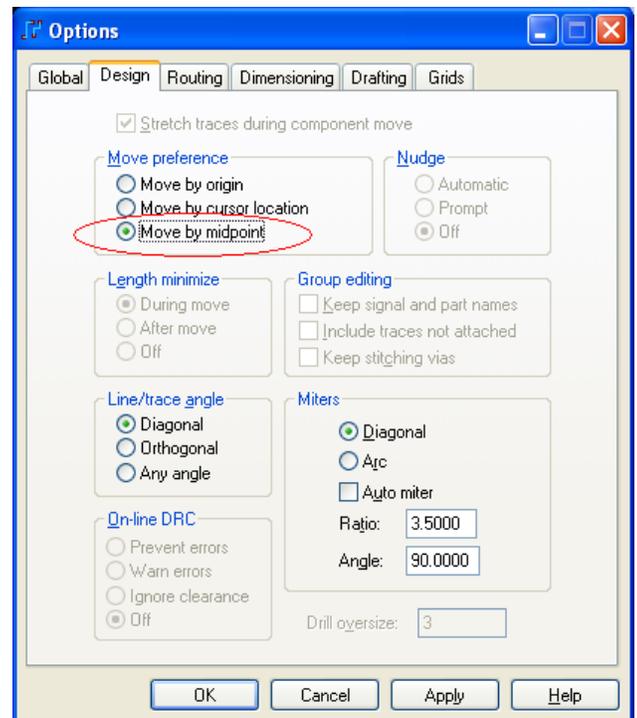
- Retrieve 2D line library objects
- Start Symbol Wizard
- Add label
- Import DXF file
- Set Drafting Options



- Right click select **Select Anything** from the filter. Drag the “Name” and “Type” strings up and to the right, away somewhat from the origin.

- Select **Tools > Options**.

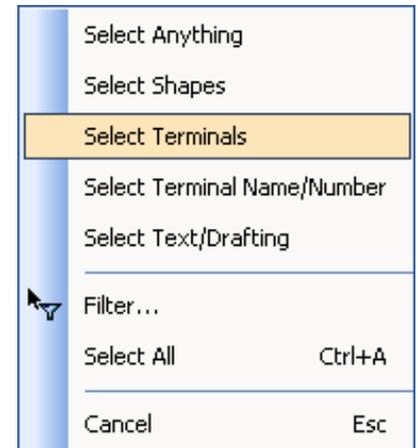
- Select the **Design** tab. Then select **Move by Midpoint** and click **OK**.



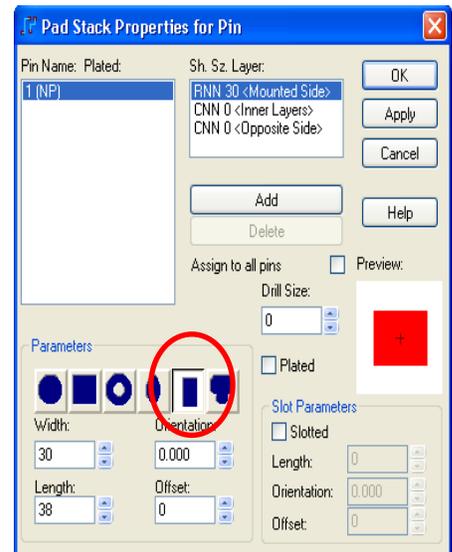
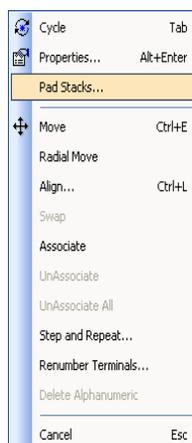
- Select the **Terminal** tool. In the Add Terminals dialog, set up the pin numbering and click OK.

- Left-click anywhere in the design; this deposits a terminal pad. Select the **Selector** tool to exit the **Terminal** tool.

Right-click and choose **Select Terminals** from the filter. Then left-click the terminal to select it.



10. Right-click and select the terminal's **Pad Stacks** opens the **Pad Stack Properties for Pin** dialog box.



11. Update the padstack properties to look like the dialog box above.

Sh. Sz. Layer:

<Mounted Side >

Select **Rectangular** pad shape

Width: **30**

Length: **38**

Orientation: **0**

Offset: **0**

<Inner Layer > set **Diameter** to **0**

<Opposite Side > set **Diameter** to **0**

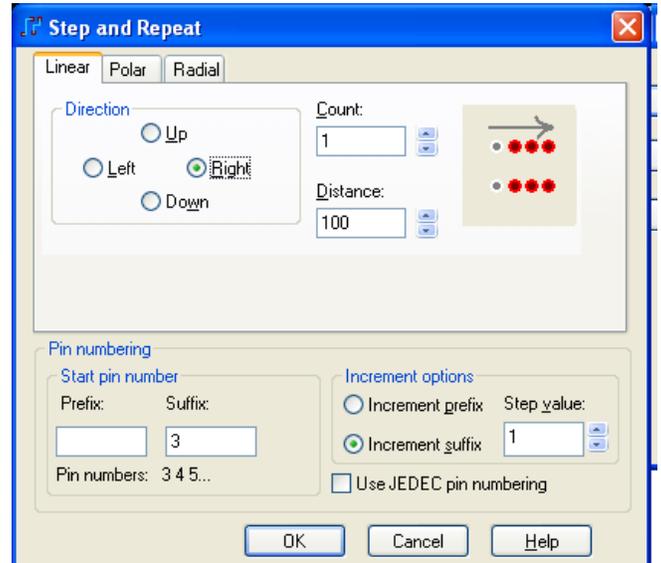
Drill Size: 0 (denotes this as a surface mount pad)

Click **OK** to exit dialog box.

12. Place the terminal 30 mils to the left of the origin.
Left-click on the terminal, then right-click and select **Move**.
Type **S -30 0**
Left-click once to set the pad down.

13. Create and place a second terminal 60 mils to the right using **Step and Repeat**.
Select terminal, then right-click **Step and Repeat**.
14. Leave all defaults, but change Distance to **60** mils; click **OK**.

You should now have two pads centered equally about the part centroid. -



15. Draw a topside silkscreen outline (default layer 26)

To draw any objects you must do two things -

1. Activate and assign a color for the appropriate layer
(use **Setup > Display Colors...**)
2. Select the desired layer with the **Layer** command
(type **L <layer number >**)
See Section 10 for a list of the default non-electrical layer assignments.

16. Select **Setup > Display Colors...**
Scroll to layer 26 and assign any color to the "Lines" column on that line (be sure both row 26 and "Lines" column are checked).

Click **OK** to exit.

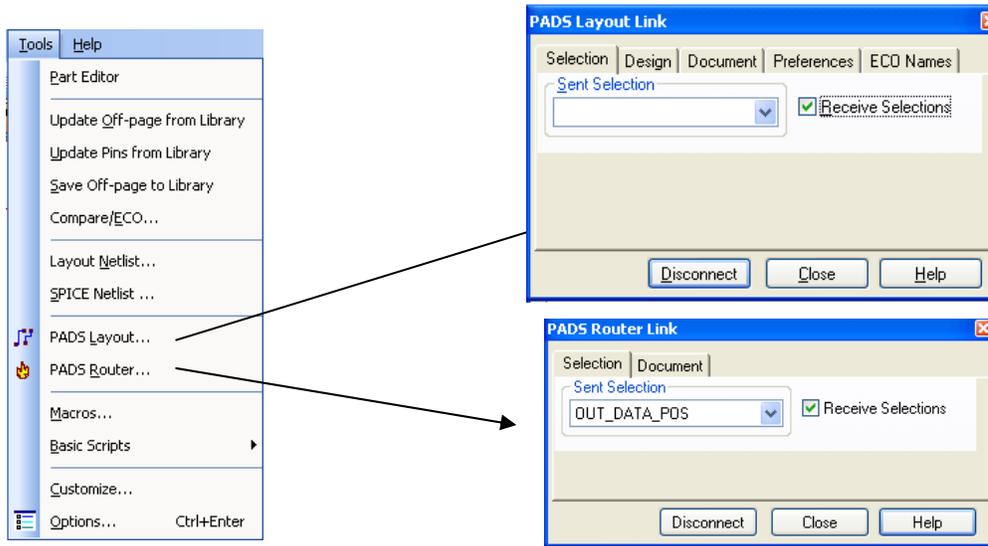
Type "**L**" (modeless command box automatically appears), then "**26**" to activate that layer.



17. Select the **2D Line** tool, and "freehand-draw" a CAP outline as shown above:
 - a. Right-click and select **Path**.
 - b. Click corners to add the path outline for each side and select **Complete** in the right menu to end the path.
 - c. Click the **Selection** icon (arrow) to exit the **2D Line** tool.
18. Save decal. Select **File > Save Decal As...** , enter any name for a decal label (e.g. 0603), and click **OK** in the dialog box to save the new part type.
19. Exit the Part Decal editor. Select **File > Exit Decal Editor**.
20. This concludes creation of a sample capacitor. Note that the eval circuit does not use this capacitor.

5.5 PADS Layout Link / PADS Router Link

OLE Automation allows object selection/highlight between schematic/layout and schematic/router, and schematic-to-PCB comparison, ECO and design rules transfer between PADS Logic and PADS Layout only, and/or PADS Logic and PADS Router. The links both provide push-button, bi-directional sync synchronization.

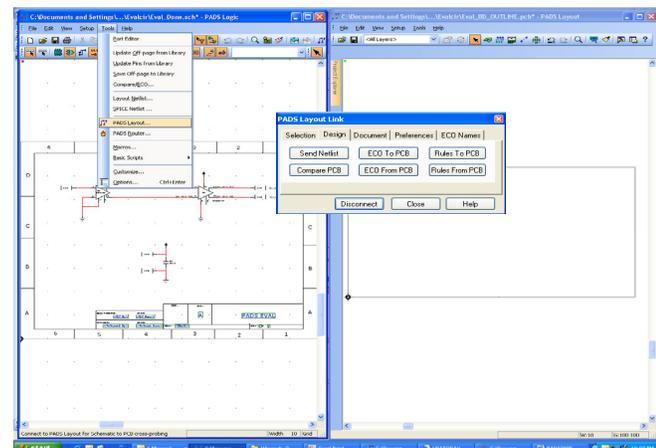


| | PADS Layout | PADS Router |
|--|-------------------------------------|-------------------------------------|
| Cross-probe component placement, Nets, Pin Pairs | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| Netlist send and compare | <input checked="" type="checkbox"/> | |
| ECO to/from PCB | <input checked="" type="checkbox"/> | |
| Design Rules to/from PCB | <input checked="" type="checkbox"/> | |

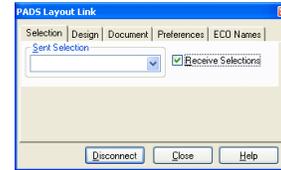
Link capabilities between PADS Logic to PADS Layout vs. PADS Router

Transfer schematic information to layout.

1. Position PADS Logic and PADS Layout windows side-by-side
2. In PADS Logic, click **File > Open** from the main menu.
3. Double-click the **Samples** folder in the File Open dialog, and open **Sch_Eval_Done.sch**.
4. In PADS Logic, click **Tools > PADS Layout** from the main menu.

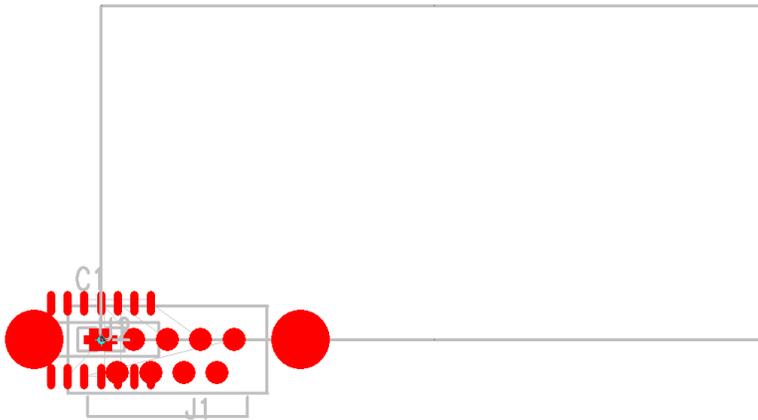


5. In PADS Layout Link, click the **Design** tab, then the **Send Netlist** button.

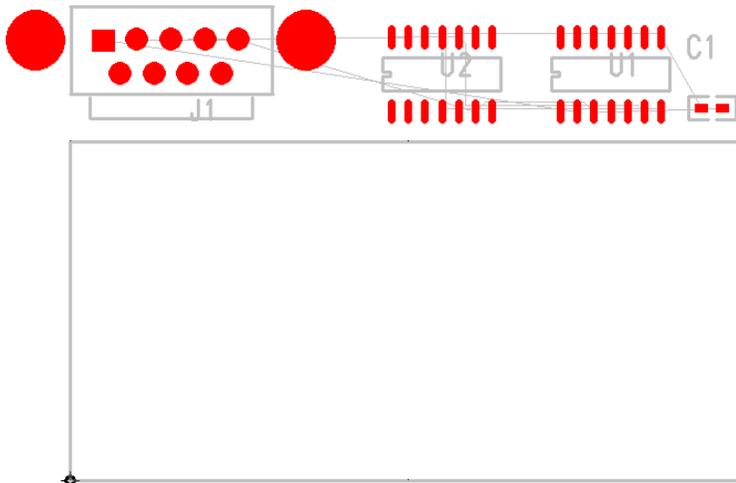


6. If the message “Schematic net list may have errors. Do you want to continue?” appears, click **Yes**.

7. The parts should appear within PADS Layout as shown.



8. Select **Tools > Disperse Components**. Click “**YES**” to the dialog box. Now components are placed outside the board perimeter as shown.



5.6 Component placement

Since designers spend a significant amount of time placing components, PADS provides the ultimate in component placement capability. With PADS Layout, you can place components individually or by group. There are multiple placement techniques:

- Drag & Drop
- X and Y coordinates
- Sequential move – parts snap to cursor
- Radial-array placement for circular (for example, DUT) board applications

Single Part Placement

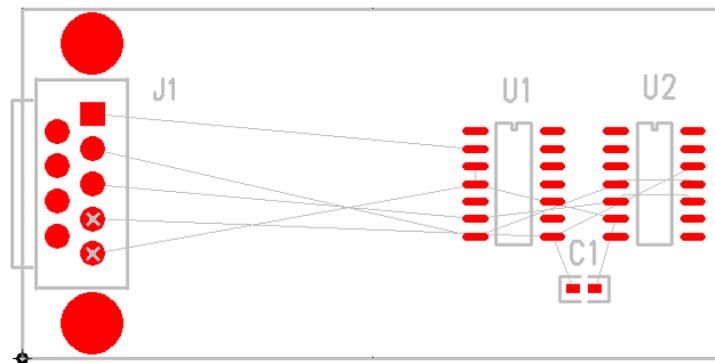
1. Right-click and click **Select Components** to set the component filter.
2. Type **G100** and press **Enter** to set the placement grid to 100 mils.
3. Drag any component to move it.
4. Press **Ctrl+R** to rotate components as you move them. Place components at the location you want and click once to release the object.

Tip: While moving a component, you can press **Esc** to cancel. While not in an action mode, press **Esc** to deselect design objects that are selected.

Group Placement

1. With nothing selected, beginning in free space draw a rectangle around a group of components in order to select them all.
2. Drag any of the highlighted objects to move the entire group and click to place the group.

Using the above methods, place all components as shown below.



Re-positioning Reference Designators

1. Right-click and click **Select Documentation**.
2. Drag each reference designator to move it. Position the Reference Designators as shown above.
Tip: Press the Tab key to rotate the component while moving it.

Tip: With any object selected, right-click to see and initiate all of the main commands possible with that object.

5.7 Vias

Any type and any number of vias can be easily defined in PADS Layout. The default via type in PADS is called a STANDARDVIA.

Vias are:

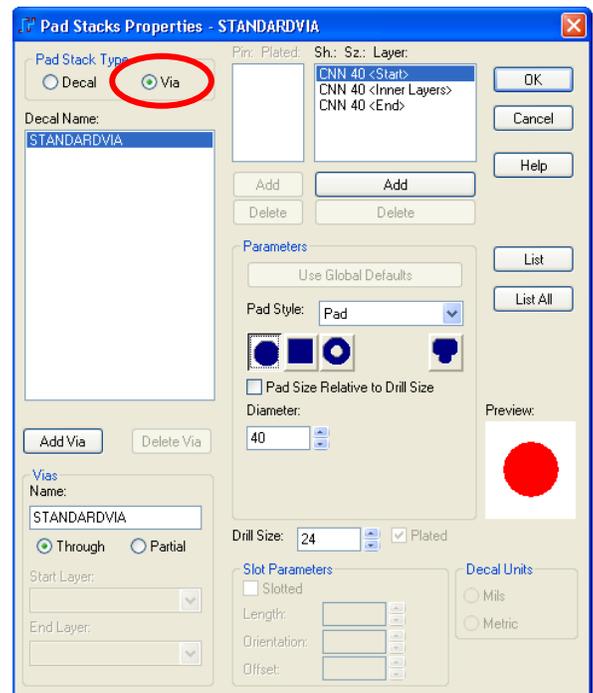
- Created through an intuitive menu
- Available as through-hole and partial via types

Changing the Via Value

To change the size of the STANDARDVIA to a smaller via:

1. Click **Setup > Pad Stacks** from the main menu.
2. In the Pad Stack Type area, select **Via**.
3. Select **<Start>** from the Sh: Sz: Layer list.
4. Type **40** in the Diameter box.
Tip: When you change the value in the Diameter box, you must click another box for the value to register.
5. Repeat for <Inner Layers> and <End> layers.
6. Type **24** in the Drill Size box.
7. Click **OK** to close the dialog box.
8. Click **“Yes”** when prompted by the message “Are you sure you want to change all vias of type STANDARDVIA”.

Note how easy it would be to set up Partial or Slotted vias.



5.8 Layer Setup

The interactive router, autorouter, and CAM Photoplot generator need the layer setup information. There are 2 methods to create plane layers:

- Split/Mixed (preferred, WYSIWYG method)
- CAM (outmoded method using negative imagery)

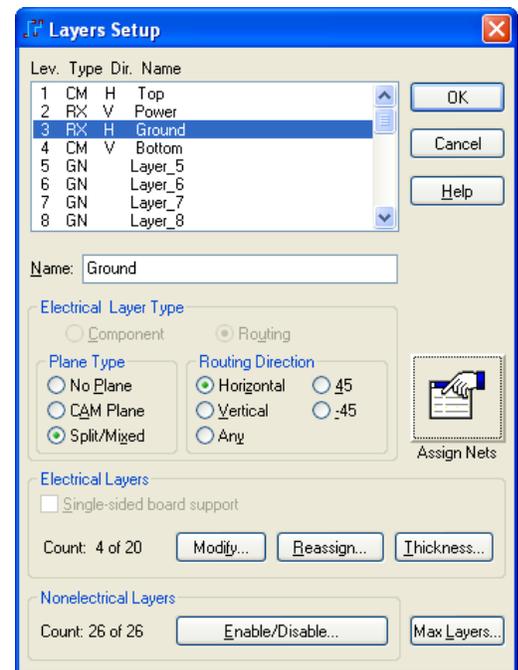
Use layer setup to:

- Change layer count
- Easily assign signal, plane, split/mixed layers
- Set routing direction biasing
- Re-assign layers

Setting up a Four Layer Board

To set up the board as four layer, with power and ground assigned to inner planes.

1. On the **Setup** menu, click **Layer Definition**.
2. In the Electrical Layers area, click **Modify**.
3. In the Modify Electrical Layer Count dialog, accept the default increase to 4 and click **OK**. Accept the default in the Reassign Electrical Layers dialog, and click **OK**.
4. Select Lev. 2, and name it **Power**.
5. In the Plane Type area, select **Split/Mixed**.
6. Click the **Assign Nets** button. The Plane Layer Nets dialog box opens.
Tip: This button is unavailable when No Plane is selected in the Plane Type area.
7. Select **+5V** and click the **Add** button.
8. Click **OK** to close the dialog box.
9. Repeat Steps 2 – 6 for Lev. 3, naming it **Ground** and assigning the **GND** net to the layer.
10. Click **OK** to close the dialog box.



Assigning Colors by Layer

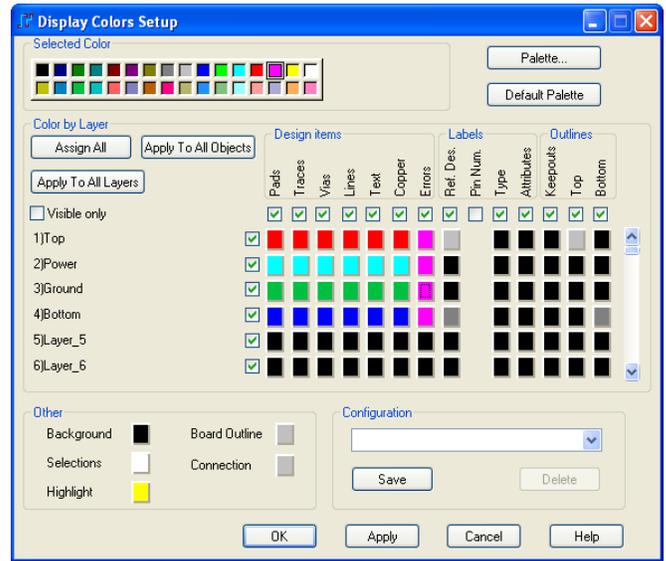
Assign Colors by Layer as follows:

| | |
|---------------|------------|
| Top | Red |
| Inner Layer 2 | Light Blue |
| Inner Layer 3 | Green |
| Bottom | Dark blue |

Assign Design Items as follows:

| | |
|--------|---------|
| Errors | Magenta |
|--------|---------|

1. Click **Setup > Display Colors** from the main menu.
2. Select a color box, then the layer or object you want.
3. Click **OK** to close the dialog box.
4. Click the **Save** button to save your design.



Tip: It's easy to switch visible layers using the Layer modeless command:

- L1** - reveals top layer color (red)
- L4** - reveals bottom layer color (green)

5.9 Passing the Design to PADS Router

The design is now ready for PADS Router – the advanced interactive design environment. You can choose to either interactively route or autoroute your design on its own; even while you work on another design in PADS Layout.

PADS Router provides:

- Simple, push-button transfer to/from either PADS Router interactive router or PADS Autorouter
- Easy set up of the routing strategy

Pass the Design to PADS Router

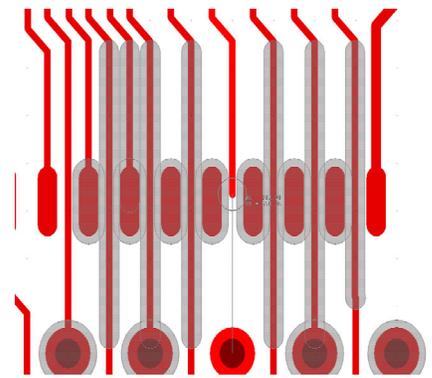
- On the main toolbar, click the **Switch to PADS Router** button and answer Yes when prompted to save the design with no undo. .

6 Introduction to PADS Routing Solutions

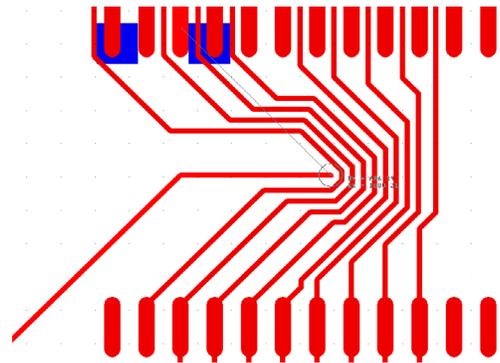
PADS Router is an advanced interactive router and an autorouter.

The PADS Router provides:

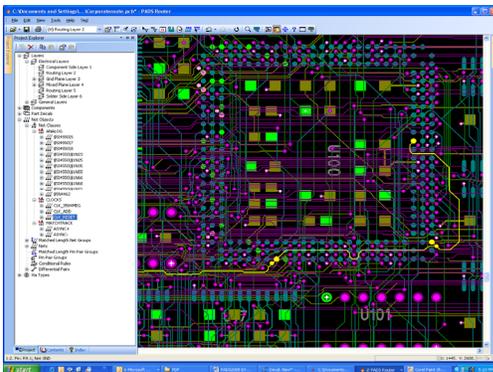
- Powerful push n' shove, plowing algorithms
- High speed routing using shape-based, gridless technology
- Diff pair, min/max length, matched length
- Semi-automatic 45°, 90°, and any-angle routing
- Adherence to extensive design rule hierarchy
- And intuitive, customizable environment
- Multiple interactive route operations:
 - Autoroute by net, component
 - Partial route (let autorouter finish)
 - Automatic trace neck-down
 - Trace smoothing
 - Auto-reroute of moved components
 - Pin/via hopping
 - Pad entry control



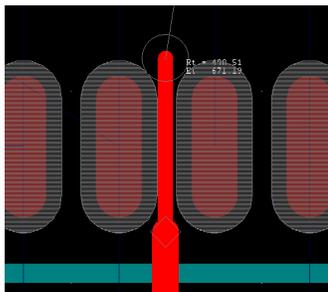
Guard bands dynamically display DRC boundaries of objects in route area



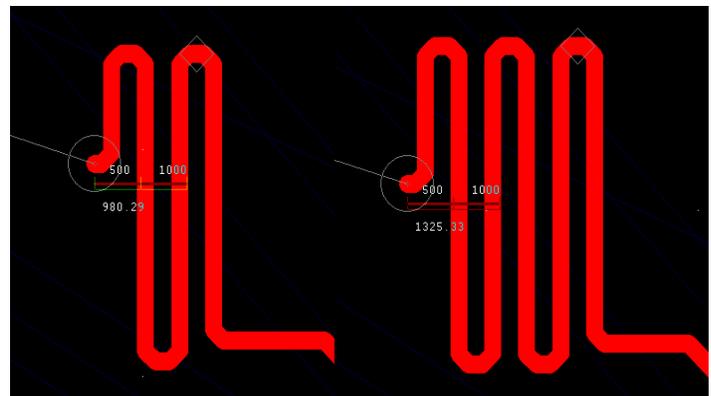
Multiple, advanced plowing modes



Critical net highlight



Trace neck-down



Real time trace monitor indicates constraint violations

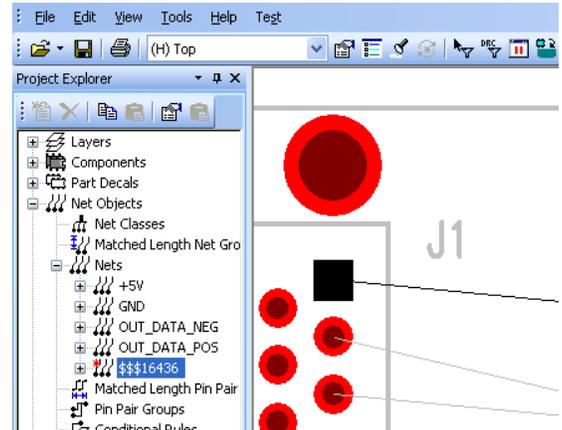
6.1 Constraint Assignment/Review

As mentioned in a prior section, PADS offers an extensive hierarchical constraint assignment capability. Using constraints, you can set critical net criteria either in the schematic tool or assign them in PADS Layout or PADS Router.

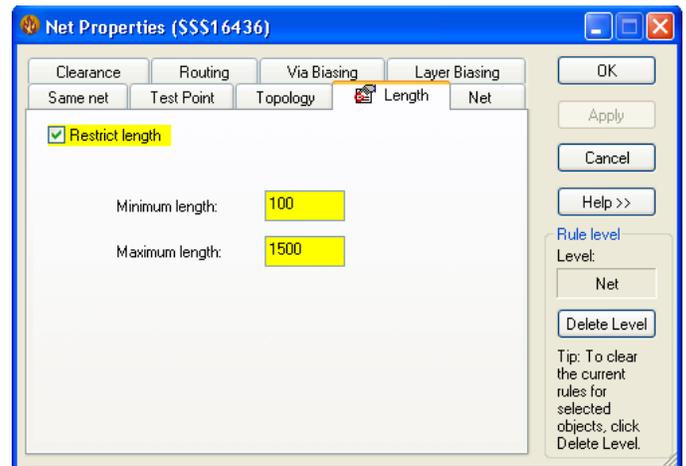
Reviewing Constrained Nets in PADS Router

To assign min/max length of 100/1500 to a net:

1. In Project Explorer, expand **Net Objects** then **Nets**, then expand the three unnamed nets beginning with the '\$' to see their pin pair connections.
2. Select the net which connects U1.2 to J1.1. Make sure you select the \$<net name> and not the pin pair.
3. Right-click and click **Properties**.
4. Click the **Length** tab.



5. Select the **Restrict Length** check box.
6. Type 100 in the Minimum length box.
7. Type 1500 in the Maximum length box.
Tip: Variations from default rules are indicated by a red icon on the tab label,  and a **YELLOW** highlight in the boxes. To see this now, click Apply.
8. Click **OK** to close the dialog box.



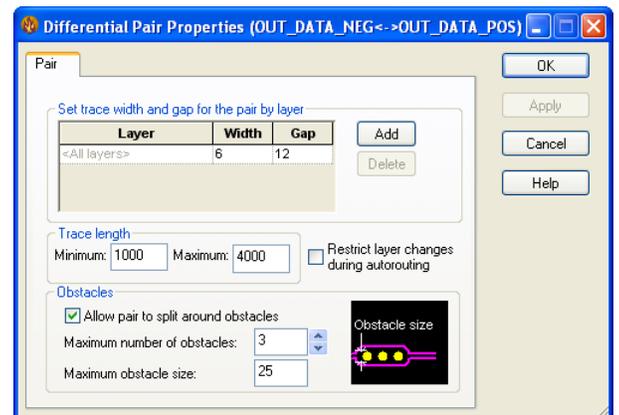
Confirming the Differential Constraints

Confirm the differential constraints assigned earlier (Section 5.3) in the schematic are present.

1. In Project Explorer, expand **Differential Pairs**, and click **OUT_DATA_NEG<->OUT_DATA_POS**.
2. Right-click and click **Properties**.

Notice the min/max trace length **1000/4000** transferred over from schematic.

Click **OK** to close the dialog box.



6.2 Interactive, high-speed routing environment

PADS Router offers the most highly functional interactive routing capabilities available in desktop PCB design. You will quickly note how intelligently traces “flow” around obstacles. You have the speed of autorouting, with the control of hand routing.

PADS Router provides:

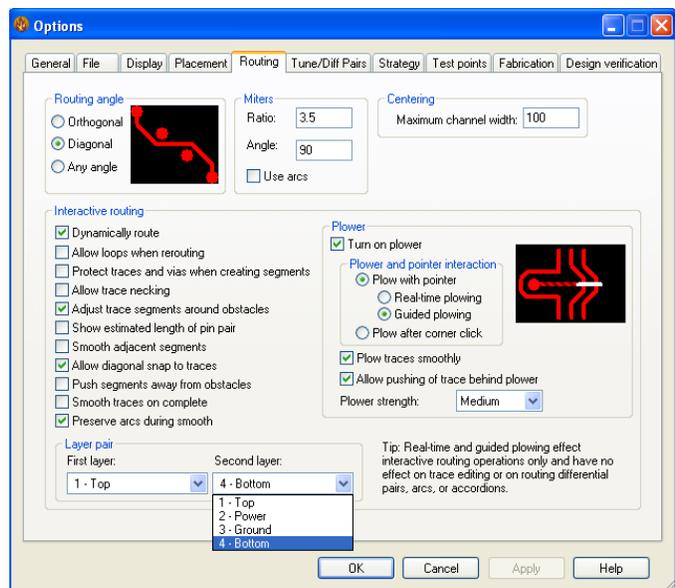
- Toggle on/off Dynamic routing, loops, protecting, trace necking, obstacle control, display, pushing, smoothing
- Routing angle - Orthogonal, Diagonal, even true “any angle” routing
- Extensive dialogs controls both interactive and auto routing
- Accordion creation with fine tuning of amplitude and gap
- Extensive real-time Plower control

Set Layer Toggles

Set the layer pair to Top and Bottom.

To determine what layers are toggled when interactively routing:

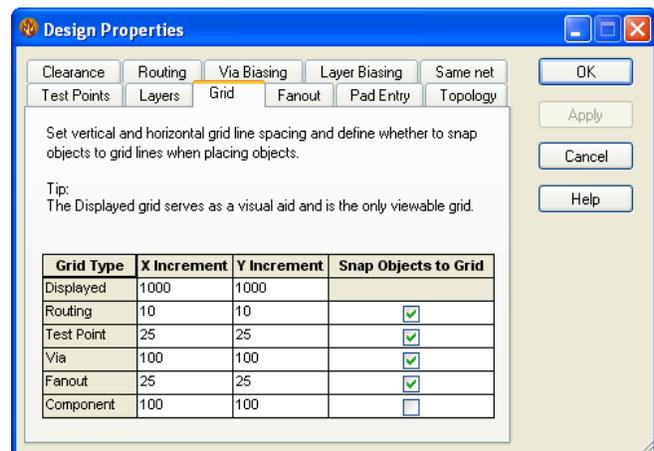
1. On the **Tools** menu, click **Options**.
2. Click the **Routing** tab.
3. Select **4 – Bottom** from the Second Layer list.
4. Click **OK**.



Set the Routing Grid

To set the routing grid:

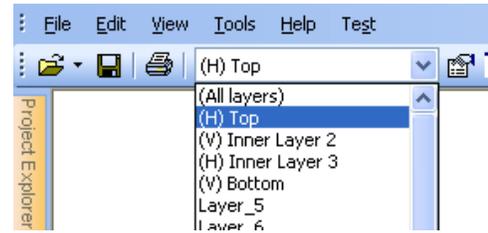
1. On the **Edit** menu, click **Properties**.
2. Click the **Grid** tab.
3. In **Routing** row, type **10** in both the **X Increment**, and **Y Increment** columns.
4. Click **OK** to close the dialog box.



Switching Layers

There are three ways to switch between layers.

1. Use Layers List in the main toolbar.
2. During interactive routing, press **F4** to toggle between layer pairs.
3. Use the Layers modeless command.
(Type **L 1** for layer 1)
(Type **L 4** for layer 4)



Routing Interactively

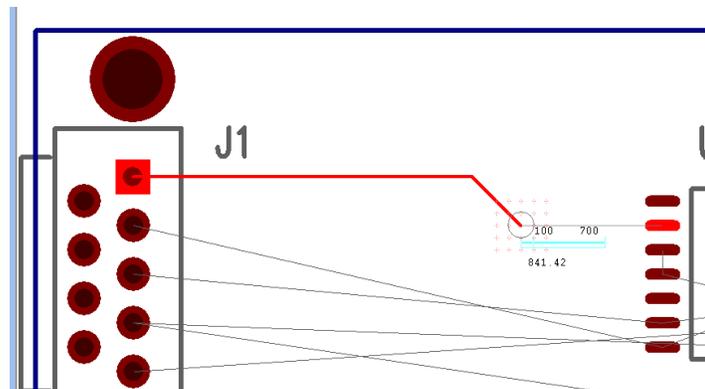
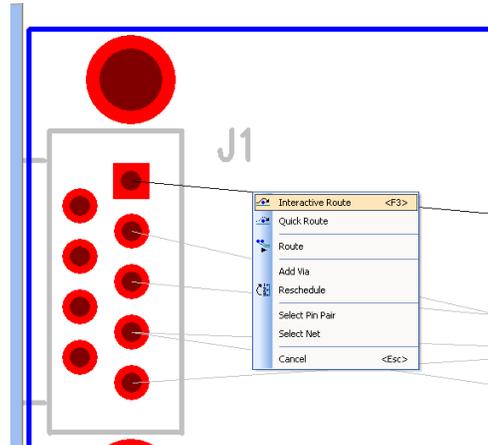
Start interactive routing:

Select J1, pin 1 (the square pin of the connector).

1. Select J1 pin 1 (the square pin of the connector).
2. Right-click and click **Interactive Route** or press **F3**.

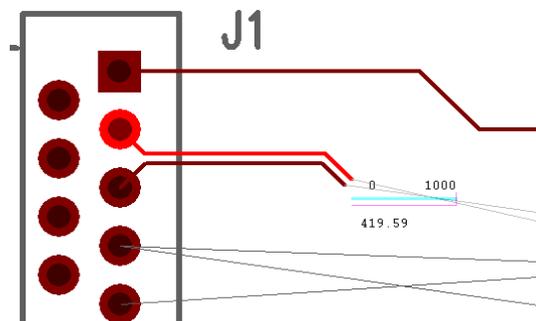
Note how the trace length monitor changes color as you route the length past 1500 mils.

3. Press **F4** to toggle between the top and bottom layers.
Tip: Press Backspace to go backwards and remove corners.
4. Click the ending pin of the connection you are routing.
Tip: Double-click while routing to autocomplete the route.



5. To route the differential pairs, Select either **OUT_DATA_NEG** or **OUT_DATA_POS** (J1.2 or J1.3), and press **F3**.

Note how the paired net also highlights and routes.



Accordions

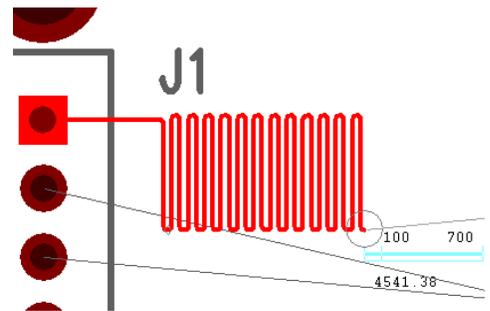
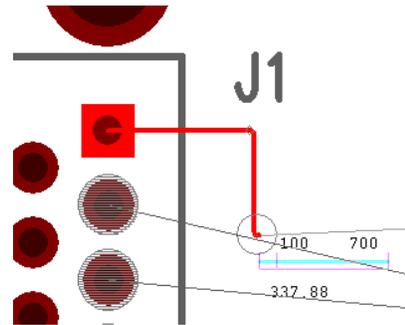
With the high speed option, nets can be routed with an accordion pattern.

Routing with Accordions

Unroute the net between U1.2 and J1.1 to use for this exercise.

Tip: You can't use the other nets because differential pairs cannot be used to route as accordions.

1. On the Tools menu select Options, Tune/Diff Pairs tab and set the Minimum Amplitude value to 20. Select Ok.
2. In the Project Explorer, select the net between U1.2 and J1.1 by holding down the Shift key and clicking on the routed area.
3. In the design area, right-click and click Unroute.
4. Select the J1.1 pin, press **F3**, and move cursor to the right.
5. Right-click and click **Add Accordion**.
6. Move the pointer in the direction you want and place the accordion.
Tip: Using the mouse, you can drag the route up, click to place a corner and then down, and click to place the second corner. This sets the upper and lower limits for the corners of the accordion.
7. Move the pointer to the right and the accordion is created.
8. Right-click and click **Complete Accordion** (or double click) to end the accordion and continue routing.



Other Route Modes

Try the various route modes that are available as a right-click as you route the board.

Tip: This menu is available only when you are actively routing.

Interactive modes

While routing a trace, try these modes ...

- ... **End** (before reaching target pad)
- ... **Arcs**
- ... changing **Width, Layer**
- ... changing **Routing Angle**
- ... toggle on/off **Dynamically Route**
- ... toggle on/off **Push Trace Behind**
- ... toggle on/off **Plow After Click**

To smooth a trace that “meanders” around the board:

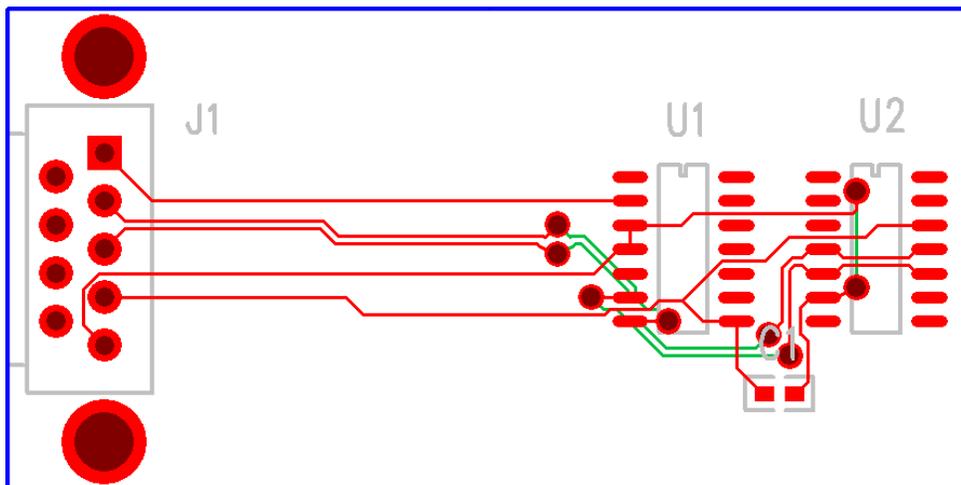
1. Select a trace segment that isn’t a direct connection.
2. Right-click and click **Select Trace**.
3. Right-click and click **Smooth Trace Pattern**.

To route some traces and “push” a trace through the routed traces using the plow mode:

1. On the **Tools** menu, click **Options**.
2. Click the **Routing** tab.
3. Change the Plower settings to see what they do.

Interactively route the remainder of the board.

| | |
|---|-----------------------|
| Add Corner | <Space> |
| Add Via | Shift+LButton+<Click> |
| Add Test Point | |
| Add Accordion | Shift+A |
| <hr/> | |
| Arc | ▶ |
| <hr/> | |
| Complete | LButton+<DoubleClick> |
| End | Ctrl+LButton+<Click> |
| Backup | <Backspace> |
| Layer Toggle | <F4> |
| <hr/> | |
| End Via Mode | ▶ |
| <hr/> | |
| Width | ▶ |
| Layer | ▶ |
| Via Type | ▶ |
| <hr/> | |
| Routing Angle | ▶ |
| <hr/> | |
| Explain Last Error | Alt+X |
| <input checked="" type="checkbox"/> Check Clearance | Shift+C |
| <input checked="" type="checkbox"/> Dynamically Route | Shift+D |
| <input checked="" type="checkbox"/> Push Trace Behind | PB |
| <hr/> | |
| No Plowing | PX |
| Plow After Click | PC |
| <input checked="" type="checkbox"/> Plow with Pointer | PP |
| Rip Up Obstructing Traces | PR |
| <hr/> | |
| Protect Traces and Vias | |
| Switch Rules | Shift+R |
| Switch Pin Pair | <Tab> |
| Dynamic Reconnect | Shift+N |
| <hr/> | |
| Cancel | <Esc> |



A sample, finished board, interactively routed.

6.3 PADS AutoRouter

The PADS AutoRouter is a shape-based gridless autorouter that is designed for high speed, high density designs. Great for fine pitch parts and dense areas alike, it uses the same routing algorithms as the PADS Router interactive router.

The PADS Autorouter can be set to route:

- Entire design
- Specific parts
- Critical nets, net class

The PADS AutoRouter features:

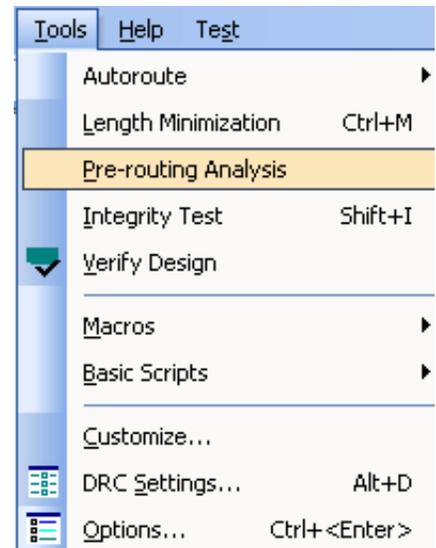
- Intuitive route strategy dialogs
- No complex programming languages to learn
- Fast learning cycle
- Low, Medium, High controls based on available routing time/density.
- *Protect Routing* to protect traces after a completed pass.
- Fanout, cleanup, tuning route passes

Autoroute a Design

1. On the **File** menu, click **Open**.
2. Select **...\Samples\Layout_Eval_Placed.pcb** and click **Open**.
3. Before routing, run the Pre-Routing Analysis tool to check the board for any potential problems prior to autorouting.
4. Group-select the entire design by dragging a cursor over all objects to highlight all nets and components.
5. On the **Tools** menu, click **Pre-routing Analysis**.

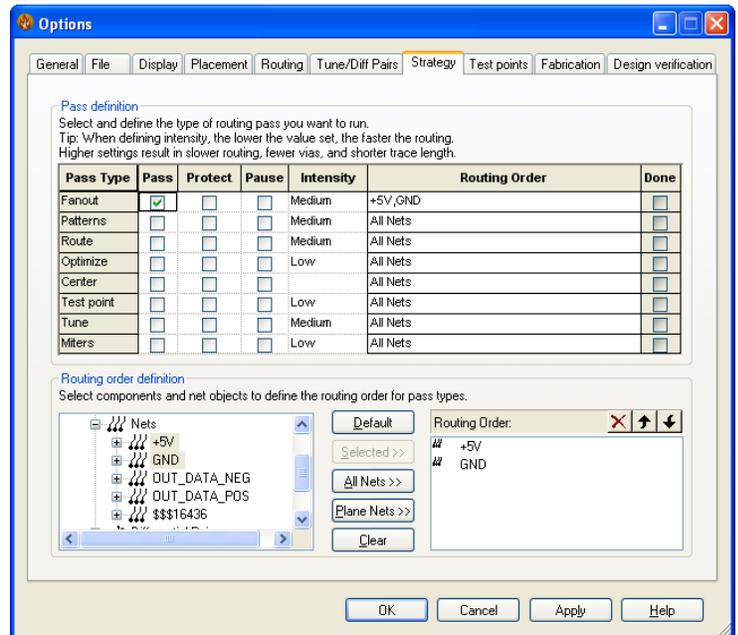
The **Output Window** opens, and may display a warning that the three critical nets cannot be routed since the net lengths exceed the assigned constraint, depending on how far the pins are.

Notice that it may recommend moving components or relaxing the constraint values, depending on component placement.

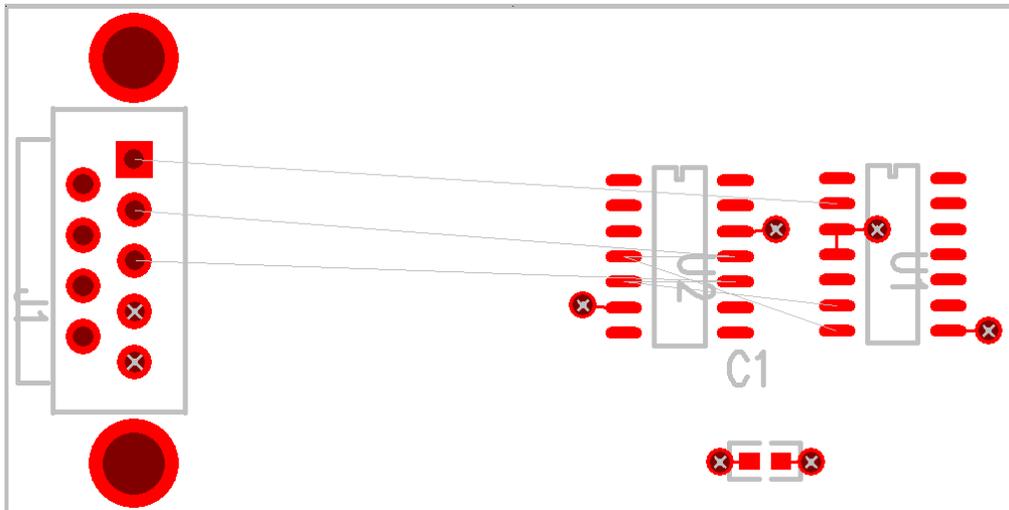


Route the power and ground fanouts.

1. On the **Tools** menu, click **Options**.
2. Click the **Strategy** tab.
3. Clear the **Route** and **Optimize** check boxes.
4. Select the **Pass** checkbox for the *Fanout* Pass Type.
5. In the **Routing order definition** section, expand the Net Objects and then the Nets grouping.
6. Select the **+5V** and **GND** nets and click **Selected** to add them to the routing order.
7. In the Routing Order list, click **All Nets** and then click the red **X** button to remove it from the list.
8. In the Pass definition area, click to clear any remaining Pass Types. The dialog box should match the screenshot at right.
9. Click **OK** to close the dialog box.
10. On the **Tools** menu, point to **Autoroute** and then click Start to run the autorouter.

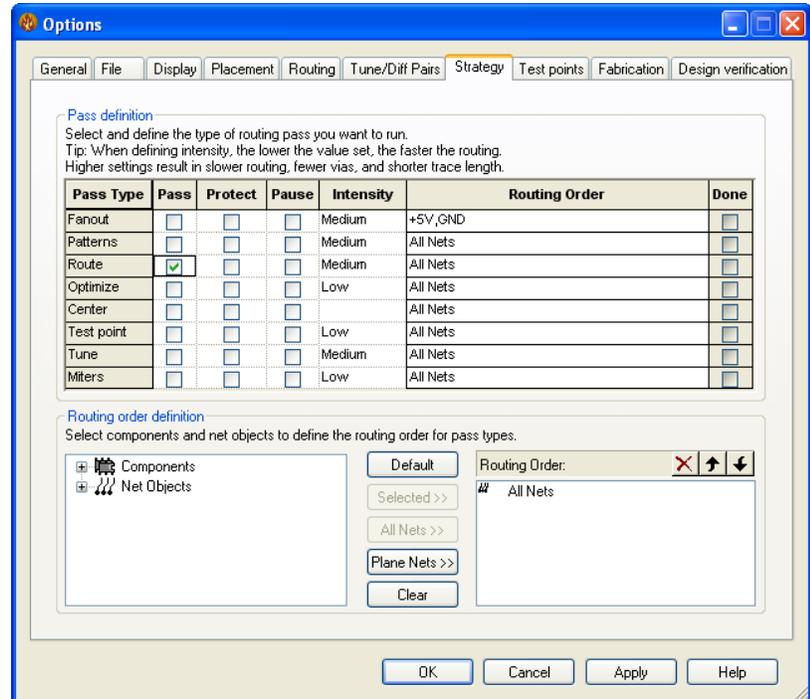


The resulting board looks like this:

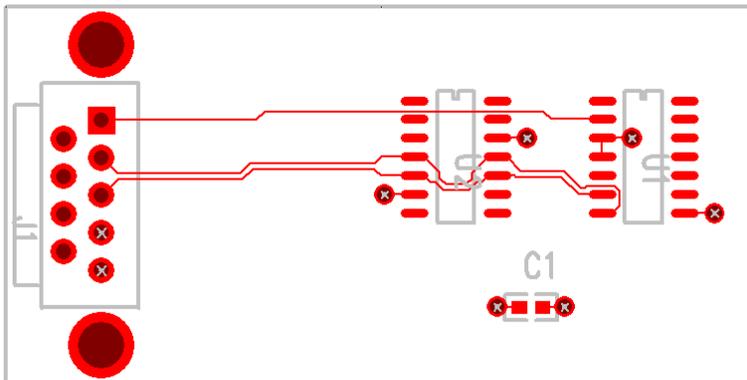


Route the signal nets.

1. On the **Tools** menu, click **Options**.
2. Click the **Strategy** tab.
3. Clear the **Fanout Pass** check box.
4. Click the **Route Pass** check box.
The dialog should match the screenshot at right.
5. Click **OK** to close the dialog box.
6. Press **F9** to route.



The resulting board looks similar to:



7. Run an **Optimize** pass using the same technique.

Unroute the entire board and try other Intensity settings.

8. Right-click and click **Select Traces/Pins** to select the traces on the entire board.
9. Right-click and click **Select All**.
10. Press **Backspace** to unroute.
11. Alter the **Intensity** setting under the Tools, Options, Strategy tab and try rerouting.
12. Save the completely routed design.
13. Click the Switch to PADS Layout button, , to open the routed design in PADS Layout.

6.4 Create Copper Pour in PADS Layout

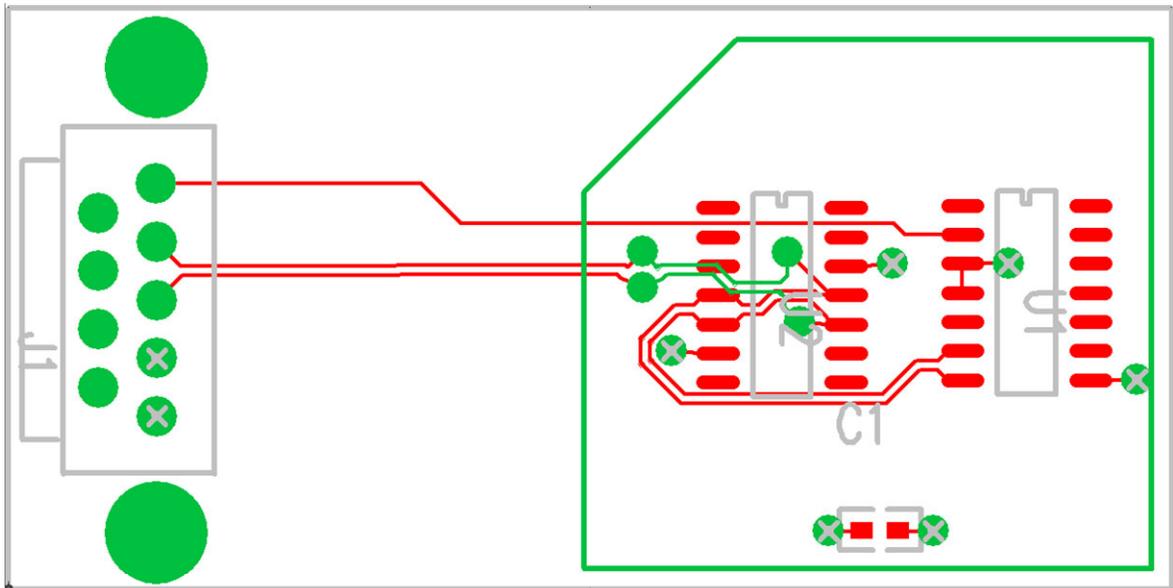
PADS Layout features a powerful and flexible copper pour capability.

With PADS Layout copper pour you can:

- Easily create power/ground/signal copper planes on any layer.
- Create copper “cut out” areas for copper voiding.
- Create “positive image” power/ground planes.
- Run extensive checking utilities to ensure proper plane interconnects.
- Support buried trace applications.
- Automatically create thermal pads.

To add a ground copper area to the bottom layer:

1. In PADS Layout, type **L4** and press **Enter** to switch to the bottom layer (layer 4).
2. Click the **Drafting** toolbar button, , to open the Drafting toolbar.
3. Click the **Copper Pour** button, .
4. Create a complete polygon in an area inclusive of some ground pins, like this using double click to complete the polygon:

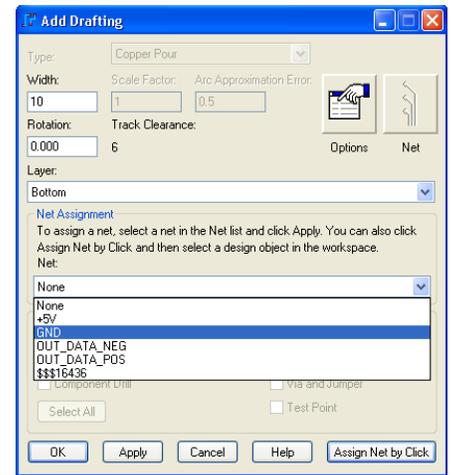


The Add Drafting dialog box opens automatically when you complete the polygon:

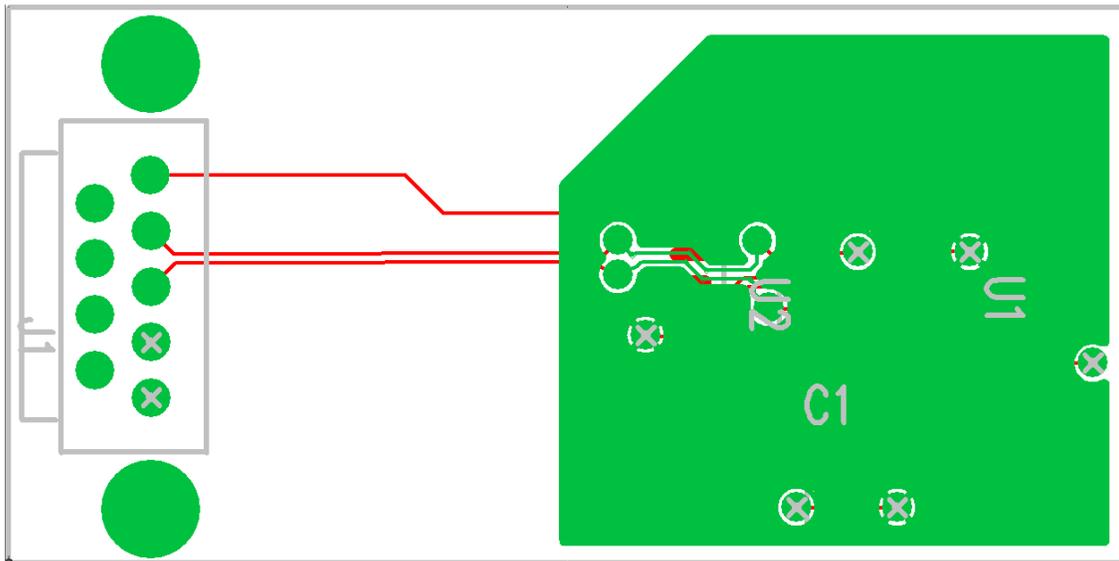
5. Select the **GND** net from the Net list and click **OK**.

Now you must select the outline and flood it.

6. Press **Esc** to exit the copper pour draw mode. The shape should remain selected.
Tip: If the shape is not selected, right-click and click **Select Shapes** to select the outline.
7. Right-click and click **Flood**.
8. Click **Yes** to Proceed with flood.



The board looks something like this:



Notice that the ground pins are connected to the copper areas with thermal relief pads, and the copper clears if traces exist on that layer.

6.5 Design verification

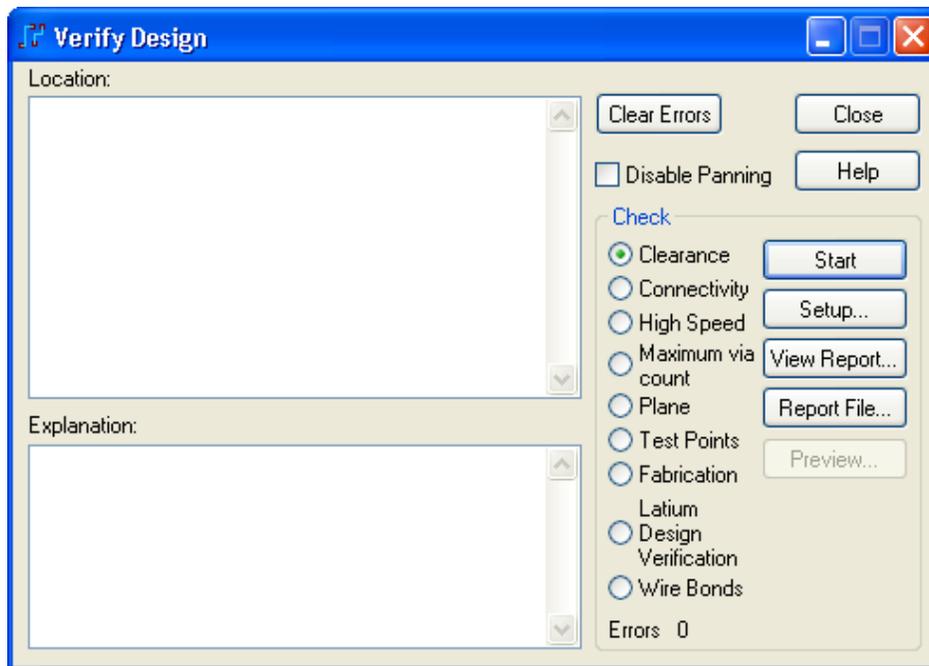
In addition to realtime design rule checking (DRC), PADS provides several very powerful design rule audits to ensure that your design accurately represents the schematic. Several checks are included with every copy of PADS, while a few others are options.

Design verification includes:

- Numerous clearance checks.
- Checks that ensure all nets have been routed.
- High speed checks such as length, delay, capacitance.
- Check to ensure maximum via count isn't exceeded.
- Plane connectivity check.

Running Various Design Verifications

1. On the **Tools** menu, click **Verify Design**. The Verify Design dialog box opens.
2. To run the various checks, click the check type (for example, Clearance) and then click **Start**.



6.6 CAM Outputs

PADS produces reliable laser photoplotting files of the highest accuracy. In addition to gerber files, it also creates all manufacturing support files and documentation including drill data, DirectCAM, and other standard data exchange formats.

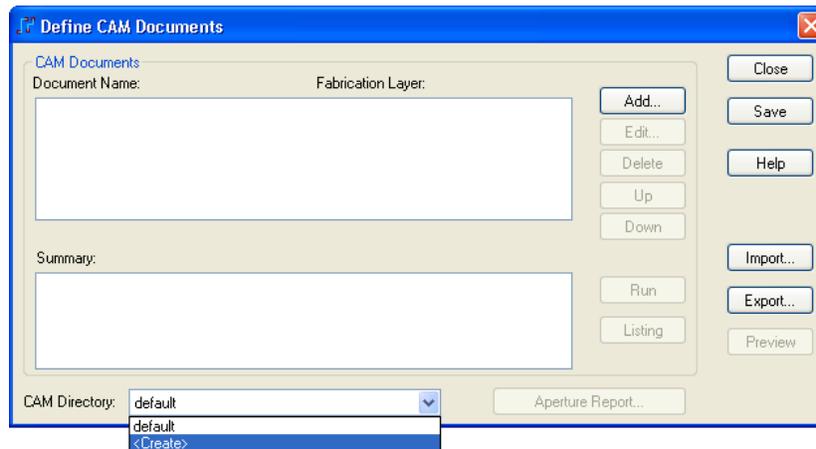
PADS CAM output provides:

- Intuitive, menu-driven board fabrication data generation
- Gerber photoplot output
- Excellon drill data
- Standard print/plot output
- Bill of Materials output for calculating board cost

Generating Gerber Files for Signal, Plane Layers

To set up the CAM directory:

1. On the **File** menu, click **CAM**. The Define CAM Documents dialog box opens.
Tip: CAM output files are known as “documents”. All documents created will be listed here.
2. Select **<Create>** from CAM Directory list dropdown to create a new default CAM project directory. The CAM Question dialog box opens.



3. Type in a new folder name, or Browse to any writable directory, and then click **OK**.

Create the Top, Signal Layer

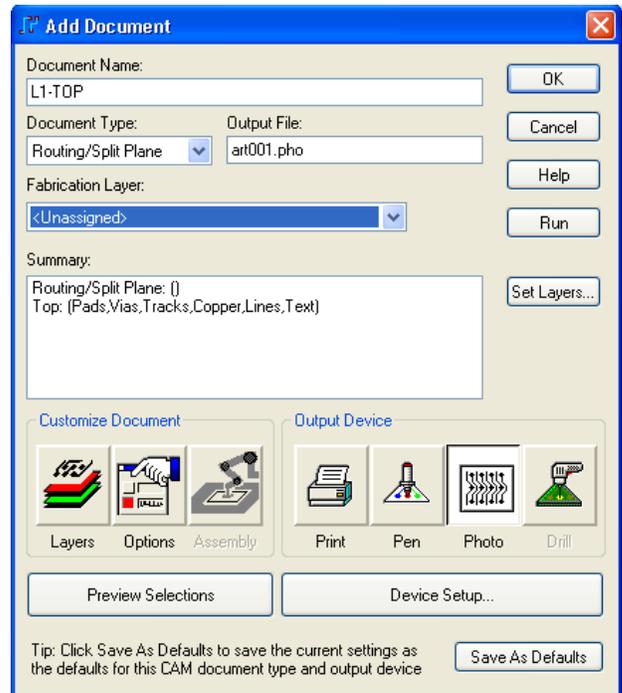
1. Click Add to create a new document. The **Add Document** dialog box opens. You will create a basic top layer Gerber file.
2. Fill out the Add Document dialog.

Document Name: L1-TOP

Document Type: Routing/Split Plane. Click Ok to Leave Layer Association as Top.

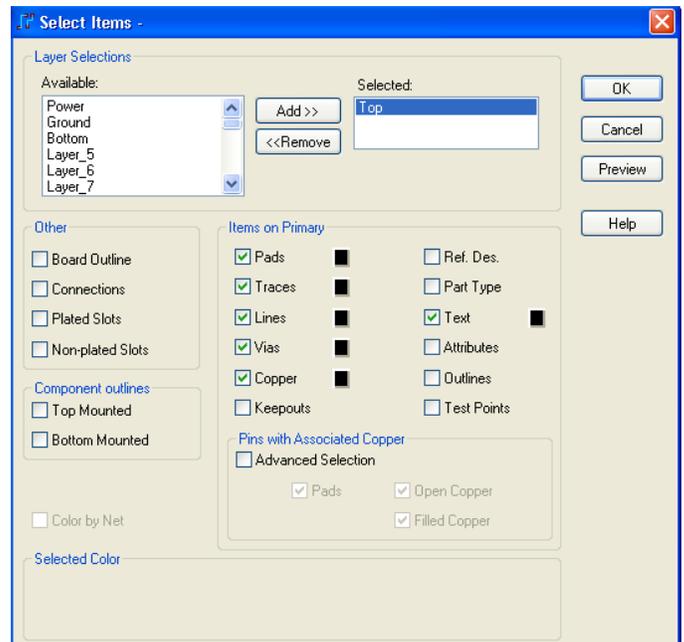
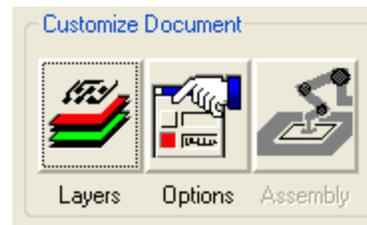
Output File: Use the default name

The dialog box should match the screenshot at right.

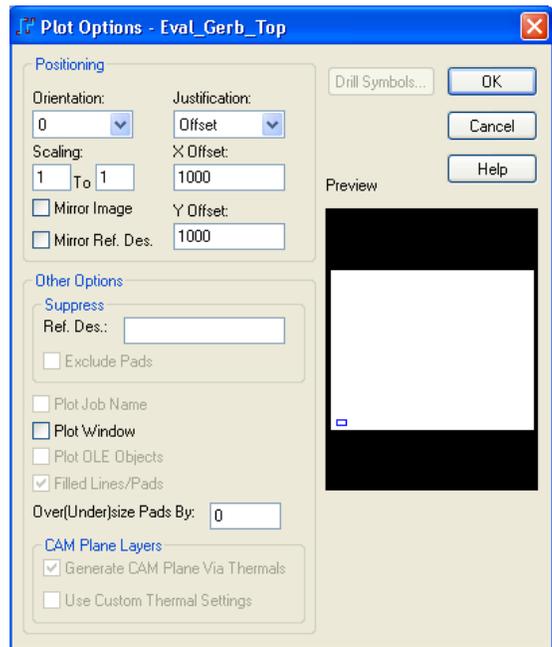


Review the Customize Document Options

1. Click **Layers** to select the elements to include in the photoplot for that particular layer. The **Select Items** dialog box opens.
2. Click **Cancel** to close the dialog box.



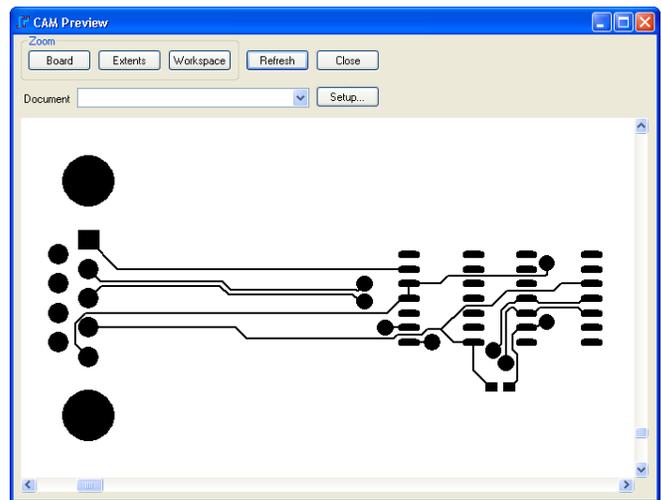
3. Click **Options** to select offset, mirroring, Ref Des suppression, over/undersizing pads and more. The **Plot Options** dialog box opens.
4. Click **Cancel** to close the dialog box.



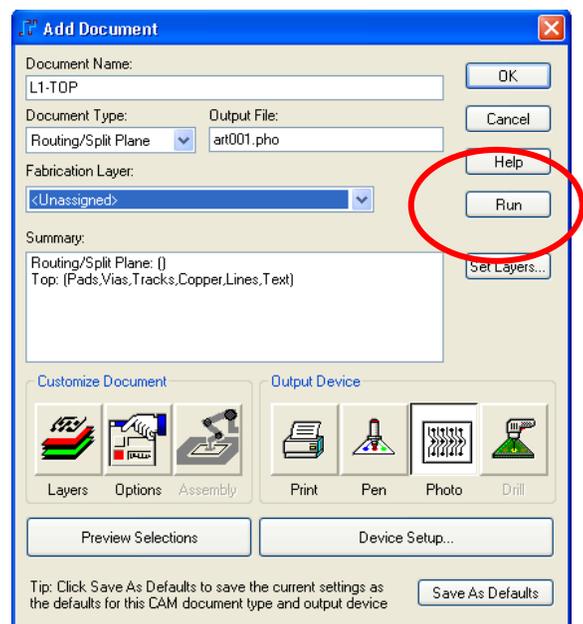
5. Click Preview Selections (lower left).
6. Zoom in to the graphic image in the lower left corner by dragging your cursor.

This is what the Gerber file should look like, depending on your results.

7. Click Close to close the Preview window.



8. Click **Run** in the **Add Document** window to generate the Gerber file.
9. Click **Yes** to complete the operation.
10. Click **OK** to close the Add Document dialog.

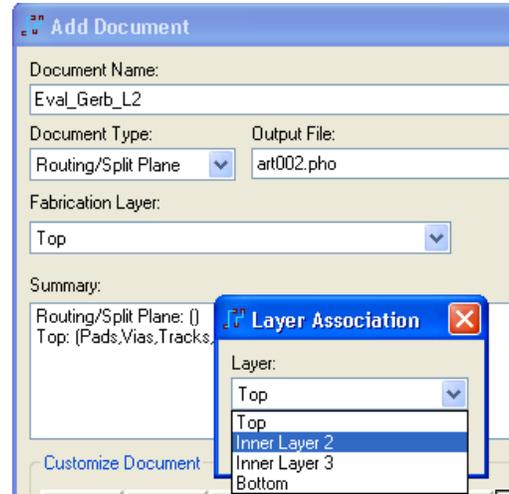


You generated the top layer, photoplot file.

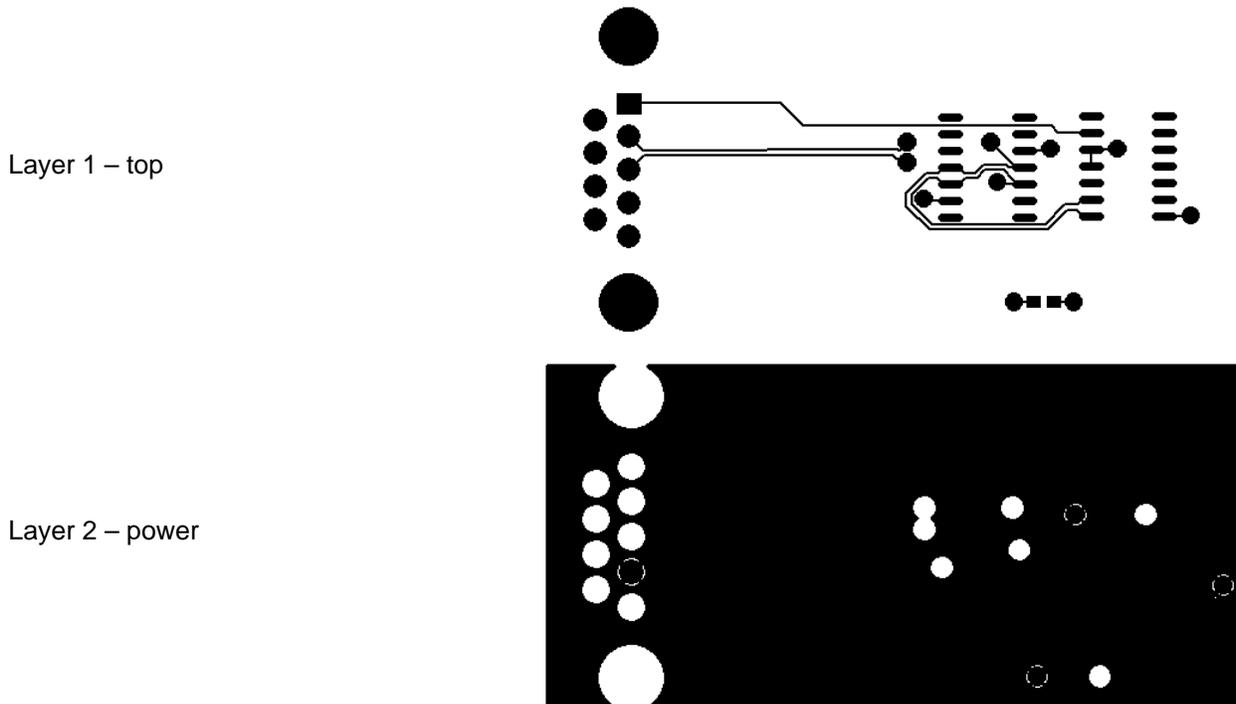
Generating a Gerber file for the Power mixed/split plane #2

Tip: You may have already assigned the +5V and GND nets as split/mixed layers to levels 2 and 3 respectively in Setup > Layer Definition, so the correct pads will receive thermal reliefs when the photoplots are generated. If you have not, do so now.

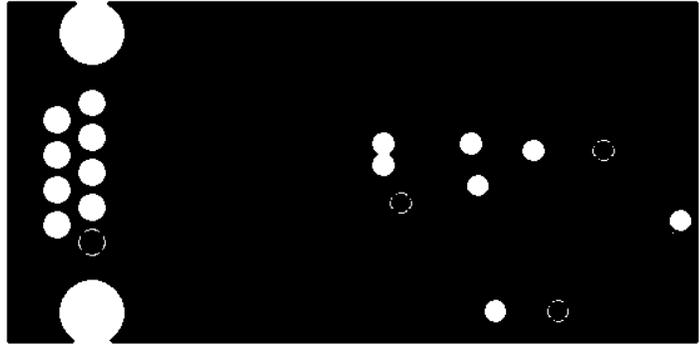
1. In the Define CAM Documents dialog box, click **Add**.
2. Name this layer **L2-PWR**.
3. Select **Routing/Split Plane** from the Document Type list. The Layer Association window opens.
4. In the Layer list, select **Power** and click **OK**.
The system defaults to the typical elements necessary to generate this layer (see Layers).
5. Click **Yes** for each dialog box.
6. Repeat for layers 3, 4, and silkscreen, etc.



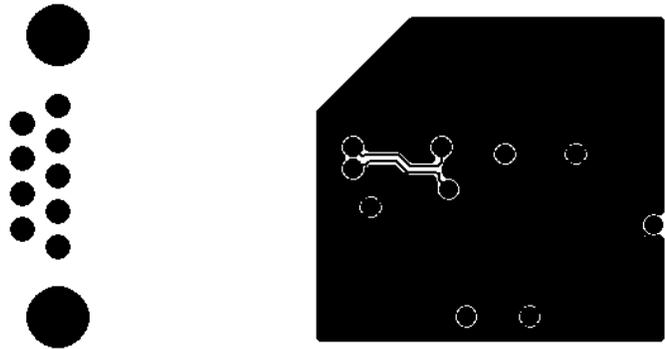
The final photoplots resemble these images.



Layer 3 – ground



Layer 4 – bottom



7 Other PADS Layout Highlights

7.1 Automation

OLE Automation is the Microsoft Standard for passing and exporting information and embedding Documents. PADS uses Automation to communicate seamlessly with other applications to pass information and/or embed documents.

7.2 Attribute support

PADS has extensive attribute support. PADS attributes give you:

- Tight integration with other company applications.
- Support for custom attributes.
- Attribute checking upon file import.
- Export to any OLE compliant tool.
- Definition using intuitive dialogs.

8 Other PADS Options

8.1 Design For Fabrication (DFF) Audit

In addition to standard design rule checking (DRC) spacing violations, PADS offers a very powerful feature called Design For Fabrication (DFF). DFF performs a variety of fabrication design rule checks, flagging potential fabrication areas before sending the design to the fabrication shop.

DFF provides checks for:

- Acid traps
- Copper slivers
- Soldermask slivers
- Traces in soldermask opening
- Silkscreen over pads
- And more

8.2 Testpoint Creation and Checking (DFT Audit option)

The DFT Audit (Design For Test) option reduces costly design iterations and ensures the testability of your designs before fabrication. A unique aspect of DFT is that testpoints are assigned during the initial routing passes, unlike other post-assignment solutions that try to fit them in after the design is complete.

The DFT audit provides two functions – testpoint assignment (routing) and testpoint coverage reports (audits).

With DFT, you can:

- Screen designs for In Circuit Test (ICT) adaptability.
- Assign/verify design testability as seen from the bottom side (typical default).
- Assign/verify testpoints for “Clamshell” (both sides) type fixtures.
- Define testability constraints for various technologies/densities. These can be stored and reused.
- Validate probes. Check for clearances such as probe to probe, probe to trace, probe to board edge.
- Generate custom reports. Reports are generated with every test point name and X/Y location including nets with missing test points. Designers can use this complete report to determine what action to take in order for the design to pass testability requirements.

8.3 Physical Design Reuse (PDR)

PDR is a unique and powerful capability for saving portions of PCB layout designs for reuse. With the PDR option, previously proven and tested sections of circuitry can be stored and reused by anyone in the organization. Such re-using design data is essential for many companies to meet their aggressive time schedules.

With PDR, you can:

- Easily reuse “building blocks” based on existing design elements, such as Multi Channel design, Concurrent Design and RF Microwave circuit replication.
- Include all design elements such as parts, traces, copper, etc.
- Have schematic independent information, which eliminates the need for time-consuming ECO's
- Save valuable redesign time from one project to the next.

8.4 Advanced Packaging And COB Toolkit

PADS Layout also offers a sophisticated advanced packaging and chip-on-board toolkit option, which provides high density connectivity through sophisticated route wizards.

This option gives you:

- Automated, any-angle BGA package routing.
- Auto-connection generation.
- Substrate array pad fanout with plating tail creation.
- Automated Die and Die Flag creation wizard.

8.5 Assembly Variants

PADS has extensive variant support through this option. Variants are created with a consistent base of components and then altered to redefine components as Installed, Non-Installed and Substituted. This allows a single base from which modifications can be made in the core design only once.

Bills of Materials (BOMs) are created from an assembly option that features both installed parts, uninstalled parts and substituted parts identifying the status of those parts.

Assembly drawings can be created based on assembly options and include or exclude parts from the actual drawing based on the status in the variant.

8.6 Mechanical Data Import/Export

This PADS Layout option provides seamless, accurate transfer of IDF mechanical data such as board outline, component packaging, and drafting documentation.

Two primary exchange formats are supported:

DXF Link

- Bidirectional interface to AutoCAD compatible systems.
- No need to recreate complex work done by mechanical engineer.

IDF Interface

- Bidirectional interface with 3D software packages.
- No need to recreate complex work done by mechanical engineer.
- Pass placement requirements and height restrictions bi-directionally

9 PADS Layout Keyboard Shortcut Commands

Tip: Print this out and keep it handy.

| Command | Action |
|----------------|--|
| G <x> {<y>} | All grids set, except the display grid. |
| GD <x> {<y>} | Display grid setting. |
| N {<net>} | Net highlighting on or off. |
| I | Distinguish protected objects on and off. |
| L <n> | Layer, set current layer to the number (Layout) or name (Router) |
| S <x> <y> | Search absolute. Moves pointer to the specified X and Y coordinates. |
| SR <x> <y> | Search relative. Moves pointer by the specified X and Y offset. |
| SS <s> | Search and select. Moves the pointer to the named object. |
| W<n> | Trace width. |
| Backspace | Unroute or backup. |
| Delete | Unroute selected object. |
| Home | Zooms to board. |
| PageDown | Zooms out at pointer. |
| PageUp | Zooms in at pointer. |
| Ctrl+B | Zoom to board. Fits the board outline into the workspace. |
| Ctrl+E | Move component. |
| Ctrl+I | Spins component . |
| Ctrl+N | New file. |
| Ctrl+O | Open file. |
| Ctrl+R | Rotates component 90 degrees. |
| Ctrl+S | Save file. |
| Shift+A | Accordion beginning, interactive routing mode. |
| Ctrl+F | Flips component. |
| Shift+click | Adds via, interactive routing. |

10 Default Non-Electrical Layer Assignment

| Layer | Element |
|-------|-------------------------|
| 21 | Solder Mask Top |
| 22 | Paste Mask Bottom |
| 23 | Paste Mask Top |
| 24 | Drill Drawing |
| 25 | --- |
| 26 | Silkscreen Top |
| 27 | Assembly Drawing Top |
| 28 | Solder Mask Bottom |
| 29 | Silkscreen Bottom |
| 30 | Assembly Drawing Bottom |