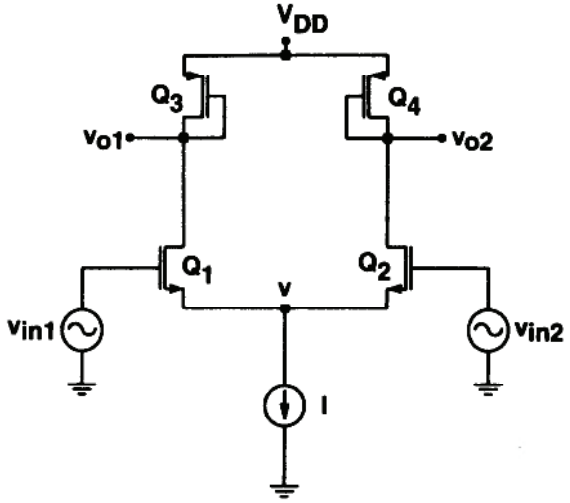

Figure 3.40. Source-coupled CMOS differential stage with diode-connected PMOS load devices.

trolled amount of positive feedback to increase the transconductance of the input device [11]. The resulting circuit is shown in Fig. 3.41 and the differential gain can be derived as

$$A_{dm} \approx -\frac{g_{mi}}{g_{ml}}(1 - \alpha)^{-1}, \tag{3.83}$$

where $\alpha = (W/L)_5/(W/L)_3$. As an example, if $\alpha = \frac{3}{4}$, the differential gain will be increased by a factor of 4.

All the differential stages described thus far have low gain and a differential output voltage. For high gain the circuit of Fig. 3.42*a* can be used. This circuit has differential input but single-ended output. Hence it performs as a combination of a differential gain stage and a differential-to-single-ended converter. In Fig. 3.42*a* transistors Q_1–Q_2 and Q_3–Q_4 form matched transistor pairs. They have equal W/L ratios. All current levels are determined by the current source I_o, half of which flows through Q_1–Q_3 and the other half flows through Q_2–Q_4. All transistors have their substrates connected to their sources to eliminate body effect and improve matching.

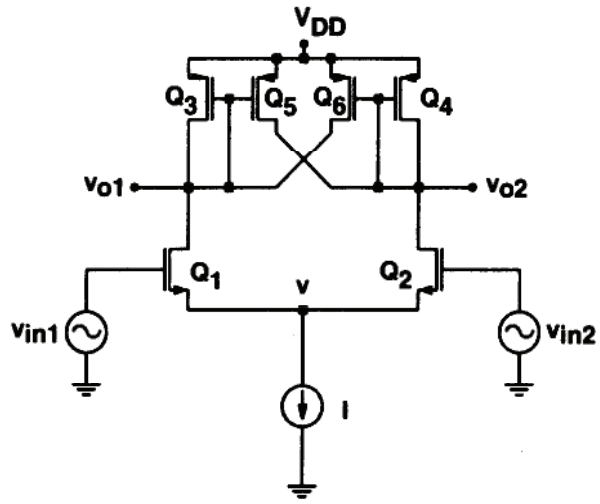

Figure 3.41. Source-coupled CMOS differential stage with positive feedback to increase gain.