

Optimum Tapered Buffer

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Abstract—Driver stages in MOS circuitry have been extensively investigated during the last decade. Recently a tapering rule for CMOS buffers was derived showing that the tapering factor (β) is determined by the ratio of output to input capacitance. The derivation fails to account for the correlation between the short-circuit current and β . As a result, the derived formula consistently overpredicts the value of optimum β , especially for large output/input capacitance ratios. We present a modified formula and a method to account for the effect of the short-circuit current that is viable for buffer stages over a wide range of output/input capacitance ratios; this newly derived formula accurately predicts the optimum tapering factors for BiCMOS as well as CMOS buffer chains.

I. INTRODUCTION

THE traditional model of the CMOS tapered buffer predicts the optimum tapering factor to be a constant, $e = 2.72$ [1], [2]. A recent study improves upon this model by showing the tapering factor to be a function of the ratio of the output to input capacitances of the buffer [3]. The new model accounts for the correspondence between decreasing feature sizes and increasing tapering factors and can be extended to encompass the large tapering factors of BiCMOS buffer chains. Discrepancies arise, however, between analytical results and simulated values: the model consistently overpredicts the optimum tapering factor. Examination of the analytical model has revealed that the dependence of β on the rise and fall times was neglected in the derivation.

To account for this β dependence we modify the analytical model and employ a graphical method for the determination of effective output capacitance. Our results show good agreement with simulation results over a wide range of output to input capacitance ratios, allowing accurate prediction of the optimum tapering factor for BiCMOS buffers in addition to CMOS buffers.

II. MODIFIED SPLIT CAPACITOR SOLUTION

The current model for the tapered buffer string, shown in Fig. 1, employs an ideal gain stage g_m along with input and output capacitances. The total delay of a chain of n buffers with a tapering factor of β is (for details see [3]):

$$T_{\text{CHAIN}} = n \left(\frac{C_{\text{OUT}}}{g_m} + \frac{\beta C_{\text{IN}}}{g_m} \right) \quad (1)$$

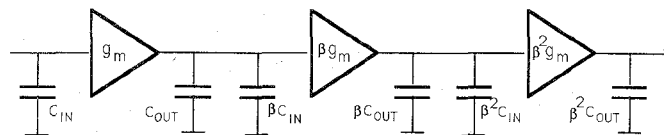


Fig. 1. Split capacitance buffer model for a three-stage buffer chain.

where

$$n = \frac{\ln(C_L/C_{\text{IN}})}{\ln(\beta)}$$

The optimal tapering factor is obtained by differentiating (1) with respect to β , which yields

$$\beta[\ln(\beta) - 1] = C_{\text{OUT}}/C_{\text{IN}}. \quad (2)$$

Included in C_{OUT} is a delay attributed to the short-circuit current [4]: as the threshold input voltage is reached, both the NMOS and PMOS transistors are turned on, producing a brief current between V_{dd} and V_{ss} that bypasses the load. The duration of the short-circuit current is determined by the input rise/fall times, which in turn are determined by β . Unfortunately, the dependence of the short-circuit current on β , and thus the dependence of C_{OUT} on β , was neglected in the derivation of (2), resulting in discrepancies between the β of the formula and that found by simulation. In order to account for this β dependence, a more rigorous analytical derivation could be attempted; however the derivation would be complicated and the resulting formula would be unwieldy and impractical.

One solution to this problem is to determine C_{OUT} using the simulated delay versus load capacitance curve. An example of such a curve is shown in Fig. 2: for a given load capacitance, a tangent to the delay curve is drawn and extended to intersect the abscissa. The total output capacitance C_{OUT} is determined by this intersection point: it is read from the graph as the absolute value of the point of intersection on the abscissa (the intersection occurs at a negative value). This value for C_{OUT} includes the effect of the short-circuit current.

The effect of the input rise/fall times on β can be illustrated using the simulated delay curve: from Fig. 3, increasing β results in an increase in the short-circuit current, which is seen as a corresponding rise in C_{OUT} .

As a first-order approximation, C_{OUT} can be expressed as a linear function of β

$$C_{\text{OUT}} = C_o + k\beta \quad (3)$$

where C_o is the output capacitance with input rise and fall times approaching zero (output capacitance without the

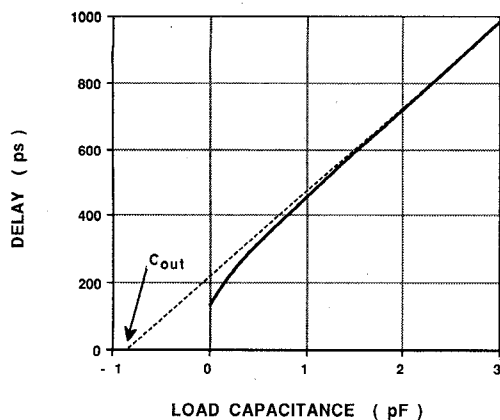


Fig. 2. Delay versus load capacitance of a CMOS buffer.

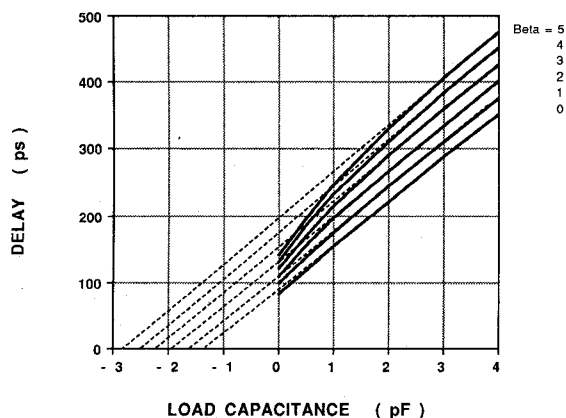


Fig. 3. Buffer delays with different tapering factors.

effect of the short-circuit current), and k is the constant first-order proportionality factor. C_O and k can be determined from delay curves that are simulated for varying tapering factors: in Fig. 3, C_O is determined as the absolute value of the intersection point with the abscissa for $\beta = 0$, and k is the average distance between adjacent intersection points. The buffer represented in Fig. 3 is characterized by $C_O = 1.3$ pF and $k = 0.3$ pF. These values are dependent on device sizes and technology. For example, an equivalent BiCMOS buffer could have a C_O three times larger. The corresponding k value would be smaller, however, since the BiCMOS buffer is less dependent on the input rise and fall times than the CMOS buffer.

Substituting (3) into (1) and differentiating with respect to β , we obtain

$$\beta[\ln(\beta) - 1] = C_O/(C_{IN} + k). \quad (4)$$

This formula is used to determine the optimum β .

Although (3) is an approximation, numerical results have shown that (4) can be used to determine β with good accuracy for a wide range of capacitance ratios. Fig. 4 shows the optimum tapering factors obtained by using the previously derived (2), the newly derived (4), and actual

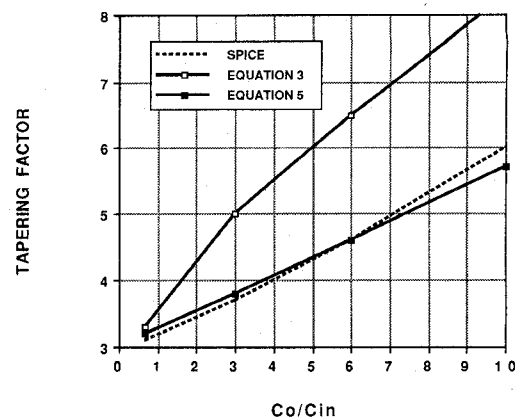


Fig. 4. Simulated and calculated tapering factors as a function of output/input capacitance ratio.

numerical simulations with buffer chains (labeled as SPICE). Since C_O is independent of β (while C_{OUT} is not), C_O/C_{IN} was employed as the independent variable of Fig. 4. The agreement between the tapering factors of (4) and SPICE simulations is very good, indicating that the first-order approximation given by (3) is adequate. On the other hand, (2) consistently overpredicts the value of optimum β especially for larger C_{OUT}/C_{IN} ratios.

The delay curve can also be applied to BiCMOS buffers, for which accurate analytical modeling of the output capacitance is effectively impossible. The C_{OUT}/C_{IN} ratio of BiCMOS buffers can exceed 10, and the application of the modified formula (4) is needed in order to determine the optimum β accurately. The procedure is the same as that outlined above for CMOS.

III. CONCLUSION

The split capacitor model was modified by including the dependency of the input rise/fall times of the buffer on the tapering factor; the expression derived with this dependency predicts the tapering factor with much better accuracy than the original model. The delay versus load capacitance curve has been introduced as an effective tool for use in determination of the buffer output capacitance. In addition, the delay curve alleviates the necessity for an analytical model of the short-circuit current. This approach can be applied to BiCMOS buffer chains, allowing optimum BiCMOS tapering factors to be predicted with the same accuracy.

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