set for the NN is composed of 1000 random input sets of voltage, flux and position values (within the operating range) and of the corresponding current evaluated by eqn. 3. To ensure the passivity of the resulting neural model, a set of 100 positions for both voltage and flux equal to zero has been also included. The best results have been obtained by using the Levenberg–Marquard training algorithm [9], which ensured a global squared error $< 5 \times 10^{-3}$ in just 500 epochs. Fig. 1 shows hysteresis loops with one minor loop computed by the lumped circuit model (i.e. eqn. 3) and by the NN model. The numerical simulation has been carried on for a position value of one quarter. The results agree exactly with those obtained in [1]. An excellent agreement of the results for both models is clearly achieved. This is further pointed out by Fig. 2, where three distinct hysteresis loops for different positions, maximum, minimum and central values, are shown. Hysteresis loops

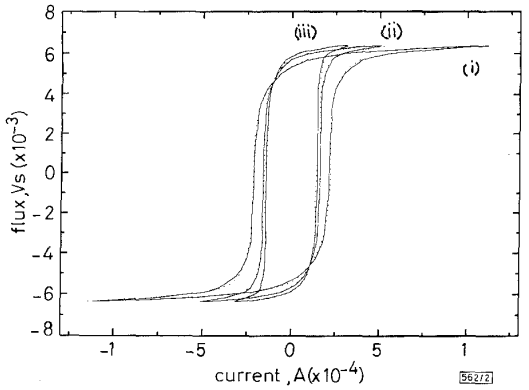

Fig. 2 *Hysteresis loops for different positions*
(i) $x = 0.455$; (ii) $x = 0.167$; (iii) $x = 0.050$
– – – – NN simulations
——— C and S simulations

were computed using both eqn. 3 and the proposed neural network model, resulting in a relative error <5%. These results can be obtained by the proposed NN model more efficiently (both from computational and memory saving points of view) than by the C and S model, whereas the NN approach offers the further advantage of overcoming some intrinsic limitations of voltage-flux modelling (i.e. the current being separable into the dissipating and restoring components).

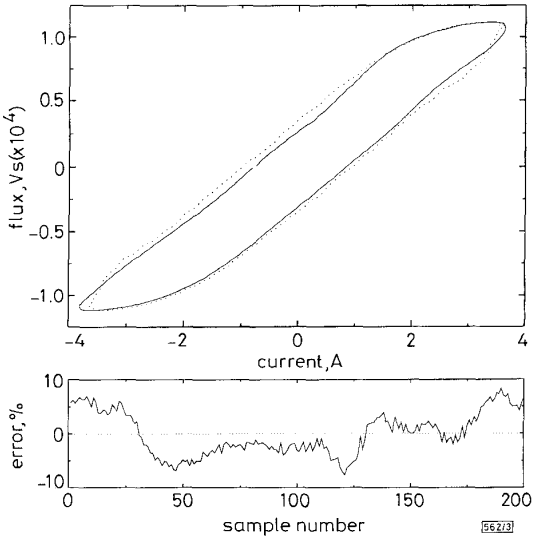

Fig. 3 *Comparison between experimental hysteresis loop and numerical neural network prediction*
– – – – NN simulation
——— experimental result

Experimental results: To further investigate the possibilities offered by the proposed NN approach, we considered the case of a switched reluctance linear actuator prototype, for which a strong dependence on the position of mobile parts on the hysteretic behaviour has been observed [7]. Only one motor winding was energised with a purely sinusoidal voltage supply. Voltage supply and current were acquired at four different positions of the mobile element (within the whole stoke of the actuator). Only one complete wave period was retained using 100 samples. Flux data were then computed by the time integral of the voltage supply. Starting from these data, we considered the same NN described in the preceding Section. The inputs of the NN are voltage, time integral of the voltage (instead of the effective flux) and position. The NN was trained using the sets of data corresponding to extreme positions and one intermediate position, with the Levenberg–Marquard algorithm. The validation set has been constituted by the fourth data acquired.

A direct comparison between measured and acquired data is shown in Fig. 3, which shows a relative error < 8%. The same experimental data were also analysed using the C and S model in [7]. Comparison of results highlights a significant reduction of the computational complexity. Indeed, numerical treatment of experimental measurements was mandatory in [7], whereas the NN approach allows a simpler model determination from experimental data. Moreover, the C and S model requires the splitting of the current into its restoring and dissipating parts, a difficult task for highly distorted voltage supply, while the NN model is directly applicable. In addition, given an arbitrary approximation, the NN memory requirements are smaller than those required by the C and S approach to store the model data into a look-up table, the numerical treatment of measures is greatly simplified, and robustness under noise results from intrinsic lowpass NN behaviour.

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Nonredundant successive approximation register for A/D converters

A. Rossi and G. Fucili

Indexing term: Analogue-digital conversion

A successive approximation register for N bit A/D converters is presented. It codes the possible 2^N conversion output values with the minimum number of FF ($\log_{2N}$), as it is nonredundant and very simple. It allows area optimisation and minor code probability error.

Introduction: The architecture of a successive approximation A/D converter usually [1] consists of a comparator, a D/A converter, and digital control logic, as shown in Fig. 1. The logic is often called 'successive approximation register' (SAR). The function of the SAR is determining the value of each bit in a sequential manner, based on the output of the comparator. If an N bit A/D successive approximation converter is implemented, there are 2^N possible conversion output values so the SAR needs at least 2^N states and so N FF. Background literature [2] reports examples of SAR composed of two separate N bit registers ($2N$ FF): a register (the 'memory' register) stores the conversion result and the other (the 'shift' register) is used to guess the result. A nonredundant SAR uses the minimum number of FF: this can be achieved using the same FF storing the conversion result to code the 2^N possible states of the FSM. The SAR proposed in this Letter uses N FF ass it is nonredundant and very simple.

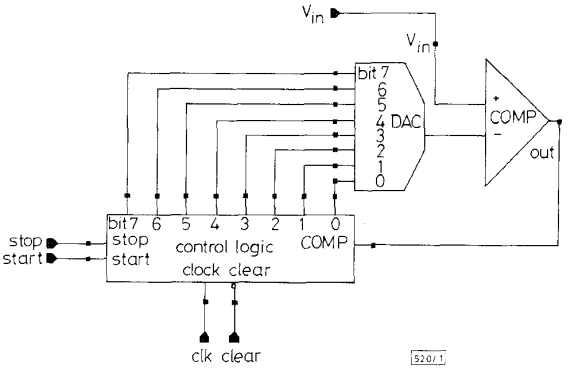

Fig. 1 *Block diagram of a standard 8 bit successive approximation A/D converter*

SAR operation: At the beginning of the conversion (initialisation step) the SAR assumes that the MSB is 1 and all other bits are 0. This digital word is applied to the D/A converter, which generates an analogue signal of 0.5FS (where FS is the range for the analogue input V_{IN}), which is compared to V_{IN}. If the comparator output is high, then the SAR makes the MSB 1. If the comparator output is low, the digital control logic makes the MSB 0. At this point the value of the MSB is known. The successive approximation steps are performed by once more applying a digital word to the D/A converter, with the MSB having its proven value, the second bit guessed at 1 and all the remaining bits having a value of 0. Again, the sampled input is compared to the output of the D/A converter with this digital word applied: if the output of the comparator is high, the second bit is proven to be 1 else 0 and so on until the LSB is determined.

Table 1: FSM sequence, $N = 8$

Conversion step	Input D/A word								Comparator output
0	1	0	0	0	0	0	0	0	a_7
1	a_7	1	0	0	0	0	0	0	a_6
2	a_7	a_6	1	0	0	0	0	0	a_5
3	a_7	a_6	a_5	1	0	0	0	0	a_4
4	a_7	a_6	a_5	a_4	1	0	0	0	a_3
5	a_7	a_6	a_5	a_4	a_3	1	0	0	a_2
6	a_7	a_6	a_5	a_4	a_3	a_2	1	0	a_1
7	a_7	a_6	a_5	a_4	a_3	a_2	a_1	1	a_0
result	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	–

From the above functional description we define the SAR as a sequential finite state machine (FSM) [3] which generates the approximation sequence of N steps (for an N bit converter) reported in Table 1 (for simplicity the $N = 8$ case is reported). Each conversion step corresponds to a state of the FSM, step 0 being the initialisation state. For a generic step (m, $m = 1, ..., N$) three actions on the single bit are possible: forcing a guessing 1, using the decision bit from the comparator, and storing the value of the bit at the (m–1) step.

The successive approximation sequence can also be described by the following algorithm: consider the m conversion step, for the (m+1) step the generic bit (k^{th}) ($k = 0, 1, ..., N$) can take the value of:

– The $(k+1)^{th}$ bit on the left more significant than the k^{th} (k–1, k–2, ..., 0) if all the less significant bits on the right and the k^{th} bit itself have value 0.

– The output of the comparator if all the less significant bits than the k^{th} (k–1, k–2, ..., 0) have value 0 and the kth bit has value 1.

– The k^{th} bit at the (m–1) step if at least one of the less significant bits than the k^{th} (k–1, k–2, ..., 0) is 1.

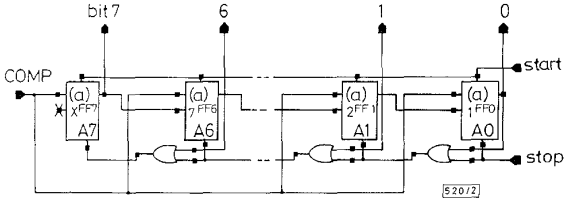

Fig. 2 *8 bit multiple input SAR*

For simplicity the FF inputs clk, clear are not drawn. Each FF has three external inputs, i.e. FF 6 takes the output of the comparator (a), the output of the FF on the left (7), and the output of the OR chain (A_6) as inputs

SAR circuitry: The basic structure of the SAR is a multiple input N bit shift register (see Fig. 2). To start the conversion the 'MSB' FF and all the other FFs are forced to the initialisation state. It is necessary to provide a mechanism that brings the shift register in the initialisation state: one method of loading the initialisation is to use FF with set and reset inputs connected to a control signal (start) which, if active, sets the MSB FF and resets all the other bits. For the next states, a generic FF (k^{th}) must have the possibility of choosing between three data inputs coming from:

– The output of the (k+ 1)th FF (shift right).
– The output of the comparator (a) (data load).
– The output of the (k^{th}) FF itself (memorisation).

By adding a multiplexer and a decoder to each FF the three inputs can be selected (see Fig. 3). Referring to the algorithm for the k^{th} FF, the all-zero state for the less significant bits than the k^{th} (k–1, k–2, ..., 0) is revealed with a OR-chain of the outputs of the FF storing them (see Fig. 2 signal A_K). The decoding logic for the k^{th} multiplexer needs these two selecting inputs to put the SAR in the correct operation mode: the output of the OR-chain of the precedent FF (A) and the output of the k^{th} FF itself (B), as in Table 2, is shown in Fig. 3.

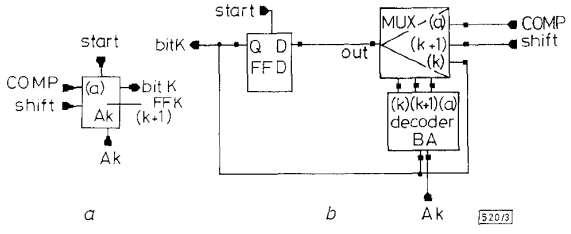

Fig. 3 *k^{th} FF symbol used in Fig. 2 and k^{th} FF internal structure*

Three input multiplexer with its decoding is evidenced
a Symbol used in Fig. 2; *b* Internal structure

To stop the conversion we can use the OR chain applying to the LSB a control signal (stop) which, if active, forces a '1' in all signals A_K so that the SAR operates in the memorisation mode (see Fig. 2). The stop signal is useful in particular when the successive approximation sequence reaches the last step (end of conversion) and the conversion result can be stored in the SAR. The output of the 'LSB' FF can be used to signal the end of conversion.

Table 2: FF outputs

A	B	operation
1	–	memorisation (k)
0	1	data load (a)
0	0	shift right (k+1)

Conclusions: This SAR codes the possible conversion output values with minor code error probability being an FSM with the minimum number of states. Also all these states are allowable conversion output values so the conversion is never stalled. An 8 bit A/D converter including the novel 8 FF SAR [4] was integrated and tested in a Multipower BCD technology and it is currently under production. It shows the correct functionality and a significant area saving (50%).

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Adaptive architecture for signal separation and interference suppression in DS-CDMA systems

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Indexing terms: Code division multiple access, Interference suppression, Cellular radio

In multi-user DS-CDMA cellular communications systems, the conventional (MF) detector performs poorly, making no use of the structure of the interferers. Various detectors offering improved performance have been suggested. The authors describe a new architecture, the 'hybrid', which combines two known techniques, and offers better performance than is achieved seperately with either technique.

Scenario: Consider a chip and symbol synchronous multi-user DS-CDMA cellular radio system, using non-ISI chip shaping and random signature sequences which are transmitted over an AWGN channel. The technique described can be generalised for the asynchronous case, but is easier to explain for the synchronous case as it allows each symbol period to be considered independently. Let the processing gain (chip/symbol) of the system be P_G. The received waveform during one symbol period can be specified by P_G samples from the output of a chip matched filter. These samples define a vector r in P_G dimensional space U. Consider this as the 'direction' of the input waveform. The (known) spreading codes used by the N wanted signals form the columns of the P_G by N matrix S . We define the operator $\mathbf{R}(S)$ as representing the space spanned by the columns of S. Also contributing to r are an unknown number of (inter-cell) interferers with unknown sequences, represented by the matrix S_I which has P_G rows and an unknown number of columns. Thermal noise is included as vector n. The column vectors d and d_I contain the data symbols (one per signal) for the desired and interfering users, respectively, for the current symbol period. The elements of these vectors are assumed to be independently randomly selected from an arbitrary signalling set. Carrier amplitudes and phases can be assumed to be incorporated into d and d_I, and are not considered separately.

The received waveform is

$$\mathbf{r} = \mathbf{S} \cdot \mathbf{d} + \mathbf{S_I} \cdot \mathbf{d_I} + \mathbf{n} \qquad (1)$$

For $N < P_G$, $\mathbf{R}(S)$ is an N dimensional subspace of U. Regardless of carrier phase and amplitude, and the data in d, all energy from the desired signals will be contained in $\mathbf{R}(S)$. Energy in subspace $\mathbf{R}(S)^{\perp}$ is therefore caused by interference or noise from an unknown source. This can he seen by considering that the received waveform can also be expressed as

$$\mathbf{r} = \mathbf{S} \cdot (\mathbf{d} + \mathbf{A} \cdot \mathbf{d_I} + \mathbf{n_S}) + \mathbf{S}^{\perp} \cdot (\mathbf{B} \cdot \mathbf{d_I} + \mathbf{n_{S^{\perp}}}) \qquad (2)$$

where

$$\mathbf{S} \cdot \mathbf{A} + \mathbf{S}^{\perp} \cdot \mathbf{B} \equiv \mathbf{S_I} \qquad (3)$$

and

$$\mathbf{S} \cdot \mathbf{n_S} + \mathbf{S}^{\perp} \cdot \mathbf{n_{S^{\perp}}} \equiv \mathbf{n} \qquad (4)$$

$S^{\perp}$ is any matrix such that $\mathbf{R}(S^{\perp}) = \mathbf{R}(S)^{\perp}$.

As $\mathbf{R}(S)^{\perp}$ only contains energy due to d_I, it can be used to reduce the effects of d_I in $\mathbf{R}(S)$, allowing d to be estimated more reliably.

The proposed detector is a hybrid of two different techniques which have been reported in the literature [1, 3]. These detectors will be briefly discussed, followed by the proposed hybrid detector.

In a realistic DS-CDMA cellular system, the signal received at any given base station will be composed of known intra-cell signals, unknown inter-cell signals, and thermal noise. The hybrid detector scheme is ideally suited to this scenario, considering $\mathbf{R}(S)$ and $\mathbf{R}(S^{\perp})$ separately, resulting in faster and closer convergence. Owing to the mobile channel varying relatively rapidly in practice, convergence speed is important for good tracking performance.

The detector described by Bar-Ness [1] 'assumes' that the input signal is composed of a linear combination of signals with known waveforms, plus noise. This detector estimates data by forming a linear combination of the outputs of a bank of conventional matched filters. The combining weights are determined by an adaptive process which minimises the correlation between the signals after combining. This detector can be considered as a signal separator as it separates out all signals of which it has knowledge, but cannot do anything against unknown interference.

The adaptive detector described by Verdu [3] is a single user detection architecture. Given the same knowledge about the wanted signal as the conventional MF detector, this detector uses a detection waveform $c = s + x$ where s is matched to the desired signal and x is adapted with the goal of minimising the output energy of the filter, with the constraint that x remain orthogonal to s. This detector adapts to the MMSE solution even though it has no knowledge about any of the interference, hence it is a blind interference canceller. It is a good choice in an environment in which nothing is known about the waveforms of the interferer.

If the received waveform consists only of signals with known signature sequences plus noise, the Bar-Ness detector converges faster than the Verdu detector. This is expected since the Bar-Ness detector uses knowledge about the structure of the interference, and thus can adapt against it more readily. If the received waveform also contains some unknown signals, then the Verdu detector generally performs better. Again, this is expected, since the Bar-Ness detector cannot adapt against signals about which it has no explicit knowledge, while the Verdu one can.

The hybrid combines the advantages of both, resulting in a detector which combines signal cancellation and interference suppression. The problems of signal separation, and of interference suppression, are dealt with separately, making better use of the available information. Results are given for two different hybrid architectures. Version '*A*' is discussed as it is simpler to explain its operation, although version '*B*' offers slightly better performance, so results for it are also shown. The difference is that the outputs of the adaptive filters are combined with the matched filter outputs at different points. In the '*A*' detector, signal separation and interference suppression occur in parallel. In the '*B*' detector, interference suppression occurs first, then signal separation; as a result of this the separator is no longer restricted to $\mathbf{R}(S)$, though it is restricted to a similar subspace with the same number of dimensions.

A diagram of the hybrid detector for two desired users is shown in Fig. 1. From the figure, note that in version '*A*' the signal separator operates directly on the matched filter outputs, linearly combining them to obtain modified soft-decision data for each user, which is less affected by intra-cell interference. Because the detector only forms linear combinations of the matched filter outputs, the resulting effective detection waveforms it forms will always lie within $\mathbf{R}(S)$. In version '*B*', the separator acts on the outputs of the combined matched filters and adaptive filters. If the adaptive filter coefficients for each user form the P_G by N matrix X, then the separator operates in $\mathbf{R}(S+X)$, which will vary during the adaptation process.