MODELING SIGMA-DELTA MODULATOR NON-IDEALITIES IN SIMULINK®

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ABSTRACT

This paper presents a complete set of SIMULINK® models, which allow exhaustive behavioral simulations of any sigma-delta modulator to be performed. The proposed set of models takes into account most of the sigma-delta modulator non-idealities, such as sampling jitter, kT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages). For each model we present a description of the considered effect as well as all of the implementative details. Simulation results on a second-order switched-capacitor sigma-delta modulator demonstrate the validity of the models proposed.

1. INTRODUCTION

Sigma-Delta ($\Sigma\Delta$) modulators are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, reduced antialiasing filtering requirements and robust analog implementation. Moreover, by trading accuracy with speed, Sigma-Delta modulators allow high performance to be achieved with low sensitivity to analog component imperfections and without requiring component trimming. In the design of high-resolution Switched-Capacitor (SC) Sigma-Delta modulators we have typically to optimize a large set of parameters, including the performance of the building blocks, in order to achieve the desired signal-to-noise ratio. In view of the inherent non-linearity of the Sigma-Delta modulator loop this optimization process has to be carried out with behavioral simulations. Therefore, in this paper we present a complete set of SIMULINK® [1] models, which allow us to perform exhaustive behavioral simulations of any Sigma-Delta modulator taking into account most of the non-idealities, such as sampling jitter, kT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages).

The following sections describe in detail each of the models presented. Finally, simulation results, which demonstrate the validity of the models proposed, are provided. All the simulations were carried out on a classical 2nd-order SC $\Sigma\Delta$ modulator architecture.

2. CLOCK JITTER

The effect of clock jitter on an SC $\Sigma\Delta$ modulator can be calculated in a fairly simple manner, since the operation of a SC circuit depends on complete charge transfers during each of the clock phases. In fact, once the analog signal has been sampled the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal. This means also that the effect of clock jitter on a $\Sigma\Delta$ modulator is independent of the structure or order of the modulator.

Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal to the converter. The error introduced when a sinusoidal signal with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given by

$$x(t+\delta) - x(t) \approx 2\pi f_{in}\,\delta A\,\cos(2\pi f_{in} t) = \delta \frac{d}{dt}x(t) \quad (1)$$

This effect can be simulated with SIMULINK® by using the model shown in Fig. 1, which implements Eqn. (1). Here, we assumed that the sampling uncertainty δ is a Gaussian random process with standard deviation $\Delta\tau$ (parameter 'delta' in Fig. 1). Whether oversampling is helpful in reducing the error introduced by the jitter depends on the nature of the jitter. Since we assume the jitter white, the resultant error has uniform power spectral density from 0 to $f_s/2$, with a to-

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tal power of $(2\pi f_{in}\,\Delta\tau\,A)^2/2$. In this case, the total error power will be reduced by the oversampling ratio [2].

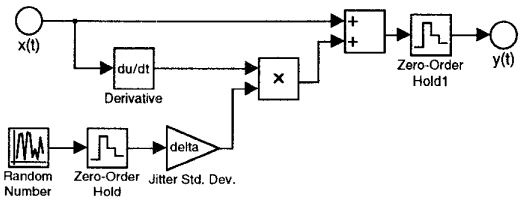

Figure 1. Modeling a random sampling jitter

3. INTEGRATOR NOISE

The most important noise sources affecting the operation of an SC ΣΔ modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifier. The total noise power of the circuit is the sum of the theoretical loop quantization noise power, the switch noise power and the op-amp noise power. Because of the large low-frequency gain of the first integrator, the noise performance of a ΣΔ modulator is determined mainly by the switch and op-amp noise of the input stage.

These effects can be successfully simulated with SIMULINK® using the model of a "noisy" integrator shown in Fig. 2, where the coefficient b represents the integrator gain which, referring to the schematic of a single-ended SC integrator shown in Fig. 3, is equal to C_s/C_f. Each noise source and its relevant model will be described in the following sub-sections.

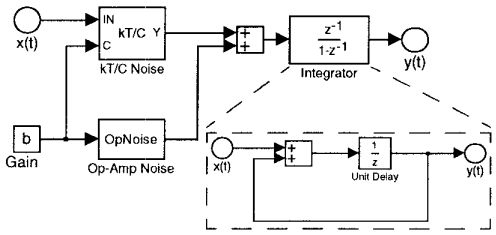

Figure 2. Model of a "noisy" integrator

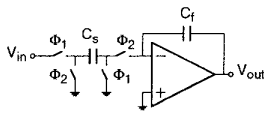

Figure 3. Single-ended SC integrator

3.1. Switches Thermal Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidths of op-amps. Therefore, it must be taken into account for both the switches and the op-amps in an SC circuit. Consider the sampling capacitor C_s in the single-ended SC integrator shown in Fig. 3. This is in series with a switch, with finite resistance R_{on}, that periodically opens, sampling a noise voltage onto the capacitor. The total noise power can be found evaluating the integral [3]

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_s)^2}df = \frac{kT}{C_s} \qquad (2)$$

where k is the Boltzman constant, T the absolute temperature and the resistance is modeled with a noise source in series with power $4kTR_{on}\,\Delta f$. The switch thermal noise voltage e_T (usually called kT/C noise) is superimposed to the input voltage $x(t)$ leading to

$$y(t) = [x(t)+e_T(t)]b = \left[x(t)+\sqrt{\frac{kT}{bC_f}}n(t)\right]b, \qquad (3)$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation, while b is the integrator gain. Eqn. (3) is implemented by the model shown in Fig. 4.

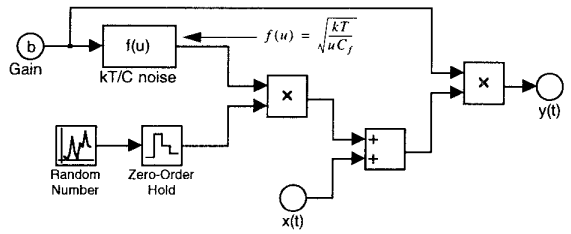

Figure 4. Modeling switches thermal noise (kT/C block)

Since the noise is aliased in the band from 0 to $F_s/2$, its final spectrum is white with a spectral density

$$S(f) = \frac{2kT}{F_s C_s} \qquad (4)$$

Typically the first integrator will have two switched input capacitors, one carrying the signal and the other providing the feedback from the modulator output, each of them contributing to the total noise power.

3.2. Op-Amp Noise

Fig. 5 shows the model used to simulate the effect of the op-amp noise. Here, V_n represents the total rms noise voltage referred to the op-amp input. Flicker ($1/f$) noise, wide-band thermal noise and dc offset contribute to this value. The total op-amp noise power V_n^2 can be evaluated, through circuit simulation, on the circuit of Fig. 3 during phase Φ_2, by adding the noise contributions of all the devices referred to the op-amp input and integrating the resulting value over the whole frequency spectrum.

4. INTEGRATOR NON-IDEALITIES

The SIMULINK® model of an ideal integrator with unity gain is shown in the inset of Fig. 2. Its transfer function is:

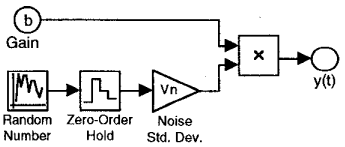

Figure 5. Op-amp noise model

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{5}$$

Analog circuit implementations of the integrator deviate from this ideal behavior due to several non-ideal effects. One of the major causes of performance degradation in SC ΣΔ modulators, indeed, is due to incomplete transfer of charge in the SC integrators. This non-ideal effect is a consequence of the op-amp non-idealities, namely finite gain and bandwidth, slew rate and saturation voltages. These will be considered separately in the following subsections. Fig. 6 shows the model of the real integrator including all the non-idealities.

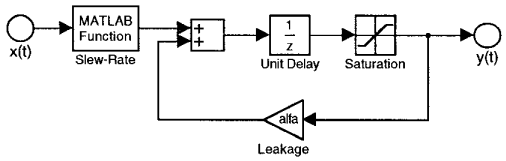

Figure 6. Real integrator

4.1. DC Gain

The dc gain of the integrator described by (5) is infinite. In practice, however, the gain is limited by circuit constraints. The consequence of this integrator "leakage" is that only a fraction α of the previous output of the integrator is added to each new input sample (parameter 'alfa' in Fig. 6). The transfer function of the integrator with leakage becomes:

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \tag{6}$$

The dc gain H_0 becomes therefore:

$$H_0 = H(0) = \frac{1}{1 - \alpha} \tag{7}$$

The limited gain at low frequencies increases the in-band noise.

4.2. Bandwidth and Slew Rate

The finite bandwidth and the slew-rate of the op-amp are modeled in Fig. 6 with a building block placed in front of the integrator which implements a MATLAB® function. The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain [4]. With reference to the SC integrator shown in Fig. 3, the evolution of the output node during the *n*th integration period (when Φ_2 is on) is:

$$v_0(t) = v_0(nT - T) + \alpha V_s\left(1 - e^{-\frac{t}{\tau}}\right),\ nT - \frac{T}{2} < t < nT \tag{8}$$

where $V_s = V_{in}(nT - T/2)$, α is the integrator leakage and $\tau = 1/(2\pi\,\mathrm{GBW})$ is the time constant of the integrator (GBW is the unity gain frequency of the op-amp when loaded by C_f). The slope of this curve reaches its maximum value when $t = 0$, resulting in

$$\left.\frac{d}{dt}v_0(t)\right|_{max} = \alpha\frac{V_s}{\tau} \tag{9}$$

We must consider now two separate cases:

1. The value specified by (9) is lower than the op-amp slew-rate, *SR*. In this case there is not slew-rate limitation and the evolution of v_0 fits Eqn. (8).
2. The value specified by (9) is larger than *SR*. In this case, the op-amp is in slewing and, therefore, the first part of the temporal evolution of v_0 ($t < t_0$) is linear with slope *SR*. The following equations hold (assuming $t_0 < T$):

$$t \le t_0 \quad v_0(t) = v_0(nT - T) + \mathrm{SR}t \tag{10}$$

$$t > t_0 \quad v_0(t) = v_0(t_0) + (\alpha V_s - \mathrm{SR}t_0)\left(1 - e^{-\frac{t - t_0}{\tau}}\right) \tag{11}$$

Imposing the condition for the continuity of the derivatives of (10) and (11) in t_0, we get

$$t_0 = \frac{\alpha V_s}{\mathrm{SR}} - \tau \tag{12}$$

If $t_0 \ge T$ only Eqn. (10) holds.

The MATLAB® function in Fig. 6 implements the above equations to calculate the value reached by $v_0(t)$ at time *T*, which will be different from V_s due to the gain, bandwidth and slew-rate limitations of the op-amp. The slew-rate and bandwidth limitations produce harmonic distortion reducing the total signal-to-noise+distortion ratio (SNDR) of the ΣΔ modulator.

4.3. Saturation

The dynamic of signals in a ΣΔ modulator is a major concern. It is therefore important to take into account the saturation levels of the op-amp used. This can simply be done in SIMULINK® using the saturation block inside the feedback loop of the integrator, as shown in Fig. 6.

5. SIMULATION RESULTS

To validate the models proposed of the various non-idealities affecting the operation of an SC ΣΔ modulator, we performed several simulations with SIMULINK® on the 2nd-order modulator shown in Fig. 7 [2], where only the non-idealities of the first integrator were considered, since their effects are not attenuated by the noise shaping. The simulation parameters used are summarized in Tab. 1 and corre-

sponds to audio standards. A minimum SNDR of 96 dB (i.e. a resolution of 16 bits) is required for audio performance.

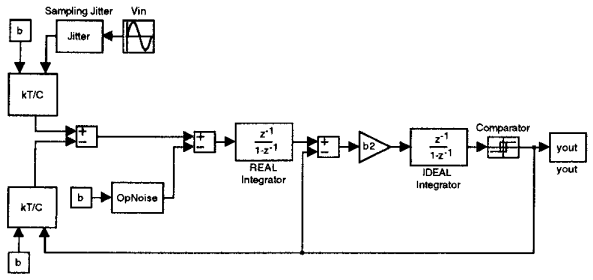

Figure 7. Second-order $\Sigma\Delta$ modulator

Tab. 2 compares the total SNDR and the corresponding equivalent resolution in bits of the ideal modulator, which are the maximum obtainable with the architecture and parameters used, with those achieved with the same architecture when one single limitation at a time is introduced.

Parameter	*Value*
Signal bandwidth	BW = 22.05 kHz
Oversampling frequency	F_s = 11.2896 MHz
Oversampling ratio	R = 256
Samples number	N = 65536
Integrator gains	$b = b_2 = 0.5$

Table 1. Simulation parameters

Integrator non-ideality	*SNDR [dB]*	*Resolution [bits]*
Ideal modulator	101.5	16.56
Sampling jitter ($\Delta\tau$ = 8 ns)	98.6	16.09
Switches (kT/C) noise (C_s = 5 pF)	98.7	16.11
Input-referred op-amp noise (V_n = 50 μV_{rms})	96.6	15.75
Finite dc gain ($H_0 = 1 \cdot 10^3$)	101	16.48
Finite bandwidth (GBW = 100 MHz)	86.7	14.11
Slew-rate (SR = 17 V/μs)	77.8	12.63
Saturation voltages (V_{max} = ± 1.34 V)	96.8	15.79

Table 2. Simulation results

Fig. 8 compares the power spectral densities (PSD) at the output of the modulator, when two of the most significant non-idealities in the first integrator are taken into account, with the PSD of the ideal modulator. The spectra put in evidence how the kT/C noise increases the in-band noise floor, while the slew-rate produces harmonic distortion. It must be noted from the above results that the non-ideal effects resulting from practical circuit limitations add up and contribute to increase the in-band noise-plus-distortion and, therefore, can become a severe limitation to the performance achievable from a given architecture. The models presented in this paper allow us to carefully predict, at the behavioral level, the performance of the real modulator.

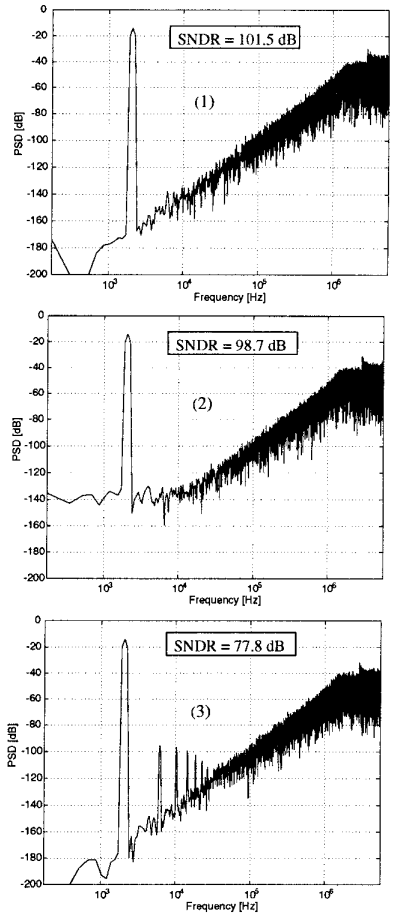

Figure 8. PSD of (1) the ideal modulator; (2) with kT/C noise, C_s = 5 pF; (3) with SR = 17 V/μs

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