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// Generated for: spectre
// Generated on: Feb 18 17:47:25 2020
// Design library name: sen_Pseudo_Resistor
// Design cell name: pseudo_PP2_test
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/opt/ams410/spectre/c35/processOption.scs"
parameters X=0
include "/opt/ams410/spectre/c35/cmos53.scs" section=cmosmc
include "/opt/ams410/spectre/c35/res.scs" section=resmc
include "/opt/ams410/spectre/c35/cap.scs" section=capmc
include "/opt/ams410/spectre/c35/bip.scs" section=bipmc
include "/opt/ams410/spectre/c35/ind.scs" section=indmc
include "/opt/ams410/spectre/c35/esddiode.scs" section=esddiodemc

// Library name: sen_Pseudo_Resistor
// Cell name: pseudo_PP2
// View name: schematic
// Inherited view list: verilogams veriloga behavioral functional module
//schematic spectre symbol
subckt pseudo_PP2 GND VA VB VDD VOC
   MP3 (net5 net5 VB VB) modp w=4u l=4u as=3.4e-12 ad=3.4e-12 ps=5.7u \
      pd=5.7u nrd=0.125 nrs=0.125 ng=1
   MP2 (net5 net5 VOC VOC) modp w=4u l=4u as=3.4e-12 ad=3.4e-12 ps=5.7u \
      pd=5.7u nrd=0.125 nrs=0.125 ng=1
   MP1 (net6 net6 VOC VOC) modp w=4u l=4u as=3.4e-12 ad=3.4e-12 ps=5.7u \
      pd=5.7u nrd=0.125 nrs=0.125 ng=1
   MP0 (net6 net6 VA VA) modp w=4u l=4u as=3.4e-12 ad=3.4e-12 ps=5.7u \
      pd=5.7u nrd=0.125 nrs=0.125 ng=1
ends pseudo_PP2
// End of subcircuit definition.

// Library name: PRIMLIB
// Cell name: presistor
// View name: schematic
// Inherited view list: verilogams veriloga behavioral functional module
//schematic spectre symbol
subckt presistor PLUS MINUS
parameters c=0 r=1K
   C1 (PLUS 0) capacitor c=c/2.
   C2 (MINUS 0) capacitor c=c/2.
   R0 (PLUS MINUS) resistor r=r
ends presistor
// End of subcircuit definition.

// Library name: sen_Pseudo_Resistor
// Cell name: pseudo_PP2
// View name: av_extracted
// Inherited view list: verilogams veriloga behavioral functional module
//schematic spectre symbol
subckt pseudo_PP2_av_extracted GND VA VB VDD VOC
   c1 (VA \1\:GND) capacitor c=4.24466e-16 m=1
   c2 (VB \1\:GND) capacitor c=4.30065e-16 m=1
   c3 (VOC \1\:GND) capacitor c=6.18219e-16 m=1
   c4 (\4\:net5 \6\:net6) capacitor c=1.27752e-17 m=1
   c5 (\2\:net5 \3\:VB) capacitor c=9.33827e-16 m=1
   c6 (\4\:VOC \6\:net5) capacitor c=2.25536e-16 m=1
   c7 (\2\:net6 \3\:VA) capacitor c=8.59416e-16 m=1
   c8 (\7\:VOC \6\:net6) capacitor c=2.59378e-16 m=1
   c9 (\6\:net5 \2\:VOC) capacitor c=6.8827e-16 m=1
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c10 (\4\:net5 \3\:net6) capacitor c=1.84927e-17 m=1
c11 (\4\:net5 \4\:VOC) capacitor c=7.73376e-17 m=1
c12 (\6\:net6 \5\:VOC) capacitor c=6.03886e-16 m=1
c13 (\4\:net5 \1\:GND) capacitor c=1.67741e-16 m=1
c14 (\4\:net6 \1\:GND) capacitor c=1.67741e-16 m=1
c15 (\4\:net5 \2\:VOC) capacitor c=1.21237e-15 m=1
c16 (\4\:net6 \5\:VOC) capacitor c=1.10389e-15 m=1
c17 (\3\:net5 \4\:VOC) capacitor c=3.39504e-17 m=1
c18 (\5\:net5 \3\:VB) capacitor c=4.62274e-17 m=1
c19 (\3\:net6 \7\:VOC) capacitor c=4.08038e-17 m=1
c20 (\5\:net6 \3\:VA) capacitor c=4.03202e-17 m=1
c21 (\4\:VOC \1\:GND) capacitor c=8.42713e-18 m=1
c22 (\3\:net5 \2\:VOC) capacitor c=1.15736e-17 m=1
c23 (\3\:net6 \5\:VOC) capacitor c=9.99216e-18 m=1
c24 (\3\:VB \1\:GND) capacitor c=5.12853e-17 m=1
c25 (\3\:VA \1\:GND) capacitor c=5.68389e-17 m=1
c26 (\1\:VOC \1\:GND) capacitor c=5.23351e-16 m=1
c27 (net5 \1\:GND) capacitor c=1.67853e-16 m=1
c28 (net5 \2\:net6) capacitor c=1.27492e-17 m=1
c29 (net5 \3\:VB) capacitor c=1.53076e-15 m=1
c30 (net6 \3\:VA) capacitor c=1.35353e-15 m=1
c31 (net5 \5\:net6) capacitor c=1.768e-17 m=1
c32 (net6 \1\:GND) capacitor c=1.67853e-16 m=1
re2 (\2\:VA VA) presistor c=0 r=0.3902
re3 (\1\:VA \2\:VA) presistor c=0 r=11.88
re4 (\3\:VA \2\:VA) presistor c=0 r=5.94
re6 (\2\:VB VB) presistor c=0 r=0.3856
re7 (\1\:VB \2\:VB) presistor c=0 r=11.88
re8 (\3\:VB \2\:VB) presistor c=0 r=5.94
re9 (\3\:net6 \4\:net6) presistor c=0 r=12.1532
re10 (\4\:net6 net6) presistor c=0 r=0.5656
re11 (net6 \5\:net6) presistor c=0 r=12.1433
re12 (\3\:net5 \4\:net5) presistor c=0 r=12.1582
re13 (\4\:net5 net5) presistor c=0 r=0.5656
re14 (net5 \5\:net5) presistor c=0 r=12.1582
re15 (\1\:GND \2\:GND) presistor c=0 r=1.8382
re16 (\2\:GND GND) presistor c=0 r=0.2528
re17 (\1\:GND \2\:GND) presistor c=0 r=1.485
re18 (\1\:VDD \2\:VDD) presistor c=0 r=1.7499
re19 (\2\:VDD \3\:VDD) presistor c=0 r=0.3532
re20 (\3\:VDD VDD) presistor c=0 r=0.1346
re21 (\1\:VDD \2\:VDD) presistor c=0 r=0.7425
re22 (\1\:VDD \3\:VDD) presistor c=0 r=0.7425
re23 (VOC \1\:VOC) presistor c=0 r=0.3092
re24 (\1\:VOC \3\:VOC) presistor c=0 r=0.2203
re25 (\3\:VOC \4\:VOC) presistor c=0 r=11.88
re26 (\1\:VOC \6\:VOC) presistor c=0 r=0.1856
re27 (\6\:VOC \7\:VOC) presistor c=0 r=11.88
re28 (\2\:VOC \3\:VOC) presistor c=0 r=5.94
re29 (\5\:VOC \6\:VOC) presistor c=0 r=5.94
rg1 (net6 \2\:net6) presistor c=0 r=19.5549
rg2 (net5 \2\:net5) presistor c=0 r=19.8581
rg3 (\6\:net6 \4\:net6) presistor c=0 r=20.0389
rg4 (\6\:net5 \4\:net5) presistor c=0 r=20.14
avD41_1 (\1\:GND \1\:VDD) nwd area=2.37075e-10 perimeter=9.79e-05 m=1
MP0 (\5\:net6 \2\:net6 \1\:VA \3\:VA) modp w=4e-06 l=4e-06 as=3.8p \
   ad=3.4p ps=5.9u pd=5.7u nrd=8.175e-02 nrs=8.175e-02 ng=1
MP3 (\5\:net5 \2\:net5 \1\:VB \3\:VB) modp w=4e-06 l=4e-06 as=3.8p \
   ad=3.4p ps=5.9u pd=5.7u nrd=8.175e-02 nrs=8.175e-02 ng=1
MP1 (\7\:VOC \6\:net6 \3\:net6 \5\:VOC) modp w=4e-06 l=4e-06 as=3.4p \
   ad=3.8p ps=5.7u pd=5.9u nrd=8.175e-02 nrs=8.175e-02 ng=1
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   MP2 (\4\:VOC \6\:net5 \3\:net5 \2\:VOC) modp w=4e-06 l=4e-06 as=3.4p \
      ad=3.8p ps=5.7u pd=5.9u nrd=8.175e-02 nrs=8.175e-02 ng=1
   avD41_2 (\1\:GND \3\:VA) nwd area=5.248e-11 perimeter=2.92e-05 m=1
   avD41_3 (\1\:GND \3\:VB) nwd area=5.248e-11 perimeter=2.92e-05 m=1
   avD41_4 (\1\:GND \5\:VOC) nwd area=5.248e-11 perimeter=2.92e-05 m=1
   avD41_5 (\1\:GND \2\:VOC) nwd area=5.248e-11 perimeter=2.92e-05 m=1
ends pseudo_PP2_av_extracted
// End of subcircuit definition.

// Library name: sen_Pseudo_Resistor
// Cell name: pseudo_PP2_test
// View name: schematic
// Inherited view list: verilogams veriloga behavioral functional module
//schematic spectre symbol
I27 (0 net09 net012 vdd! VOC_schematic) pseudo_PP2
I24 (0 net2 net6 vdd! VOC_layout) pseudo_PP2_av_extracted
V6 (vdd! 0) vsource dc=3.3 type=dc
V5 (net012 0) vsource dc=1.65-X type=dc
V4 (net09 0) vsource dc=1.65+X type=dc
Vo2 (net6 0) vsource dc=1.65-X type=dc
Vo1 (net2 0) vsource dc=1.65+X type=dc
simulatorOptions options reltol=100e-6 vabstol=1e-6 iabstol=1e-12 temp=27 \
   tnom=27 homotopy=all limit=delta scalem=1.0 scale=1.0 \
   compatible=spice2 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 digits=5 \
   cols=80 pivrel=1e-3 sensfile="../psf/sens.output" checklimitdest=psf
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
dc dc param=X start=-1.65 stop=1.65 step=10m oppoint=rawfile maxiters=150 \
   maxsteps=10000 annotate=status
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub
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