```
// Generated for: spectre
// Generated on: Aug 16 18:22:30 2016
// Design library name: eds16m011
// Design cell name: sec_ord
// Design view name: schematic
simulator lang=spectre
global 0
include "/home/cadence/cadence_tools/cadence_ms_labs_614/models/spectre/gpdk.scs" section=stat

// Library name: eds16m011
// Cell name: inv_biasing
// View name: schematic
subckt inv_biasing out vdd vin\+ vin\- vss
    NM0 (out vin\- net5 vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    NM1 (net5 net010 vss vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    NM2 (net010 vin\+ net5 vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    PM2 (net010 vin\+ net09 vdd) pmos1 w=(2u) l=1u as=800f ad=800f \
        ps=3.46667u pd=3.46667u m=(1)*(3)
    PM1 (net09 net010 vdd vdd) pmos1 w=(2u) l=1u as=800f ad=800f \
        ps=3.46667u pd=3.46667u m=(1)*(3)
    PM0 (out vin\- net09 vdd) pmos1 w=(2u) l=1u as=800f ad=800f \
        ps=3.46667u pd=3.46667u m=(1)*(3)
    C0 (out 0) capacitor c=1p
ends inv_biasing
// End of subcircuit definition.

// Library name: eds16m011
// Cell name: tiq
// View name: schematic
subckt tiq vdd vin vout vss
    NM2 (vout net2 vss vss) nmos1 w=(1u) l=1u as=600f ad=300f ps=3.2u \
        pd=1.6u m=(1)*(2)
    NM0 (net2 vin vss vss) nmos1 w=(1u) l=1u as=600f ad=300f ps=3.2u \
        pd=1.6u m=(1)*(2)
    PM0 (net2 vin vdd vdd) pmos1 w=(8.5u) l=1u as=5.1p ad=5.1p ps=18.2u \
        pd=18.2u m=(1)*(1)
    PM2 (vout net2 vdd vdd) pmos1 w=(8.5u) l=1u as=5.1p ad=5.1p ps=18.2u \
        pd=18.2u m=(1)*(1)
ends tiq
// End of subcircuit definition.

// Library name: eds16m011
// Cell name: dff_tri
// View name: schematic
subckt dff_tri ck ckbar q qbar vdd vin vss
    NM4 (net17 q vss vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    NM3 (qbar ckbar net17 vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    NM2 (q qbar vss vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
    NM1 (net21 vin vss vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    NM0 (qbar ck net21 vss) nmos1 w=(2u) l=1u as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
    PM4 (net023 q vdd vdd) pmos1 w=(8u) l=1u as=4.8p ad=4.8p ps=17.2u \
        pd=17.2u m=(1)*(1)
    PM3 (qbar ck net023 vdd) pmos1 w=(8u) l=1u as=4.8p ad=4.8p ps=17.2u \
        pd=17.2u m=(1)*(1)
    PM2 (q qbar vdd vdd) pmos1 w=(8u) l=1u as=4.8p ad=4.8p ps=17.2u \
        pd=17.2u m=(1)*(1)
    PM1 (net024 vin vdd vdd) pmos1 w=(8u) l=1u as=4.8p ad=4.8p ps=17.2u \
        pd=17.2u m=(1)*(1)
    PM0 (qbar ckbar net024 vdd) pmos1 w=(8u) l=1u as=4.8p ad=4.8p ps=17.2u \
        pd=17.2u m=(1)*(1)
ends dff_tri
// End of subcircuit definition.

// Library name: eds16m011
// Cell name: sec_ord
// View name: schematic
I52 (net035 vd 0 net014 vs) inv_biasing
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I0 (net20 vd 0 net6 vs) inv_biasing
I56 (vd net035 net29 vs) tiq
I32 (c cb con net030 vd conn vs) dff_tri
I2 (cb c q qb vd net29 vs) dff_tri
V8 (net11 0) vsource dc=-50m type=dc
V7 (net13 0) vsource dc=50m type=dc
V1 (vs 0) vsource dc=-450m type=dc
V0 (vd 0) vsource dc=450m type=dc
NM10 (net037 cd net013 net013) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
NM9 (net035 cb net014 net014) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
NM8 (net20 cbd conn conn) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
NM7 (net013 cb 0 0) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
NM5 (conn q net13 vs) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
NM4 (conn qb net11 vs) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
NM3 (net03 c 0 0) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
NM2 (net20 c net6 vs) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
NM1 (net31 cbd net03 vs) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u \
        pd=5.2u m=(1)*(1)
NM0 (net14 cd con con) nmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
C8 (net037 net035) capacitor c=1p
C7 (net013 conn) capacitor c=500.0f
C6 (net014 net013) capacitor c=1p
C2 (net31 net20) capacitor c=1p
C5 (net6 net03) capacitor c=1p
C3 (net03 con) capacitor c=250f
V2 (net14 0) vsource dc=0 type=sine ampl=225m freq=1K
V6 (cbd 0) vsource type=pulse val0=0 val1=900.0m period=10u delay=5.1u \
        rise=100n fall=100n width=3u
V5 (cd 0) vsource type=pulse val0=0 val1=900.0m period=10u delay=100.0n \
        rise=100n fall=100n width=3u
V4 (cb 0) vsource type=pulse val0=0 val1=900.0m period=10u delay=5u \
        rise=100n fall=100n width=3u
V3 (c 0) vsource type=pulse val0=0 val1=900.0m period=10u rise=100n \
        fall=100n width=3u
PM0 (conn q net11 vd) pmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
NM6 (conn qb net13 vd) pmos1 w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
pss  pss  fund=1K  harms=0  annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
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