```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3
 4  entity my_clock is
 5     generic( f_osc: integer := 50_000_000;
 6              f_clk: integer := 1_000_000);
 7     port(    mclk:  in std_logic;
 8               rst:  in std_logic;
 9               clk: out std_logic);
10  end entity;
11
12  architecture arch of my_clock is
13  begin
14     process(mclk, rst)
15        variable counter: integer range 0 to f_osc := 0;
16        variable state: std_logic := '0';
17     begin
18        if(rst = '1') then
19           counter := 0;
20        elsif(mclk'event and mclk = '0') then
21           counter := counter + 1;
22           if(counter < f_clk / 2) then
23              state := '0';
24           elsif(counter >= f_clk / 2) then
25              if(counter = f_clk) then
26                 counter := 0;
27                 state := '0';
28              else state := '1';
29              end if;
30           end if;
31        end if;
32        clk <= state;
33     end process;
34  end arch;
```