A 2.45 GHz Low Cost, High Performance VCO

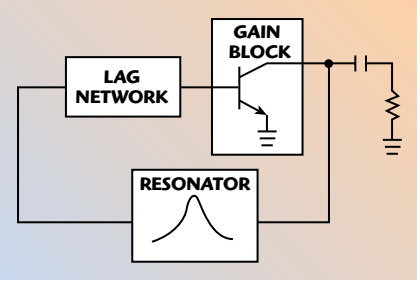
This article addresses performance and cost issues associated with voltage-controlled oscillator design. Although the example design is application specific, the methods demonstrated apply to microwave oscillator design in general. CAE and on-the-bench techniques are used for a comprehensive approach to the designing of microwave oscillators.

Engineers are under constant pressure to reduce the cost of microwave designs without sacrificing their performance. At 100 K volumes, oscillators can be produced at a fraction of the cost when compared to that of small-quantity purchased oscillators. This article presents a design procedure along with a practical example. An attempt is made to clarify some of the concerns associated with low cost, high performance microwave oscillator design. Performance considerations include low phase noise, linear monotonic tuning, low harmonic emissions and adequate output power.

INITIAL TOPOLOGY SELECTION

All oscillator circuits require a gain block and a feedback method. The topology used here is based on the Barkhausen criteria for oscillation. ***Figure 1*** shows that the design requires a network to provide the gain, a frequency selection network (resonator) and enough phase lag so that the overall phase for the loop is equal to 2π radians. A small-signal scattering parameter approach is used to evaluate the design. This method enables the use of a network analyzer for the bench evaluation.

Fig. 1 A basic oscillator configuration.



Before proceeding with the design, Lesson's equation for single-sideband phase noise $\mathcal{L}_{PM}$ is examined.[1] The various factors concerning single-sideband phase noise can be considered using this equation:

$$\mathcal{L}_{PM}\left(\text{dBc / Hz}\right) = 10\log\left[\frac{1}{2}\left[\left[\left(\frac{F}{2Qfm}\right)^2 + 1\right] \bullet \left(\frac{C}{fm} + 1\right) \bullet \left(\frac{NkT}{P}\right)\right] + \frac{2kTR_vK_v^2}{fm^2}\right]$$

where

k = Boltzmann's constant
T = temperature in Kelvin
F = frequency of oscillation
fm = offset frequency
Q = loaded Q
P = RF power at amplifier input
N = noise factor
C = flicker noise corner frequency
R_v = tuning diode noise resistance
K_v = tuning gain (MHz/V)

(The equation has been modified to include the effects of varactor tuning.) Practical reduction of the oscillator's noise sidebands is addressed by increasing the loaded Q and signal-to-noise ratio (SNR) and decreasing both the flicker and varactor modulation noise contributions.

Jim Carlini
Detection Systems
Fairport, NY

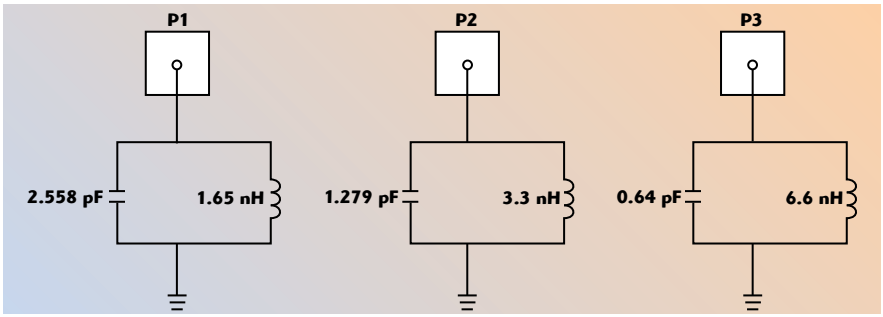


Fig. 2 Three 2.45 GHz tank circuits used in the simulation.

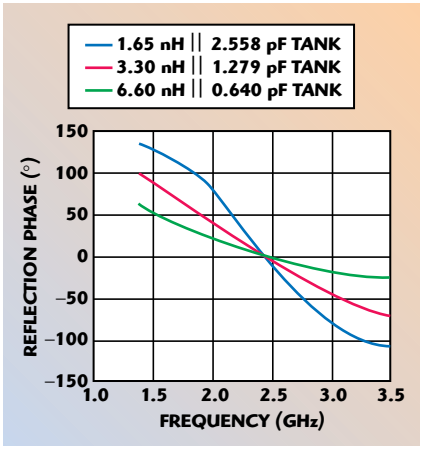


Fig. 3 Simulation results for the three tank circuits.

RESONATOR DESIGN

The unloaded Q of the resonator ultimately limits the oscillator's loaded Q. The relationship between the loaded Q and noise sidebands can be written as $-10\log(Q_{loaded})^2$. This relationship holds true until the ratio of the loaded Q to unloaded Q exceeds 2/3. To achieve a high unloaded Q the design must maintain the lowest possible series resistance and achieve the lowest possible L/C ratio for the components used in the tank. A fast change in the reflection phase on either side of the resonant frequency indicates a high unloaded Q. ***Figure 2*** shows three 2.45 GHz tanks used in the simulation. The simulation results shown in ***Figure 3*** clearly indicate that the 1.65 nH || 2.558 pF tank circuit produces a rapid change in the reflection phase on either side of the resonant frequency, making it the best L/C combination for the proposed resonator.

A novel design approach was taken that uses a Coilcraft microspring air-core coil. (This coil is available at greatly reduced cost when compared to that of a typical distributed ceramic or Teflon resonator.) It was estimated that the 1.65 nH coil could maintain a Q of at least 180 at 2.5 GHz. This Q value was determined to be high enough for the intended resonator design. The air-core inductor is a primary component in lower frequency RF oscillator designs. The problem at microwave frequencies is that the inductor Q degrades with frequency, particularly as the coil approaches its self-resonant frequency (SRF). The SRF for the 1.65 nH inductor is greater than 10 GHz, thus eliminating this concern.

Care must be used in the selection of the tank circuit's capacitive element. As the capacitor's reactance is reduced, its potential to reduce the unloaded Q of the intrinsic tank resonator is increased. A new line of high Q RF capacitors made by American Technical Ceramics was investigated. It was determined that these RF capacitors displayed an equivalent series resistance (ESR) similar to that of most microwave capacitors at 2.5 GHz but with a substantial reduction in cost. ***Figure 4*** shows the circuits used in the simulation. As the ESR of the capacitors used in the tank increases, the overall Q of the tank will decrease. As the tank's unloaded Q is reduced, its 3 dB bandwidth increases. This characteristic is shown in ***Figure 5*** using single-port Z parameters. The 0.707 point of the Z parameter's magnitude response represents the tank circuit's 3 dB bandwidth. Note how the band edges move out in frequency as the capacitor's ESR increases from 0.2 to 0.8 Ω.

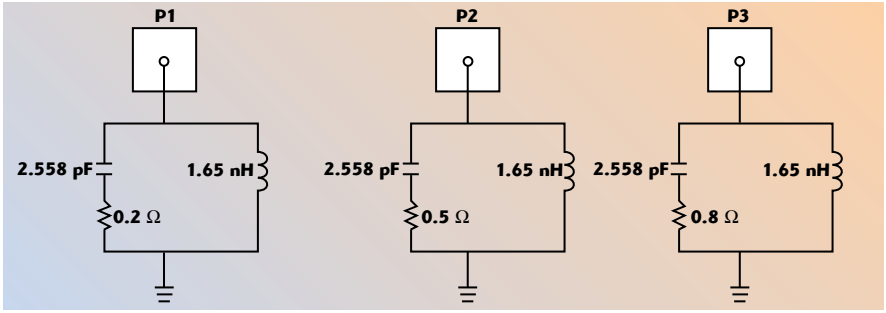


Fig. 4 Tank circuits used for the Z-magnitude simulation.

RESONATOR DECOUPLING

The resonator is now evaluated as a two-port network. Decoupling elements are used to improve the resonator's loaded Q. This configuration provides valuable insight concerning the design of the intended oscillator. One method used to study the loaded Q for a two-port network is to evaluate the rate of change in the phase slope, which can be expressed as $d\phi/d\omega$ or group delay GD. The group delay differentiation process eliminates the linear portion of the phase response and transforms the deviations from linear phase into deviations from constant group delay. It can be shown that the loaded Q is related to the group delay by $Q_{loaded} = \pi f_o GD$. Group delay is the rate of change in the phase of the forward transmission coefficient vs. frequency. The nice thing about using group delay as a figure of merit in resonator design is that it can be evaluated with a simulator such as Microwave Harmonica and also measured on the bench with a network analyzer. Note that the end coupling capacitors used increase the capacitive loading on the tank resonator. This effect requires the capacitor(s) in the tank circuit to be

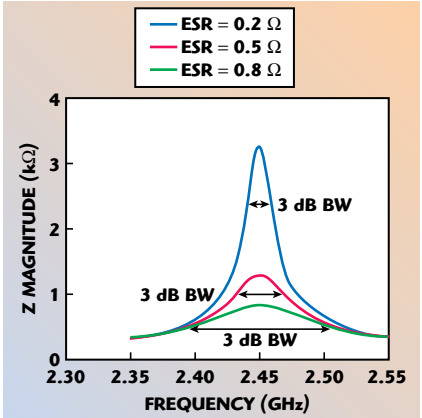


Fig. 5 Effects of the capacitor's ESR on the tank circuit's Q.

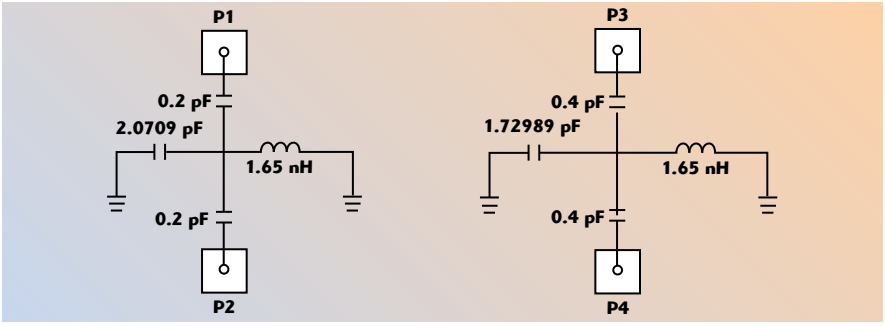


Fig. 6 The decoupled resonators.

tweaked in order to re-center the resonator's center frequency.

To examine the trade-offs concerning insertion loss and loaded Q, a swept display of several decoupled resonators is shown. Different degrees of decoupling were used, as shown in ***Figure 6***. The 1.65 nH inductor is held constant while the tank's capacitor is adjusted to center the frequency at 2.5 GHz. The simulation results shown in ***Figure 7*** clearly display the increase in both group delay and insertion loss as the amount of decoupling is increased. The degree of decoupling used in the final oscillator is a trade-off between the goals of adequate start-up gain and maintaining the resonator's loaded Q.

GAIN BLOCK DESIGN

Often a discrete transistor can provide a much more cost-effective solution than a MMIC. Although a little more work is involved in designing an oscillator using a discrete solution, it is well worth it if low cost is a primary design concern. It is also advisable (although not necessary) to use a device that presents a reasonable degree of match at the intended frequency of oscillation. The device's close match helps to ease the oscillator's gain requirements.

A network that can provide for good spurious suppression should surround the transistor and usually produces unconditional stability at low RF frequencies. At lower frequencies, simple resistor biasing can be used to accomplish this goal. As the frequency increases, it is advisable to use choke biasing networks in order to avoid degrading the gain of the transistor any more than need be. A useful method for preventing modding is to use resistive loading at out-of-band frequencies. This configuration is used so as not to degrade the gain at the desired frequency. A resistor in the DC biasing network also can be used for the prevention of spurious moding. This goal is accomplished using a 51 Ω resistor. ***Figure 8*** shows the intended gain block.

The required biasing current has a strong effect on the oscillator's close-in noise performance. As the bias current is increased, the close-in phase noise that results from the device transposing low frequency baseband noise is degraded. This low frequency AM and PM noise is converted into frequency fluctuations at the carrier by a nonlinear mixing process. This type of noise is referred to as 1/f noise. In addition, as the bias current is increased the device's noise figure also increases, further degrading the oscillator's noise performance. This result is due to a decrease in the oscillator's SNR. Contrasting the goals of minimizing the transistor's bias current to reduce noise is the fact that the signal portion of the oscillator's SNR is improved with increased bias current. This effect occurs because the absolute value for the noise sidebands does not vary with the signal level produced by the oscillator. It has been noted that both noise figure and low frequency 1/f noise (flicker noise) are not affected significantly by an increase in the bias voltage.

After evaluating cost and performance for various families of transistors, an NE6X6-type device was chosen. These transistors are reasonably priced, and data from the manufacturer show that the NE6X6 devices have both low noise figure and low 1/f noise characteristics. The transistor's V_{CEO} (collector to emitter breakdown voltage with the base held open) is 6 V DC. With V_{CE} set to 3 V, there is ample margin for peak-to-peak variations in the steady-state signal.

It was decided to use the simple biasing network shown previously to reduce circuit complexity and cost. A DC bias current of approximately 10 mA was used to determine a balance for the various noise-related bias concerns. In addition, S-parameter data with 10 mA bias are available from the manufacturer for the entire 6X6 family of transistors.

SUBSTRATE CONSIDERATIONS

Since the design frequency is 2.45 GHz, the PCB material is a significant consideration. In this application it is considered preferable that the utilized

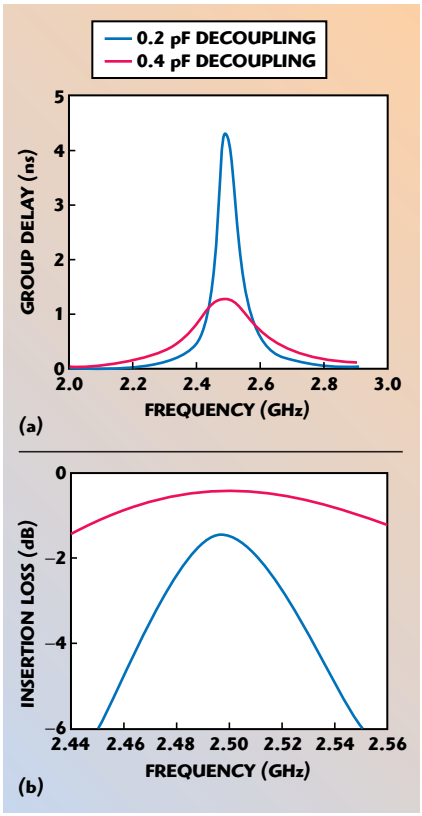


Fig. 7 Decoupled resonator performance; (a) group delay and (b) insertion loss.

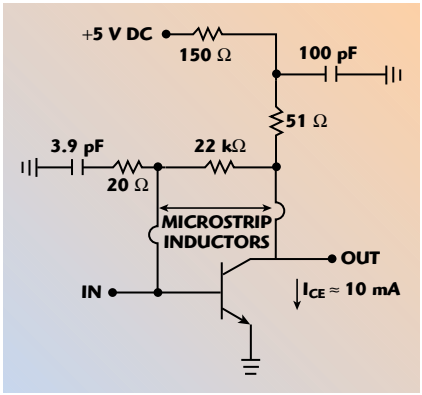


Fig. 8 The gain block's schematic.

material be very inexpensive and provide a well-controlled dielectric constant. This characteristic is required because the printed portion of the circuit is used to control the amount of phase lag between the transistor and resonator. Since the printed portion of the circuit exhibits only a relatively minimal effect on the resonator's loaded Q and loop gain, the attenuation resulting from the substrate's dielectric losses was not considered overly critical. After evaluating several options, including various sources of FR4 material, it was decided to use a low cost material available from GIL Technologies with a dielectric constant of 3.86 ±0.08. In addition, the substrate material is available for approximately the same price as FR4.

THE FINAL CONFIGURATION

Having chosen the topology, a linear simulation was performed. This procedure allows for precise adjustments in the phase for the intended design. A 2 pF capacitor located at the collector is used to couple the signal to the 50 Ω load. The initial schematic for the oscillator is shown in ***Figure 9***. A break in the circuit is produced in order to enable a two-port analysis technique to be used. It is best to make the break at a point in the circuit where a reasonable degree of match exists. The goal is to adjust the decoupling capacitors C2 and C3 to allow enough gain for the start-up condition while minimizing the degradation to the loaded Q. The desired gain margin for the open loop in this design is between 3 and 4 dB. A minimum of 3 dB is suggested for adequate start-up gain. The 4 dB maximum is recommended to prevent the transistor from hard limiting any more than necessary. As the transistor is driven harder into limiting, it will tend to increase the production of undesired harmonics. Reducing the loop gain also helps reduce the change in the transmission phase during the oscillator's transition from small-signal to large-signal conditions.

It is critical for the transmission phase to be 0° at the peak of the resonator magnitude response. It has been shown that degradation in the resulting noise sidebands due to nonoptimal transmission phase is related by 40log(cos θ).[8] The microstrip transmission lines are used to adjust transmission phase. After simulating the intended oscillator design with various transistors from the NE6X6 family it was determined that the model NE696M01 device would produce the required start-up gain. The f_t for the NE696M01 transistor is 14 GHz with a 3 V, 10 mA bias. This f_t is somewhat higher than desired for a 2.45 GHz oscillator and is typical of the type of trade-offs involved in oscillator design. The simulation of the intended oscillation is shown in ***Figure 10***. A 50 Ω, 0.61 λ length of microstrip is used to bring the transmission phase to 0° at 2.45 GHz. The gain response is peaked at 2.45 GHz. A gain of 2.63 dB is a bit low but considered enough for start-up concerns. The simulator shows that the group delay is 4.67 ns. The loaded Q for the small-signal simulation is approximately 36. (This Q value shows the potential for low noise performance.) The goals for the initial simulation stage of the oscillator design have been achieved.

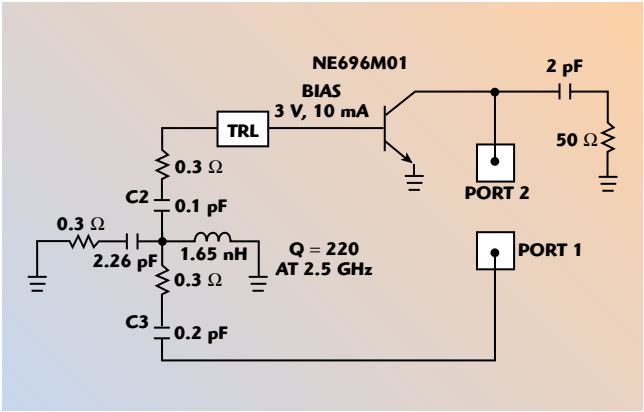


Fig. 9 The initial oscillator schematic.

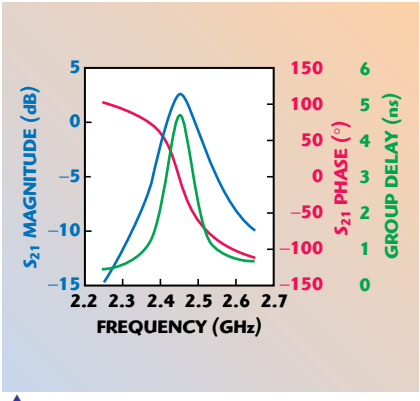
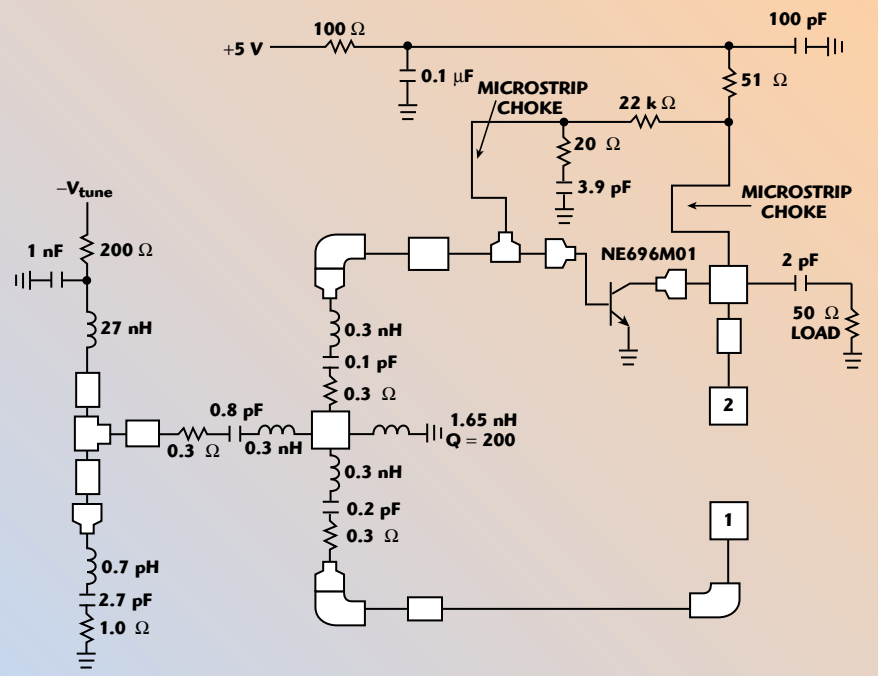


Fig. 10 The open-loop simulation.

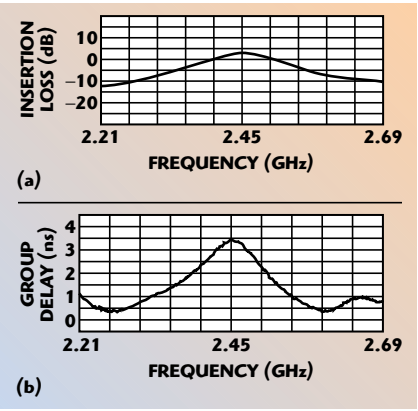
TUNING CONSIDERATIONS

Tuning of the oscillator's center frequency is accomplished by using a varactor tuning diode. Since the cost of the components becomes a critical concern the tolerance used is often not as tight as that of more extensive components. As an example, a 0.2 pF capacitor nearly doubles in price as the component tolerance is increased from ±0.1 to ±0.05 pF. It is advisable to allow for deviation in the center frequency as a result of component variations when evaluating tuning options. This design is intended for use in security sensor applications and is required to tune from 2.435 to 2.465 GHz. The oscillator's tuning bandwidth must extend far enough on either side of these band edges to account for all of the component tolerance variations. This concern must be juggled with the fact that the tuning diode's noise contribution is magnified as its tuning gain is increased. The tuning gain is simply df/dV. The tuning diode is decoupled to reduce its tuning gain by using a capacitive series combination in the resonator tank circuit. One of these capacitors is the tuning diode.

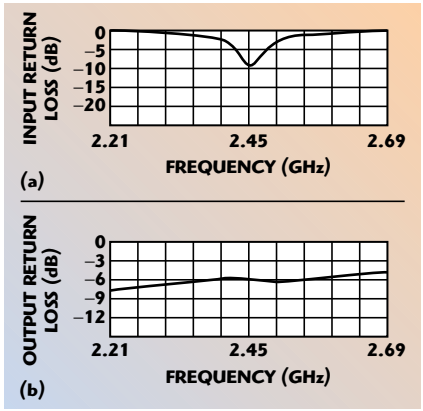
The tuning diode's effect on the oscillator's phase noise performance can vary greatly depending on the type of tuning diode used, its tuning gain and its Q. The modulation noise produced by the tuning diode is summed with the noise sidebands of the oscillator and can degrade the oscillator's phase noise performance. Much of this noise is due to the modulation of the tuning diode junction capacitance by baseband noise. Reducing the baseband biasing resistance helps to reduce varactor modulation noise. In this design the varactor biasing resistor is only 200 Ω. In addition, using a varactor with a less abrupt tuning curve reduces the tuning diode's nonlinearity. However, as the tuning curve becomes less abrupt, tuning linearity may be sacrificed. Furthermore, the tuning diode's series resistance degrades the oscillator's loaded Q. It is suggested that samples of various tuning diodes be evaluated on the test bench prior to final selection.



▲ *Fig. 11 The final schematic.*



▲ *Fig. 12 The oscillator's (a) insertion loss and (b) group delay.*

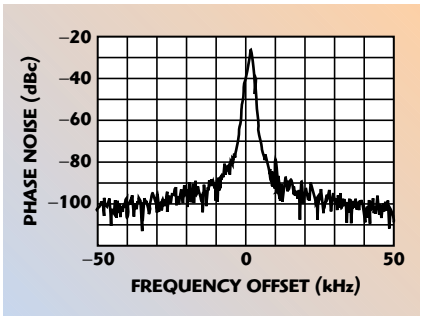


▲ *Fig. 13 The oscillator's (a) input and (b) output return losses.*

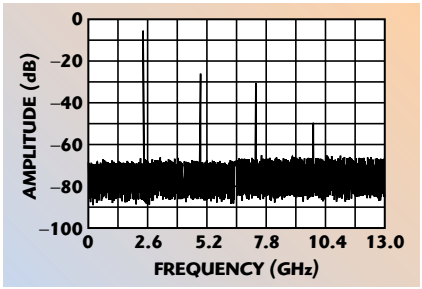
THE FINAL PROTOTYPE

The final schematic is shown in ***Figure 11***. The rest of the microstrip has been added, and provisions for the tuning diode have been made. The phase has been tweaked to adjust for various distributed discontinuities and parasitic reactances. Low inductance microwave grounding is maintained by using 31-mil-diameter vias to decouple all lumped components.

Having established a promising design with the simulator, the prototype VCO was constructed. An HP 8720B vector network analyzer (VNA) was used to evaluate the open-loop oscillator. The number of test frequency points determines the minimum resolution when recording group delay data on the VNA. This resolution is then increased from minimum by varying the VNA's smoothing aperture. In this way the best possible display of group delay is obtained. A display of the oscillator group delay and insertion loss is shown in ***Figure 12***. The magnitude of both transmission responses is peaked at the intended frequency of oscillation. The input and output return loss of the resonator is shown in ***Figure 13***. The low reflections measured at the resonant frequency validate the VNA analysis technique. Having analyzed the group delay, the actual loaded Q is determined to be 26. This value is 25 percent lower than the original simulated value and is attributed to slightly tighter coupling in the actual circuit. However, a loaded Q of 26 is considered respectable for such a low cost design and justifies the resonator selection.

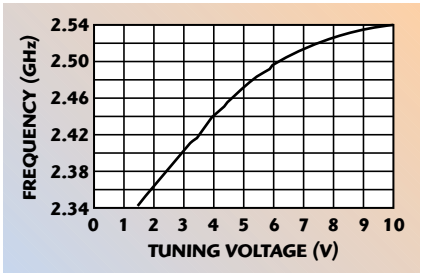


▲ *Fig. 14 The oscillator's phase noise at 2.45 GHz in a 1 kHz RBW with 20 dB input attenuation.*



▲ *Fig. 15 The oscillator's harmonics.*

Fig. 16 The oscillator's output frequency vs. tuning voltage. ▼



After evaluation of the oscillator with the network analyzer, the closed-loop analysis is performed and the complete circuit is assembled. The output power and phase noise were measured. ***Figure 14*** shows the phase noise to be –95 dBc at 10 kHz offset using a 1 kHz resolution bandwidth. This noise level is considered more than adequate for most communication receiver applications. The output power is 5.2 dBm at 2.45 GHz, which is a respectable signal level. The resulting RF-to-DC efficiency is greater than nine percent. The VCO's harmonics are shown in ***Figure 15***. It is apparent by the fact that the second harmonic is down by approximately 20 dB that the emission's performance is quite satisfactory. By varying the tuning voltage between 3.3 and 5.9 V the frequency changed linearly from 2.41 to 2.49 GHz. ***Figure 16*** shows the output

frequency vs. applied tuning voltage. Across this tuning span the output power varied by only 1.3 dB and variations in phase noise were measured to be less than 2 dB. Tuning was accomplished using a low cost SMV1234-079 tuning diode from Alpha Industries. A second oscillator was built and tested in order to verify the design. (The test results were nearly identical.) Using typical high volume pricing this circuit was built for less than $1.30.

CONCLUSION

A design technique for using a commercially available simulator (Microwave Harmonica) to evaluate low cost options for a 2.45 GHz oscillator has been demonstrated. The design was later analyzed on the bench using a VNA and spectrum analyzer and was shown to display low phase noise, linear tuning and low harmonic emissions. The output power was verified to be more than adequate for many applications. The only on-the-bench optimization was to the tuning diode used. A practical microwave oscillator design has been demonstrated.

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Jim Carlini *has been in the field of RF electronics since 1980 and is currently an RF design engineer at Detection Systems. He spent many years working on microwave receivers for the government and defense electronics industry, and now designs wireless UHF data links as well as S- and X-band microwave sensor products for security applications. One of his main responsibilities is the investigation of low cost design solutions. Carlini's primary interest is in microwave electronics.*