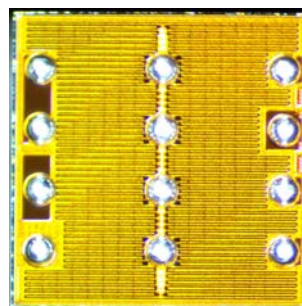


EPC2025 – Enhancement Mode Power Transistor

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Features:

- V_{DS} , 300V
- Maximum $R_{DS(ON)}$, 150 m Ω
- I_D , 4 A
- Pb-Free (RoHS Compliant), Halogen Free



Applications:

- Ultra High Frequency DC-DC conversion
- Medical
- Solar
- LED Lighting

EPC2025 eGaN[®] FETs are supplied only in passivated die form with solder bars

Die Size: 1.95 mm x 1.95 mm

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	300 V
Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
Continuous Drain Current, 25 °C, θ_{JA} = 26	4 A
Maximum Pulsed Drain Current, 25 °C, T_{pulse} = 300 μ s	20 A
Optimum Temperature Range	-40 °C < T_J < 150 °C

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Voltage (BV_{DSS})	$V_{GS} = 0$ V, $I_D = 120$ μ A	300 V
Maximum Drain – Source Leakage	$V_{DS} = 240$ V, $V_{GS} = 0$ V	100 μ A
Maximum $R_{DS(ON)}$	$V_{GS} = 5$ V, $I_D = 3$ A	150 m Ω
Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1$ mA	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	$V_{GS} = 5$ V	2 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -4$ V	-100 μ A

$T_J = 25$ °C unless otherwise stated

Specifications are with Substrate shorted to Source where applicable

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DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C_{ISS} (Input Capacitance)	$V_{DS} = 240\text{ V}, V_{GS} = 0\text{ V}$	194 pF
C_{OSS} (Output Capacitance)		38 pF
C_{RSS} (Reverse Transfer Capacitance)		0.1 pF
Q_G (Total Gate Charge)	$V_{DS} = 240\text{ V}, I_D = 3\text{ A}$	1850 pC
Q_{GS} (Gate to Source Charge)		610 pC
Q_{GD} (Gate to Drain Charge)		300 pC
$Q_{G(TH)}$ (Gate Charge at Threshold)		420 pC
Q_{OSS} (Output Charge)	$V_{DS} = 240\text{ V}, V_{GS} = 0\text{ V}$	20 nC
Q_{RR} (Source-Drain Recovery Charge)		0

$T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

Specifications are with Substrate shorted to Source where applicable

THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	12	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	64	$^{\circ}\text{C/W}$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

EPC2025 – Enhancement Mode Power Transistor

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Figure 1:

EPC2025: Typical Output Characteristics at 25°C

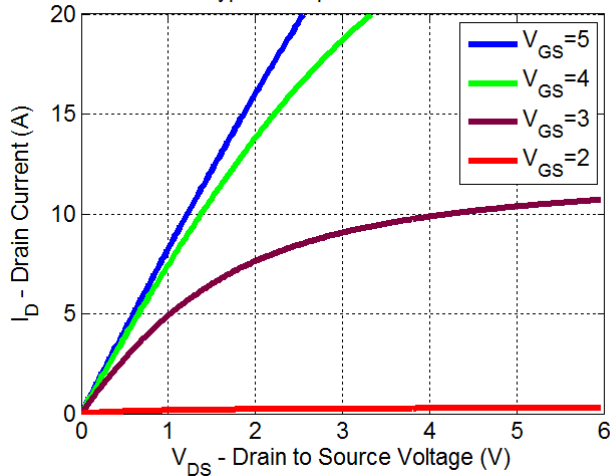


Figure 2:

EPC2025: Transfer Characteristics

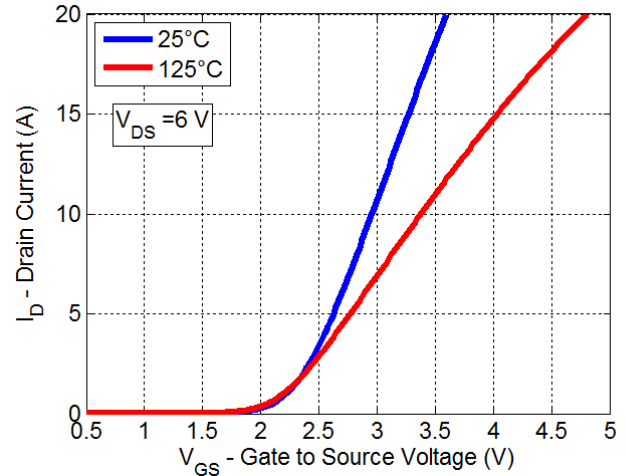


Figure 3:

EPC2025: $R_{DS(ON)}$ vs V_{GS} for Various Drain Currents

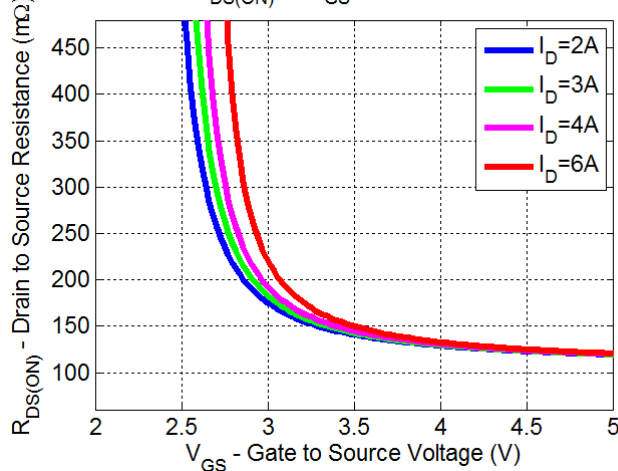


Figure 4:

EPC2025: $R_{DS(ON)}$ vs V_{GS} for Various Temperatures

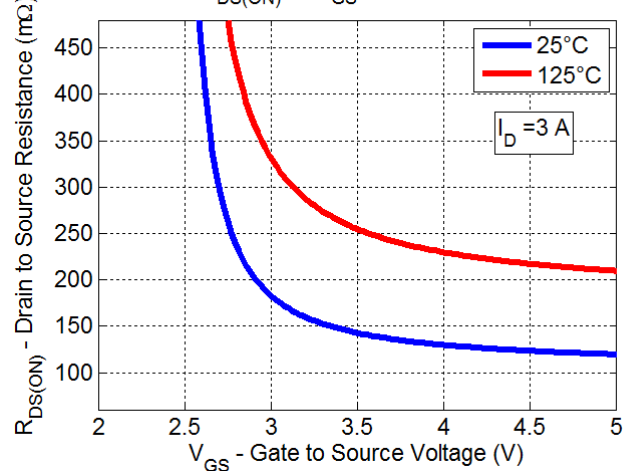


Figure 5a:

EPC2025: Capacitance (Linear Scale)

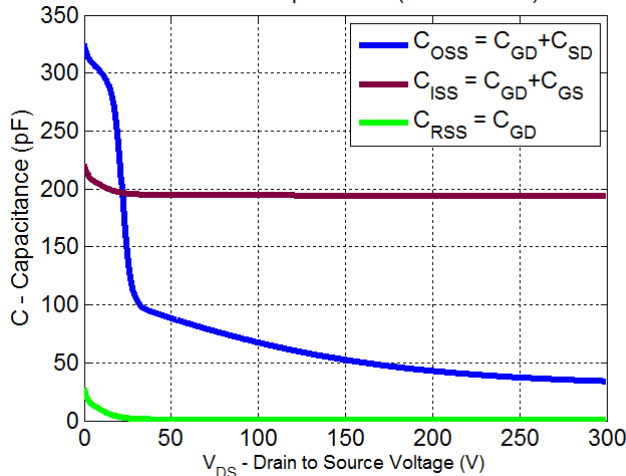
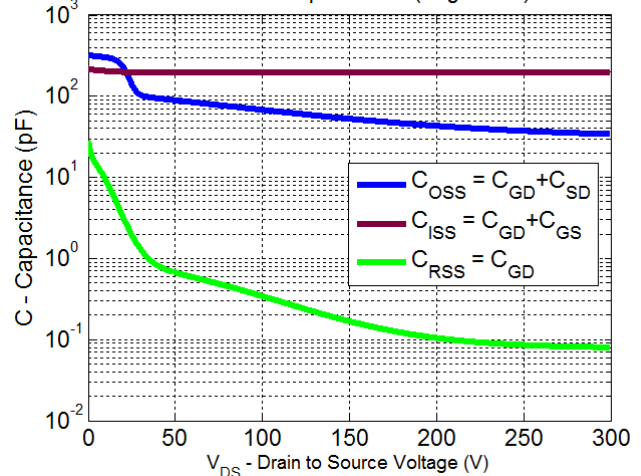


Figure 5b:

EPC2025: Capacitance (Log Scale)



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Figure 6:

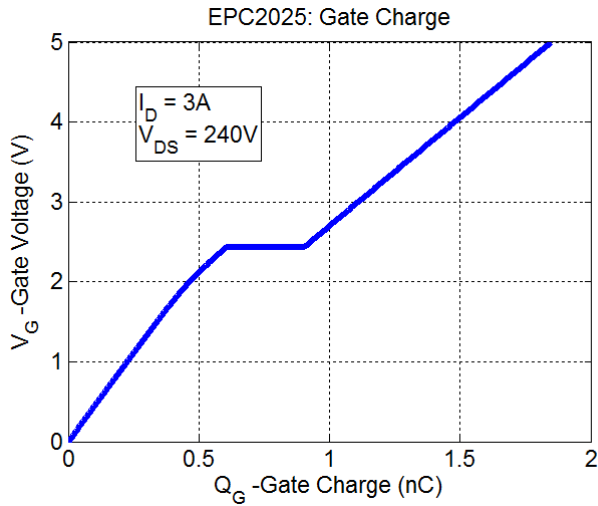


Figure 7:

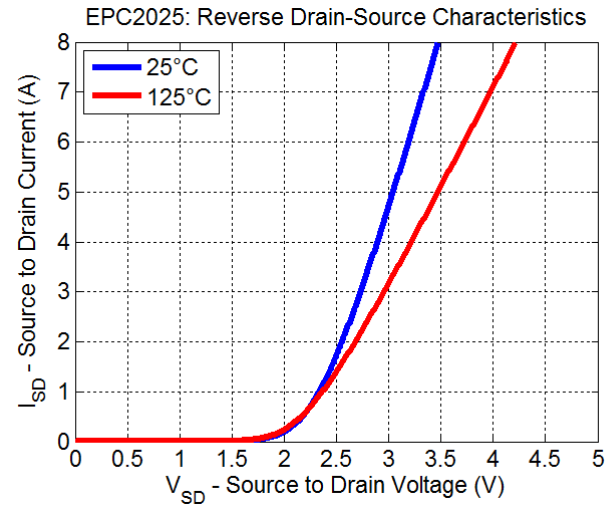


Figure 8:

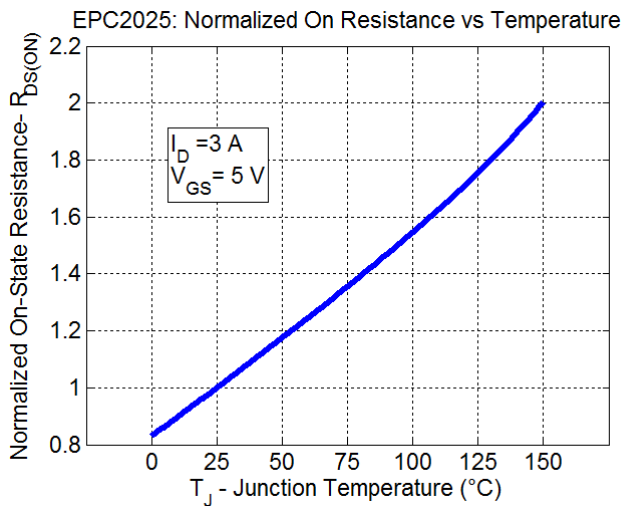
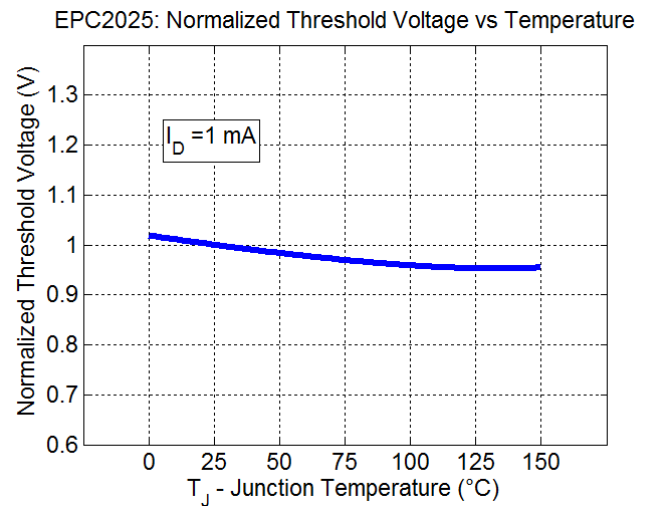


Figure 9:

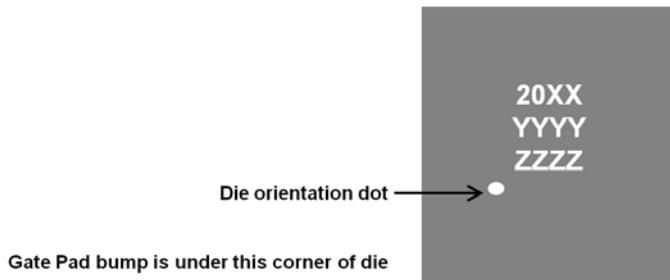


All measurements were done with substrate shorted to source

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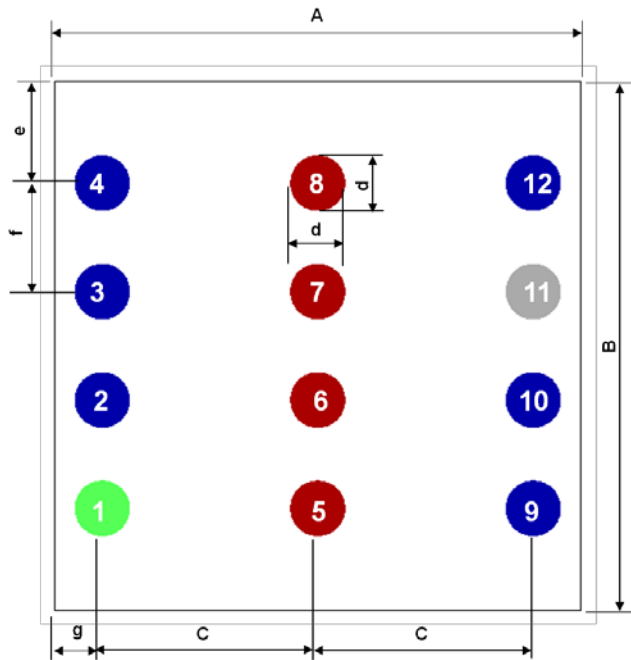
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2025ENGR	20xx	YYYY	ZZZZ

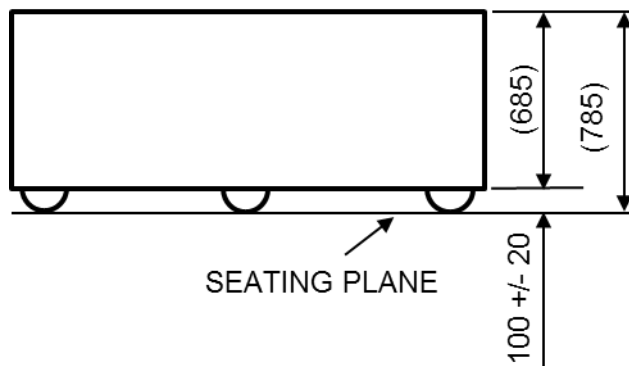
DIE OUTLINE

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1920	1950	1980
B	1920	1950	1980
C	800	800	800
d	197	200	203
e	360	375	390
f	400	400	400
g	160	175	190

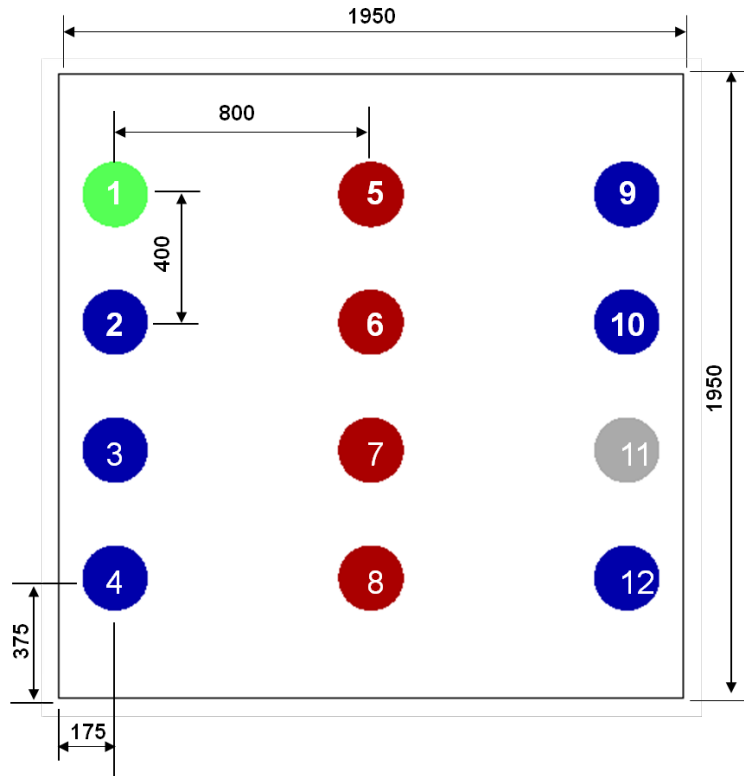
Side View



EPC2025 – Enhancement Mode Power Transistor Preliminary Specification Sheet

RECOMMENDED LAND PATTERN

(Units in μm)



Pad 1 is Gate
Pad 2,3,4,9,10,12 are Source
Pad 5,6,7,8 are Drain
Pad 11 is Substrate

Land pattern is solder mask defined

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398

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