4 Passive Components

In this chapter, a brief summary of the main characteristics of the passive components that are essential to the design of any integrated circuits will be given.

4.1 MOS Capacitors

The analysis of the MOS capacitor is generally the first step in the study of the MOSFET transistor. As a matter of principle, we can regard it as a capacitor having plane and parallel plates, the polysilicon gate and the doped silicon, with the gate oxide as insulator.

In practice, it is possible to fabricate a capacitor by contacting the source and drain junctions of a transistor, as depicted in Fig. 4.1.

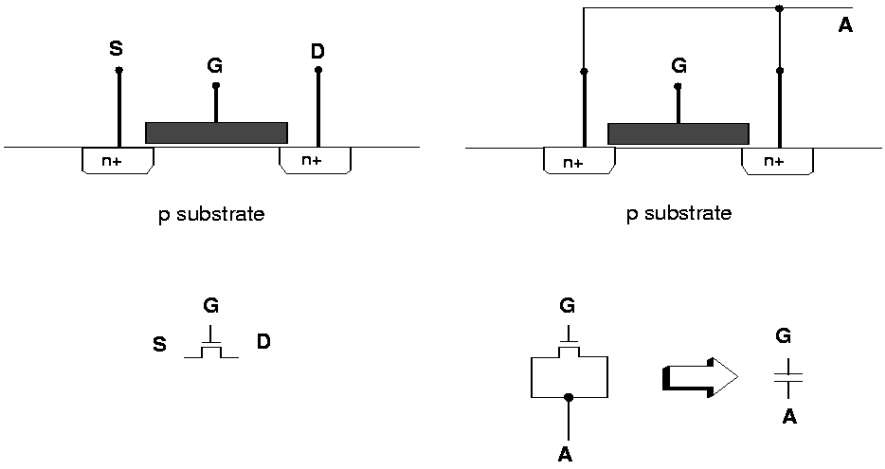

Fig. 4.1. Fabrication of a capacitor from a MOS transistor

For the simplest configurations to fabricate a capacitor realized by directly contacting the p substrate (Fig. 4.2), three different configurations should be distinguished. Let's consider the p-type substrate connected to ground.

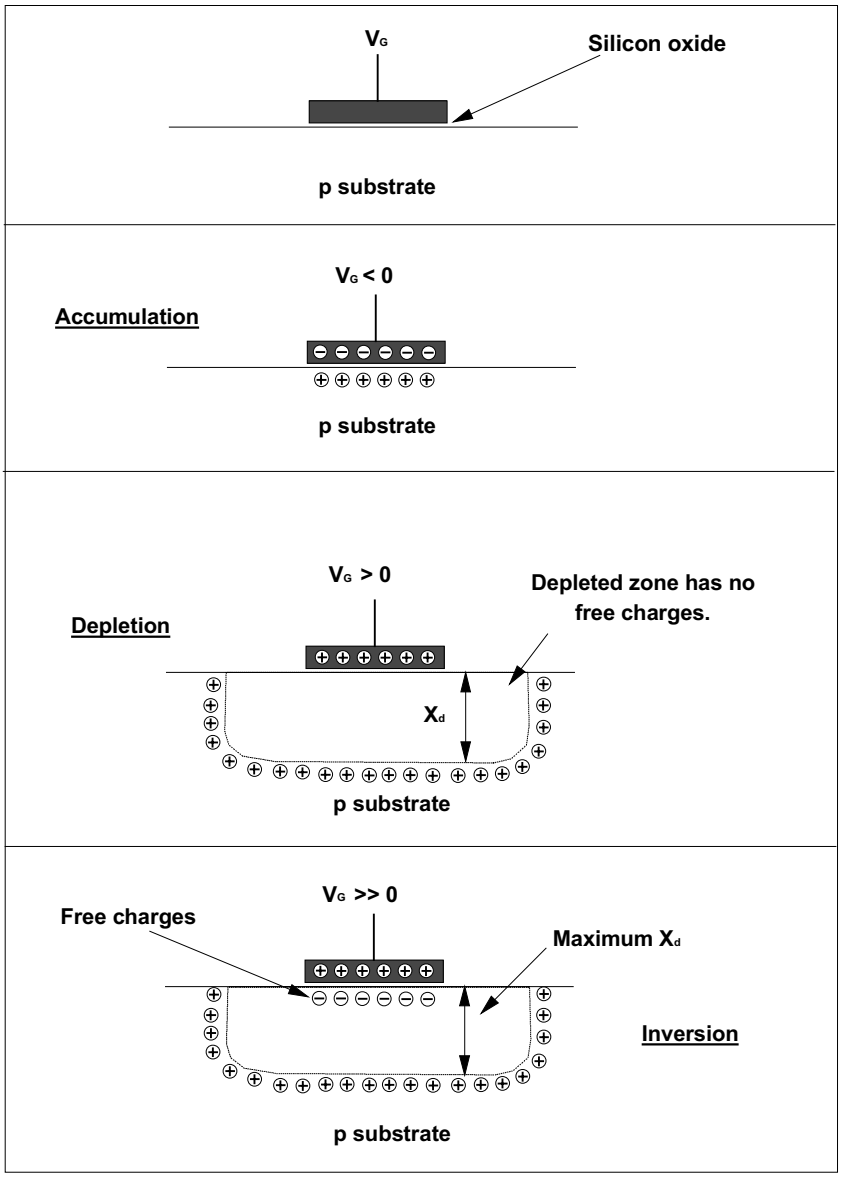

Fig. 4.2. Operating regions of a MOS capacitor: accumulation, depletion, and inversion

- *Accumulation.* Applying a negative voltage to the gate ($V_G < 0$), a layer of holes is induced at the oxide-semiconductor interface. The net charge of the semiconductor is, hence, positive, owing to the accumulation of the holes in excess with respect to the equilibrium.

The value of the capacitance is then $C = \varepsilon/t_{ox}$, where ε is the silicon oxide permittivity and t_{ox} is the oxide thickness. In this case, all of the voltage drop, V_G, is located between the conductive plates or entirely in the oxide.

- *Depletion*. As the gate voltage increases, i.e. as V_G becomes positive, the p-type mobile charge is removed from the oxide-silicon interface. A depletion region having thickness x_d and voltage drop Ψ_S forms, where:

$$V_G = V_{ox} + \Psi_S \tag{4.1}$$

- *Inversion* As V_G further increases, also x_d increases. If the voltage applied to the gate is above a critical value, referred to as threshold voltage, V_{TH}, a layer of electrons is induced at the oxide-silicon interface, inverting the polarity of the silicon. When $V_G > 0$ but below V_{TH}, the value of the capacitance is given by the series capacitors related to the two regions, the oxide and the depleted region.

4.2 CMOS Technology Capacitors

In a typical CMOS process, several types of capacitors are theoretically available:
- Poly/n-well capacitor with low or high voltage oxide;
- PMOS capacitor with low or high voltage oxide;
- Poly1/poly2 capacitor.

For the present technological processes, the value of the specific capacitance for the n-well capacitors is around 1.5 fF/μm^2 in case of HV capacitors, 3 fF/μm^2 in case of LV capacitors, and 2 fF/μm^2 in case of interpoly capacitors. The gate capacitance of a MOS transistor equals the value of a MOS capacitor having the same oxide thickness.

The n-well capacitors are designed like p-channel transistors without source and drain diffusions (Fig. 4.3). The value of capacitance as a function of the gate voltage with grounded n-well is shown in Fig. 4.4.

Such a structure (poly/n-well) has a constant value of capacitance in both accumulation and inversion. In accumulation, a negative charge crowding is located at the bottom plate of the capacitor. The inversion zone, i.e. the positive charge crowding in the silicon, can be obtained only at low frequency, since the positive charge accumulation is a slow phenomenon. Therefore, we can deduce that the poly/n-well capacitor satisfactorily operates only if the gate voltage is positive enough.

The PMOS capacitor is instead a p-channel transistor having the drain shorted with the source, as sketched in Fig. 4.5. In this case, the inversion region is reached faster owing to the presence of p^+-type diffusions. In fact, the p^+ regions provide the positive charge for the inversion.

This is valid only for the inversion case, i.e. Vg negative.

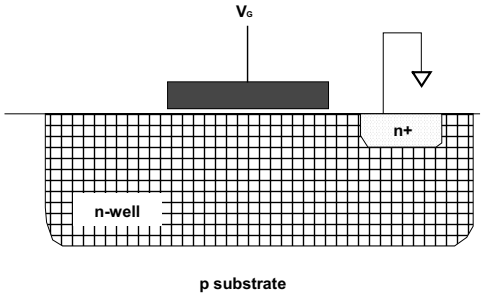

Fig. 4.3. Practical realization of a poly/n-well capacitor

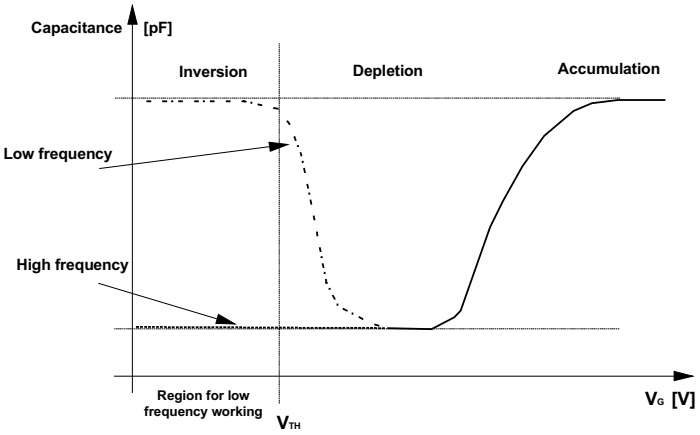

Fig. 4.4. C-V characteristic of a poly/n-well capacitor

Let's consider the practical case of a device in which both positive and negative charge pumps (see Chap. 15) are present and operate at the frequency of 30 MHz.

In the positive charge pumps, which are able to generate voltages higher than the supply voltage, the poly/n-well capacitors operate in the accumulation region since the poly gate has a higher voltage than the n-well. Hence, the majority carries (electrons) that are present at the oxide-semiconductor interface are provided by the bulk at a time rate that is negligible with respect to the switching frequency. The case of the negative pumps, which generate voltages below the ground potential, is different. In fact, in this case, the MOS system operates in the inversion region and the minority carriers (holes) can be provided only by the bulk at a rate that can be measured in seconds. Two p^+ diffusions are therefore added to the capacitor structure so as to generate minority carriers. At low frequency, the channel is in thermal equilibrium with the p^+ regions, and we can assume that the required carriers are instantaneously provided to the interface. At high frequency, the holes are not able to diffuse from the p^+ regions toward the middle of the channel with

the speed required to follow the signal applied to the gate. This causes channel RC parasitic effects that become more relevant when the carrier mobility is low and the distance between the p^+ regions is great.

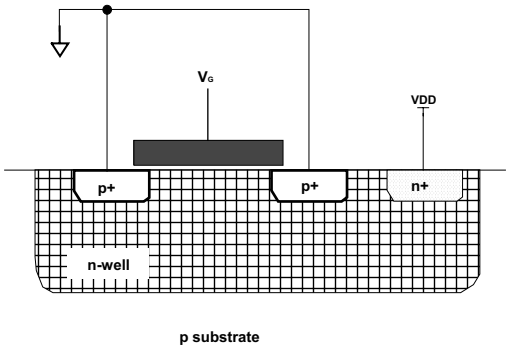

Fig. 4.5. PMOS capacitor

Let's now calculate the maximum frequency of the gate signal that can be applied to this type of capacitor in inversion. The time constant associated with the channel can be expressed as:

$$\tau_{ch} = R_{ch} \cdot C \tag{4.2}$$

where C, which is the capacitance associated with the gate oxide, can be calculated starting from the channel dimensions:

$$C = C_{ox} \cdot W \cdot L \tag{4.3}$$

R_{ch} is the channel resistance and can be obtained from the characteristic of the MOS transistor in the linear region:

$$\frac{1}{R_{ch}} = \frac{W}{L} \cdot \mu_{eff} \cdot Q_{inv} \tag{4.4}$$

Q_{inv} is the charge per unit of area in the inversion layer and μ_{eff} if the effective mobility. Based on the three foregoing equations, we can calculate the frequency associated with the channel RC:

$$f_{ch} = \frac{1}{2\pi\tau_{ch}} = \frac{1}{2\pi} \cdot \frac{\mu_{eff} Q_{inv}}{C_{ox} L^2} \tag{4.5}$$

In particular, we can notice that the frequency of the pole scales down as the square of L, which is the distance of two p^+ diffusions. This is the reason why it is very important to accurately determine the value of L of the capacitors of the negative charge pumps.

It is also possible to fabricate capacitors without using the silicon as plate, such as in the case of the poly1/poly2 capacitor. The CMOS processes that use two layers of polysilicon, i.e. the processes for non-volatile memories, offer this possibility.

Furthermore, metal layers can also be used to fabricate capacitors. The main limitation is in the value of capacitance that can be obtained. For a typical process, the thickness of the gate oxide ranges between 120 Å and 150 Å, whereas the inter-metal dielectric that forms the insulating layer between the two metal plates is some thousands of Angstroms thick. Therefore, the size of a capacitor fabricated with metal plates (i.e. metal1/metal2) is nearly 50 times larger than a poly1/poly2 capacitor having the same capacitance.

Moreover, the quality of the insulator is much different in the two cases. The gate oxide is the best possible solution offered by the present technology, since it has been studied and refined to fabricate all the transistors. Generally, the intermediate dielectric of the metal1/metal2 capacitor does not have such a high qua ity[1].

4.3 Integrated Resistors

The available resistors are all those that can be fabricated with the various layers produced by the technological process. In Table 4.1, the available layers are summarized with the value of resistance and its variation for a typical 0.35 μm CMOS process.

It is common practice to calculate the value of an integrated resistor in squares (indicated with the symbol □). In fact, the layout is a top view in which only the sides of the rectangles are dimensioned, whereas the depth is fixed and defined by the process. Therefore, we typically refer to the sheet resistance. Once the sheet resistance is known, we can obtain resistors of the required value by placing one or more squares (or fractions of squares) in series.

Table 4.1. Sheet resistence of different layers

Layer	Sheet Resistance [Ω/□]
n^+ (active area)	50 ÷ 60
n-well	600 ÷ 1200
Poly2 with silicide	5 ÷ 7
Poly2 without silicide	50 ÷ 100
Metal1	0.08
Metal2	0.04

[1] By the way, it is worth telling this story. The authors participated in the design of a device that included an A/D converter realized with metal1/metal2 capacitors. Once the devices were delivered, many of them were returned by the customers since they did not work properly and were considered as “failures”. After further tests, many of them resulted to be good either immediately or after a night in the oven. The problem was due to the material used to planarize the dielectric layer between the metal plates. Such material absorbed humidity, modifying the value of capacitance due to the ions present in the water. The subsequent heating removed the charge and the devices worked fine.