MOS Differential LNA Design Tutorial

J P Silver

E-mail: john@rfic.co.uk

1 ABSTRACT

This tutorial describes the theory and design on a MOS Differential Low noise amplifier using source de-generation. A worked example is given together with the associated Agilent ADS simulation circuits and plots.

2 INTRODUCTION

The MOS LNA Design tutorial describes the design of a single stage LNA using source degeneration technique to provide a good noise match. A cascade output stage was added to the source degenerated stage provide improved gain & reverse isolation.

This tutorial describes the design of a differential LNA using the same design specification and device models.

There are several advantages in using a differential design. Firstly, the virtual ground formed at the 'tail' removes the sensitivity to parasitic ground inductances, which makes the real part of the input impedance purely controlled by the source degeneration inductance (**Ls**). Secondly the differential amplification of the signal ensures attenuation of the common mode signal, in most systems this common mode signal will be noise! Thirdly, the use of Gilbert mixers and image rejection schemes require to be fed from a differential source.

3 LNA SINGLE-STAGE DESIGN

The design equations are the same as for the single stage LNA design and are summarized below:

$$Rin = Rg + \frac{L_s.g_m}{C_{gs}} + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) \text{ Can be re - written as}$$

$$Rin = Rg + Ra + j[X_{LS} - X_{CGS}] \text{ Where } Ra = \frac{L_s.g_m}{C_{gs}}$$

Therefore, the impedance of the MOSFET without feedback is:

$$Rin = Rg - jX_{CGS} \rightarrow Rin = -jX_{CGS}$$

Adding series feedback adds the following term to the original input impedance:

$$Ra + jX_{LS}$$

Additionally, another inductor is added in series with the gate **Lg** that is selected to resonate with the **Cgs** Capacitor.

What we are trying to achieve is:

$Rin = \frac{L_s.g_m}{C_{gs}}$ Where Rin may be say 50 ohms.

Lg is designed so that at the resonant frequency it cancels out Cgs ie

$$j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) = 0$$

In most LNA designs the value of Ls is picked and the values of gm and Cgs are calculated to give the required Rin.

4 DESIGN EXAMPLE

The aim of this example is to design step-by-step a narrow band LNA (Low noise amplifier) to work over the Bluetooth frequency band. A summary of the required specification for the LNA is given in **Table 1**.

Parameter	Specification	Units
Frequency	2.45 to 2.85	GHz
Noise Figure	<3.5	dB
Voltage Gain	>20	dB
Power Gain	>10	dB
Power consumption	<100	mW
Source/load impedance	50	ohms
Load Capacitance	0.4	pF

Table 1 Required specification for the Bluetooth front end LNA.

For this design we will be using the Agilent CMOS14 0.5um process that allows a minimum gate length of 0.6um.

The schematic of the single ended LNA (half of the final differential LNA design) is shown in **Figure 1**.

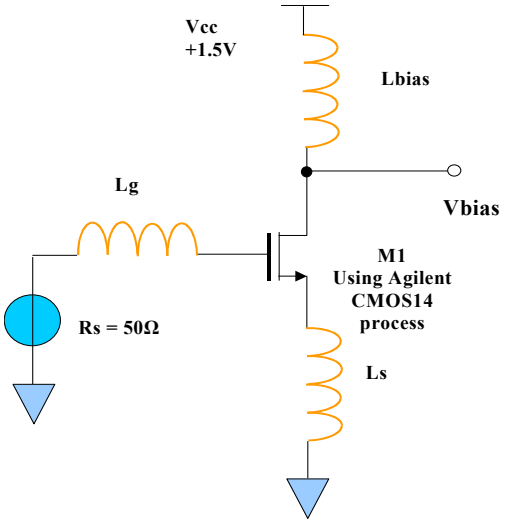

Figure 1 Initial single-stage LNA schematic

4.1 STARTING VALUE OF DE-GENERATION INDUCTOR LS.

The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is typically about 10nH (anything bigger would probably be too big to be put on the chip).

For this example we will pick a value of 1.0nH.

We now find the cut-off frequency defined as:

$$\omega_T = \frac{gm}{Cgs} = \frac{Rs}{Ls} = \frac{50}{0.5E^{-9}} = 1E^{11}\text{rad/sec}\ (\sim 16\text{GHz})$$

4.2 OPTIMAL Q OF INDUCTOR

Optimal Q is given by:

$$QL = \sqrt{1+\frac{1}{p}}$$

$$\text{Where } p = \frac{\delta.\alpha^2}{5.\gamma}$$

The parameters for p are dependant on the CMOS technology but typically

γ is set between 2 - 3 (normally 2)
δ is set to 2 - 3 times the value of γ (normally 4)
α is assumed to be 0.8 - 1 (take to be 0.9)

$$p = \frac{4.(0.9)^2}{5.4} = 0.162$$

$$QL = \sqrt{1+\frac{1}{0.162}} = 2.67$$

4.3 EVALUATION OF LG

$$Lg = \frac{Q_L.Rs}{\omega_o} - Ls$$

Where ω_o = centre frequency =

$$2\pi.2.65E^{9} = 1.665E^{10}\ \text{rad/sec}$$

$$Lg = \frac{2.67.50}{1.665E^{10}} - 1E^{-9} = 7.52\text{nH}$$

4.4 FIND CGS (GATE-SOURCE CAPACITANCE)

$$Cgs = \frac{1}{\omega_o^{\,2}(Lg+Ls)}$$

$$Cgs = \frac{1}{(1.665E^{10})^2(7.52E^{-9}+0.5E^{-9})} = 0.45\text{pF}$$

4.5 FIND W

$$Cgs = \frac{2}{3}Cox.W.L_{min}$$ rearrange to get W ie

$$W = \frac{3}{2}\frac{Cgs}{Cox.L_{min}}$$

$$Lmin = 0.6E^{-6}\text{m};\ Tox = 1.01E^{-8}\text{m}$$

$$\varepsilon ox = \varepsilon ox\,.\,\varepsilon o$$

Where
εs = dielectric constant for silicon = 3.9 and
εo = dielectric constant for free space = $8.854E^{-14}$F/cm

$$Cox = \frac{\varepsilon ox}{Tox} = \frac{3.9 \times 8.854E^{-14}}{1.01E^{-8}} = 3.419E^{-3}\text{pF/um}^2$$

$$W = \frac{3}{2}.\frac{0.45}{3.419E^{-3}.0.6} = 330$$

$$W = 330\text{um}$$

4.6 CALCULATE GM

$$gm = \omega_T.Cgs$$

$$gm = 1E^{11}.0.45E^{-12} = 0.045A/V$$

4.7 V EFFECTIVE

$$Veff = (Vgs - V_T) = \frac{gm.L_{min}}{u_n.Cox.W}$$

u_n = device mobility = 433cm/V
Converting units gives:

$$Veff = \frac{45000.0.6}{164.330} = 0.5V$$

With VT = 0.67V

Therefore, we need to apply

(0.67 + 0.5) = 1.16V to the gate

4.8 BIAS CURRENT ID

$$Id = \frac{1}{2}.gm.V_{eff} = \frac{1}{2}.0.045.0.5 = 11mA$$

(9) Estimated Optimum Noise Figure

$$Fopt = 1 + \frac{2\gamma}{\alpha}\left(\frac{\omega_o}{\omega_T}\right)\sqrt{p\left(|c| + \sqrt{p} + \sqrt{1+p}\right)}$$

Take $|c| = 0.4$

Fopt =

$$1 + \frac{4}{0.9}\left(\frac{1.665E^{10}}{5E^{10}}\right)\sqrt{0.162\left([0.4] + \sqrt{0.162} + \sqrt{1+0.162}\right)}$$

Fopt = 2.12 = 10log(2.12) = 3.26dB

To complete the design another N-type is added as the cascode stage with the same W/L ratio as the LNA device. The cascode stage is connected at a iode ie the gate is DC connected to the drain to ensure the device is in saturation. Finally it is assumed that on-chip spiral inductors will be used in the design, which will have a typical loaded Q of 6.

5 DIFFERENTIAL LNA DESIGN

The basic circuit of the differential LNA is shown in **Figure 2**. As can be seen each half of the differential amplifier is in fact the single LNA designed earlier in this tutorial (ie with a 50ohm input impedance set by making gm = 20mS), with the degenerating inductors (Ls) connected together at the 'virtual earth'. At this point the a current source is connected to the negative supply set to give twice the current flowing down one of the LNA sections.

The ADS schematic showing the differential LNA is shown in **Figure 3**. Note to supply a differential signal to each LNA input, an 'ideal' balun (balanced to unbalanced) transformer has been used (We could also use two AC sources each set to 0.5V and opposite polarity). In addition another balun is used on the amplifier output to re-combine the signal to allow the voltage gain to be simulated.

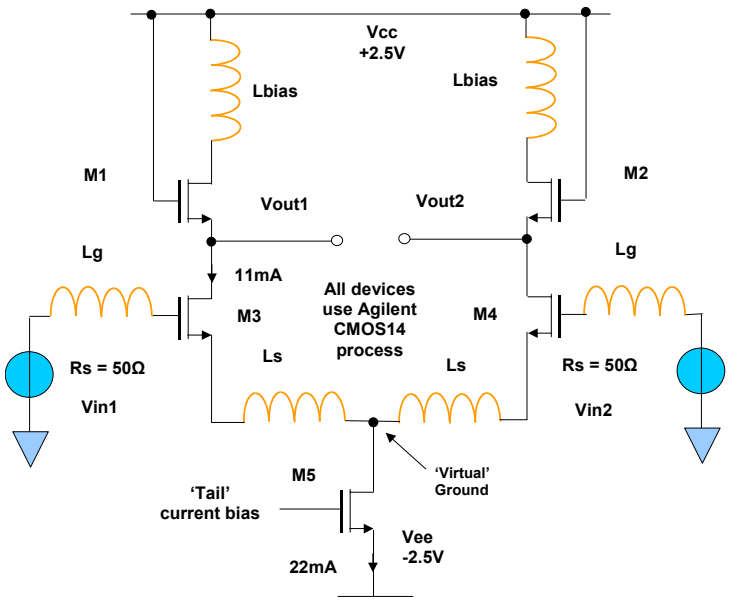

Figure 2 Schematic of the differential amplifier LNA using two single stage LNA's from the previous tutorials. Circuit values are Lg = 7.52nH ; Ls = 1nH; M1,M2,M3 & M4 W/L = 330 (Lmin = 0.5um).

Calculation of Load Inductor:

$$fo = \frac{1}{2\pi\sqrt{C_{out}.L_{Load}}}$$

Assumimg a load capacitor of 0.4pF then L_{Load} =

$$L_{LOAD} = \frac{\left(\frac{1}{2\pi.fo}\right)^2}{C_{out}} = \frac{\left(\frac{1}{2\pi.2.5E^9}\right)^2}{0.4E^{-12}} = 10nH$$

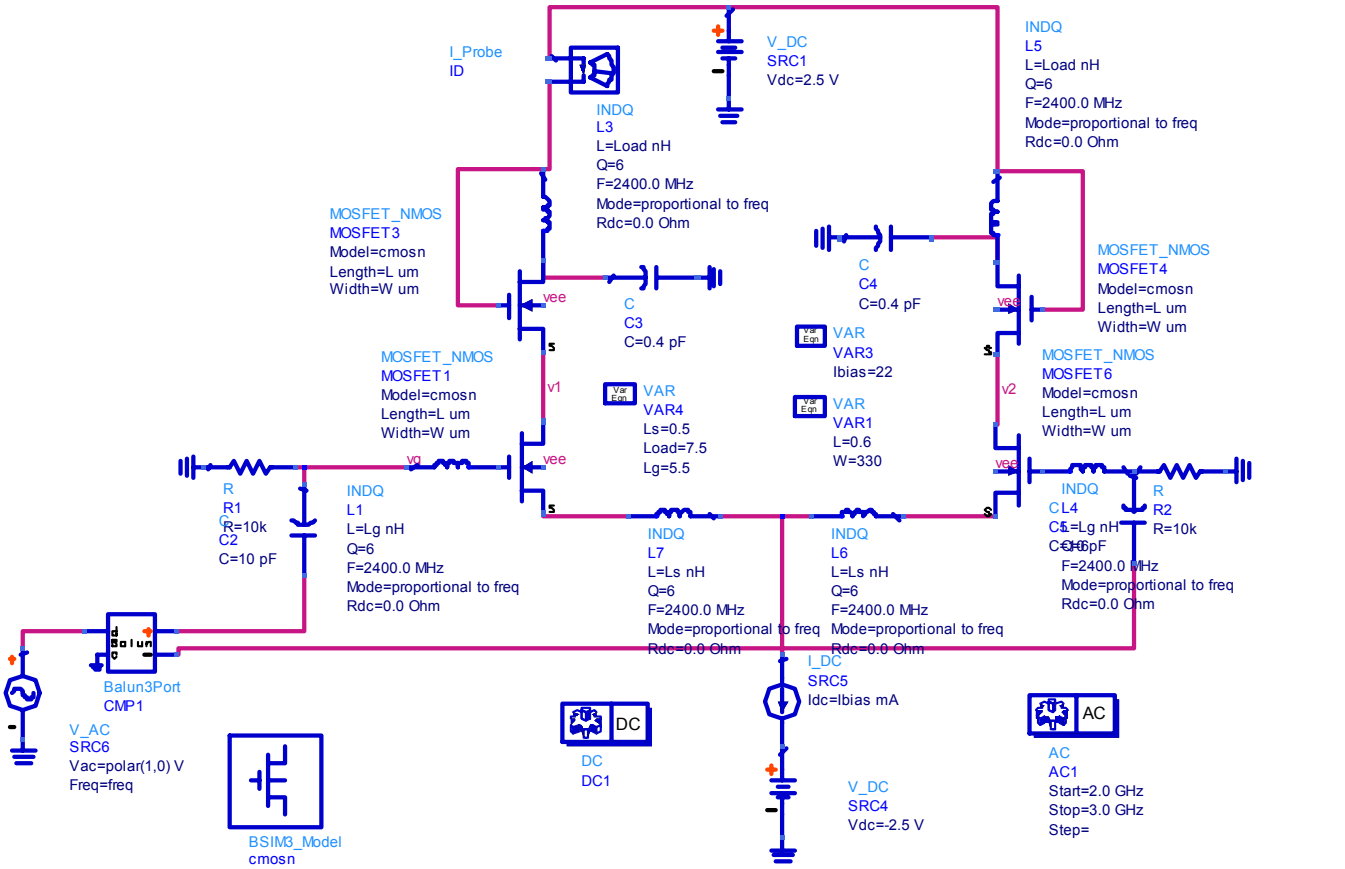

Figure 3 ADS schematic of the Common-source Differential LNA. The differential input voltage is supplied vai the balun transformer (CMP1). An ideal current source has been added at this stage on the 'tail' set to 22mA so that 11mA will flow down each 'arm' of the LNA. The 0.4pF load capacitors (representing a typical load of say a gilbert mixer) have been added to each of the two output nodes V1 & V2.

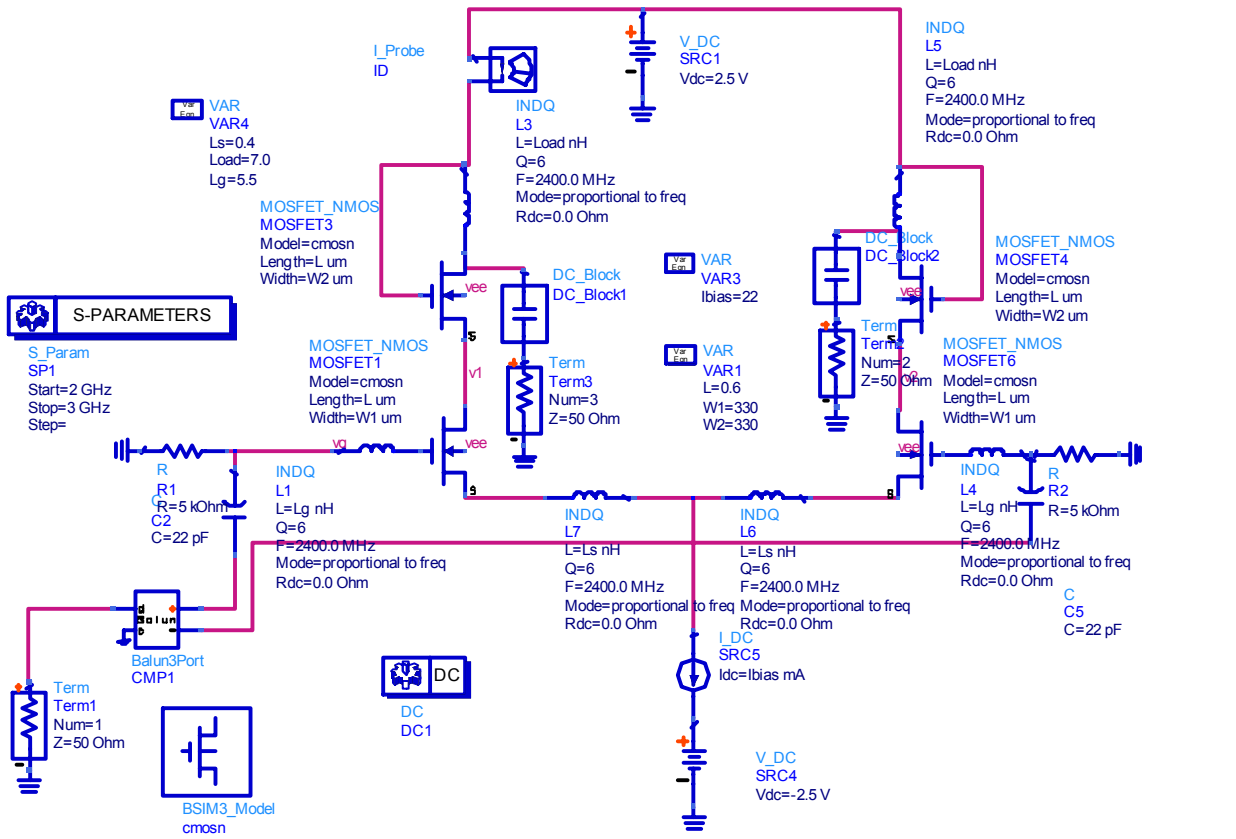

Figure 4 ADS schematic of the Common-source Differential LNA. The small signal input power is supplied via the balun transformer (CMP1). An ideal current source has been added at this stage on the 'tail' set to 22mA so that 11mA will flow down each 'arm' of the LNA. The two output nodes V1 & V2 are now terminated in 50-ohm loads – Note the DC blocks to ensure that the DC bias condition, is not upset by the loads.

5.1 ESTIMATION OF DIFFERENTIAL GAIN

$$gm = \sqrt{2.Kp.\frac{W}{L}.I_{DS}} =$$

$$gm = \sqrt{2 \times 170E^{-6}.\frac{300}{0.6} \times 11E^{-3}} = 0.043$$

$$A_{LNA} = \frac{gm.Q_{LOAD}}{Co.2\pi o.2} = \frac{0.043 \times 6}{0.4E^{-12} \times 2\pi \times 2.5E^{9}} = 41$$

$$A_{LNA}(dB) = 20\log(41) = 32dB$$

This gain is for one C-S stage and as the output are not combined the gain of the differential amplifier will be half that for a single stage ie 3dB less. This will make the predicted gain of our example 29dB. **Note** to centre the gain response the load inductors were reduced to 7nH.

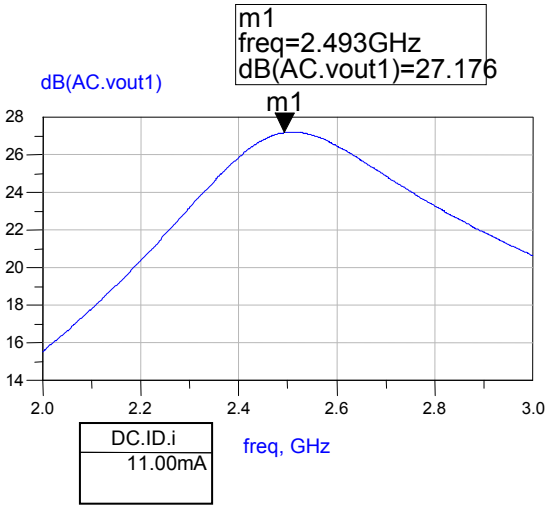

Figure 5 Simulation result of the ADS schematic shown in Figure 3. The predicted voltage gain is 29dB, which is pretty close to the simulated result and much greater than the specification of 20dB. Note to centre the gain response, the load inductors were reduced from 10nH to 7nH.

5.2 S-PARAMETERS

The differential voltage gain is predicted to be ~29dB exceeding our specification for voltage gain, but power gain requirement has to met too. To check the power gain ie S21 we need to configure the ADS schematic of the LNA with an S-Parameter simulator. This is show in **Figure 4** with the resulting simulation result shown in **Figure 6.**

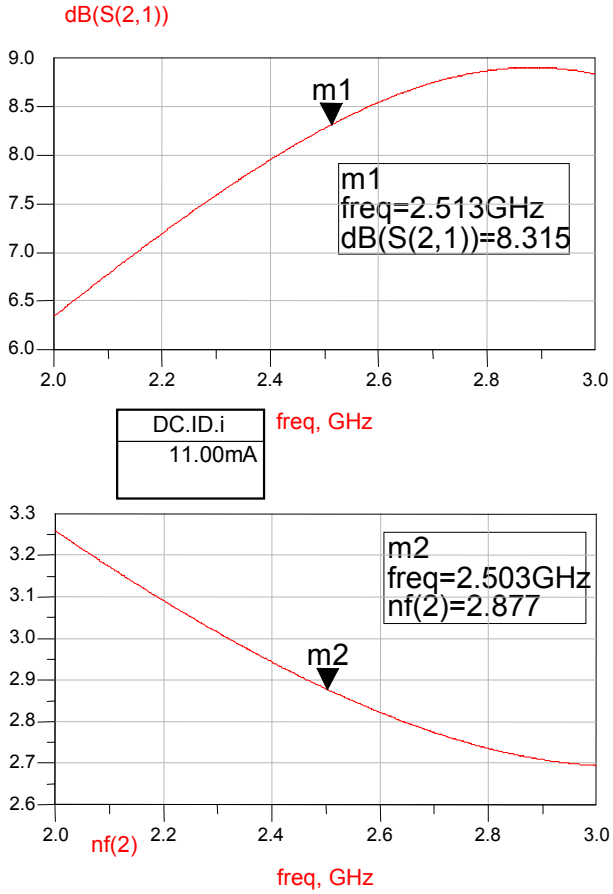

Figure 6 Simulation of power gain (S21) and noise figure of the LNA using the setup shown in Figure 4.

The simulation plot of **Figure 6**, shows the classic gain/noise trade-off of LNA design. To peak the gain at 2.5GHz we need to increase the gate inductance (Lg), to peak the noise we need to decrease the noise figure. The noise specification for this LNA is <3.5dB so there is a little margin to allow for gain peaking, but the power gain is too low at 9dB.

There are a number of ways to increase the gain:

(1) Increase W/L ratio of cascode.
(2) Increase current.
(3) Reduce Ls.
(4) Add another C-S stage to each output node.

The effect of optimizing Lgate for best power gain is shown in **Figure 7**, however although the noise figure is within the specification the power gain is still short of 10dB. By adjusting the current, W/L ratios and device inductances (ie Lg & Ls) it was possible to achieve the required design goals for gain and noise at the expense of power consumption.

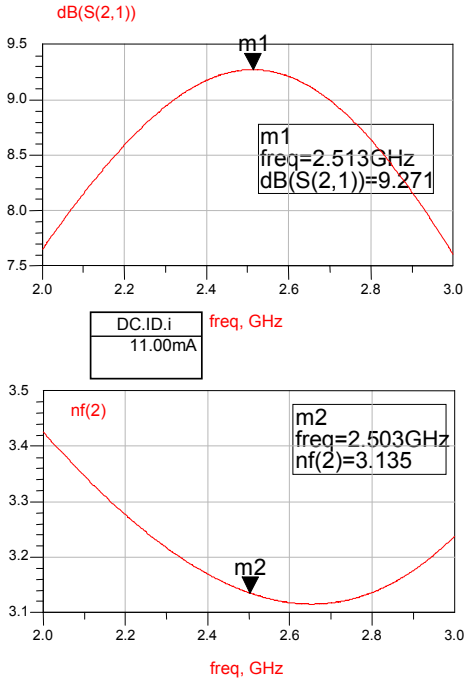

Figure 7 ADS simulation of the circuit shown in Figure 4 with each Lgate increased to 7nH to center the gain response at 2.5GHz. Note that the noise figure has now degraded to 3.1dB. Further optimization is required to increase S21 to > 10dB.

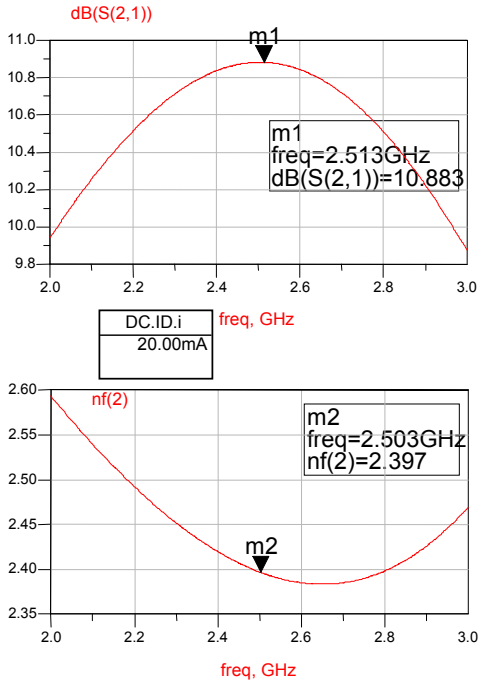

Figure 8 ADS simulation of the circuit shown in Figure 4 with Lg decreased to 4.5nH, Ls reduced to 0.35nH, Cascode width increased to 660um, Input device width increased to 530um and the current through each arm increased to 20mA .

Although the specification for power gain is now met, a 1.8dB margin might be unacceptable when taking into account process and temperature variations. Therefore, the final design gain is increased by adding simple C-S stages with inductive loads and decoupled on the output by small value capacitor. This output stage is DC coupled to the output of the first 'cascode' stage so that is receives a correct bias to be in saturation. The increased gain will greatly improve the noise figure of the receiver as the noise figure of the second stage (most likely the mixer) will be reduced by ~1/gain_LNA.

The modified circuit and increased gain responses are shown in **Figure 9** and **Figure 10**.

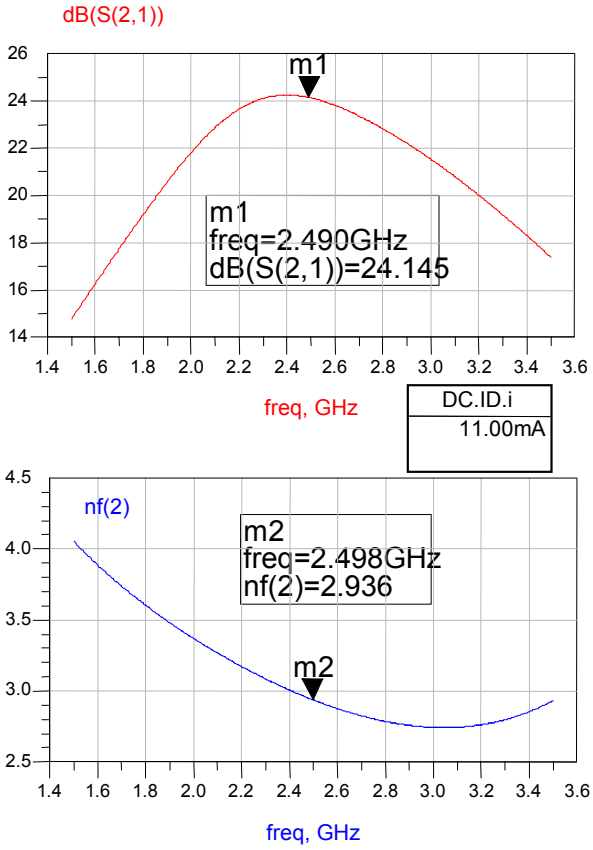

Figure 9 Gain & noise plots from the differential LNA with added C-S stage on the output (with a tuned inductive load).

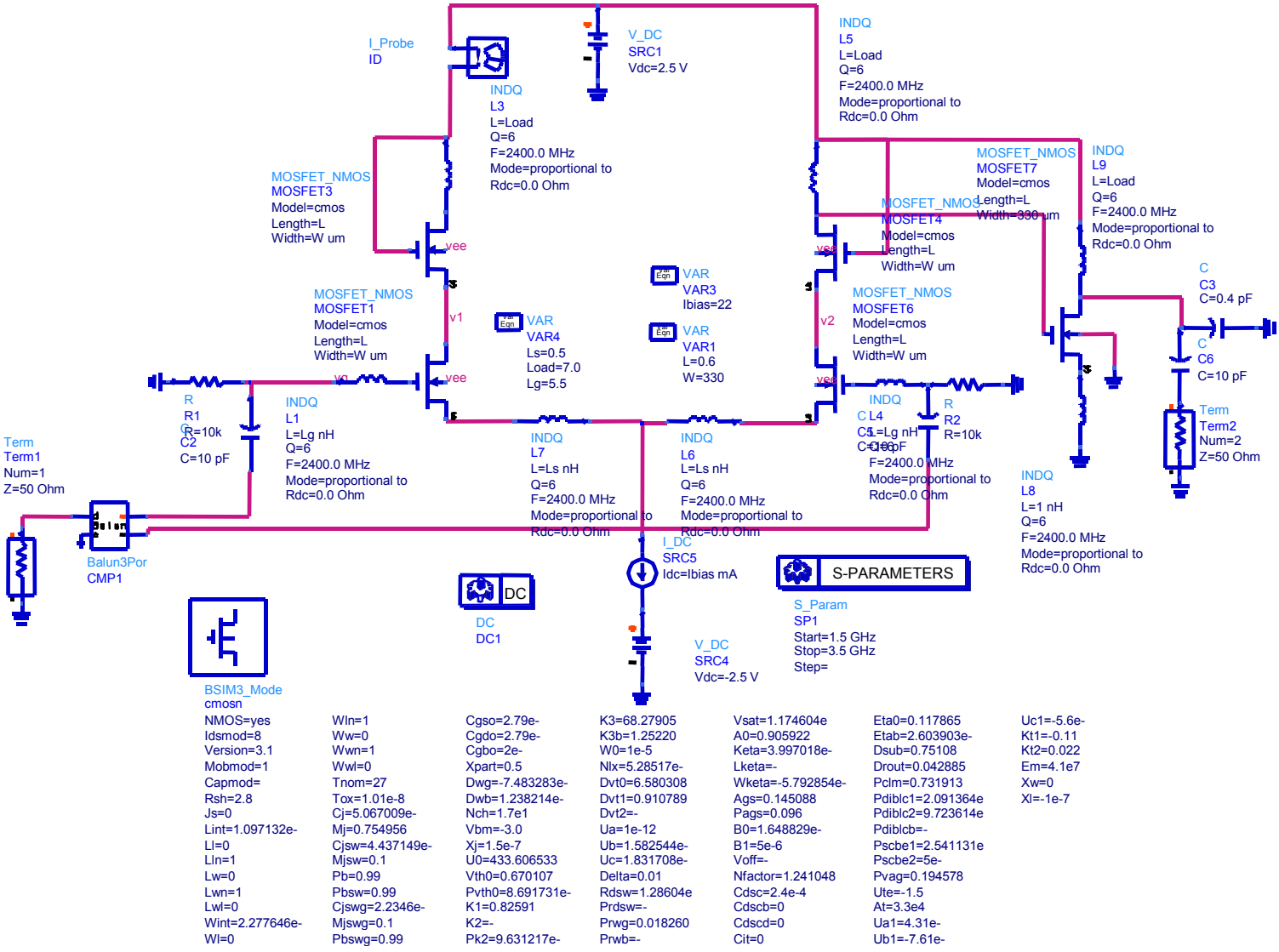

Figure 10 ADS schematic of the differential LNA with a C-S stage added to the cascode output. Note for clarity only one extra C-S stage has been added, normally another stage would be added to M1. To complete the design a current mirror (and associated bias network) will replace the ideal 11mA current source (SRC5).

6 LINEARITY

This final section deals with estimating the 1dB gain compression point and IM3 (3rd order intermodulation products). If an amplifier is driven hard enough the output power will begin to roll off resulting in a drop of gain known as gain compression. The measurement of gain compression, is given by the 1dB gain compression point. This parameter in another measure of the linearity of a device and is defined as the input power that causes a 1dB drop in the linear gain due to device saturation. An example of the 1dB compression point is shown in **Figure 11**.

We can get a rough estimate of the gain compression of the LNA a non-linear expression of the input and output parameters can be expanded using Taylor's theorem. This results in the following equations for 1dB gain compression point and IM3 [3].

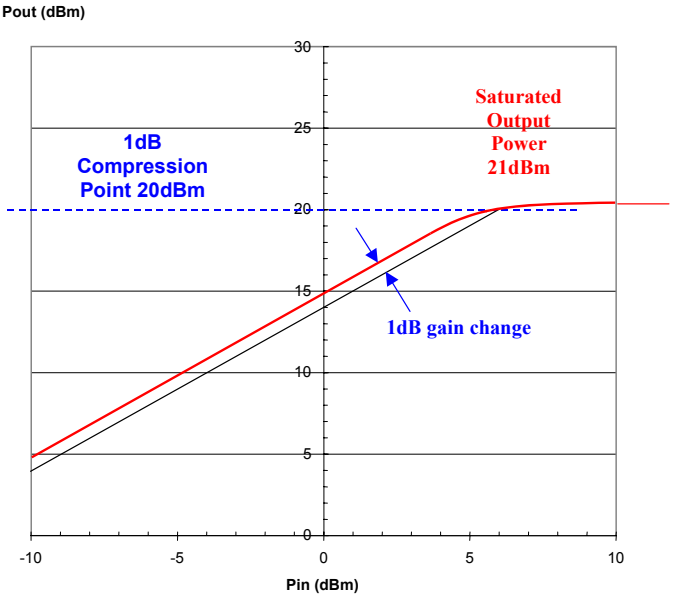

Figure 11 Compression point plot. The red curve is the gain compression characteristic of a 15dB gain amplifier. The parallel black line is 1dB below and represents a gain of 14dB. The input power where the amplifier gain crosses the 1dB down line is know as the 1dB input compression point.

$$I_{DSAT} = W_{vsat}.C_{ox}.\frac{V_{od}^{\ 2}}{V_{od} + E_{sat}.L}$$

With

V_{od} = Voltage overdrive = Vgs - Vt and

E_{sat} = Velocity saturation field strength given by

$$E_{sat} = \frac{2V_{sat}}{\mu_{eff}} \quad \text{Where} \quad \mu_{eff} = \frac{\mu_o}{1 + \vartheta.V_{od}}$$

$$P_{1dB} \sim 0.29 \frac{V_{sat}.L}{\mu_1.Rs} V_{od} \left(1 + \frac{\mu_1.V_{od}}{4V_{sat}.L}\right)\left(1 + \frac{\mu_1.V_{od}}{2V_{sat}.L}\right)^2 \quad - (1)$$

to convert to dBm = 10 log (1000*P1dB)

$$P_{IIP3} \sim \frac{8}{3}\frac{V_{sat}.L}{\mu_1.Rs} V_{od} \left(1 + \frac{\mu_1.V_{od}}{4V_{sat}.L}\right)\left(1 + \frac{\mu_1.V_{od}}{2V_{sat}.L}\right)^2 \quad - (2)$$

$$\mu_1 \cong \mu_o + 2\vartheta\, Vsat.L$$

Example

Running the simulation shown in **Figure 10**, the values of Vgs = 1.26V.

Using the spice model data for the Agilent CMOS14 0.5um we have:

L = 0.6um,
μ0 = 433 cm^2/(V*s),
θ = 0.1,
Rs = 50 ohms,
VT = 0.67V
Vsat = 1.73E^5 m/s

First convert numbers to metre format:

μ0 = 433 cm^2/(V*s), = 0.433 m^2/(V*s
L = 0.6um, = 0.6E^{-6}m.

$$V_{od} = V_{gs} - V_T = 1.26 - 0.67 = 0.59V$$

$$\mu_1 \cong 0.433 + 2x0.1x1.73E^5.0.6E^{-6} = 453$$

Feeding these values into equations 1 & 2 yields

P1dB = 9.39dBm and IIM3 = 19.02dBm.

The equations 1 & 2 were entered into a spreadsheet, along with a range of Vod from 0.01 to 5V.

The table of results is shown in **Table 2**.

Vod (V)	Input 1dB Comp (dBm)	IIMP3 (dBm)
0.01	-10.05	-0.41
0.5	8.42	18.05
0.59	9.39	19.02
1	12.77	22.40
1.5	15.74	25.37
2	18.09	27.72
2.5	20.07	29.70
3	21.80	31.43
3.5	23.34	32.97
4	24.73	34.37
4.5	26.01	35.64
5	27.19	36.82

Table 2 Calculated 1dB compression point & 3rd order intercept point.

The following two graphs show the plotted data of the data shown in **Table 2**.
1dB compression point is shown in & 3rd order intercept point is shown in **Figure 12** and **Figure 13** respectively.

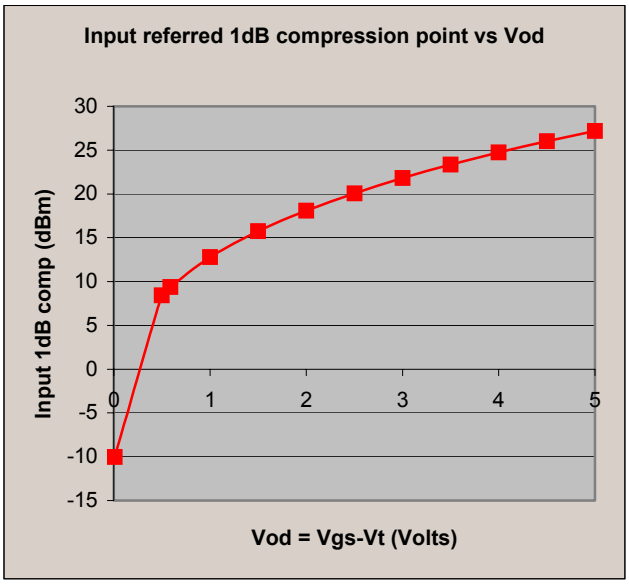

Figure 12 Referred to input 1dB compression point plot using the CMOS 14 Spice data

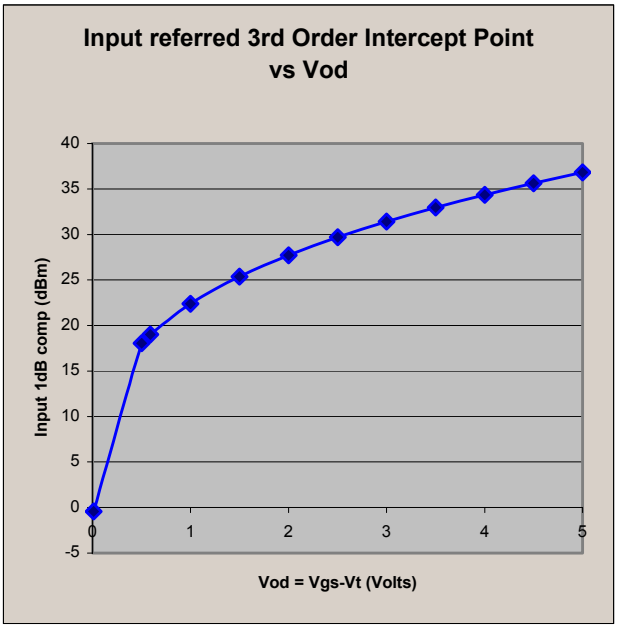

Figure 13 Referred to 3rd Order Intercept point (IIMP3) plot using the CMOS 14 Spice data

Figure 14 shows the ADS simulation setup to allow the 1dB compression point to be simulated.

The sub-circuit Diff_MOS_LNA is shown in **Figure 15**.

The resulting plots are shown in **Figure 16** (harmonic spectrum) and **Figure 17** (gain compression plot).

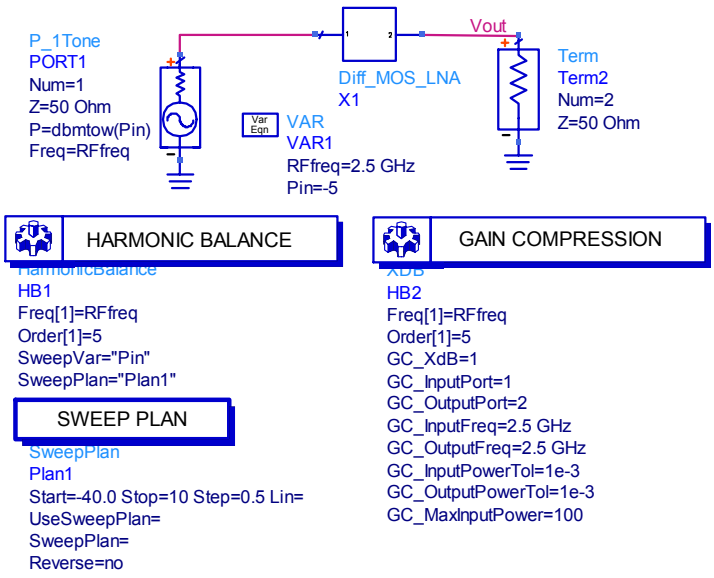

Figure 14 ADS simulation setup to measure the 1dB compression point of the LNA. The sweep plan sets the input power sweep. The harmonic balance allows the LNA harmonics to be plotted and the gain compression block allows a pin vs pout plot to be generated.

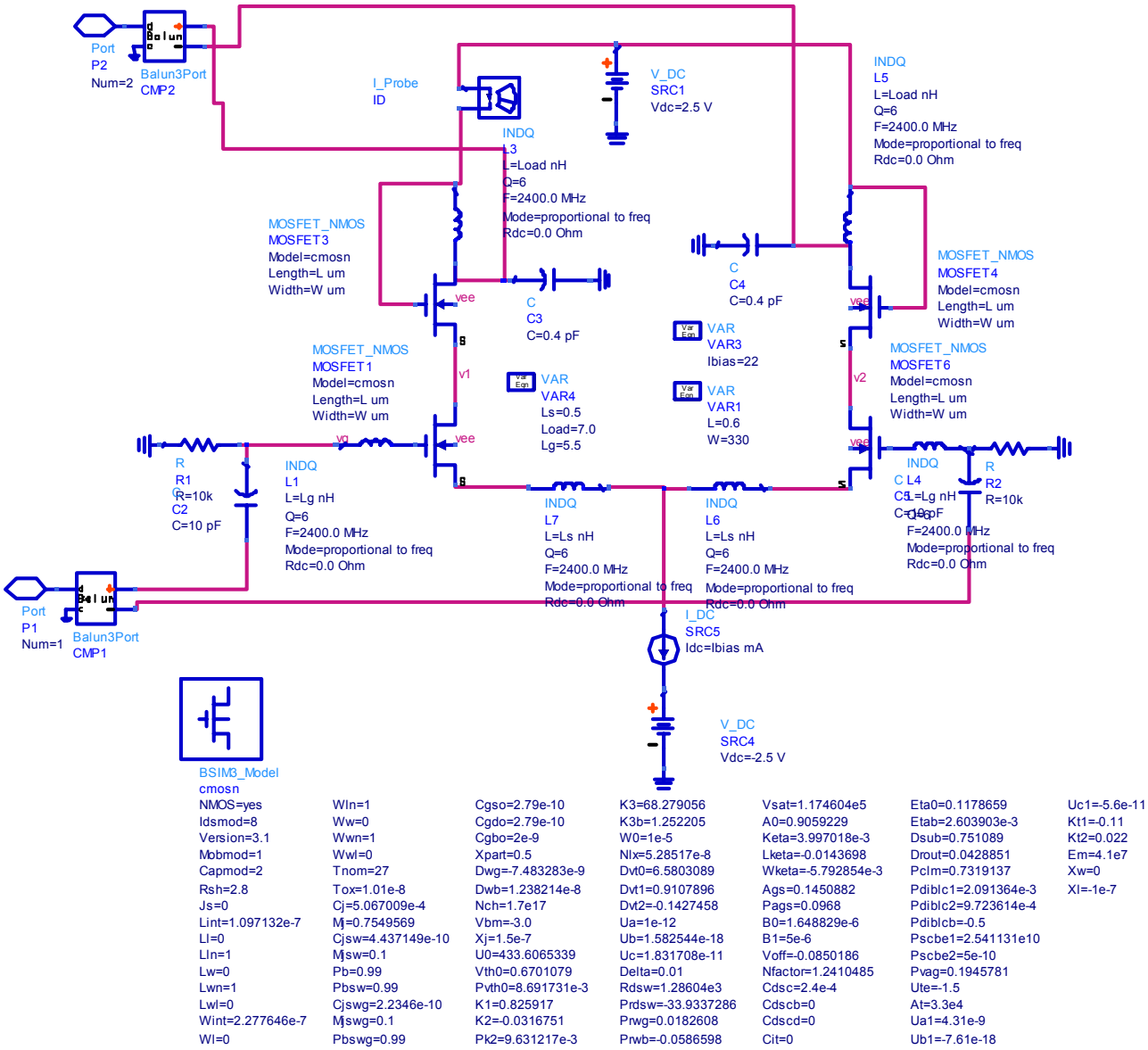

Figure 15 Addition of Baluns on the Differential amplifier to allow gain compression simulation. Note the polarity of signals on the output balun.

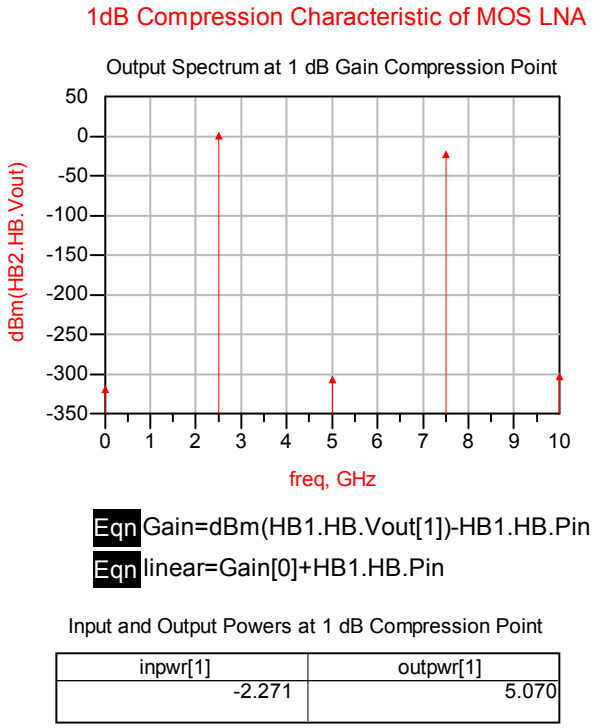

Figure 16 Harmonic spectrum of the MOS LNA with a prediction of the 1dB compression point of +5.-7dBm (-4dBm input referred).

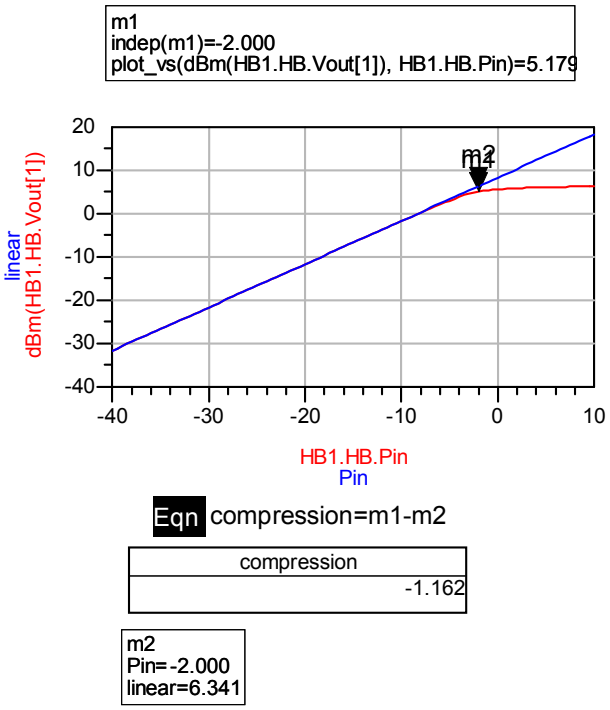

Figure 17 Gain compression plot of the MOS LNA. The markers m1 and m2 are adjusted to give a compression of 1dB, giving an output 1dB compression point of +6.3dBm.

The gain compression calculation agrees with the simulation value to within 1dB at 7.5dBm (Simulation value calculated at 6.5dBm).

Finally, to increase the gain margin of the LNA another C-S stage could be added to the 'cascode' output. This output stage is DC coupled to the output of the first 'cascode' stage so that is receives a correct bias to be in saturation. The increased gain will greatly improve the noise figure of the receiver as the noise figure of the second stage (most likely the mixer) will be reduced by ~1/gain_LNA.

We could combine the outputs of the LNA by adding a current mirror to the cascode stages as shown in **Figure 18**. Note care has to be taken as the additional current mirror will drop voltage and it may be necessary to raise the supply rail slightly. Alternatively, the cascaded LNA could feed a second stage differential amplifier stage. This amplifier could then be loaded with a current mirror to sum the outputs.

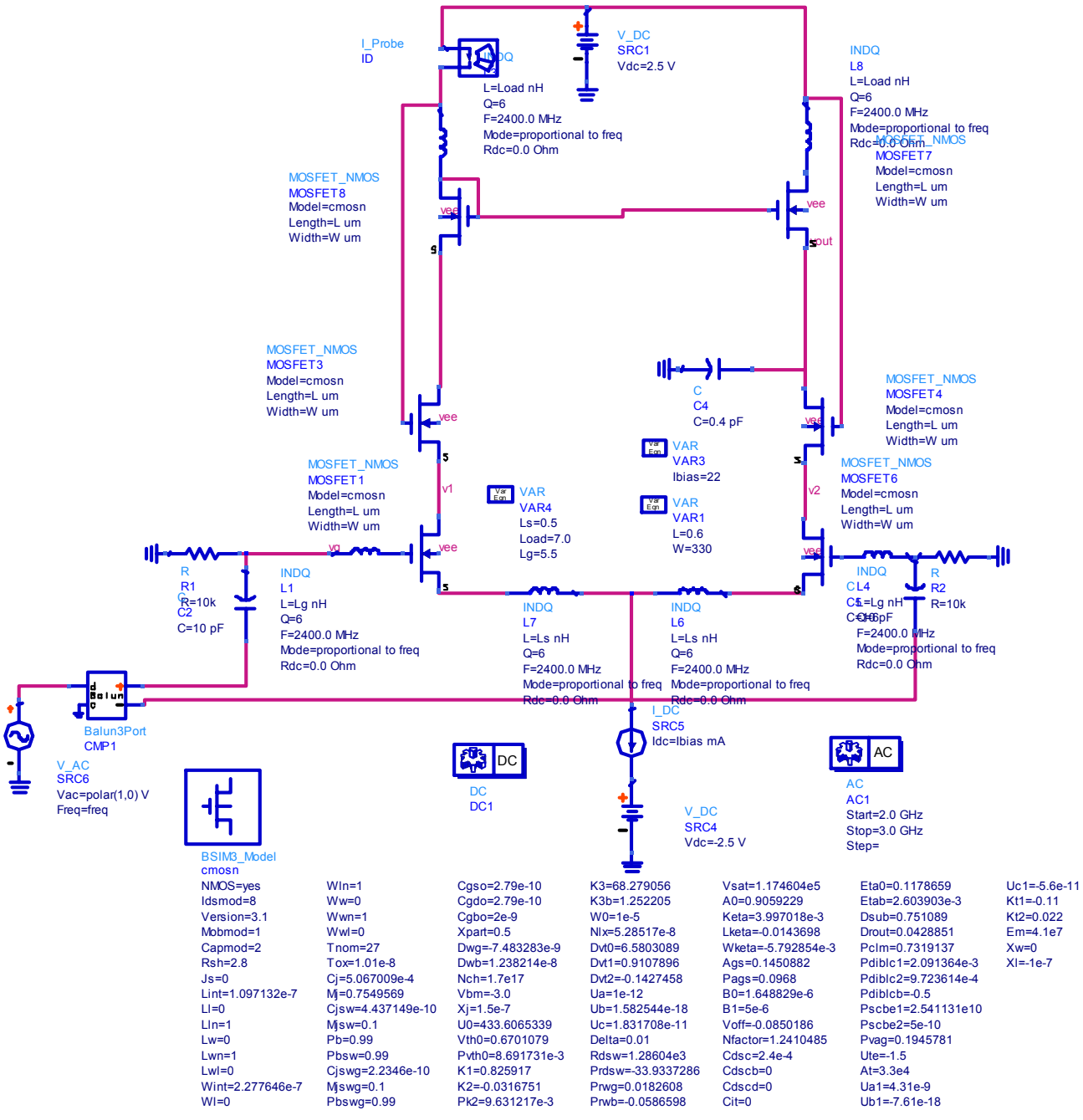

Figure 18 Addition of a current mirror to the LNA to combine the differential outputs to a single output. Note care has to be taken as the additional current mirror will drop voltage and it may be necessary to raise the supply rail. Alternatively the cascaded LNA could feed a second stage differential amplifier (with current mirror to sum the outputs) where the differential signal could be combined.

7 SUMMARY

This tutorial gave the design equations to design a differential LNA using shunt feedback realized with on-chip inductors. A design example of a 'bluetooth' LNA was given, with the associated step-by-step design process to meet a given specification. ADS simulations have been given to predict the various circuit parameters of gain, noise figure and power consumption, all summarized in **Table 3**.

Further discussions, described how the power gain could be further increased by adding another C-S stage to each 'cascode' stage output.

This increased the power gain to >20dB and would greatly improve the noise figure of the receiver, as the noise figure contribution of the following mixer stage would be reduced by a 1/gain_LNA.

Parameter	Specification	Prediction	Units
Frequency	2.45 to 2.85	2.45 to 2.85	GHz
Noise Figure	<3.5	2.8	dB
Voltage Gain	>20	27	dB
Power Gain	>10-15	11.4*	dB
Power consumption	<200	165**	mW
Source/load impedance	50	50	ohms
Load Capacitance	0.4	0.4	pF

* Power gain > 20dB with another C-S stage added.
** Including 'tail' current mirror network not shown in the simulation schematics.

Table 3 Summary of simulated device performance.

Finally the definition of linearity was given, together with the associated equations for the calculation of 1dB gain compression point and 3rd Order Intercept point.

A worked example was given, together with ADS Simulations showing close agreement with the hand calculations and the ADS simulations.

8 REFERENCES

[1] T.H Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, ISBN 0 521 63922 0, Chapter 2.

[2] C.S Kim, M Park, C-H Kim, Y C Hyeon, H K Yu, K Lee, K S Nam, "A fully integrated 1.9GHz CMOS Low-noise amplifier" in IEE Microwave and guided wave letters, Vol 8, No 8 August 1998.

[3] T Soorapanth, T.H Lee, "RF Linearity of Short-Channel MOSFETs", IEEE Journal of Solid State Circuits, vol. 32, no. 5, May 1997