

This is p. 4 from Elad Alon's "Microsoft Word – hw1\_sol\_09.doc", which is part of the homework solutions of the EE240 lectures found here: [http://www.edaboard.com/attachments/32826d1214214821-ee240\\_4995-rar](http://www.edaboard.com/attachments/32826d1214214821-ee240_4995-rar)

2. In this problem we will look at the design of MOM capacitors in our 7-level metal process. Unless otherwise noted, you should assume that all metal layers have a thickness  $T = 0.2\mu\text{m}$ , minimum width  $W = 0.14\mu\text{m}$ , minimum horizontal spacing  $S = 0.14\mu\text{m}$ , vertical spacing  $H = 0.2\mu\text{m}$ , and that the insulator is  $\text{SiO}_2$ . You can assume that the separation of the lowest layer of metal from the substrate is also  $H = 0.2\mu\text{m}$ , and that the inter-layer vias have the same width as the wires they are connected to. For simplicity, you can ignore fringing fields in all of these calculations.
- a. What is the maximum capacitance density (in  $\text{fF}/\mu\text{m}^2$ ) you can achieve with a simple horizontal parallel plate? What is the ratio of capacitance to bottom plate parasitic?

**Solution:**

Define  $N$  as the number of layers (7 in our case).  
 $C_{\text{HPP}} = (N-1)\epsilon_{\text{ox}}/H = (6 \cdot 3.9 \cdot 8.85 \text{ pF/m}) / 0.2\mu\text{m} = 1.035 \text{ fF}/\mu\text{m}^2$   
 $C_{\text{bot,HPP}} = \epsilon_{\text{ox}}/H$   
 $C_{\text{HPP}}/C_{\text{bot,HPP}} = 6$

- b. What is the maximum capacitance density (still in  $\text{fF}/\mu\text{m}^2$ ) you can achieve with a vertical parallel plate? Now what is the ratio of capacitance to bottom plate parasitic?

**Solution:**

$$C_{\text{VPP}} = \epsilon_{\text{ox}} \frac{NT + (N-1)H}{S(W+S)} = 3.9 \cdot 8.85 \text{ pF/m} * \frac{7 \cdot 0.2\mu\text{m} + 6 \cdot 0.2\mu\text{m}}{0.14\mu\text{m}(0.14\mu\text{m} + 0.14\mu\text{m})} = 2.289 \text{ fF}/\mu\text{m}^2$$

$$C_{\text{bot,VPP}} = \epsilon_{\text{ox}} \frac{W}{H(W+S)} = 3.9 \cdot 8.85 \text{ pF/m} * \frac{0.14\mu\text{m}}{0.2\mu\text{m}(0.14\mu\text{m} + 0.14\mu\text{m})} = .0863 \text{ fF}/\mu\text{m}^2$$

$$C_{\text{VPP}}/C_{\text{bot,VPP}} = 26.53$$

- c. In some processes, placing an inter-layer via requires the metal line to be wider than the minimum allowed. For this problem, let's assume that a metal line with a via must be at least  $0.21\mu\text{m}$  wide. In this case (and still ignoring fringing fields), what structure gives you the highest capacitance density, and what is that density?

**Solution:**

Let us compare the new vertical structure, and a "hybrid" capacitor like the one described in lecture that uses no vias (hence allowing minimal width) but alternates the terminals of the capacitor in both the vertical and horizontal directions in order to use both of those fields.

First, let's recalculate the density of the vertical parallel plate with the wider metal lines:

$$C_{\text{VPP}} = \epsilon_{\text{ox}} \frac{NT + (N-1)H}{S(W+S)} = 3.9 \cdot 8.85 \text{ pF/m} * \frac{7 \cdot 0.2\mu\text{m} + 6 \cdot 0.2\mu\text{m}}{0.14\mu\text{m}(0.21\mu\text{m} + 0.14\mu\text{m})} = 1.831 \text{ fF}/\mu\text{m}^2$$

The hybrid capacitor has a density of:

$$C_{\text{hyb}} = \epsilon_{\text{ox}} \left( \frac{NT/S}{(W+S)} + \frac{(N-1)W/H}{(W+S)} \right) = 3.9 \cdot 8.85 \text{ pF/m} * \frac{7 \cdot 0.2 / 0.14 + 6 \cdot 0.14 / 0.2}{0.14\mu\text{m} + 0.14\mu\text{m}} = 1.75 \text{ fF}/\mu\text{m}^2$$

**Continuation from p.5:**

Note that although our simplified calculation seems to indicate that the pure vertical parallel plate with the wider metal lines has slightly higher density than the hybrid structure, if we were to include fringing fields the hybrid structure would almost certainly have higher density.