Altium Designer

Module 18: Routing and Polygons

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18.1 Routing

18.1.1 Interactive routing

Routing is the process of defining connective paths between the nodes in each net.

Altium Designer includes a powerful Interactive Routing engine to help you efficiently route your board. There are two interactive routing commands, both are launched from the **Place** menu.

- **Interactive Routing** – you place track segments to route the selected connection. The routing engine attempts to find a path from the start of the connection (or last click location), to the current cursor location. The path it finds depends on the current routing mode, you can choose between: *Walkaround*, *Push*, *HugNPush* or *Ignore*. When you click, all segments will be placed (except the last one if the look-ahead option is enabled). You can also auto-complete the connection up to the target pad by holding the Ctrl key as you click, if the routing engine can identify a path. Existing routes can also be re-routed by simple placing new segments, with old redundant routing being removed when you finish defining the new route path (if the loop removal option is enabled).
- **Differential Pair Routing** – this command is used to route a pair of nets simultaneously. To do this, the nets must be defined as a differential pair.
- Once you have chosen one of the interactive routing commands, click on a connection line to commence routing that connection. Interactive routing shortcuts can be accessed at any time during routing by pressing the Shift+F1 keys, or by displaying the **Shortcuts** panel.

18.1.1.1 Managing connectivity

Once components are placed into a PCB file, *connection lines* display to indicate which pads belong in each net, and must be routed to create the connectivity defined in the schematic.

- Whenever there is an operation on a copper layer that affects connectivity, the PCB Editor analyzes the PCB to determine if any connections have changed. If you have routed a connection (joined 2 pads with track segments on a copper layer), the connection line between those 2 pads is no longer displayed. Also, if a shorter path for any connection is possible because of a routed connection, a shorter connection line is displayed.
- The arrangement or pattern of the connection lines in a net is called the *topology*. The default topology for all nets in a board is Shortest, as determined by the applicable Routing Topology design rule. Because it is shortest, as you move components around the connection lines may jump from one pad in the net to another pad in the net, maintaining the shortest possible length of connection lines for that net.
- You can change the color of the connection lines for a net in the *Edit Net* dialog, double click on the net name in the **PCB** panel to open the dialog.

18.1.1.2 Interactive Routing track width

When you select one of the **Interactive Routing** commands and start routing, the track width that you start with is determined by the **PCB Editor – Interactive Routing** settings in the *Preferences* dialog, working in harmony with the applicable Width Constraint design rules.

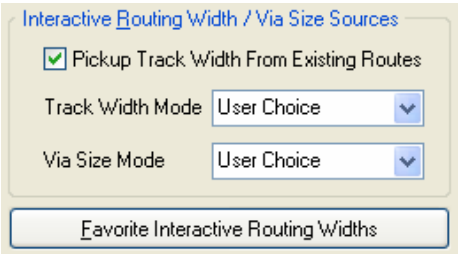


Figure 1. Interactive routing behavior is determined by these settings.

While the preferences allow you to change the width as you route, it is always constrained by the applicable rule – if you attempt to change it outside the range defined by the rule it will automatically be clipped back to the rule min or max, whichever is closer.

Track Width / Via Size Mode

- **User Choice** – With this mode enabled the routing width is selected from the list of favorite widths, press Shift+W while routing to display the list. Use the **Favorite Interactive Routing Widths** button in the preferences dialog to configure the list.
- **Rule Minimum** – With this mode enabled the Minimum size setting in the applicable design rule will be used.
- **Rule Preferred** – With this mode enabled the Preferred size setting in the applicable design rule will be used.
- **Rule Maximum –** With this mode enabled the Maximum size setting in the applicable design rule will be used.

Note: You can cycle between the above modes while interactive routing by pressing the **3** (for Track Width) or **4** (for Via Size) shortcut keys, the current setting is indicated on the Status bar.

18.1.1.3 Editing during Routing

As well as SHIFT+W to change the track width, there is another level of editing available as you route. Pressing the TAB key will open the *Interactive Routing for Net* dialog (Figure 2), where you can configure many of the interactive routing options, as well as edit the routing width and via size attributes.

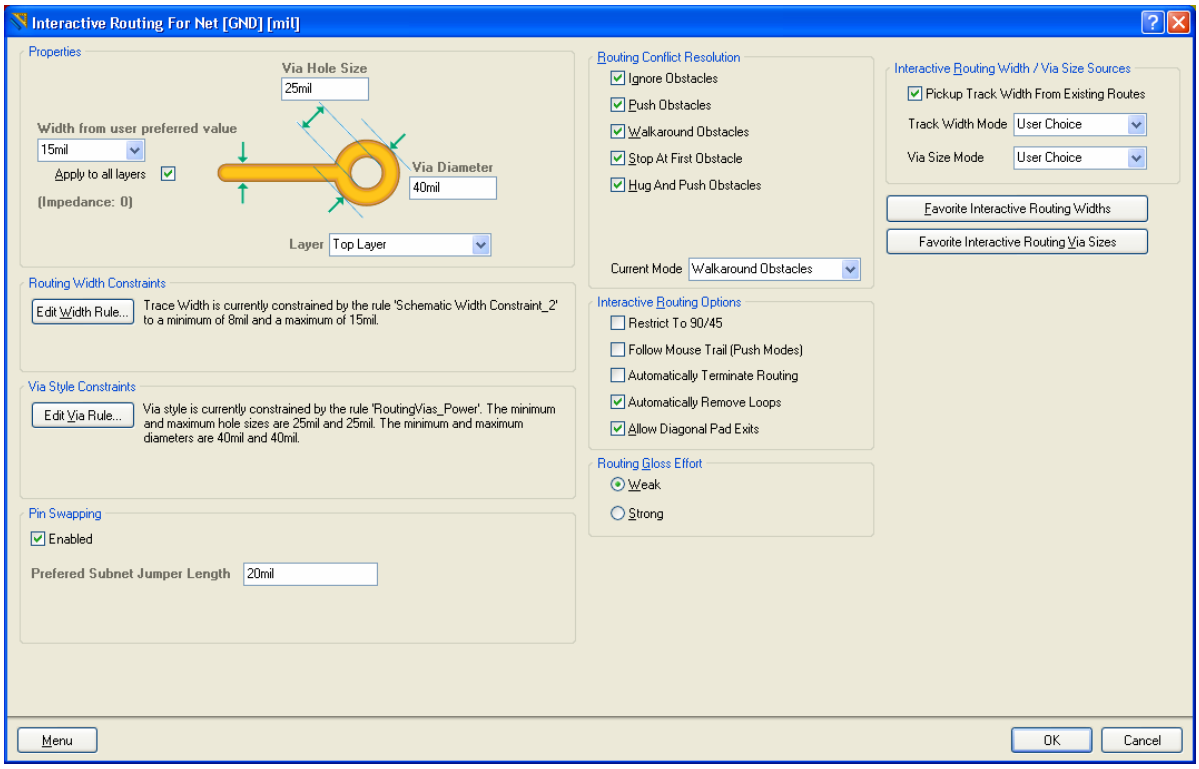


Figure 2. Interactive Routing dialog

18.1.1.4 Handling conflicts during Interactive Routing

As you route interactively you will be placing track segments amongst other objects that are already on the board. You can control how Altium Designer should handle a potential routing conflict. The conflict resolution mode is set in the **PCB Editor – Interactive Routing** page of the *Preferences* dialog, the applicable settings are shown in **Error! Reference source not found.**.

Conflict resolution modes include:

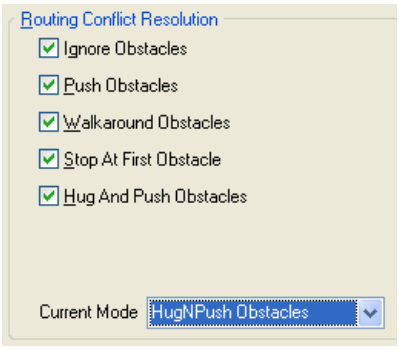


Figure 3. Define how interactive routing conflicts are handled.

- **None –** this is the Ignore mode, where conflicts are permitted. You can route over the top of existing objects. Violations are highlighted.
- **Push Conflicting Objects –** in this mode all existing tracks and vias will be pushed to make room for the new route.
- **Walkaround Conflicting Object –** in this mode the new route will *walk around* existing obstacles, or jump them if possible. As you move the cursor, the routing engine continually attempts to find the shortest path from the last click location to the current cursor location – click to define intermediate locations if you don't like the calculated path.
- **Hug And Push Conflicting Object –** in this mode the routing engine will follow existing objects, and only push them when there is insufficient room for the track being routed. In this mode the route path tends to follow the path you draw with the cursor.
- **Stop At First Obstacle –** in this mode the routing engine will stop at the first obstacle that gets in the way.

> **Note:** Press the **Shift+R** shortcut keys to cycle through the different modes while you are routing, keep an eye on the status bar to see which mode you are currently in.

18.1.1.5 Additional Interactive Routing Options

Altium Designer's routing capabilities have been developed to make the routing process efficient. There are another set of options that go toward that efficiency, which are also set in the **PCB Editor – Interactive Routing** page of the *Preferences* dialog (Figure 4).

These include:

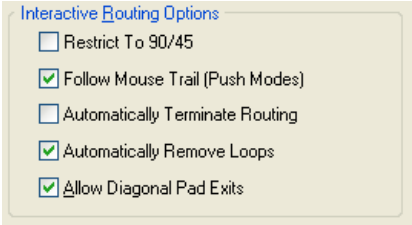


Figure 4. Additional interactive routing options.

- **Restrict to 90/45 –** there is a total of 5 possible routing corner modes, cycled through as you press SHIFT+SPACEBAR during interactive routing. Enabling this option will restrict this list to 2, you will only choose between 90 degree or 45 degree corners.
- **Automatically Terminate Routing –** with this option enabled, when you click on the target pad both the current track segment and the look-ahead segment are placed and you are automatically *released* from that route, ready to start on another connection.
- **Automatically Remove Loops –** with this option enabled, loops that are created during manual routing are automatically removed.

> **Note:** Automatic Loop Removal can be disabled on an individual net if you require routing loops in that net. Double-click on the net name in the PCB panel to access the net properties to alter this setting.

- **Hug Existing Traces (Walkaround Mode) –** with this enabled walkaround mode still attempts to find the shortest path from the last click to current cursor location, but makes hugging existing objects a higher priority than shortest distance.

18.1.1.6 Routing Gloss Effort

Weak or **Strong** are the two Options available here. The Routing engine will either optimise or tidy-up routes 'weakly' or 'strongly'. *Glossing* is the term used to describe how much of a 'clean up' the Routing engine should undertake.

18.1.1.7 Look-ahead routing

The PCB Editor's interactive routing mode incorporates a *look-ahead* feature that operates as you place tracks during routing. The track segment that is connected to the cursor is a look-ahead segment. The segment between this look-ahead segment and the last-placed segment is the current track that you are placing.

If look-ahead mode is active, you can use the look-ahead segment to work out where you intend to place the next segment and to determine where you wish to terminate the current segment. When you click to place the current segment, its end point will be positioned exactly where you need to commence the next segment. This feature allows you to quickly and accurately place tracks around existing objects and plan where the next track segment can be placed.

As you use the look-ahead segment to guide your routing, you will notice that the track end does not always remain attached to the cursor, it clips as you approach an existing obstacle (if the conflict resolution mode is set to stop at first conflicting object). This feature prevents you from violating any clearance constraints.

Note: The look-ahead mode can be toggled off and on while interactively routing by pressing the 1 key. If look-ahead is off each click will place both the 2nd last and the last track segments.

18.1.1.8 Working with the Electrical Grid

Whenever you are placing an electrical object, like a track during routing, the Electrical grid is active. An octagonal graphic on the cursor indicates that the Electrical Grid is in operation, pulling the cursor to an existing object on the board. This feature is ideal for routing to off-grid pads. You can inhibit the electrical grid if there is a situation where it is working against you; hold the CTRL key during interactive routing to do this.

Note: Shift+E cycles through the three electrical grid modes, including; off, on for current layer, on for all layers. The current state is displayed on the Status bar.

18.1.1.9 Changing the routing - automatically remove loops, or drag tracks

Altium Designer has 2 methods for changing existing routing: rerouting using the Interactive Routing command, and dragging track segments.

- **Loop removal** is a feature that automatically removes redundant track segments as you re-route a connection. Using loop removal you can easily re-route existing routing, as soon as you terminate routing any redundant routing is automatically removed. This includes complex routes that pass through many layers, redundant vias are automatically removed along with track segments.
- **Dragging tracks**, you can also drag track segments and preserve the 45 angle to the adjoining track segments. To do this first click to select the segment and the special cursor will indicate the mode (Figure 5). Then click and drag to move the segment. Alternatively, instead of clicking once to select the track segment first, hold the CTRL key as you click and drag on the segment.

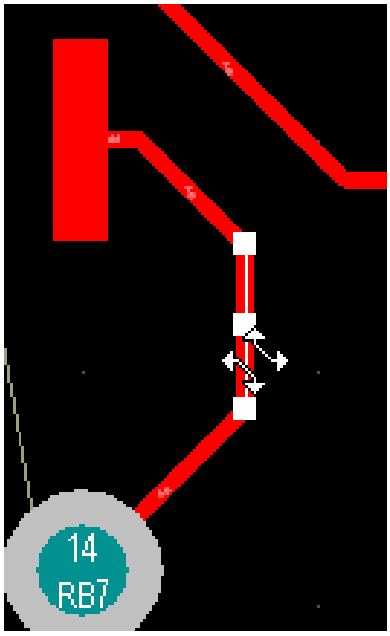


Figure 5. Note the special cursor, indicating that corner angles will be preserved when the selected segment is dragged.

- **Dragging Arcs**, you can also drag arc segments and preserve their concurrency. Simply click to select the routing segment(s) you wish to drag – the cursor will change to a quad arrow, see Figure 76 for more details– and then click and drag to slide to the new location. Alternatively, use the Ctrl+click & drag shortcut to drag without having to select first.

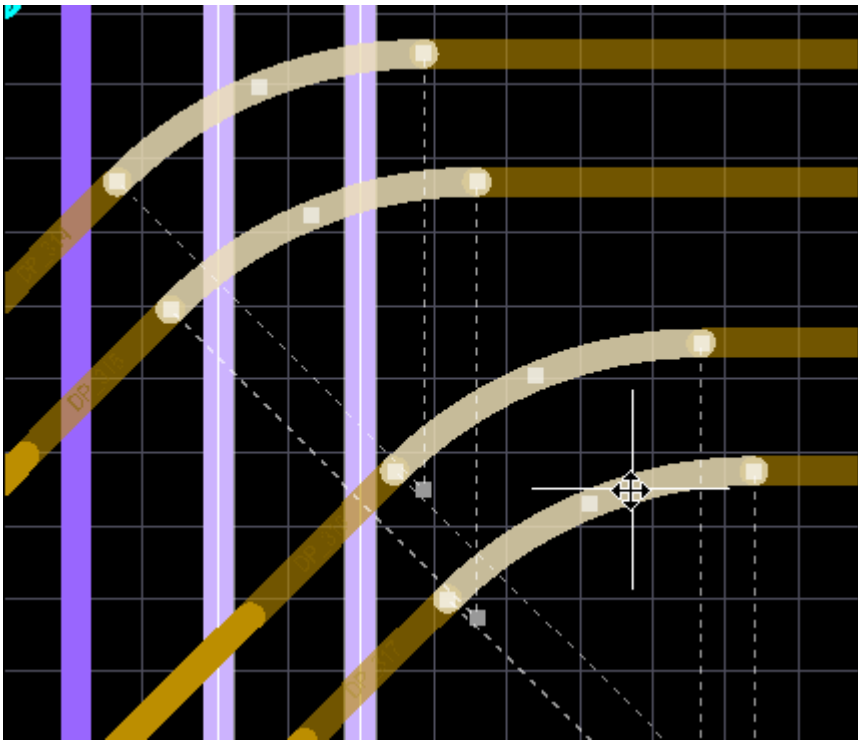


Figure 6. Note the special quad arrow cursor that appears when dragging arcs.

18.1.2 Exercise – Interactive Routing

In this exercise, you will route all the connections between the LCD module (`LCD1`) and the PIC microcontroller (`U1`).

1. Select **Place » Interactive Routing** and then, starting at the right-hand side of LCD1, route the connections from the LCD1 pads to the U1 pads.
2. Attempt to route one of the power nets.
3. As you are routing the connections, explore the various interactive routing options. Press the **~** key (or **Shift+F1**) to display them.
4. If you are going well, route the rest of the board.

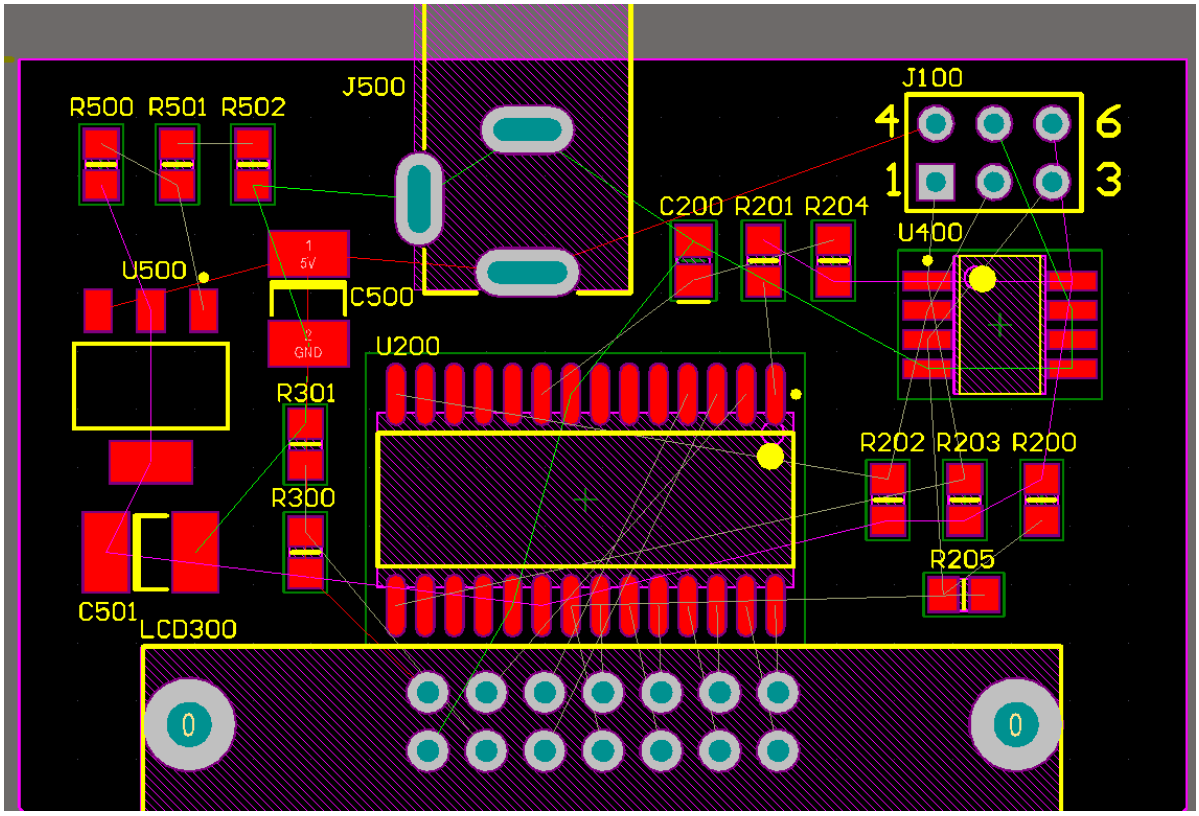


Figure 7. The placed board, ready to route.

Tips for routing

- It can help to change the connection line color for important nets. To do this, double-click on the net name in the PCB panel.
- You can also control which connection lines are displayed by pressing the N shortcut to pop up a display control menu.
- Disabling the display of specific layers, such as the component overlay, can also help. Press the L shortcut to pop up the *View Configurations* dialog.
- Press the * key on the numeric keypad to switch to the next signal layer while routing.
- Press the CTRL+G shortcut keys to display and edit the current snap grid. 5 mils works well for this design.
- For a 2 layer board it is generally advisable to have one layer for predominantly horizontal routing, and the other for predominantly vertical routing.
- Press SPACEBAR during routing to toggle the start-end for the 45 degree track.
- Press SHIFT+SPACEBAR to toggle the corner mode.
- While routing a net, press the SHIFT+R shortcut keys to cycle the conflict resolution modes – keep an eye on the status bar to check the current mode.
- While routing a connection, hold CTRL as you click to automatically complete the routing of that connection.
- To examine the routing of a net, CTRL+Click on the routed net to highlight the entire net. CTRL+CLICK in free space to clear the highlight. Use the **Mask Level** button to control the fading.

18.1.3 Differential Pair Interactive Routing

Differential signaling is fast becoming the preferred signaling interface method, driven by the ever increasing signal speeds in electronic products. Altium Designer has excellent support for differential signaling – from defining pairs on the schematic, through to interactive differential pair routing on the PCB.

- Differential pairs are routed as a pair – that is you route two nets simultaneously. To route a differential pair select **Place » Differential Pair Routing** from the menus. You will be prompted to select one of the nets in the pair, click on either to start routing.
- Press the Tilda (~) or **Shift+F1** keys to display a list of differential pair routing shortcuts.

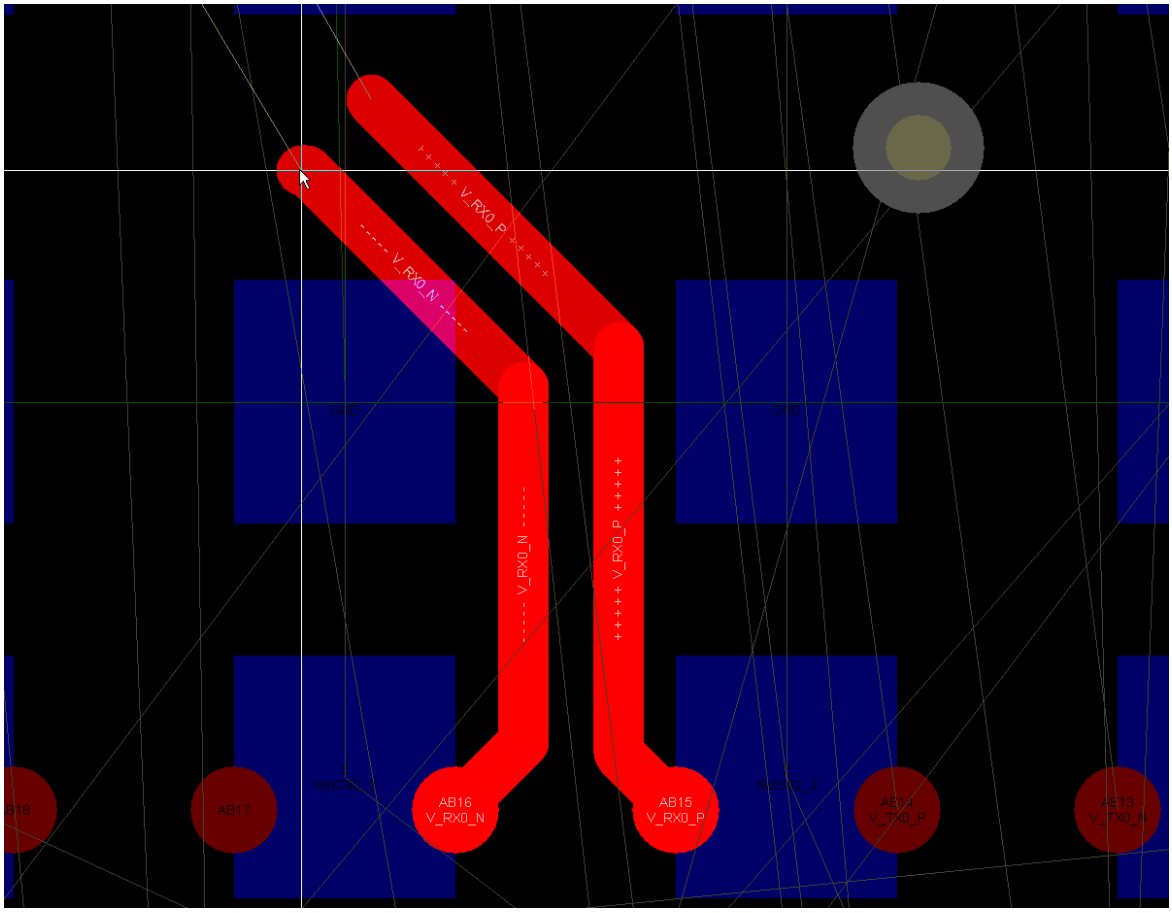


Figure 8. A differential pair being routed, note that both connections in the pair are routed simultaneously.

Note: For more information on Altium Designer's differential pair routing capabilities, refer to the application note, *Interactive and Differential Pair Routing*.

18.1.4 Multi trace routing

There is two ways of using the multi trace routing, by dragging multiple track ends, or by placing multiple traces.

- The smart drag function allows a group of tracks to be selected and then extended as a single entity. You can use successive drags to continue to add new segments.

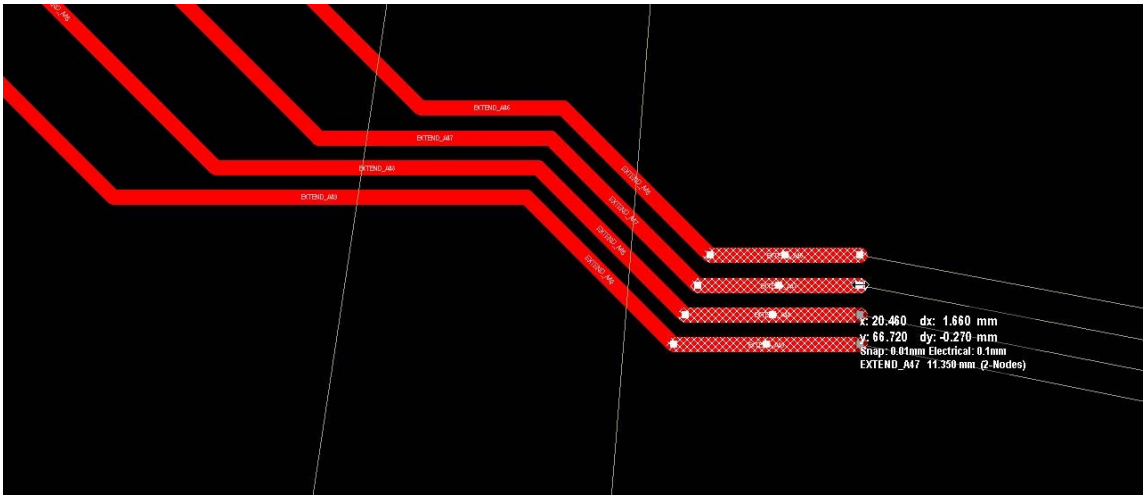


Figure 9. The smart drag tool can be used to extend selected traces, as shown above.

- The smart drag tool is a basic tool in that it only works on existing bus routes. The alternate approach is to use the multi trace routing tool, **Place » Interactive Multi-Routing**.
- Using this command you can start with an unrouted component and effectively pull the routing out of the *selected* component pads.
- The multiple traces are then automatically gathered together, as shown in Figure 10. Simply move the cursor around as you place the multiple traces to explore various gather options.

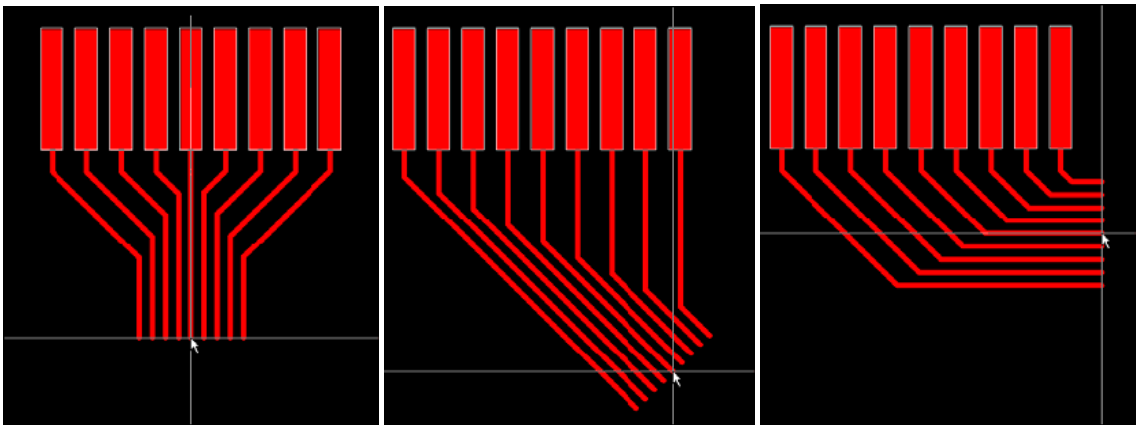


Figure 10. Use Multiple Traces command to start from selected pads in an unrouted component. Move the cursor to explore gathering options.

- Rather than selecting component pads one by one, hold the **Ctrl** key as you click and drag a rectangle to select multiple pads. Holding Ctrl limits the selection to the pad objects only, rather than selecting the parent component. This technique also works with the **Select Touching Line** and **Select Touching Rectangle** commands.
- Press the **Tab** key to open the **Bus Routing** dialog, where you set the Bus Spacing (track center to track center separation).

- Alternatively, use the **,** (comma) and **.** (full stop) shortcuts to interactively decrement and increment the bus spacing, in steps of the current snap grid.
- Press the \ (Backslash) to change the end alignment (once the first set of segments has been placed).
- Press the **~** (Tilda) or **Shift+F1** keys for a list of interactive shortcuts.

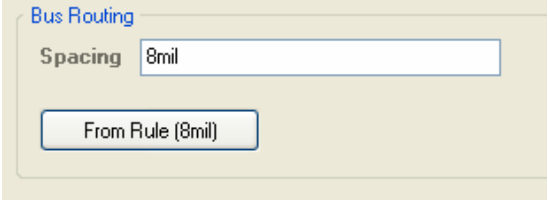


Figure 11. Setting the bus routing spacing.

18.1.5 Interactive Length Tuning

Matching route lengths is a standard technique for maintaining data integrity in a high-speed digital system, and an essential ingredient of differential pair routing. **Interactive Length Tuning** allows a dynamic means of optimizing and controlling net lengths by allowing variable amplitude patterns to be inserted according to the available space, rules, and obstacles in your design.

- Launched from **Tools » Interactive Length Tuning** menu, tuning can be based on: design rules, properties of the net, or values you enter into a dialog. Once launched, click on the routed net and move the mouse along the route path to add tuning segments.
- The Interactive Length Tuning cursor guides you during the tuning process. The yellow cursor bars indicate the possible minimum and maximum lengths. The green bar indicates the target length, and the sliding indicator shows how close you are to achieving a match, as shown in Figure 12.
- Press Tab during length tuning to open the *Interactive Length Tuning* dialog (Figure 12), where the tuning behavior is configured.
- Target Length can be controlled to meet: design rules, an existing routed net, or manual.
- Three tuning styles available: Mitered with Lines, Mitered with Arcs, and Rounded.
- Option to precisely clip tuning patterns to **Target Length** when Mitered with Lines and Mitered with Arcs styles are used.
- Tuning patterns and properties (such as pitch and amplitude) can be controlled using shortcuts, press Shift+F1 for a list.

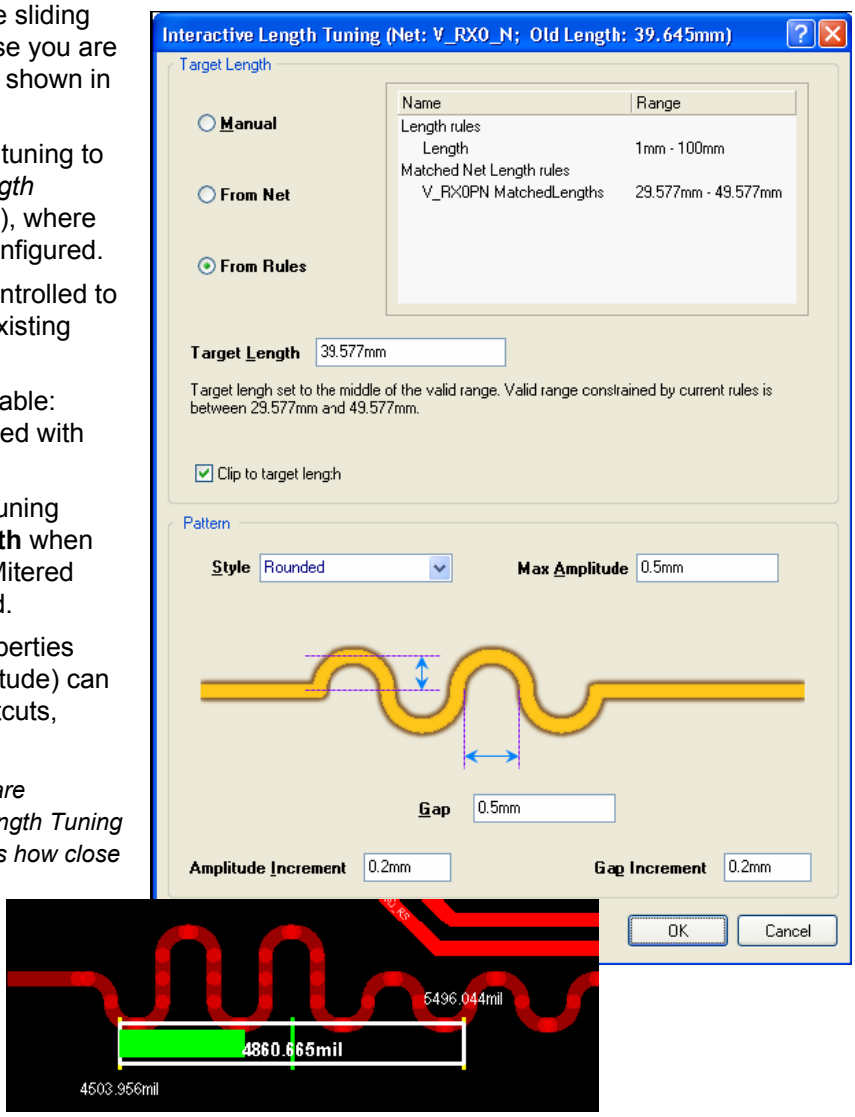


Figure 12. Tuning parameters are configured in the Interactive Length Tuning dialog. The tuning cursor shows how close the current route length is to the required length.

18.2 Testpoint System

Testing is an important part of the board manufacturing process. After fabrication, the board must be tested to ensure no short or open circuits. Once fully populated with all its components, a board is tested again to ensure signal integrity and device operation. To aide in this process, it is fundamentally beneficial to have a scheme of points on the board – testpoints – which the testing equipment can probe and perform the required tests.

The location of testpoints on a board will depend on factors including the mode of testing and the test equipment used. For example, when performing bare-board fabrication testing, the board is not populated and so all pads and vias are 'fair game' when it comes to assigning testpoints. The locations used for testpoints when performing in-circuit assembly testing however, will almost always be different. As the board is populated, you may no longer have probe access to component pads and certainly no access to pads and vias under a component!

Altium Designer provides a powerful system to handle your testpoint needs and enhance the testability of your boards, allowing you to separately assign testpoints for bare-board fabrication testing and/or in-circuit assembly testing as required. Testpoints can be assigned manually or, in a more streamlined and automated fashion, using the *Testpoint Manager*.

18.2.1 Considering Your Testpoint Strategy

Before jumping into the assignation of pads and vias for use as testpoint locations, it is a good idea to step back and think about what is required. The following are just some pointers to consider when defining a strategy to incorporate testpoints into a design:

- When choosing the side of the board that testpoints will be allowed on, consideration should be given to the testing processes and associated fixtures that will be used. For example, will the board be probed from the bottom side only, the top side only, or both sides.
- A testpoint underneath a component (on the same side of the board as the component) is usually used at the bare-board testing stage. This should be taken into consideration when planning testpoint locations for assembled board testing.
- It is advisable to locate all testpoints on one side of the board only, using vias to achieve this if necessary. The reason for this lies in the fact that a dual-head test fixture incurs greater cost than a single-head test fixture.
- The more non-standard and complex your pattern of testpoints, the more costly it will be to configure a fixture with which to test the board. The best philosophy is to develop a methodology that will result in generic testability. A well-honed and adaptable testpoint policy will allow different designs to be tested efficiently and cost-effectively.
- Careful consideration should be given to any via tenting requirements of the design. Tenting a testpoint-designated via will effectively block test probe contact. Even partial tenting using a liquid photoimageable (LPI) solder mask will cause contact problems, as the mask liquid will tend to run away through the via hole. Peelable solder mask may indeed be used to provide temporary tenting of such designated vias, but this can often prove quite costly.
- Consult with your fabrication and assembly houses closely to make sure any specific design parameters are taken into account when specifying testpoints. These could include testpoint-to-testpoint clearances and testpoint-to-component clearances that may be stricter than normal placement and routing clearances.

18.2.2 Pad and Via Testpoint Support

Altium Designer provides full support for testpoints, allowing you to specify pads (thru-hole or SMD) and/or vias to be used as testpoint locations in fabrication and/or assembly testing. A Pad or Via is nominated for use as a testpoint by setting its relevant testpoint properties – should it be

a fabrication or assembly testpoint, and on which side of the board should it be used as a testpoint. These properties are set from within the Pad or Via properties dialogs.

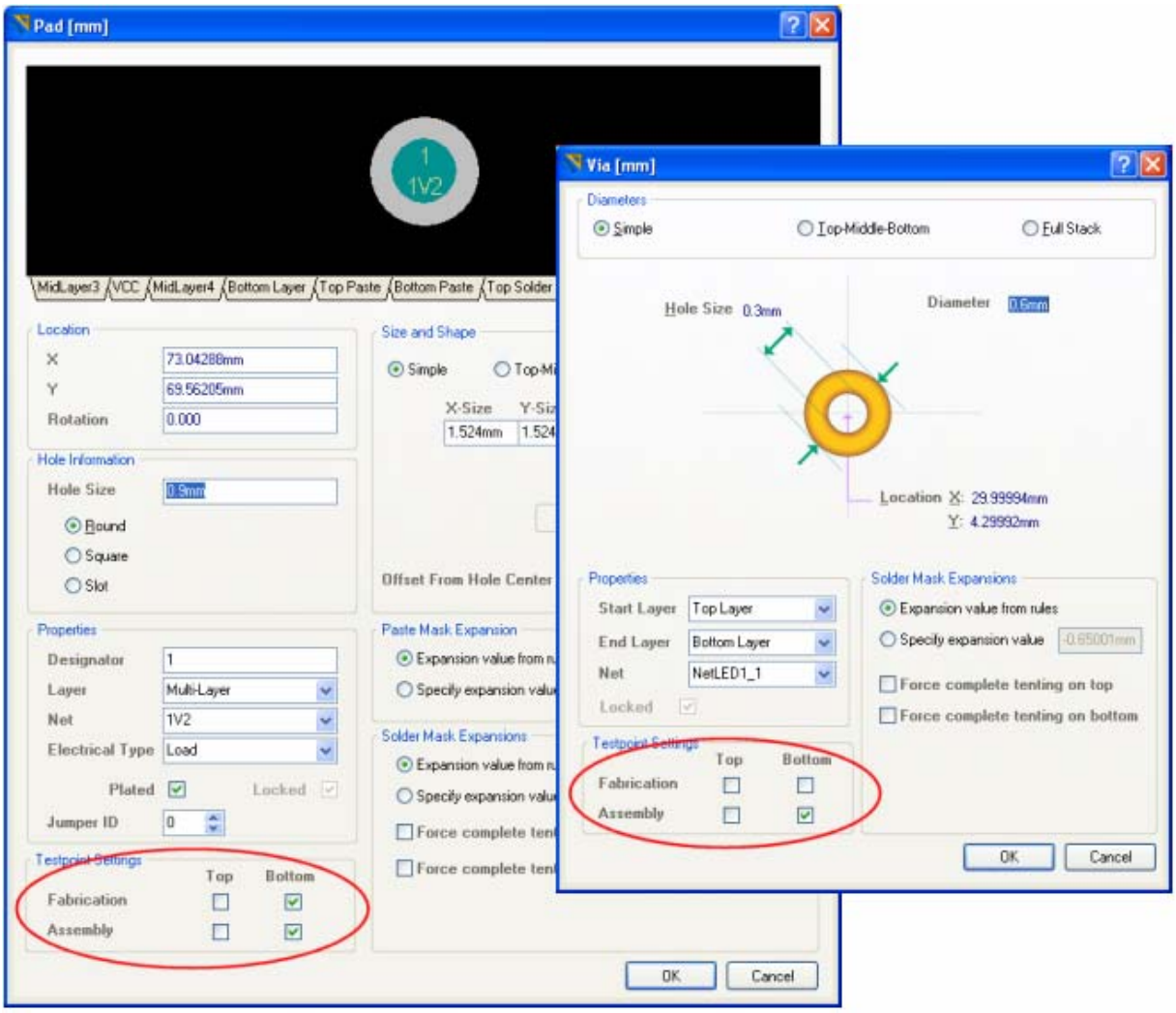


Figure 13. A pad or via is specified for use as a testpoint through the relevant options in its associated properties dialog.

You can automatically assign testpoints based on defined design rules and using the *Testpoint Manager*. This automated assignment simply sets the relevant testpoint properties for the pad/via in each case. You of course have the option to manually specify testpoints – in essence, handcrafting at the individual pad/via level – giving you full control over the testpoint scheme employed for your board.

18.2.3 Design Rules

The constraints of a PCB design should be thought out and implemented as a well-honed set of design rules. To implement a successful testpoint scheme – where all defined testpoints can be accessed and used as part of the bare-board and/or in-circuit testing, governing constraints must be put in place. To this end, the following rule types are definable as part of the PCB Editor's Design Rules system:

Access and define rules of these types from the *PCB Rules and Constraints Editor* dialog (**Design » Rules**).

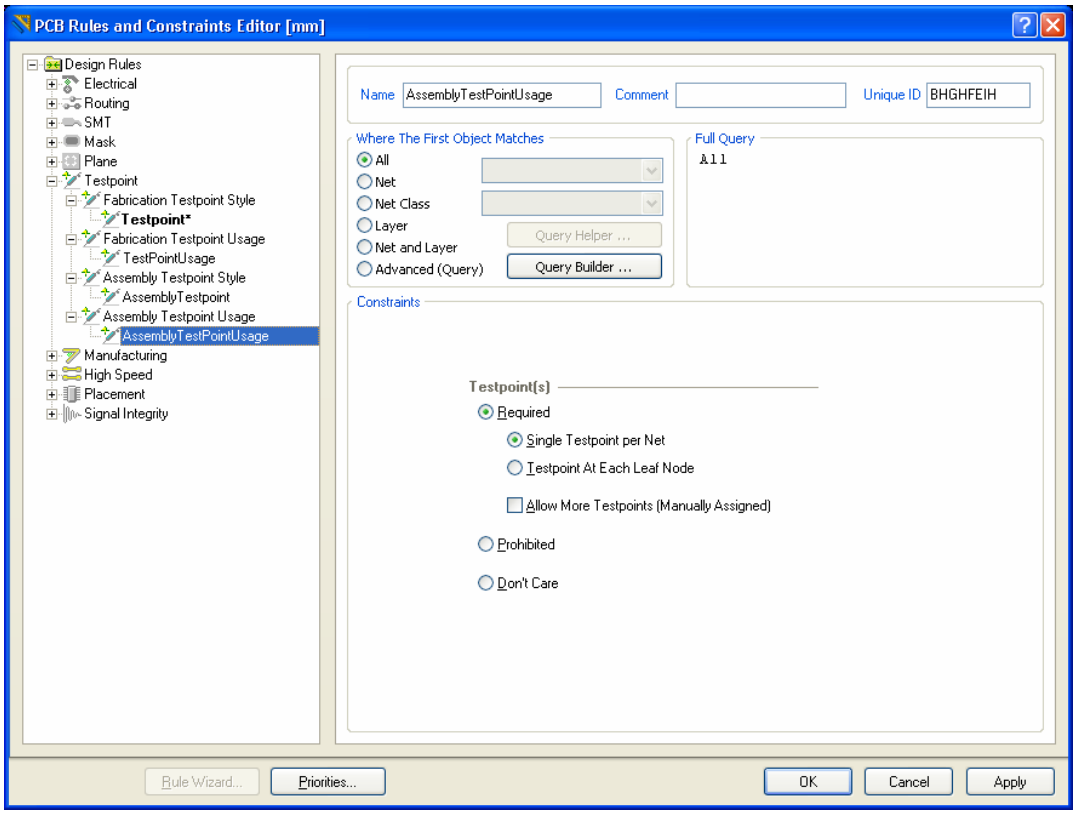


Figure 14.Define separate design rules to constrain which pads and/or vias in the design can be used as Fabrication testpoints and Assembly testpoints, and which nets require testpoints.

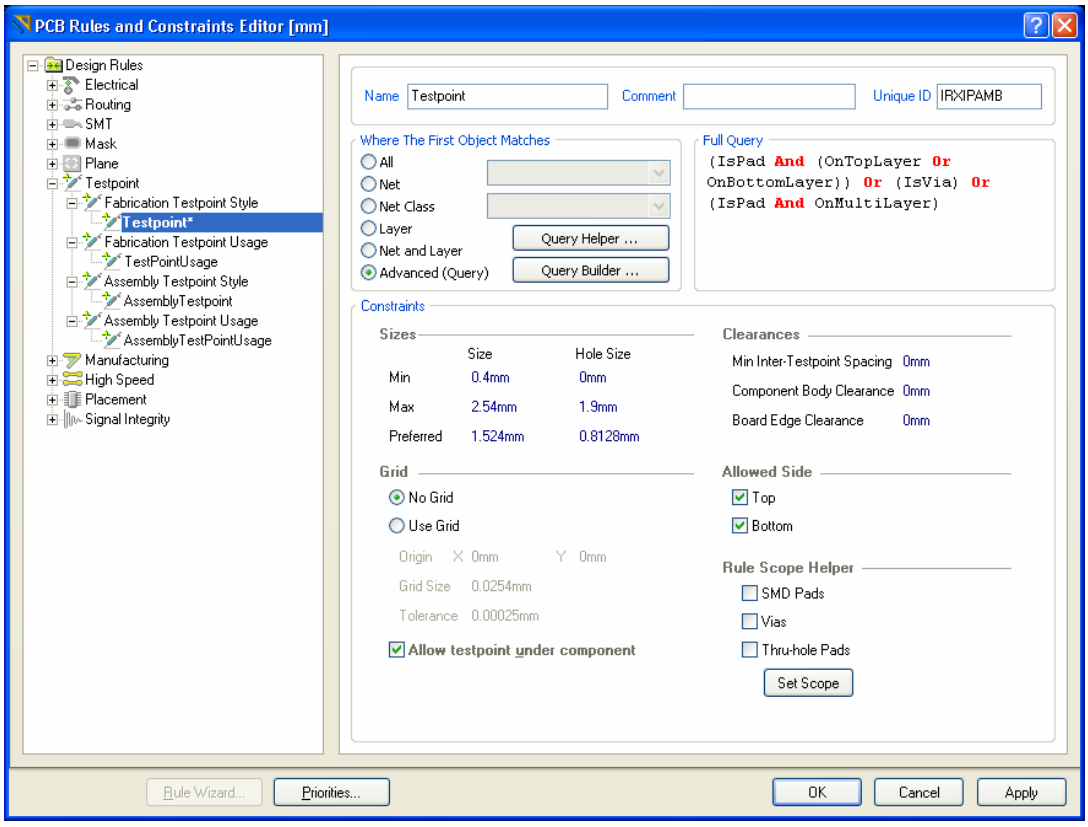


Figure 15. Define separate design rules to constrain which pads and/or vias in the design can be used as Fabrication testpoints and Assembly testpoints, and which nets require testpoints.

The Testpoint Style and Usage rules are identical, in terms of constraints, between the two testing modes (fabrication and assembly). The style rule essentially specifies constraints that a pad or via has to meet in order to be considered for selection as a testpoint location. The usage rule simply specifies which nets require a testpoint. When defining a style rule, the rule scope can be quickly created to target the precise pad and/or via objects for testpoint consideration, using the *Rule Scope Helper*.

The testpoint design rules are used by the *Testpoint Manager*, the Autorouter, Online and Batch DRC processes and also during output generation.

Default Fabrication and Assembly Testpoint Style and Testpoint Usage rules exist. You should check whether these rules meet your board requirements and make changes as necessary.

When opening PCB designs or importing design rules created in a release of the software prior to the Summer 09 release, Testpoint Style rules will become Fabrication Testpoint Style rules and Testpoint Usage rules will become Fabrication Testpoint Usage rules.

18.2.4 Managing Testpoints

Assigning testpoints manually can be a painstaking and laborious job at the best of times. Imagine this task on a more complex board, populated with hundreds of components (possibly on both sides of the board) and the process cries out for a more automated method of testpoint assignment. To cater for streamlined management of testpoints in your board designs, Altium Designer equips the PCB Editor with a *Testpoint Manager*.

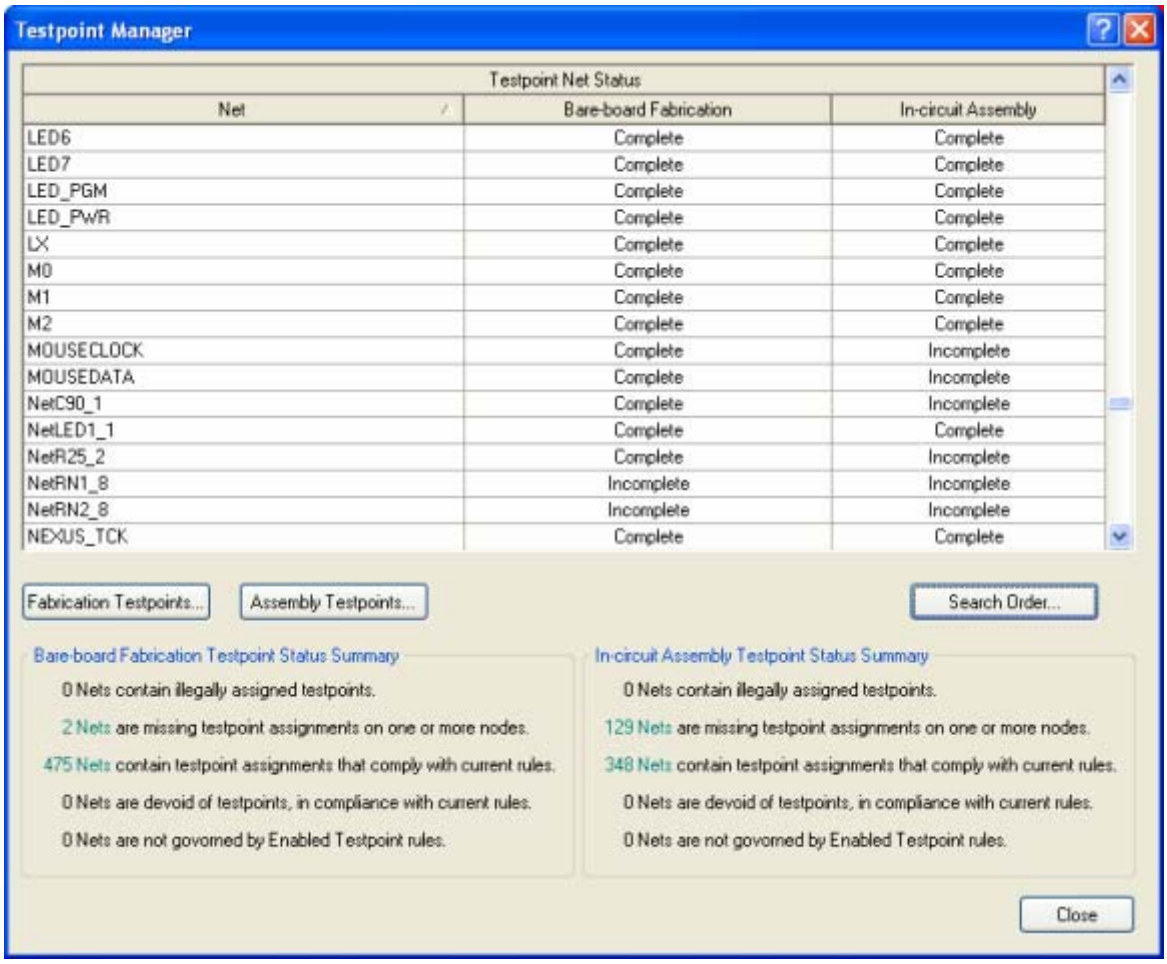


Figure 16. Manage your fabrication and assembly testpoint requirements quickly and efficiently using the Testpoint Manager.

Accessed from the PCB Editor's main Tools menu (**Tools » Testpoint Manager**), the *Testpoint Manager* provides controls allowing you to automatically assign and clear testpoints from the one convenient location. A listing of all nets in the design is provided, with status to indicate testpoint coverage – either `Complete` or `Incomplete` – for both bare-board fabrication and in-circuit assembly testing.

Whether assigning testpoints for some or all of the nets in a design, the *Testpoint Manager* follows the style and usage rules defined for fabrication and assembly testpoints. Where rules are defined to use a single testpoint per net, a definable search order of pad/via object types is provided – giving you even finer control over the priority by which such objects are considered.

A full summary of the testpoint status – for both testing modes – is also displayed and this updates with each assignment or clearance action performed.

The *Testpoint Manager* replaces the **Tools » Find and Set Testpoints** and **Tools » Clear All Testpoints** commands found in releases of Altium Designer prior to the Summer 09 release.

18.2.5 Checking the Validity of Testpoints

Defined fabrication and assembly testpoint rules are followed as part of the PCB Editor's Design Rule Checking (DRC) facility. Online and/or Batch DRC checking can be enabled for the various rule types from within the *Design Rule Checker* dialog (**Tools » Design Rule Check**).

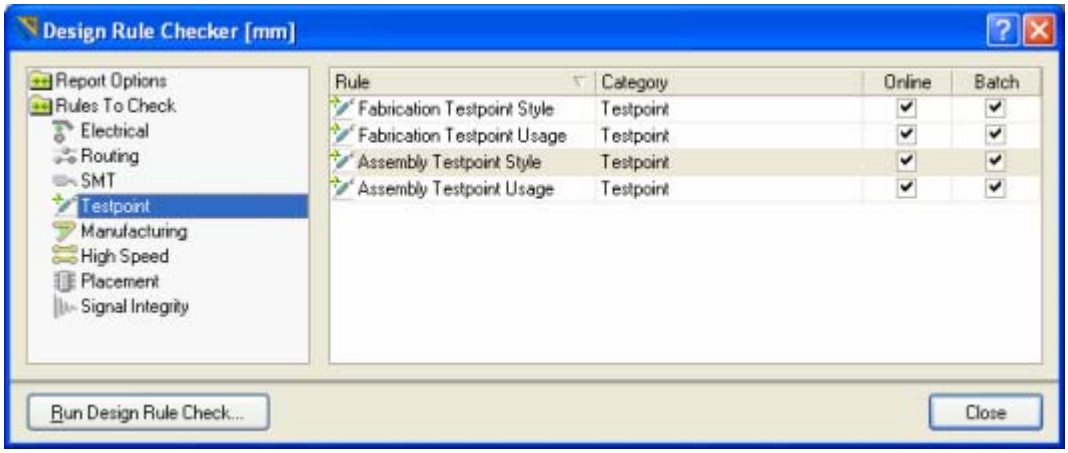


Figure 17. Include your testpoint design rules as part of the Online or Batch DRC processes.

18.3 Adding and removing teardrops

Teardrops are a common technique for guarding against drill breakout during the board fabrication phase.

- The **Tools » Teardrops** command is used to add or remove tear-dropping from pads and/or vias.
- Options are configured in the **Teardrop Options** dialog (Figure 18).
- To remove teardrops use the **Remove** option in the **Teardrop Options** dialog.
- Teardrop shapes are created by adding additional short track or arc segments.
- Use the **Report** option to identify pads/vias where teardrops could not be added.

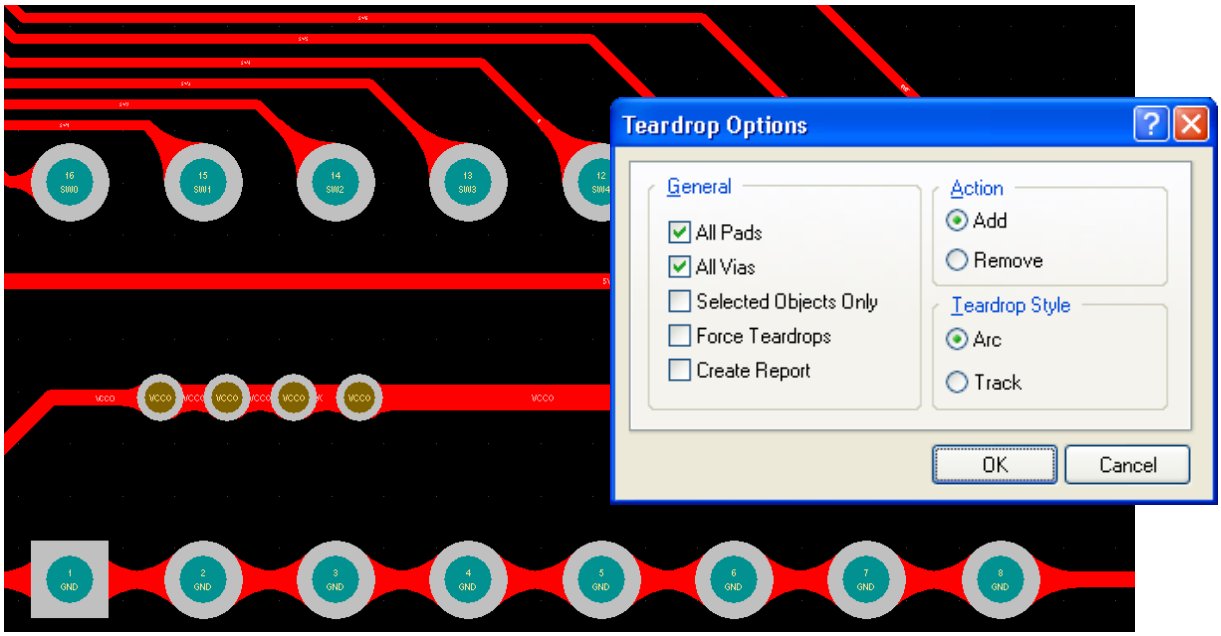


Figure 18. Teardrops build up the copper at each track entry to pads and vias.

- Choose the **Selected Objects Only** option to control which pads/vias should have teardrops added.
- The **Force Teardrops** option will apply teardrops to all pads and/or vias, even if it results in a DRC violation.

> **Note:** Arc-style teardrops can create complex shapes at the pads/vias. When polygons are poured over routing with arc-style teardrops, part of the polygon near the teardrop can "break off" (a section of the polygon is missing). If this occurs try a Solid style polygon instead of Hatched, or change the teardrop style from Arc to Track.

18.4 Automatic routing

Altium Designer's autorouter is a topological autorouter – it uses topological mapping to find routing paths on the board. The Autorouter adheres to all electrical and routing design rules, except the Routing Corners and Differential Pair design rules.

18.4.1.1 Autorouting tips

- The board must include a closed boundary on the Keep Out layer.
- Design rules must be correctly defined for the router to be able to route, it will not route connections that would result in a design rule violation. If there are potential rule conflicts they will be detailed at the top of the *Situs Routing Strategies* dialog. Always check that the rules are appropriately defined before starting the autorouter.
- Routing layer directions must be configured. Default directions are assigned, but these do not take into consideration any existing manual routing, so they should always be checked. Routing layer directions are configured by clicking the **Edit Layer Directions** button in the *Situs Routing Strategies* dialog.
- You can protect pre-routed connections, fan-outs and entire nets by enabling the **Lock all Pre-routes** option in the *Situs Routing Strategies* dialog (**Auto Route » Setup**). This option also protects fan outs and partially routed connections.
- Objects with a net name that are not locked may be moved/ripped up during routing.
- Objects placed on the Keep Out layer create blocks for the router on all layers.
- Signal layer keepout objects create blocks for the router on that signal layer.
- The router does not consider objects on the mechanical layers.
- The router is sensitive to connection lines running at very shallow angles, experiment with the alignment of components to observe this.

18.4.1.2 Running the Autorouter

- The Autorouter requires minimal set up. To run the router using a default strategy, select **Auto Route » All** to display the *Situs Routing Strategies* dialog, select a strategy, and click OK to start routing.
- Use the **Auto Route » Stop** command to terminate autorouting.

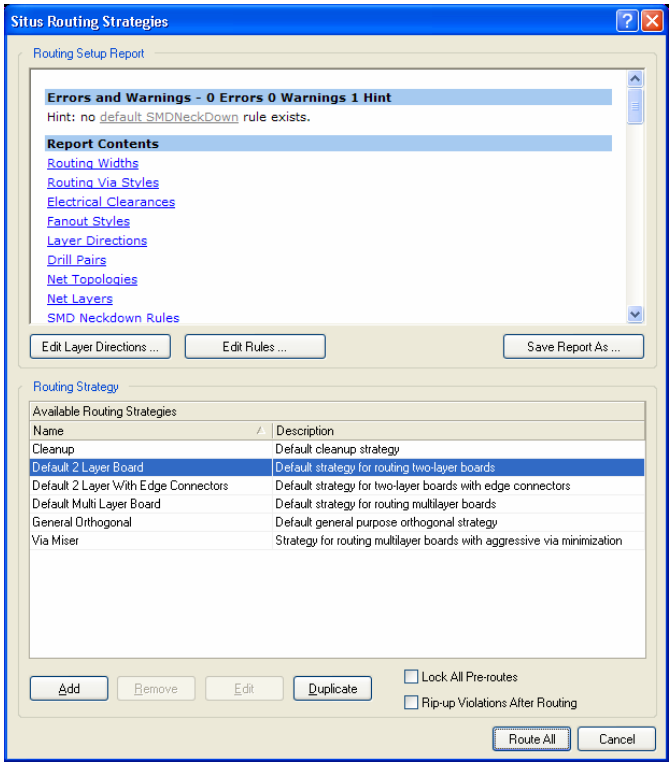


Figure 19. Autorouter strategy dialog

18.4.1.3 Creating a Custom Routing Strategy

- To create a custom routing strategy select one of the default strategies in the *Routing Strategies* dialog and click **Duplicate**.
- As well as defining the set of routing passes, you can also control the via cost, and the router's tendency to route more diagonally or more orthogonally. If you enable the Orthogonal option in the *Situs Strategy Editor* you should add a Recorner pass to the strategy.

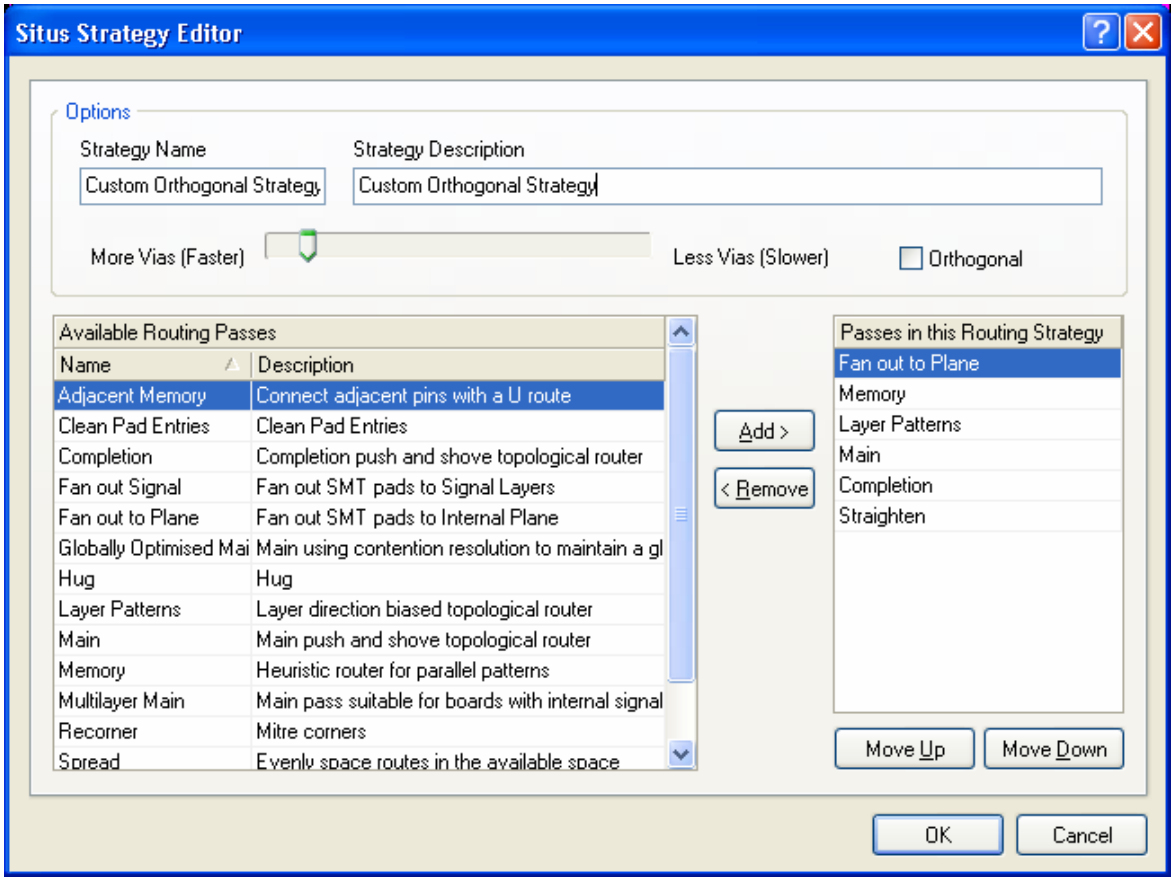


Figure 20. Custom routing strategy using cheaper vias and orthogonal routing

18.4.2 Exercise – Autorouting

1. Select **Autoroute » All** from the menus.
2. Select the **Default 2 Layer Board** strategy, enable the **Lock All Pre-routes** option if you would like to keep your hand routing, and click the **Route All** button.
3. Examine the routing results. To more easily check each layer, press the **Shift+S** shortcut to toggle to single layer mode, then press the * key to toggle back and forth from Top layer to Bottom layer. To highlight the routing of a particular net hold the **CTRL** key and click on the net. Repeat this where there are no objects under the cursor to clear the highlight. If you have the board in single layer mode, you can enable the **Show All Primitives in Routed Net** checkbox in the *Preferences* dialog to show the routing on all layers.
4. Now unroute (**Tools » Un-route**) so it can be rerouted using a custom strategy. To do this, duplicate the Default 2 Layer Board strategy, set the **More Vias** slider to close to the left end, enable the **Orthogonal** checkbox, and add a **Recorner** pass before the **Straighten** pass (as shown in Figure 20).
5. Autoroute the board with the custom strategy.

6. When you are happy with the routing results, save the board.

18.4.3 BGA Escape routing

The BGA escape routing engine will attempt to route each pad out to just beyond the edge of the device – making the remaining routing challenge much easier.

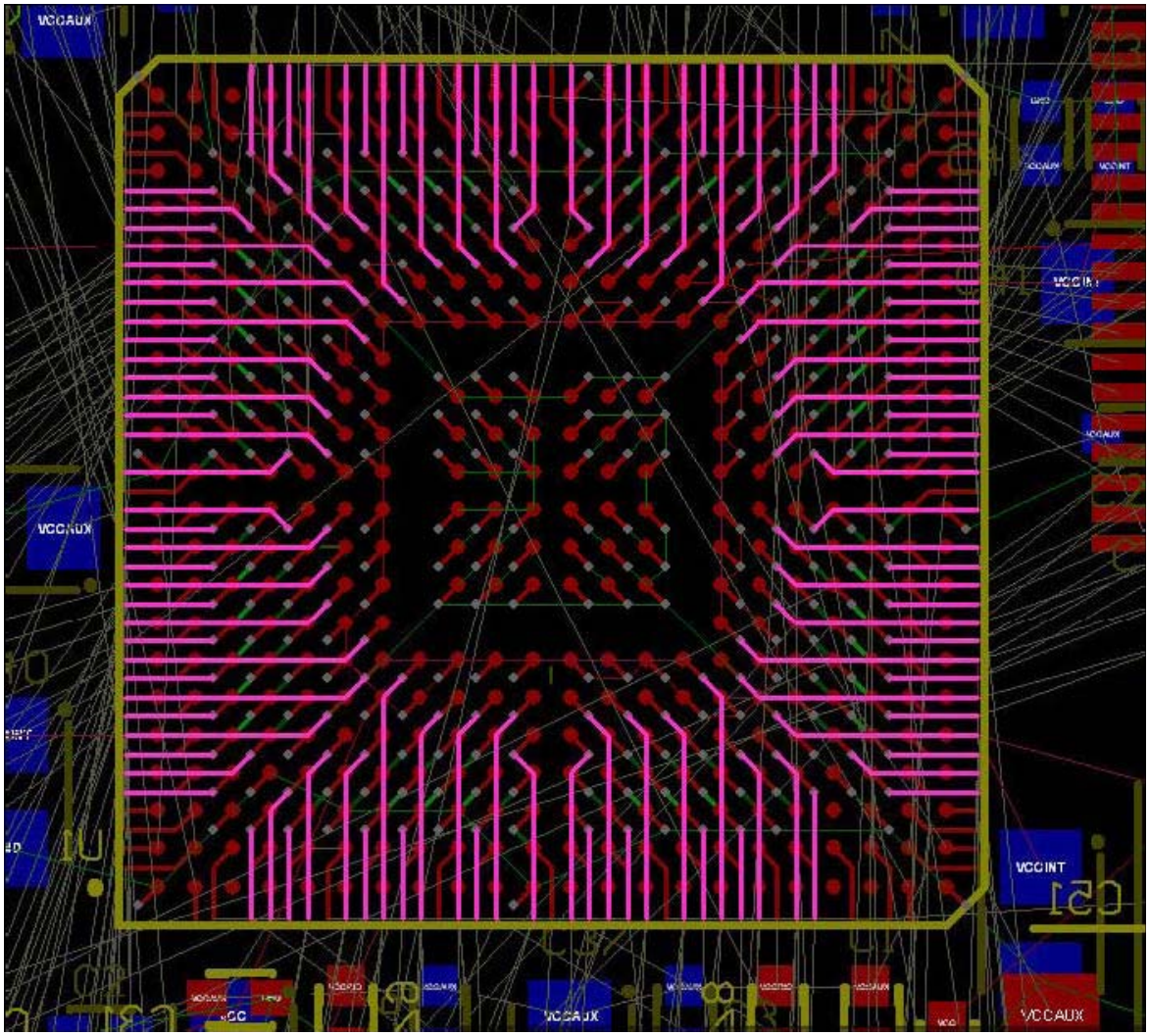


Figure 21. Note how the escape route feature presents each connected pad as an accessible route outside the edge of the BGA.

- Figure 21 shows the escape routing from a 1mm pad pitch BGA. Used inner pads are first fanned out using the traditional dog-bone (a short route with a via on the end) to access another layer, and then from the via they are escape routed out just beyond the edge of the device, working through the available routing layers until all pads have been escape routed.
- Right-click on a BGA and select **Component Actions » Fanout Component** from the context menu. The routing will be done in accordance with the applicable design rules (track and via sizes). A report of all pads that could not be escape routed will be generated and opened, click on an entry in the report to cross probe to the PCB and examine that object.

> **Note:** The most common reason escape routing fails is because the vias will not fit between the BGA pads. Ensure that there is a suitable Routing Via Style design rule configured to allow suitably small vias to be used for escape routing.

18.5 Polygons and the Polygon Manager

A signal layer polygon is an area of copper which is placed over existing objects, such as tracks and pads, but automatically pours around them, maintaining the specified clearances.

- A polygon can placed to define any enclosed shape.
- A signal layer polygon maintains clearances, defined by the Clearance design rules, from other copper objects.
- A signal layer polygon can be connected to a net.
- A polygon can be Solid or Hatched.
- A Solid polygon is built from Region objects. The advantage of this style of polygon is that there is typically much less data to store in the PCB file, and also less data in the CAM (Gerber or ODB++) files. Also region objects have sharp corners, so the polygon can sometimes better fill the space between other objects.
- A Hatched polygon is built from tracks and arcs. The advantage of this style of polygon is that the CAM processing software does not need to understand polygonal shape definitions.
- Polygons can be placed on other layers, but only pour around other objects on signal layers.
- Polygons can be created from a selected set of primitives, such as lines, as long as they form a closed boundary. Use the command in the **Tools » Convert** submenu.
- Polygons can be shelved, a process that hides them from other design objects, but does not remove them. Shelved polygons can be restored at any time.

18.5.1 Placing a polygon

- Place a polygon using the **Place » Polygon Pour** menu command or the  toolbar icon. This displays the *Polygon Pour* dialog, where you set up the parameters for the polygon. Note that there are 2 different styles of polygons available:
  - **Solid polygon** – the polygon is constructed from multiple, multi-sided region objects. This style of polygon requires that your fabricator supports polygonal objects in Gerber or ODB++ files (most do). Using these polygons will give much smaller design files.
  - **Hatched polygon** – the polygon is constructed with track segments and arcs.
- Once the parameters are set up, click **OK** and draw the polygon in the workspace. The corner styles for the polygon are the same as those available during routing, press **Shift+Space** to cycle through the corner modes.

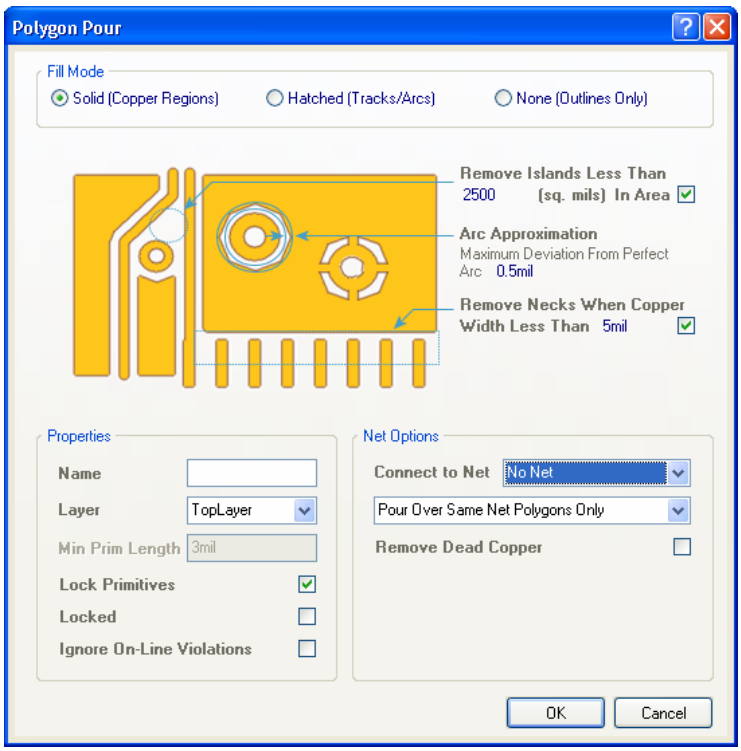


Figure 22. Polygon Pour dialog

The parameters for Polygons include:

Net Options

- **Connect to Net –** selects the net to be connected to the polygon.
- **Pour Over options –** existing polygons, or existing polygons and existing tracks within the polygon which are part of the net being connected to can be covered by the new polygon.
- **Remove Dead Copper –** removes any part of the polygon that cannot connect to the plane net.

Properties

- **Name –** The Name property identifies this polygon. Edit this field to define the name of this polygon. The Name property can be used in the **InNamedPolygon** query to highlight or scope rules, as a member of a polygon class and so on.
- **Layer –** select the signal layer that the polygon is to be placed on.
- **Min Primitive Length** – Tracks or arcs below this setting are not placed when pouring a polygon.
- **Lock Primitives –** if unchecked, individual objects (i.e. tracks or arcs) that make up the plane can be deleted.
- **Locked -** If this option is checked, the polygon is fixed in the workspace and can not be moved by the auto-placer or directly manipulated graphically. If you attempt to manually move the polygon, the warning message "Object is locked, continue?" will pop up, allowing you to move the polygon without unlocking it. The locked attribute remains set after this move. If this option is unchecked, the polygon can be moved directly without confirmation.
- **Ignore On-Line Violations** - Enable this option if you want your PCB document that has polygons, to be scanned for online violations by the Design Rule Checker. This is computationally intensive. Turn this option off to speed up the operations by ignoring polygons especially complicated polygons during the automated design rule checking.

Plane Settings (Hatched and Outlines Only)

- **Track Width –** width of tracks that make up the polygon. If Track Width is equal to the Grid Size, the polygon ends up as solid copper. If Grid Size is greater than Track Width, the polygon ends up as hatched.
- **Grid Size –** spacing between tracks that make up the polygon.
- **Surround Pads With**
  - *Octagons* **–** Places a track to form an octagon around pads.
  - *Arc* **–** Places an arc around pads.
- **Hatch Mode**
  - *90-Degree Hatch* **–** Polygon is hatched with horizontal and vertical tracks.
  - *45-Degree Hatch* **–** Polygon is hatched with tracks at 45 degrees and 135 degrees.
  - *Vertical Hatch* **–** Polygon consists of only vertical tracks.
  - *Horizontal Hatch* — Polygon consists of only horizontal tracks.

Plane Settings (Solid)

- **Remove Islands** – remove any region that has an area less than specified.
- **Arc Approximation** – solid polygons use short straight edges to surround existing curved shapes (such as pads). This setting defines the maximum allowable amount of deviation.
- **Remove Necks** – narrow necks that have a width less than this amount are removed.

18.5.2 Editing a polygon

Note: To edit a polygon, first make the layer that the polygon is on the active or current layer.

- To change any of the parameters once a polygon has been placed, double-click on the polygon, or select **Edit » Change** and click on the polygon. When the *Polygon Pour* dialog opens change the settings, click **OK**, and you are will be prompted to re-pour the polygon.

Moving a polygon

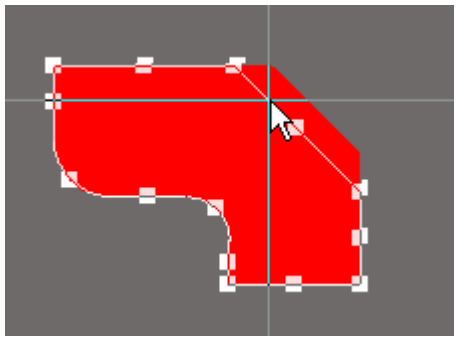
- Move a polygon as you would any other object. Click, hold and move it to the new location. When you release the mouse button, you will be prompted to re-pour the polygon.

Deleting a polygon

- To delete a polygon, select it, then press Delete on the keyboard.

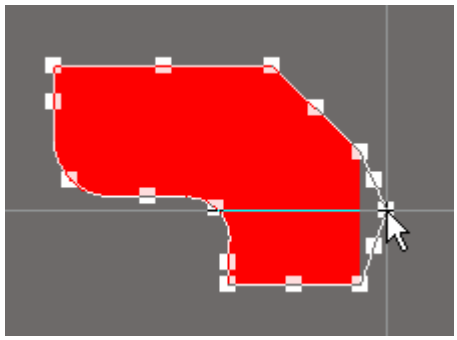
Pouring a polygon with a larger clearance

- Often you will want the polygons to have a larger clearance than the standard track to track clearances. This can be achieved by adding a new, higher priority clearance design rule, with one of the object Queries set to **InPolygon**, and the rule clearance set to the required higher value. The **Polygon Manager** can be used to easily create a targeted clearance rule for you.



Click on the edge away from a vertex to slide that entire edge.

Click on an arc to resize it.



Click on a midpoint vertex to 'break' the edge.

Figure 23. Reshaping a polygon

18.5.2.1 Reshaping a polygon

A polygon can be reshaped at any time. This is done by entering **Move Vertices** mode.

- To do this, right-click on the polygon and select the **Move Vertices** command from the **Polygon Actions** submenu.
- Click on a corner or midpoint vertex and drag it.
- Click on an edge away from the vertex to slide the entire edge.
- To add vertices, click and drag on a midpoint vertex.
- To convert a vertex into an arc, hold down **Shift+A** as you click and drag a vertex. Note that this only works when nearby vertices have not been moved from their original state.
- To delete a vertex, click on the corner vertex beyond the one you want to delete, and press the Delete key on the keyboard. Note that the order of the vertices is determined by the order they were originally placed.
- After dropping out of Move Vertex mode you will be prompted to repour the polygon.

18.5.2.2 Polygon cutouts

A polygon cutout, or hole inside a polygon, is actually an object in its own right – a **Region** object with the **Polygon Cutout** property enabled.

- Place a cutout in a polygon using the **Place » Polygon Pour Cutout** command. The standard corner styles are available, use **Shift+Space** to cycle through them.

18.5.2.3 Slicing polygons

Often it is easier to cut off part of a polygon, rather than resize it to a new shape.

- Select the **Place » Slice Polygon Pour** command to slice a polygon into two or more separate polygons.
- After launching the command, filtering will be applied to the document, temporarily dimming all objects except polygons. Place line objects through the polygon to define the slice path, using the standard cornering modes. Ensure that the last slice segment is placed beyond the polygon edge when you exit, then right click to drop out of slice mode. The 2 polygons will be re-poured, delete either if necessary.

18.5.2.4 Shelving a polygon

If you are modifying a design, perhaps changing components and modifying routing, existing polygons can be shelved, to temporarily remove them from the workspace. Shelved polygons are not deleted from the design, and can be restored at any time.

- To shelve an individual polygon, right-click on it and select **Polygon Actions » Shelve Polygon** from the context menu.
- To shelve specific polygons, select them first and use the **Shelve Selected** command instead.
- To restore shelved polygons, use the **Restore** command in the **Tools » Polygons Pours** submenu.
- Alternatively, use the **Polygon Manager** to selectively Shelve and Restore polygons.

18.5.2.5 Converting hatched polygons to solid polygons

If you are updating an existing design, you may wish to convert hatched polygons to solid polygons. This can be done using the **Tools » Polygon Pours » Convert Polygons to Solid** command. Note that older hatched polygons used an edge with a defined width, so during the conversion process you will have the opportunity for the software to expand the polygon by half the original polygon boundary width. Note that this will not affect the polygon clearance, the new polygon will still meet your clearance design rules. This process is done to ensure that the new polygon completely fills the area covered by the old hatched polygon.

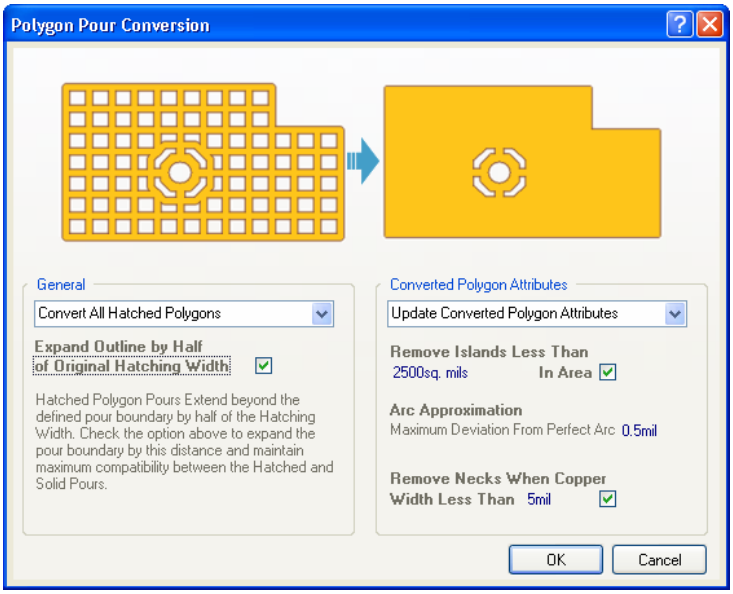


Figure 24. Polygon hatched to solid conversion dialog.

18.5.3 Managing polygons – the Polygon Manager

Even a small design can include a large number of polygons, to help manage them Altium Designer includes a Polygon Manager.

- Select **Tools » Polygon Pours » Polygon Manager** to open the *Polygon Pour Manager* dialog.
- All polygons are listed in the upper **View/Edit** region of the dialog, click to display a specific polygon in the viewer down the bottom.
- Polygons can be named, use this if you want to target a specific polygon with a design rule.
- The action buttons (**Repour**, **Shelving**, etc) can be used on polygons selected in the **View/Edit** list.
- Use the pour order when there are small polygons completely enclosed within larger polygons, in this situation the smaller polygons must be poured first. The **Auto Generate** button will order the polygons from smallest area to largest area, on a layer-by-layer basis.
- The rule creation buttons build a design rule that targets the polygon(s) currently selected in the **View/Edit** list, select them before clicking the rule creation button.

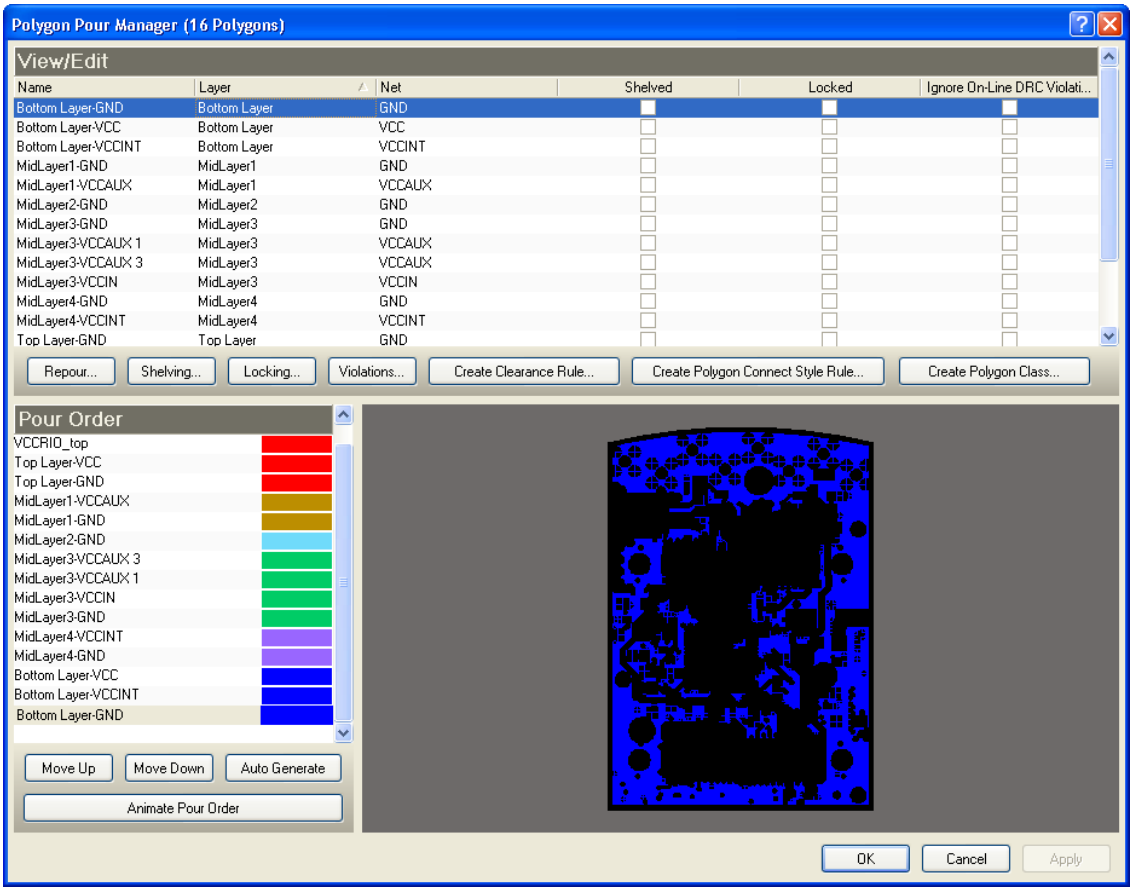


Figure 25. Use the Polygon Pour Manager to examine and manage all polygons on the board.

18.5.4 Exercise – Working with polygons

In this exercise, you will place a polygon plane on the top layer of the Temperature Sensor PCB.

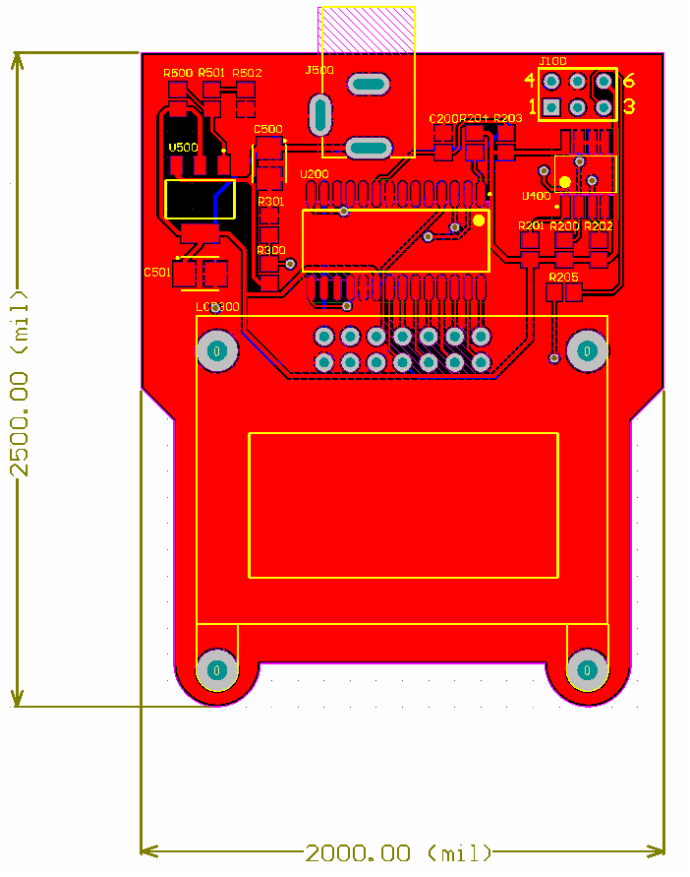


Figure 26. the Temperature Sensor PCB with a solid polygon.

1. Place a solid polygon on the top layer covering the entire PCB,
   - connected to net GND,
   - named Top Layer-GND,
   - enable the **Pour Over All Same Net Objects** option,
   - enable the **Remove Dead Copper** option.
   - Don't worry about exactly following the board shape, since copper outside the keepout boundary will not be connected to GND, it will be removed.
2. Select **Design » Rules** from menus, and display the **Electrical Clearance** section.
3. Right-click to create a new *Clearance* rule and call it *Polygon to keepout clearance*
4. Set the top query to **InPolygon**
5. Set the bottom query to `OnLayer('Keep-Out Layer')`
6. Set the clearance to **20mil**.
7. Click the **Priorities** button and make sure this new rule has the highest priority.
8. When the Rules dialog is closed the online DRC will run and flag the polygon as a violation, since it does not comply with this new design rule.
9. Repour the polygon so that obeys the new polygon clearance rule.
10. Perform a final design rule check (DRC) to ensure there are no problems with your board. Refer to Module 12 - Design Rules to refresh your memory on checking the design rules.
11. Save the board.