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Layout Considerations for Switchers

Layout Considerations for Switchers

- Noise-coupling mechanisms
- Locating the high-di/dt loops
- "Ground rules"
- Copper requirements for high-current paths
- Component placement strategy
- Gate-drive layout requirements
- Power FETs and decoupling
- Switch-node design
- Output capacitors
- Control-circuit considerations
- Noise considerations
- Thermal considerations

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How Does Noise Couple in a System?

There are four and ONLY four mechanisms for noise to propagate through a system

1) Conductive

2) Near-field magnetic (transformer)

3) Electric field (capacitor)

4) Far-field electromagnetic (radio)

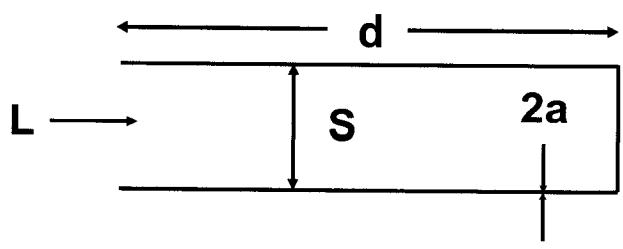
Before we discuss Printed Circuit Board (PCB) design techniques to minimize noise issues, let us briefly review the sources of noise. Much of what tends to plague power design is conducted noise. It generally is produced when high-di/dt currents encounter stray inductance in the power path, producing large voltage spikes and high-frequency ringing. Any time two circuits share a common conductor (such as a ground plane), the potential for interaction between the circuits exists.

Near-field magnetic effects are caused by direct flux linkages between magnetic fields and conductors. Any conductor with a high-di/dt current will have an associated magnetic field and therefore has potential to couple the information it is carrying to an adjacent conductor.

Electric fields couple through capacitive effects. The coupling is proportional to the area of the source and victim circuits that are in close proximity. The higher the dv/dt of the signals being carried by the source of the noise, the better the coupling efficiency.

The thing that is probably blamed the most but is in fact responsible the least for circuit operation problems is radiated fields. The higher the di/dt in a conductor and the larger its loop area, the better transmitter it becomes. Due to the extremely long wavelengths (relative to the size of most circuits) of low-frequency signals, radiated interference is only likely for very-fast-moving signals. Minimize loop areas to minimize the quality of the unintended antennas you are creating.

Self-Inductance



$$L = \frac{\text{Magnetic Flux}}{\text{Current}}$$

$$L = \frac{\mu d}{\pi}\left[\ln \frac{S}{a}\right]$$

Assumes d >> S >> a

L gets BIGGER as loop area increases

L gets SMALLER as wire diameter increases

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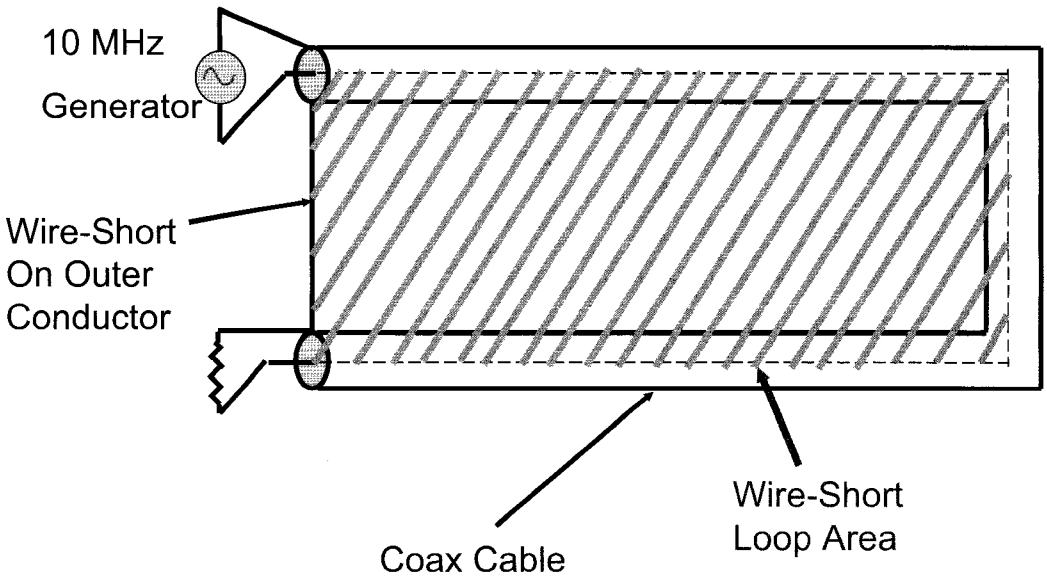
PCB traces have inductance. Thicker traces (effectively bigger wire diameter) will reduce the inductance, but only slightly. The area enclosed by the current loop (and there is ALWAYS a loop) has the greatest effect on stray inductance. Keep current paths directly adjacent to their return paths, parallel on the same layer, or directly above/below on adjacent layers.

Wire-Short Loop Area



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Signals in a system are NOT VOLTAGES going from one pin to the next over wires.

Signals are CURRENTS that must go from a source of energy and they must RETURN to that same source of energy.

Current takes the path of least IMPEDANCE, NOT of least RESISTANCE!

Impedance is the vector sum of the circuit resistance plus the circuit reactance: $Z = R + jX$

For frequencies of a few kHz or greater. e.g. > 3 kHz:

The path of least impedance will be the path of least reactance.

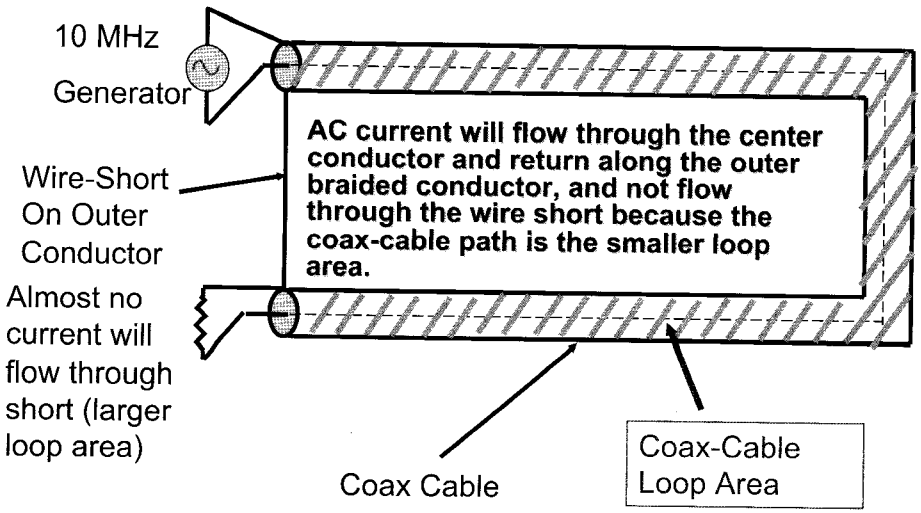
The path of least reactance will be the path with least self-inductance.

The path with least self-inductance will be the path with the smallest loop area.

At DC most of the current would go through the wire-short because it has the least resistance.

At AC above a few kHz, current will not go through the wire-short because of the large loop area having more inductance. Compare the area made by the wire-short and the center conductor (above) with the area of the coax outer conductor and the same center conductor, shown on the next slide.

Current Takes the Path of Least Impedance (Coax-Loop Area)



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The loop area of the coax is much smaller then the loop area with the wire-short.

At frequencies above a few KHz, the return-current path will be through the coax outer conductor because it is the path of least loop area/least inductance/least impedance.

Conductive Coupling

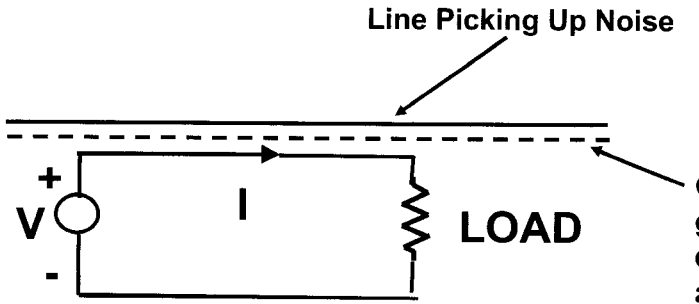
- **Common impedance**
- **Requires two or more conductive contacts**
- **This mode is responsible for over 90% of noise problems!**

Examples:

- **AC- or DC-power leads**
- **Grounding connections**
- **A shared signal path**

PCB traces, like wires, have resistance, self-inductance, mutual-inductance, and capacitance to adjacent traces. A common problem with ground noise is having a noisy node directly connected to a ground plane. Your ground plane is useful as a reference only if there is precisely zero current flowing in the ground plane. If there is any current at all flowing through the ground plane, there will be a voltage gradient across the plane. Two circuits now connected at different points along the plane will see a different reference potential and the potential for cross talk exists. Keep noisy current signals out of the system ground plane!

Near-Field Coupling – Electric (E) or Magnetic (H) ?



Disconnect the LOAD!
If no current is flowing and the noise problem is still present, then the coupling mode is Electric Field (E)

To reduce electric-field coupling:

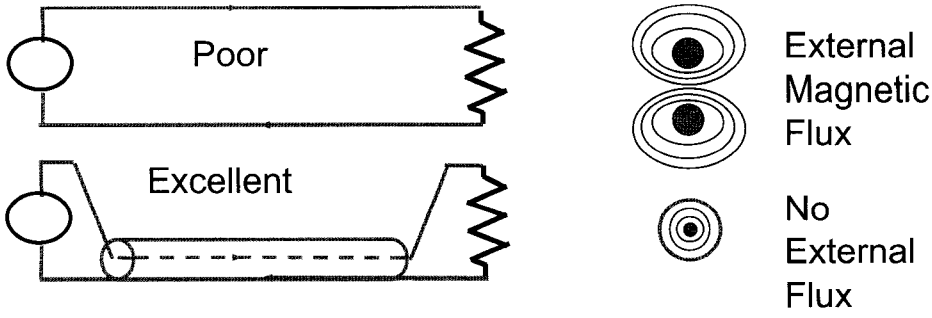
Place a guard trace between the radiating trace and the trace picking up noise. Tie the guard trace to a low impedance with the same voltage potential as the circuit picking up the noise.

To reduce or eliminate magnetic-field coupling:

Reduce or eliminate loop area, separate the distance between circuits, use self-shielding techniques to allow the return-current conductor to surround the signal conductor. Use toroidal or Pot Core inductors.

Magnetic-field coupling is very difficult, if not impossible, to shield at the receiver. It is best to stop the SOURCE of the problem.

Magnetic Self-Shielding



If the return current can completely enclose the signal current, excellent magnetic field containment will result.
Any techniques that will reduce self-inductance will also reduce or eliminate magnetic fields.

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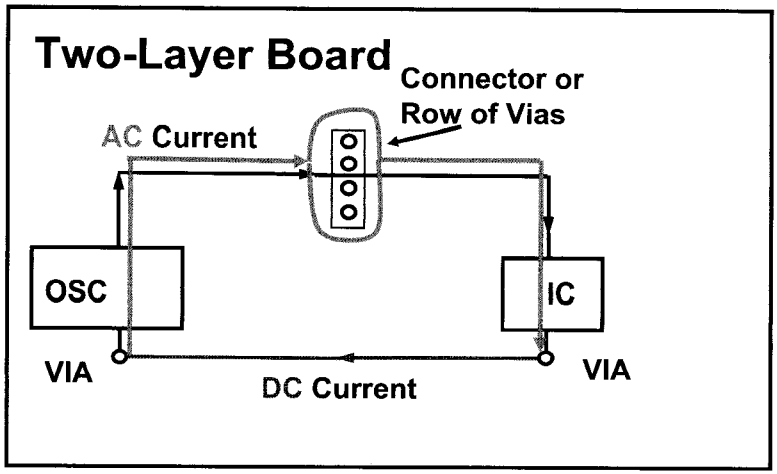
Magnetic flux is inversely proportional to the square of the distance from the conductor-carrying current. Conductors carrying equal and opposing currents will create flux that cancels each other. By enclosing a signal by a ground shield (like in a coax cable), the flux is practically enclosed in the wire itself and will not disturb neighboring circuits. Note that each of the conductors produces precisely the same magnetic flux that it would if it were separated from its return conductor. The secret to success is the fact that the fields in the source and return conductors are equal and opposite. When placed in close proximity, they tend to cancel. Always try to optimize field cancellation in your circuit layouts.

How Hidden Antennas are Made on a PCB



Row of vias opens up ground plane between pins and causes AC-return current to flow around gap in plane. The gap will radiate at whatever frequency is ¼ λ = gap length!

Far-field (electromagnetic) coupling:

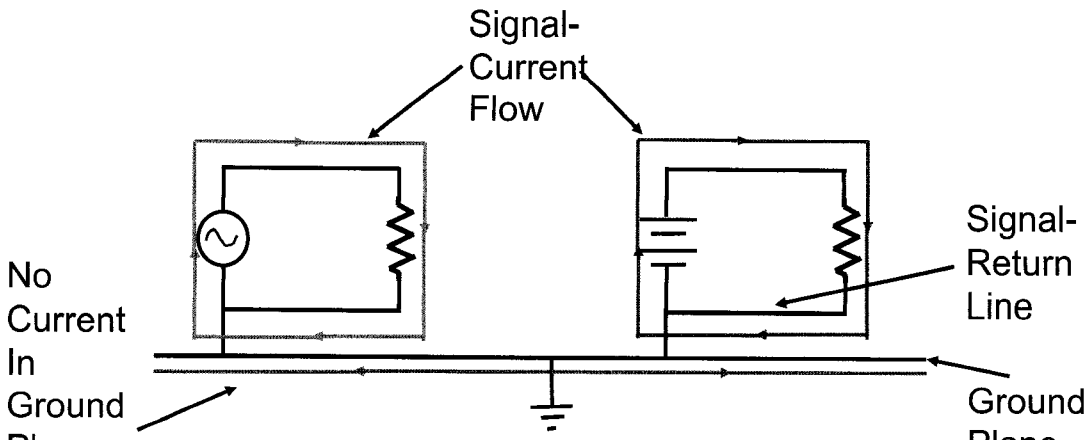
To minimize electromagnetic radiation or pick-up:

1.Keep antenna surfaces free of common-mode current

2. Minimize antenna area

3. Keep antenna length $< \lambda / 20$

Signal Return vs Ground



Signal currents return to the source via their own signal-return paths. Signal current does NOT flow through ground!

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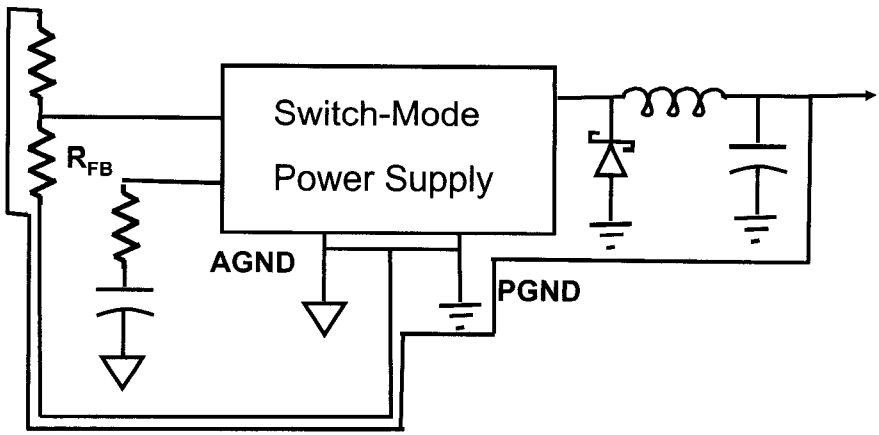
The basic rule of thumb to employ if you have currents flowing in your ground plane is:

Ground isn't!

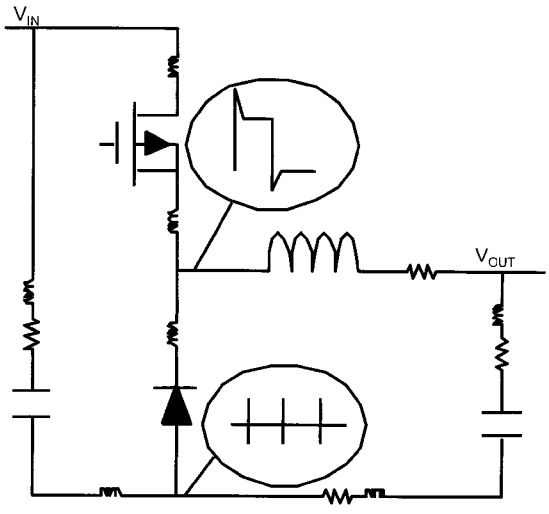
Remember, all conductors have resistance, even planes! Signal currents flowing through a ground plane will cause a voltage gradient across the ground. To ensure the ground reference is the same across the board, it is better to have signal-return paths kept locally, as shown. Imagine what the ground currents would look like if the two resistors depicted above were simply connected to the ground plane with a simple via dropped through a pad.

Signal Grounding Example



Connect AGND and PGND together at the chip RFB. You must have a signal-return path to the AGND/PGND-junction point. Minimize the loop area for AGND and PGND circuits. Feedback resistors should be physically close to the feedback pin. Power and signal-return (ground) connections should be run close together to minimize loop area.

Impact of High di/dt



- All elements, including PCB traces, have parasitic L, R, C
- High di/dt through parasitic L produces voltage spikes
- Must avoid injecting these currents into the ground plane

First, identify high-di/dt paths

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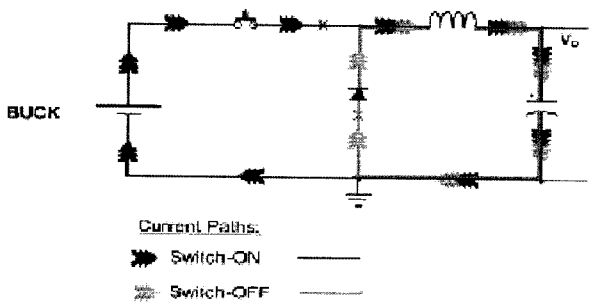
If you think about the buck topology, you have to ask the question: Why should there be spikes on the output and where do they come from? There is an inductor, generally operating in continuous- conduction mode, in series with the output. So, by definition, there are no high-di/dt currents allowed to flow through the output capacitor. There should be no spikes on the output. But in reality, the observed spikes are frequently very large. How can this be and how do we control the problem? The source of the problem is usually high-di/dt currents being injected into the ground plane and polluting the entire circuit board; EMI wise, that is.

High-di/dt currents will cause disturbances on our boards that show up as spikes all over the circuit. They tend to have very fast edges and therefore very-high-frequency components associated with them (remember Fourier analysis?). High frequencies tend to radiate better than low frequencies and will seem to be present wherever we try to make a measurement, especially if they get injected into the ground plane. So the goal is to keep the ground plane quiet!

Okay, we've managed to determine that we believe the solution is to control our high-di/dt currents. But before we can decide how to control these troublemakers, we had better have a methodology for determining where they are in the first place.

Locating the High-di/dt Loops

- Draw the switch-ON current path in one color
- Then draw the switch-OFF path in another
- Any part of the circuit that has only a single color is a high-di/dt path
- Works for all topologies
- Here's a buck example:



Okay, so now what's the fix?

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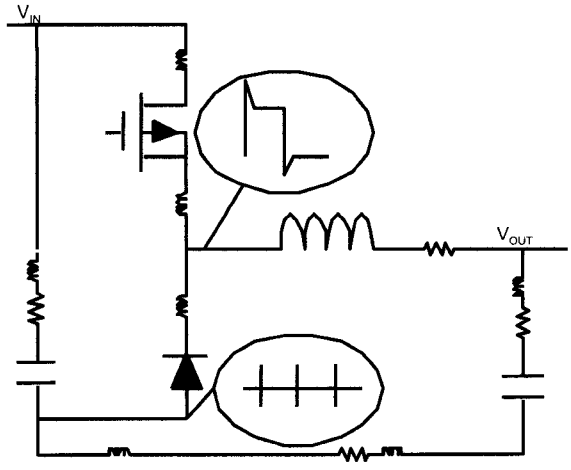
The diagram above shows a neat trick to help find the offenders. Simply look at the current paths in the various switch states and draw the loops in a different color for each switch state. For instance, in the buck example above, with the switch on, current flows from the input capacitor, through the switch, the inductor, and then the output capacitor and back through the ground plane to the input- cap return. On the second half of the cycle, the inductor is forcing current to flow through the output cap, ground, the catch diode, then back to the inductor. Draw the first loop in red, for example, and the second in blue. Now look to see where only one color exists on a path. The single-color paths are the high-di/dt paths, and as such will need your undivided attention during the layout phase!

How to Deal with the Noise Generators



- Note the re-route of the diode-return path
  - Forces pulse currents directly back to input cap
  - Keeps high-di/dt currents out of ground
  - Diode anode may actually be a bit noisier, but who cares?
- Can apply the same rationale to all topologies

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The fix in the buck example is to route the diode anode directly back to the input-cap ground terminal. This forces the ground current to flow in a continuous manner that is in fact equal to the inductor current. If done properly, the path length of the anode connection is not significantly longer than if it were simply connected to the ground plane. Of course in a synchronous regulator all the above reasoning applies to the low-side-FET source connection.

For a boost topology, simply imagine swapping the FET and the diode in the circuit above and also swapping the input and output labels. The buck has been turned into a boost and the current paths look essentially the same as they did before. So the proper place to return the switch ground is the bottom of the output cap as opposed to the input cap for the buck.

Low-Side-FET Grounding

- **Do not connect low-side-FET source directly to ground plane. Spike generator!**
- **Instead, run separate ground "shape" from FET source to input-cap ground and via the *capacitor pad* to ground plane**

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A word of caution to emphasize the point about the low-side FET or the anode of the diode. It is a noisy node and should not be directly connected to the ground plane. Doing so will inject noise into the ground plane and corrupt it for the rest of the nodes depending on it. If you see spikes on the output of a buck regulator, this connection was probably made incorrectly. In an ideal design there would be no spikes on the output of a buck regulator. In general, any spikes that do appear on the output are conducted in through the ground rail. With careful attention to the low-side-switch grounding to the input capacitor, output spikes can be nearly eliminated or at least greatly reduced from what is commonly accepted as inevitable for a switching regulator.

Ground Rules 1

- **Ground plane can only be a true reference if NO current is allowed to flow in the plane**
- **Avoid letting very noisy currents flow in the main ground plane. Run separate shapes on top layer**
- **Use single-point ground for all sensitive circuitry**
- **Segregate analog (small-signal) and power grounds**

Since we've already decided that ground is a conductor with parasitics the same as any other conductor, then it follows that if any current flows through this ground conductor, there will be an associated voltage drop. As such, there's no place that you can point to and say this represents the common reference point for all circuitry. That statement is true only for that one fixed location and, unless all ground connections return through zero-current traces to this one point, there is no other location on your PCB that can be assured of being at the same potential. This will cause all kinds of headaches if ignored. Assume you have a stable ground at your peril.

The solution is to carefully partition grounds so as to know precisely where control signals get referenced relative to high-current ground paths. For control circuits like feedback dividers and soft-start capacitors, connect the ground referenced end of the part directly to the SGND pin of the control IC (if available). There may be large currents flowing through the main plane beneath and a significant associated-voltage gradient. If you drop the bottom end of a feedback divider into a convenient point on the plane you may well introduce an error of many millivolts into your output voltage. It's more difficult to route a separate trace from the divider to the SGND pin, but there's almost no reasonable way to estimate the current paths through your ground planes, so assume they are a problem and design accordingly.

Ground Rules 2

- **Don't cut the layer-2 ground plane**
- **Solid ground plane acts as a "shorted turn" to EMI**
- **Bypass to the ground PINs, not the plane**
- **Can help to make a ground shape on layer 1**
- **Keep high-di/dt loops on layer 1**
- **Ground plane is for DC distribution and signal reference only**

Keep the layer-2 ground plane contiguous so it can act as the high-DC current path and also as the RF-return path for very high-frequency signals. But avoid using this as an analog ground return for your control circuitry (or sensitive analog front-end stuff as well). Also, be careful of the high-di/dt currents and keep them out of this plane to the maximum degree possible. You don't want to corrupt this return path anymore than is strictly necessary.

One successfully-used technique is to daisy-chain a small ground trace from the SGND pin of a controller IC to all the small-signal component grounds. A large top-level plane is a viable approach as long as it only connects to the main plane at one point and also carries no high-di/dt power returns. In many cases, there simply is not enough room for this scheme to work and the daisy-chain design works just fine.

Something to be careful of is that many CAD programs will not readily allow you to segregate the two grounds and make a single-point connection between them. You have to find a way to lie to the software and tell it what it wants to hear. Don't even think of compromising your ground scheme because your CAD package makes it hard to do the grounding correctly.

Ground Rules 3

- **Consider grounds as you would any power-path conductor. Make sure there's enough metal!**
- **Be sure to look at the integrity of the ground plane after all vias are added between layers**
- **Use 2 oz copper plane in applications over 5 amps if at all possible**
- **Use multiple ground layers if possible**

It's common to assume that ground is a solid, magical reference plane. But in many cases this tendency to ignore the realities of the ground scheme has led to tiny little connections left in the ground plane to carry very high currents or supposedly short return paths having to meander half way across a PCB to get to a real "ground". When there are lots of vias or traces laid in through the ground plane you need to make sure you look at the ground plane and verify that it hasn't been nearly cut into pieces. Instead of a 2"-wide plane you may see a 20-mil-wide remnant after the plane gets cleared from around all the vias. This is not quite what was intended. It's a very good idea to turn off all layers except ground at the end of a design and make sure you still have good plane integrity when you're done laying in all the signal and power traces and dropped a collection of vias through the board.

High-Current Copper Requirements 1

- **Do not use minimum width traces**
- **Approximate trace width as follows:**
  Where T = trace width in mils, A is current in amps, and CuWt is copper weight in oz

$$T = \left(-1.31 + 5.813 \times A + 1.548 \times A^2 - .052 \times A^3\right) \times \frac{2}{CuWt}$$

- **Formula works over a range of 1A to 20A**

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Most designers tend to ignore the trace width since it's generally not a concern for digital applications. The usual approach is to try and design for minimum trace width. This will get you in lots of trouble with high-current designs. The formula above is derived by curve-fitting the standard mil-spec curve that's been published for decades now. It's a reasonable estimate over a fairly wide range of currents. In general, where you're looking at high-current paths, more copper is better.

There's a tendency to use ½ oz copper on top-side high-speed layers since you can etch to finer pitch with the thinner material. But that's not a good power strategy. Where possible, at least try to get 2 oz for inner plane layers where fine pitch is not an issue. Most PCB fab houses are able to do selective plating on outer layers. This can be done to thicken up the copper in the high-current paths but adds cost and therefore is infrequently done. If you can use multiple layers for high-current connections, use large numbers of vias to interconnect them.

High-Current Copper Requirements 2

- **Some examples:**
  - **1A, 1 oz Cu, trace width = 12 mils min**
  - **5A, ½ oz Cu, trace width = 240 mils min**
  - **20A, ½ oz Cu, trace width = 1275 mils min**
- **Clearly lots of width required for high currents with lightweight copper planes**
- **These widths are designed for an approximate 10°C temp rise. Wider is better!**
- **Try to design for 30 mils per amp for 1 oz Cu and 60 mils per amp for ½ oz Cu**
- **Shapes with switching currents should be wider**

A 50 mil, ½ oz trace may fuse open when used at more than 10A. Keep in mind too, that the top- side copper in particular is the primary thermal path to the cooling air flowing over the PCB. Since the thermal resistance of copper is much lower than the fiberglass board material, the more copper that's left in place, the lower the overall thermal resistance of the assembled board.

High-Current Copper Requirements 3

- **Via considerations:**
  - **For microvias, design for 1A/via max**
  - **For 14 mil diameter or larger, 2A/via max**
  - **For 40 mil diameter or larger, 5A/via max**
- **For better heat spreading, allow vias to fill with solder**
- **Leave copper alleyways between clusters of vias. Avoid "swiss cheese"**

Vias are a necessary evil in many cases and should be avoided as current-carrying elements in the power path, if at all possible. The only time they become desirable is if they can be used to introduce redundant copper areas to a design, such as an inner layer being hooked in parallel to an outside trace area.

Vias do have potential use as heat pipes, in effect, that have the ability to help conduct top-side- generated heat to the back side of a PCB. The more vias that can be connected to a hot plane area, the more heat spreading can be achieved.

Something to watch for when using lots of thermal vias is that the internal ground planes can get badly cut up and end up with nearly no useful current path. This is particularly likely to occur on very small boards like voltage-regulator modules.

Component Placement Strategy 1

- **Design power-path layout first. Plan a clean power flow for high-current path. Keep multi-phase layouts symmetrical**
- **May help to work from the output back towards the input source**
- **Locate sense resistors and inductors, then FETs and input caps**
- **Keep copper width requirements in mind!**
- **Take inputs and outputs ACROSS THE CAPACITORS**

There's a tendency to think that the controller is the most important part of the design and so that's the place to start. Nothing could be further from the truth. You want to start with the power-path components since they are large and require fat interconnects. It's a lot easier to find ways to sneak in little signal traces than the large plane areas associated with the power path.

Lay out the power parts in such a way that the power flow makes logical sense and the enclosed loops are as small as possible. Try and force return currents to flow either next to or under their respective source current. This minimizes the loop area and reduces the magnetic fields that will radiate from the board's surface. The equal and opposite fields produced tend to cancel one another. The closer the conductors, the more effective the cancellation.

Once all the power components have been placed, look for quiet areas to locate the control circuits.

Component Placement Strategy 2

- **Control circuits go in last. Small traces, easy to route**
- **The higher the impedance and/or gain, the smaller the node should be, especially FB pins, input to op amps, comp pin, etc.**
- **Low Z nodes can be big, including outputs, so put FB components near the inputs**
- **Play with some "Paper Dolls" to see the power flow**

Follow the grounding suggestions discussed earlier. Keep the highest impedance traces short since they will have the greatest tendency to pick up stray fields. So as an example, the two resistors in a feedback divider should be located very close to the FB pin of the regulator, not near the power supply's output. The connection from the top of the divider to the supply output is a very low impedance connection, and as such will be quite immune to noise pickup. The error amplifier input, in contrast, is a very high Z input and will be very susceptible to stray field induced noise. There's a tendency to want to make sensitive nodes large in the mistaken belief that this will offer some shielding effects. In fact this increases the capacitance to space and increases the likelihood of noise pickup. Make sensitive traces narrow and as short as possible. You may have seen small RC filters at the input to the V_{CC} pins of some switching regulator controllers and thought that the idea was to prevent the controller from creating noise on the V_{CC} supply. In fact for a 5V V_{CC}, the supply will often be used for gate-drive power as well as possibly logic in the main system. This tends to be a very noisy rail and so the RC filter is used to filter the supply voltage to the controller! Therefore, keep the V_{CC} bypass caps as close as possible to the controller's V_{CC} pin and connect the other end directly to ground, preferably at the controller's ground pin. If the V_{CC} rail supplies only control circuits in the IC, connect the bypass to AGND. If the rail supplies gate drives, bypass to PGND. Probably the single biggest cause of radiated emission problems from switching power supplies is conducted emissions on long input power lines. Shielding can help, but the ultimate fix is to reduce the AC currents in the input lines. This implies good decoupling and filtering of the input currents to the regulator. Keeping the loop between input caps and FETs as small as possible is another key way to keep this under control. Use the capacitor connection techniques discussed above for both input and output caps. It's worth creating a set of "Paper Dolls" for your main power components and lay them out to see how the main power path interconnects will flow.

Component Placement Strategy – Rules of Thumb

- **You can put inductance in series with an inductor, but do it on the quiet side, NOT the switch-node side**
- **30 mils per amp for 1 oz Cu and 60 mils per amp for ½ oz Cu**
- **1A of DC MAX per via is a good design goal**
- **Vias to bypass caps should be placed tangent to the pad, two per pad is preferred**
- **Minimize stray inductance in the power path!!!**

Trace inductance in series with an inductor is not generally much of a concern. It will simply have the effect of increasing the total inductance in the path. In contrast, you don't want to add a significant amount of capacitance in parallel with an inductor. That's the analog of adding inductance in series with a capacitor and will cause problems. If you must add some inductance in series with an existing inductor, it's usually better to make the output path the longer one so you minimize the size of the noisy switch node.

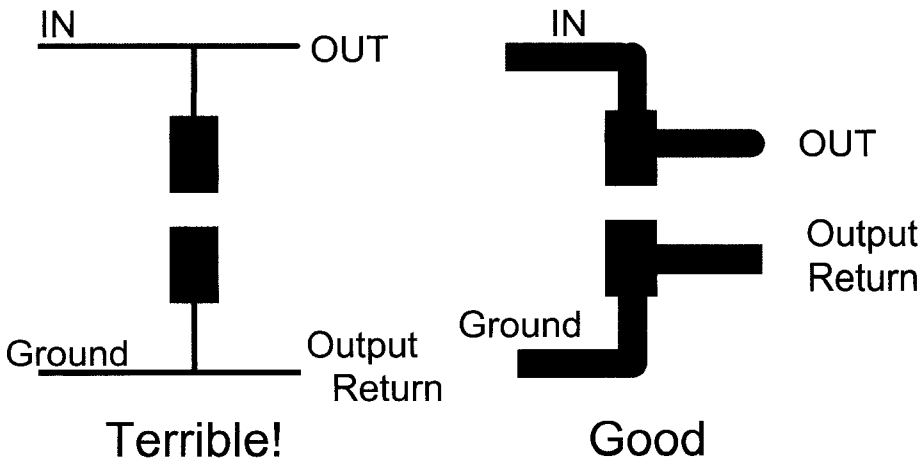
At the risk of being redundant, pay close attention to the size of current-carrying paths. More copper is almost always better in high-current paths.

We've already discussed the use of vias to connect bypass caps to planes. A minimum of one via connected tangent to each pad of the capacitor is required. Two per pad is better, and three is slightly better, but way down the diminishing-returns curve. You can't have too many, but beyond two, they will do you very little added good.

The mantra through board layout needs to be "minimize stray inductance". Treat every high-di/dt path as a high-frequency RF connection (because it is!). You may be inclined to say "But I'm only running at 100 kHz", but the fast edges will have frequency components out to the tens of MHz to possibly hundreds of MHz. Don't ever forget that when doing a layout.

Connecting Bypass Capacitors 1

- ***Connecting to output bypass caps***



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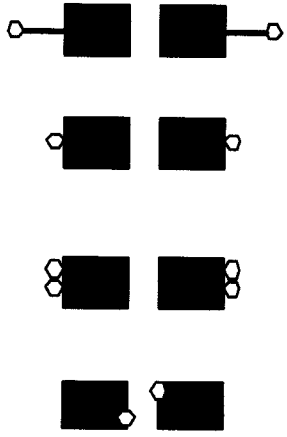
Take a look at the two layouts above. An output capacitor is intended to be connected to the surface-mount pads in each case. The design on the left will not do a very good job of reducing ripple and spikes due to the high inductance connections to it. The straight-through connection paths from the input to the output is likely a lower impedance path than the path through the capacitor.

In the case on the right side, the input and output traces are much heavier so they will be lower impedance connections. But the more significant consideration is the physical orientation of the traces relative to the capacitor. Note that the current path is through the capacitor pad and the output connections come directly from the capacitor pads as well. This is the lowest impedance connection viewed from the perspective of the output looking back into the capacitor. About the only improvement that could be realized would be to make the traces wide enough that they effectively degenerate into a couple of planes. If multiple decoupling caps are used, it's best to create top-side shapes on which all the parts sit. If the capacitors need to connect to internal ground or power planes, use a large number of vias to connect these shapes to the inner layers.

Connecting Bypass Capacitors 2

Connecting to high-frequency bypass caps:
This assumes a connection into internal planes



- Long thin traces add inductance and effectively isolate the capacitor
- Keeping vias close to pads minimizes parasitic inductance
- Doubled vias further reduce inductance
- This technique further reduces inductance by reducing the high-frequency loop area

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High-frequency bypass capacitors need to be connected with minimum added inductance. Many times design rules in place tend to force solutions like the top design shown above. That capacitor will be a complete waste of money and space since the added inductance will effectively decouple it from the load. The best approach is shown on the bottom of the slide. The enclosed loop area is minimized and there's good field cancellation. This makes for a low-inductance interconnect.

The second or third approach tend to be used most commonly. The vias should be placed tangent to the pad. Going from single vias to doubled-up vias will make for a 10% to 20% reduction in parasitic inductance. Adding a third via will result in only a 1% or 2% additional improvement and is well down the diminishing-returns slope.

Gate-Drive Layout

- **Place drivers close to MOSFETs**
- **Keep C_{BOOT} and V_{DD} bypass caps very close to driver**
- **Minimize loop area between gate drive and its return path: low inductance**
- **SW-pin connection should be 0.015" wide or larger, as should the gate connections**
- **Minimize stray inductance in the power path!!!**

The gate connections to external FETs are very-high-di/dt paths and as such need careful thought. Worse yet, the connection between driver ground and FET source will act like a parasitic multiplier since the inductance will act as a gain-degeneration element for the power device. Long connections here will dramatically slow the rise/fall times of the FET switches. This is particularly important for the high-side FET in buck applications. Try and lay the gate-to-driver connection directly over the source-to-driver ground connection to minimize the area enclosed by the resulting loop and use traces around 15 mils wide (0.3mm).

And to re-emphasize, minimize stray inductance!

Power FETs and Decoupling

- **Minimize loop area enclosed by high-side FETs, low-side FETs, and input caps**
- **Connect the low-side FET's source to the input-cap ground, then to the ground plane**
- **Use copper pours for drain and source connections to power FETs**
- **Use lots of vias to tie into inner layers**
- **Minimize stray inductance in the power path!!!**

As discussed earlier, the loop between the input cap, high-side FET, and low-side FET needs to be minimized. This is probably the most critical path in buck designs.

Follow the guidance discussed about low-side-FET-source grounding at the input-cap ground to minimize output spikes and be sure to use large copper pours for the main power connections to the MOSFETs. This is helpful not only electrically, but also thermally.

The same philosophy applies to the use of vias. More is better. Just think of the inductances all connected in parallel. They also act as thermal passages to the back side and inner layers of the board. Fill with solder if possible. While not nearly as good as copper either electrically or thermally, solder is much better than air and that's what would fill the holes otherwise.

By the way, be sure to minimize stray inductance in the power path!

The Switch Node

- **Requires a contradiction:**

  As large as possible for current handling,
  yet as small as possible for electrical noise reasons

- **Swings from V_{IN} to ground at Fsw.**
  Very-high-dv/dt node! Electrostatic radiator

- **Solutions:**
  - **Keep inductor very close to FETs, Sw-node short**
    Put on multiple layers
  - **Minimize stray inductance in the power path!!!!**

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The switch node of a buck is a great electrostatic radiator as it swings between V_{IN} and ground at Fsw. Displacement currents will flow in an effort to charge and discharge the capacitance between the switch node and the ground planes and free space. In general, it is better if minimized. For other than buck regulators, take a look at any nodes that swing through high potentials and look for ways to minimize the capacitance to the rest of the world. If, for instance, the drain of a TO-220 FET is tied to a heatsink for thermal management, try and place the drain at a DC potential and allow the source to fly up and down. This prevents high-AC, common-mode currents from flowing through the capacitance to the heatsink.

Oh, and at the risk of sounding repetitive, "minimize stray inductance in the power path".

Control Circuit Layout

- **Use single-point ground for AGND-PGND connection**
- **Can use top-side "daisy-chained" ground or separate plane area for SGND connections**
- **Keep V_{CC} bypass cap close to pins**
- **Route sensitive signals away from noisy nodes, and no noisy signals near sensitive nodes**
- **Keep feedback Rs and Cs close to pins**

It's generally desirable to tie the controller IC's AGND and PGND pins together at a single point that also ties to the ground plane. If you have room for a dedicated, top-side ground shape, you can use that as the return for all ground-referenced control circuits (feedback divider, soft-start cap etc.). In most cases that will not be a viable option. Using a small trace that daisy-chains from the AGND pin to the various small signal grounds is an excellent alternative. If you need to route this trace through multiple layers there will be a problem with the layout software wanting to tie the via to an internal ground plane. That would destroy the whole point of wanting to segregate this trace. You need to find a way to fool your software into doing what you want. One approach is to come up with a separate AGND symbol. This allows you to tie all the signal-ground points together through multiple layers without connecting to the internal plane. However, you will generate a DRC error when you try and connect the AGND and PGND. In some programs you simply accept the error and ignore it knowing full well what it is. Some programs will not allow you to connect the two separate nets on the schematic. If you make a connection between the two nets with a "line" as opposed to a "wire", the program will allow the nets to coexist. The appearance of the schematic is good, but you will generate a DRC error on the PCB.

Probably the single most important area to avoid from a noise perspective is the switch node. That area and the adjacent area around the inductor have potential to cause a great deal of trouble with small signal paths. Be especially wary if using an unshielded, open-core structure inductor. The stray fields surrounding the inductor can corrupt current-sense and feedback signals very easily. You should also avoid putting a controller/regulator too close to an open-core inductor if possible. We've seen several instances of regulators getting confused by magnetic fields from an unshielded inductor. In some cases turning the inductor 180° can help.

Control Circuit Layout

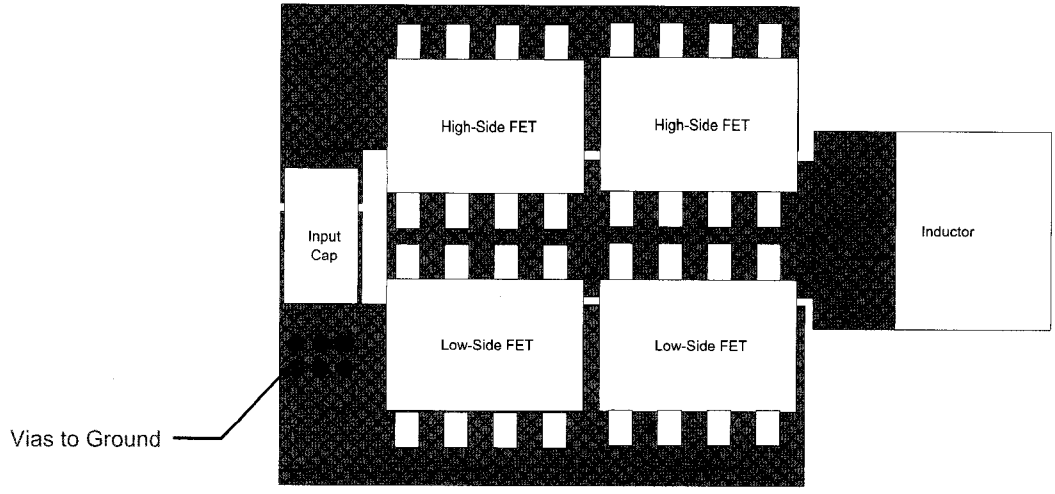
- **Make long runs to low-impedance nodes, short runs to high-impedance nodes**
- **Route current-sense traces parallel to one another – minimize differential-mode noise pickup**
- **Keep most small signal traces thin – lower capacitance to surrounding signals**
- **Route Sense+/Sense- as a parallel run**

The lower the AC impedance of a signal run, the less likely it is to be corrupted by stray fields. Therefore, if given a choice as to which end of a component to make the long run, always choose the lowest-impedance end. An example is the feedback-divider top resistor. Given a choice of locating the resistor close to the high-impedance error-amp input and the low-impedance output connection, always place it close to the error amp and make the long run to the output voltage.

When running current-sense traces, try to keep the two lines parallel to one another and as close together as possible. That way, any noise picked up will likely get picked up equally and cancel differentially. It will look like a common-mode signal and so it will be subject to the CMRR of the receiving amplifier. But at least you won't be injecting purely differential noise signals. The same rationale applies to such things as remote sense lines.

Keep the small signal traces small. They will be less susceptible to capacitively-coupled noise pickup. In cases where long runs must be made with high-Z signal paths, place the conductors parallel to one another on an inner layer and surround with grounded copper on all sides. In essence, build a PCB-coax cable.

Example of Clean Layout - Single Sided



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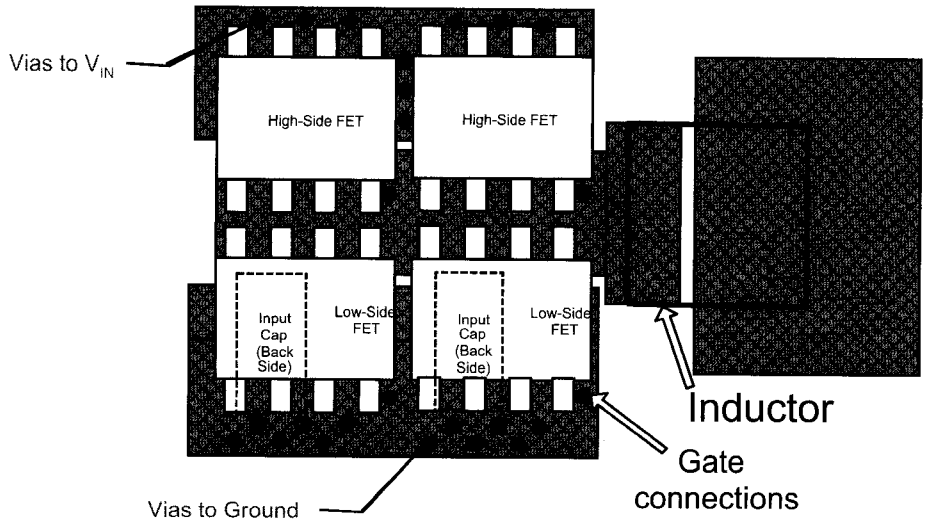
If you're forced to keep the input capacitor on the top side of the board, this approach is a decent alternative. Note that the ground vias are close to the cap ground, not at the FET-source connections. Otherwise the recommendations of the previous slide all apply here as well. Note that the input cap should be a high-frequency ceramic capacitor, but has to be large enough to handle a significant amount of energy. Something on the order of 1μF or more for currents of several amps is appropriate at this location. Use 10 μF or so for currents greater than 20A. The main-input supply-bulk capacitors can be located a short distance away. The local bypass needs only handle the very-high-speed edges of the FET currents.

Example of Clean Layout - Two Sided



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Here's an example of a reasonably clean layout for two parallel FETs, top and bottom, in a buck configuration. Note the locations of the decoupling caps on the back side. There would be a plane area between the cap V_{IN} terminals and the high-side FET-drain connections. In practice, there needs to be small cutouts around the high-side-FET gate pins. Install vias to inner-layer gate traces alongside the gate pins so as not to destroy the integrity of the switch-node power path. If you need to add more metal to the switch node, it will generally work out okay to double the number of layers dedicated to this connection and add a number of vias close to the FET pins and near the inductor pad.

Note that the pad connected to the output side of the inductor is larger than the switch-node side. It's okay to run this island under the inductor and stop just short of the switch-node side pad. It's tied to the output and is an AC ground and, as such, will not inject noise. It will act as a pretty good heatsink for the inductor however.

Thermal Equations

- Correct thermal design requires understanding of how heat is generated by power-dissipation flow
- We model the thermal equations after Ohms Law :

$$V = I * R$$

- P (Watts) = V * I or V^2/R or I^2*R
- RMS: $V_{rms} = V_{peak} / 1.414$
- Efficiency: $\eta = P_{Load} / P_{Total}$
- The Thermal Equivalent of Ohm's Law :

$$TempΔ\ (°C) = Power\ (W) * θ\ (°C/Watt)$$

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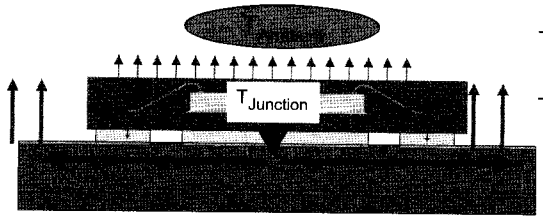
Correct thermal design requires understanding of how heat is generated by power-dissipation flows. Heat is generated within the IC and must flow to the cooler ambient air around the device. As heat flows, there is a thermal resistance which causes a temperature gradient.

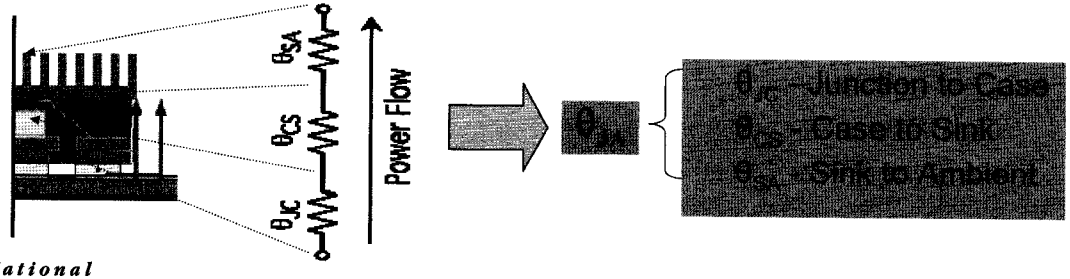
For thermal equations, Ohm's Law is used, with voltage, current, and electrical resistance being replaced with temperature, power, and thermal resistance.

Power Flow Model



θ_{JA} - Thermal resistance from the Junction to Ambient

At each interface from the junction to the ambient air there is an associated thermal resistance



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Thermal resistance is defined in degrees Celsius per watt. As power is dissipated, there is a temperature change. The higher the thermal resistance, the higher the temperature rise.

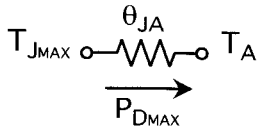
At each interface from the junction to the ambient air, there is an associated thermal resistance. The temperature rise for each interface is above the next interface in the direction of heat flow from the junction to the ambient. Heat flows from the hottest to the coolest point.

The most effective path for thermal is metal (i.e. traces, ground, leads, etc.). Plastics provide poor conduction paths.

Thermal Design Considerations

- Correct thermal design means designing so under the worst-case operating conditions the IC will not be damaged or have its protection circuits activated
- "Operating Ratings" in datasheet will specify a maximum junction temperature specified as T_{JMAX},commonly 125 °C
- Using Ohm's Law with the changes for thermals and using worst-case values, the simple equation below is derived:

$$T_{JMAX} = (P_{DMAX} * \theta_{JA}) + T_A$$



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The datasheet, under "Operating Ratings", will have a maximum junction temperature specified called T_{JMAX}.

This value is commonly 125°C.

Using Ohm's Law with the changes for thermals and using worst-case values, the simple equation below is derived:

$$T_{JMAX} = (P_{DMAX} * \theta_{JA}) + T_A$$

Note: Despite the similarity to Ohm's Law, thermal equations have nowhere near the accuracy we expect from electrical equations. Decimal place accuracy is wasted, and rounding up parameters to integer values is always justified. Even then, the mechanical factors involved can mean calculated values can be off by as much as 30%.

Example θ_{JA} by Package Type

• Micro SMD	θ_{JA} = 95 °C/W
• SC-70	θ_{JA} = 450 °C/W
• SOT-23	θ_{JA} = 180 °C/W
• LLP-6	θ_{JA} = 50 °C/W
• MSOP-8	θ_{JA} = 200 °C/W
• SO-8	θ_{JA} = 160 °C/W
• eTSSOP-20	θ_{JA} = 40 °C/W
• TSSOP-16	θ_{JA} = 85 °C/W

* These are examples only. For actual value, refer to individual product datasheet.

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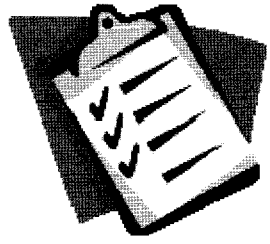
θ_{JA} is a function not only of the package but also of the heat flow in the system including the PCB layout including copper thickness, width, ground plane heat dissipation, heat sink, airflow, etc.

Things to Review for Thermal Considerations

- Loss elements are sources of heat
  - LDO, buck, boost have different highest-loss elements
  - Differences in duty cycle, V_{IN} lead to different elements also
- Oz of copper (Cu)
  - 0.5 oz to 2.0 oz – keep traces wide and thick!
- Amount of copper in mm^2
  - 645 mm2 and up – flood the board with copper
- Thermal vias
  - How many and in what pattern
  - Solder-fill vias – spreads heat better
- Air flow
  - ~70% reduction w/ 2.5m/s airflow
  - Avoid placing power parts in airflow shadows



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Here is a checklist of the thermal considerations we discussed and a summary of the recommendations for better thermal design. Understand the sources of heat and how to spread it away from components that need to stay cooler.

Layout Considerations Summary

- **Know where the high-di/dt paths are in your design and minimize their loop area**
- **Use good grounding strategies**
- **Minimize parasitic inductance!**
- **Segregate signals and power**
- **Leave plenty of copper**
- **Add thermal vias where possible**
- **National Semiconductor application notes:**
  - **Layout Guidelines for Switching Power Supplies, AN1149**
  - **SIMPLE SWITCHER® PCB Layout Guidelines, AN1229**

Here is a checklist of the layout considerations we discussed for noise reduction. Realize that PCB traces have impedance (both resistive and reactive) and current takes the least path of impedance.