from: David M. Binkley: "Tradeoffs and Optimization in Analog CMOS Design"

current and shape factor are held constant. Over the 0 to 70 °C commercial temperature range, however, the technology current increases by only 13 % resulting in an inversion coefficient decrease of less than 12 %. These temperature changes are for the mobility temperature exponent of $BEX = -1.5$ used for Table 3.9 and Figure 3.5.

As mentioned in the previous section, if $BEX = -2$, the technology current is temperature independent. This would result, correspondingly, in a temperature-independent inversion coefficient. If the inversion coefficient were temperature independent, however, this would mean only that the region and numerical level of MOS inversion would remain constant with temperature. Transconductance, for example, would still decrease with temperature due to increasing thermal voltage as described later in Section 3.8.2.4.

The usual modest drop in inversion coefficient with temperature due to increasing technology current lowers the level of inversion. This would normally be expected to increase the transconductance efficiency and transconductance as described later in Section 3.8.2.4. However, the increase in the thermal voltage is more significant, resulting in an overall decrease of transconductance efficiency and transconductance.

3.5.4 Threshold Voltage

The design methods and examples described in this book involve selecting drain current, inversion coefficient, and channel length for optimum tradeoffs in performance. This is consistent with threshold-voltage, independent design where drain bias current is held fixed or perhaps varied with temperature to hold transconductance constant. Threshold voltage, however, is important in evaluating the operating gate–source voltage, $V_{GS} = V_T + V_{EFF}$, which is equal to the sum of the threshold voltage, V_T, and the effective gate–source voltage, $V_{EFF} = V_{GS} - V_T$. V_{GS} must be maintained at sufficiently low values to ensure bias compliance, especially in low-voltage designs.

The threshold voltage change with temperature, described in Table 3.7, is modeled by the threshold-voltage temperature coefficient, TCV. Figure 3.6 shows the measured threshold voltage for nMOS devices in a 0.8 μm, PD SOI CMOS process from 20 to 300 °C (293 to 573 K) [21]. This is an extremely wide temperature range encompassing very high temperatures supported by SOI CMOS processes because of low drain–body leakage resulting from drains placed on insulating material instead of inside the normal silicon substrate. In Figure 3.6, the threshold voltage decreases almost linearly by 0.45 V over the temperature increase of 280 °C. This gives a value of $TCV = -0.45\,\text{V}/280\,°\text{C} = -1.6\,\text{mV}/°\text{C}$. The magnitude of pMOS threshold voltage decreases a similar amount with increasing temperature. While increasing temperatures usually lower transconductance, voltage gain, and bandwidth, increasing temperatures actually lower the threshold voltage. This usually favorably lowers V_{GS} since the threshold voltage usually decreases more compared to the temperature-related increase in V_{EFF}.

3.5.5 Design Considerations

Temperature effects on parameters like the thermal voltage, mobility, transconductance factor, technology current, inversion coefficient, and threshold voltage must be considered in design. In this book, we will focus on selecting drain current, inversion coefficient, and channel length for optimum tradeoffs in performance at a selected nominal temperature. This is done using performance predictions given in tables and figures, which are included in the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet. Performance can then be predicted at other temperatures. This involves first finding the temperature-corrected inversion coefficient as described in Section 3.5.3, followed by evaluating performance using the temperature-corrected thermal voltage, mobility, or other relevant process parameters. When using the spreadsheet, the temperature input cell can be changed, and multiple columns can be used for the minimum, nominal, and maximum temperature. However, device inversion coefficient inputs must be changed to hold a constant channel width since the inversion coefficient changes modestly with temperature for a constant drain current and device shape factor.