Matching Of Transistors

Prepared By
VIMAL GOHEL

what is mismatch ?

- deviation of measured raio from the intented ratio is called mismatch of two transistors
- delta = [(x2/x1)-(X2/X1)]/ (X2/X1)
  - where x2/x1 are measured ratio and X2/X1 is intended ratio
- Two Types of Matching
  - Voltage matching : Differential Amplifier
  - Current matching : Current Mirror

Voltage and Current Matching

1. VOLTAGE MATCHING :
2. Causes varation in Gate To source Voltages of different transistors
3. Improvement of Voltage Matching :

minimize the Delta(Vgs)
Low Effective Gate Voltage : < 0.1V
Large W/L ratio

4. CURRENT MATCHING:
5. causes variation in Drain to source Current
6. Improvenent of Current Matching :
   reduce difference of Drain currents
   High Gate Effective Voltage : 0.3V-0.5V

Matching- Lay out Point of view

Depends on three factors

- SIZE
- SHAPE
- ORIENTATION

PARAMETERES :

- GEOMETRIC EFFECTS
- DIFFUSION AND ETCHING EFFECTS
- THERMAL AND STRESS EFFECTS
- COMMON CENTROID LAYOUT OF MOS

- long channel transistors are more matched compare to short channel

Geometric effects

1. GATE AREA
   - affects threshold voltage mismatch
   - Inversly proportional to the root of Gate Area (Weff * Leff)
   - Gate oxide thickness :
     thin oxide is better match compare to Thick oxide
     backgate doping varies Voltage Matching
     feild scaling depends on Oxide mismatch and Threshold mismatch

- Channel Length Modulation
  - mismatch of two transistor directly proportional to change in Drain to Source voltages of two transistors and inversl y proportional to length of two trnsistors
  - Oreintation
  - Matching of transistors Transconductance should be the same.
  - Depends on Carreir Mobilities
  - Depends on Oreintation
  - Depends on Stress Gradient
  - Different Crystal Axis exhibits Difference Transconductance under Stress Gredient
  - Stress induces mobility variation- induces current mismatch-tilted wafer induces current mismatch of 5%
  - Stress Gradient can be avoided by putting them in same

DIFFUSION AND ETCHING EFFECTS

- PolySilicon Rate Variation
  - poly area does not etch uniformly always
  - Depends Opened Area to the Etchent , Large poly opening clears more quickly compare to small poly area
  - so Large edges of poly is overetched compare to smaller edges of poly
  - this causes the variation in gate length
  - Put DUMMY transistors of same size
  - DUMMY is usually connected to electrode to prevent the unknown floating potential

- Contacts over Active Gate :
  - placements of contacts over active gates induces threshold voltage mismatch
  - other potential mechanism due to the localized silicidation of contacts
  - Sometimes silicide penetrates through the poly which alters the work function of gate and varies threshold voltages
  - contacts on thick feild oxide does not alter the transistor property

- Diffusion near Channel:
  - Excess diffusion causes extendability of the junction to the near by transistor
  - It varies the Threshols voltage and Transconductance of the transistor
  - e.g. N+ sinker in Analog BiCMOS process should be spaced away by minimum twice of their junction depth
  - Well also affects mismatch of transistor

NMOS v/s PMOS

- some expertises notice that NMOS transistor matches more then PMOS transistor
- PMOS has 30-50% more transconductance variation compare to NMOS

THERMAL AND STRESS EFFECTS

- Magnitude of gradients depends on the saperation of centroids
- Oxide Thickness Gradients
  - Depends on the Temprature and oxidizing atmosphere
  - Thick oxides often exhibits concentric rainbow colored things indicates radial oxide thickness gradients
  - Thin Gate Oxides also exhibits radial oxide thickness
- Stress Gradients :
  - It causes the variation in career mobilities which ultimately affects transconductance
  - Reduce the stress gradient proper layout pattern can be followed like Common Centroid

- Metalization induce stress :
  - routing metal leads over active gate area creates stress induces mismatch
  - In case we have to cross, we use other dummy metal leads to have same characteristic of all transistor
- Thermal Gradient :
  - Voltage matching primarily depends on threshold voltage
  - Threshold voltage decrease with tempreture, Workfunction of gate changes
  - Current Matching primarily depends on Transconductance
  - It depends on Carrier mobilities which has large tempreture coefficeint

COMMON CENTROID METHOD

- Gradients mismatche depends on distance between centroids
- CCM greatly reduce distance, cancel the long range variation because its a linear function of distance
- transistor equal number of left oriented and right oriented segments they are match perfectly
- Chirality Factor :Right oriented segments minus Left oriented segments
- Set of Rules for CCD :
  - Coincidence
  - Symmetry
  - Dispersion
  - Compactness
  - Orientation

- MOS transistot matching
  - Minimal Matching : precise current, 10mv , bias current network
  - Moderate matching :offset voltage 5mv ,current mismatches less then 2%,opamps and comparators
  - Precise Matching : offset voltage 1mv, current mismatches less then 0.1%,