Design of Low Pass Butterworth Filter using AMS 0.35µm ASIC Process C35B4

Manraj Singh Gujral, M.Sc.

School of Electronics & Computer Science, University of Southampton, SO17 1BJ, UK

msg1g10@ecs.soton.ac.uk

Abstract— **This document investigates the processes used in implementing a Butterworth filter with CMOS 0.35µm (C35B4 – CMOS, 4-Metal) process to a given set of specification using AMS – Analog/Mixed Signal Design Kit, HIT-Kit v 3.70. The Report is submitted along with a Softcopy of a Cell library (*op_amp_rev3*) containing the entire design elements.**

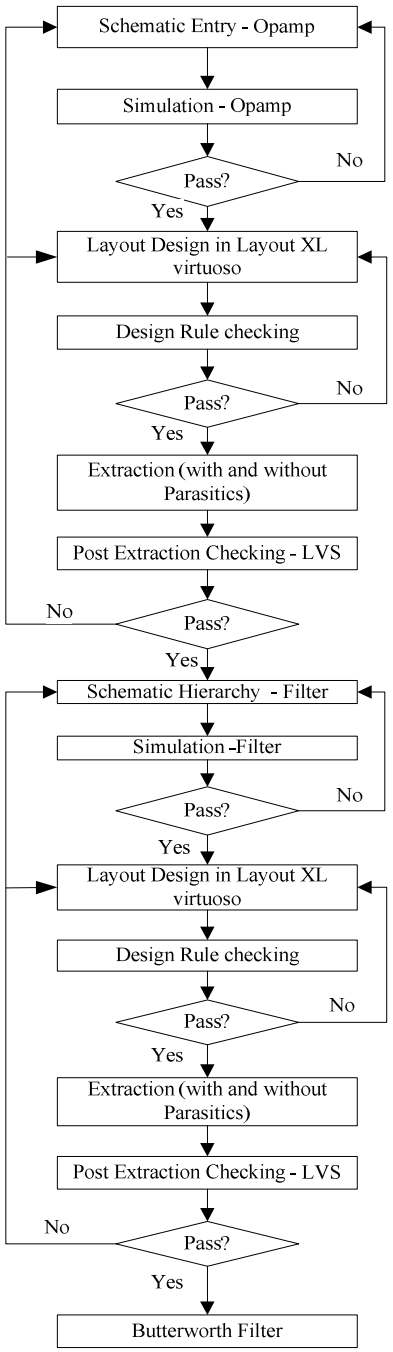
***Keywords*— Butterworth, Filter, Cadence, Design flow, Tools and techniques**

INTRODUCTION

A design flow of any process heavily depends on the tools available to the designer. Every milestone in the process is therefore monitored and corrected for generating a better output. The Cadence Custom IC Design therefore is one such software used in the industry for various purposes. We look to design a Butterworth filter in a bottom-up approach that matches certain specification. The purpose is to identify the design stages and continually monitor the outputs at each stage. Cadence presents a lot of exhaustive list of tools that we would need to achieve the filter design in given amount of time. Please note that, a target of acceptable output is essential in this work like this since over-optimizing might result in a better design, but at a cost of time.

Cadence Custom IC Design Tool lets us use variety of features for our approach, a Flow chart, as seen in the Flow Chart 1, best explains that process. The first step involves the transistor level schematic be entered in the cell library *op_amp_rev3* → *cmos035_op_amp* → *schematic.* This completes the first step of our design and it needs to be checked and saved. The simulation of the opamp is carried out by making a symbol and simulating it in a test bench. (*op_amp_rev3* → *cmos035_op_amp_test* → *schematic).* The errors encountered are usually small in this step and easily debugged. *op_amp_rev3* → *cmos035_op_amp* includes *layout*, *extracted_without_parasitics*, and *extracted* (with parasitics) cell views. Similarly, the Butterworth filter is stored in *op_amp_rev3* → *butterworth_final.* Similarly the cell views include includes *schematic, symbol, layout*, *extracted_without_parasitics*, and *extracted* (with parasitics) views. Butterworth Test jig is stored in *op_amp_rev3* → *butterworth_test_final.* This document will present a walkthrough the entire design cycle as shown in the flow chart 1.

FLOW CHART I
FLOW CHART FOR CADENCE WORKFLOW [1]



A. *Op-Amp Description*

A Simple op-amp consists of 3 stages.

1. A Differential Input Stage
2. A common source amplifier stage
3. Output Buffer Stage

Each Stage has a specific role in the Op-Amp

A Differential Stage takes in input in the form of a Differential Voltage, V+ w.r.t V- . The Open loop Gain of a Differential Stage is very high and therefore it supplies nearly constant current in the output.

A Common source amplifier with Frequency Compensation stage because of its low-pass characteristics acts as an Integrator. Therefore, a constant current input from the First Stage results in linearly increasing output.

The output buffer ensures that the Op-Amp is not being loaded to the output circuitry. In construction it is merely a voltage follower and isolates the Op-Amp circuitry from the output.

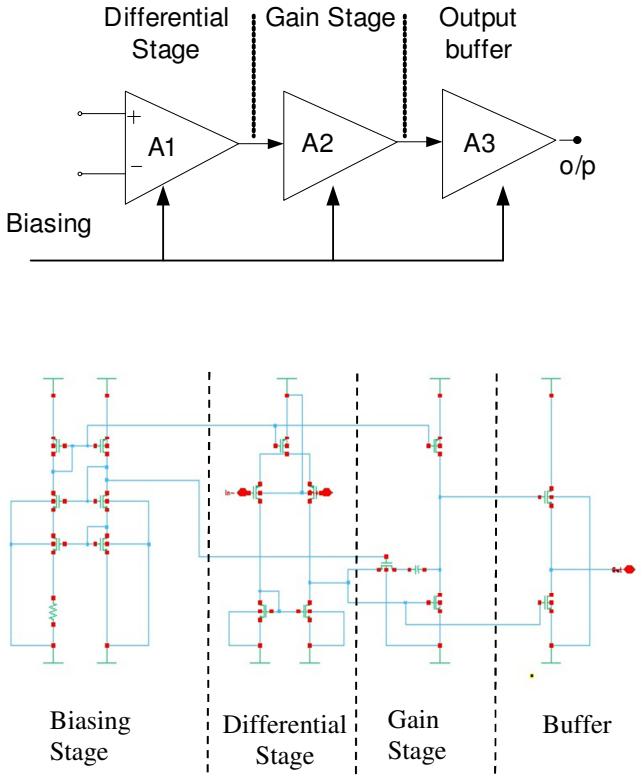


Fig. 1 Stages of an Operational Amplifier and its Schematic View in Cadence

B. *Op-Amp Layout*

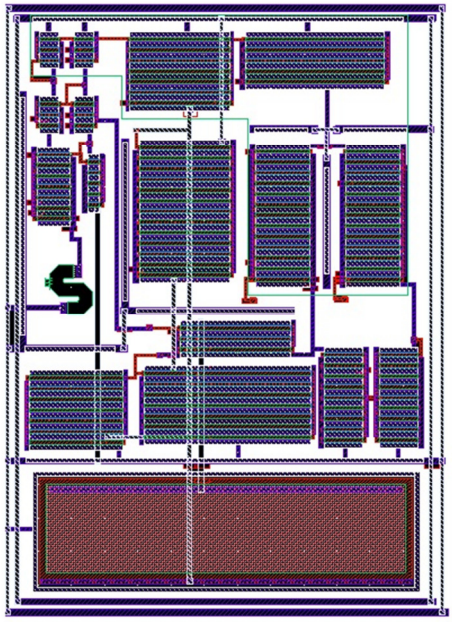


Fig. 2 A floor plan image of an Extracted (with parasitics) Op-Amp in Virtuoso. Dimension 92 µm X 67 µm

The Floor plan for Op-Amp includes:

1. Arranging all the PMOSs together and sharing the same NWELL, and grouping them near the vdda!.
2. Arranging all the NMOSes together closer to vssa!.
3. Placing the Capacitor in the periphery to avoid any interference with the data path.
4. Placing Current mirrors as close as possible and with the same orientation and layout for better matching.
5. Using a row of NDC contacts, almost 75 contacts, on vdda! , and PDC contacts on vssa! acting as a shield against noise and providing substrate taps.
6. Guard ring implementation across the whole Op-Amp for better noise protection.
7. All the three-stages element, Differential Stage Gain stage and Output buffer stage, respectively arranged as close to each other as possible to avoid connections over long distances.

C. *Determining the Filter Transfer Function*

There are several types of filter such as the Low pas, High pass, Band Pass and so on. There are several ways of implementing them such as A Chebyshev Filter or a Bessel Filter [2]. For this exercise we consider a Low Pass Butterworth low pass filter whose characteristics are similar to the curve shown in Figure 4 & 5

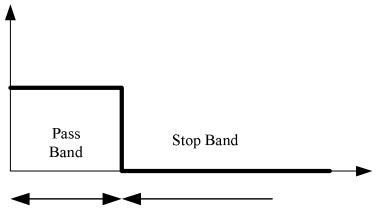


Fig. 3 (a)

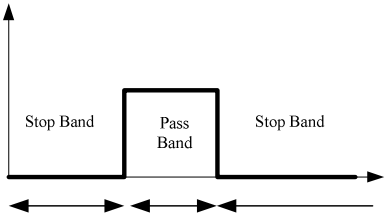


Fig. 4(b)

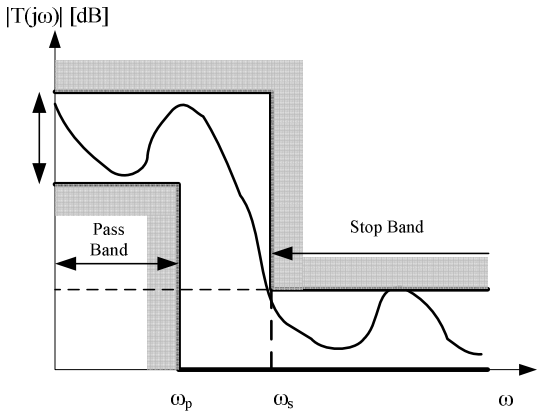


Fig. 5(c)

Fig. 6 (a) Ideal Low Pass Filter characteristics (b) Ideal Band Pass Filter characteristics (c) A practical Filter with ω_p and ω_s [3]

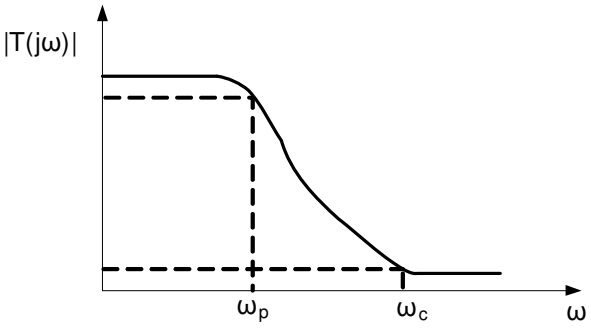


Fig. 4. Behaviour of a Low Pass Butterworth filter [4]

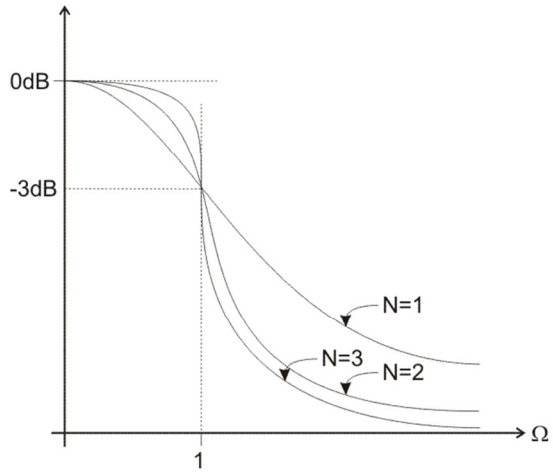


Fig. 5 The frequency response of a normalized Butterworth filter with increasing Order, N [4]

The order of the Filter can be found out by using

$$|T\ (jw)|^2 = \frac{G_o}{1+\left(\frac{\omega_S}{\omega_C}\right)^{2N}}$$ - Equation (1) [3]

Where, G_o is the DC gain.
ω_c is the Cut off frequency
ω_s is the Stop band frequency
N is the order of the filter

Therefore by the given specification of our design we can first start by calculating the Order of the Butterworth filter.

As per the specification:

ω_c is 2.4229 MHz

ω_s is supposed to be twice the cut-off frequency of 2.845 MHz

The Pass Band gain of 40dB and Stop Band Attenuation of 40dB.

Power supply is specified as V_{dd} = 1.65 V, V_{ss} = -1.65 V and GND = 0 V.

By substituting these values in equation 1, we get an approx. value of *6.3*, which we can round of to be 7, i.e., a 7th Order filter.

During the simulation, the error for a 7th order filter was more than 2 %. Error is calculated by a simple technique of $\left|\left(f_{desired} - f_{actual}\right)/f_{desired}\right|$.

Also, the Capacitances values were reaching an order above 10p F which during the Layout-XL stage was found to be very large in size.

Therefore, an 8th Order Filter was implemented to satisfy both, the design specification condition of achieve a 0 dB at twice the cut-off of ω_c of 2.4229 MHz and 0 dB at 2 x ω_c. and to have a reasonable size of the overall Layout.

The simulation of 8th Order filter is therefore presented.

N	Normalised Denominator Polynomials in Factored Form
1	(1+s)
2	$(1+1.414s+s^2)$
3	$(1+s)(1+s+s^2)$
4	$(1+0.765s+s^2)(1+1.848s^2)$
5	$(1+s)(1+0.618s+s^2)(1+1.618s^2)$
6	$(1+0.518s+s^2)(1+1.414s+s^2)(1+1.932s+s^2)$
7	$(1+s)(1+0.445s+s^2)(1+1.247s+s^2)(1+1.802s+s^2)$
8	$(1+0.390s+s^2)(1+1.111s+s^2)(1+1.663s+s^2)(1+1.962s+s^2)$
9	$(1+s)(1+0.347s+s^2)(1+s+s^2)(1+1.532s+s^2)(1+1.879s+s^2)$
10	$(1+0.313s+s^2)(1+0.908s+s^2)(1+1.414s+s^2)(1+1.782s+s^2)(1+1.975s+s^2)$

Table. 1 Normalised Denominator Polynomials in Factored Form [2]

We substitute the

The Gain of the 2nd Order filter

The Gain of a 2nd order Filter is dependent on the damping factor, ζ. Therefore we keep the coefficient of "s" in the Butterworth polynomial of the specific order (here the 7th Order) such that, ζ. = 0.707.

Also, to ensure cut-off frequency, *fc*, we need to adjust the gain. Therefore we ensure

$$A_v = 3 - \alpha \qquad \text{- equation (2) [5]}$$

Where α is the coefficient of "s" in the from the 7th Order filter, which will be subsequently changed to 8th order.

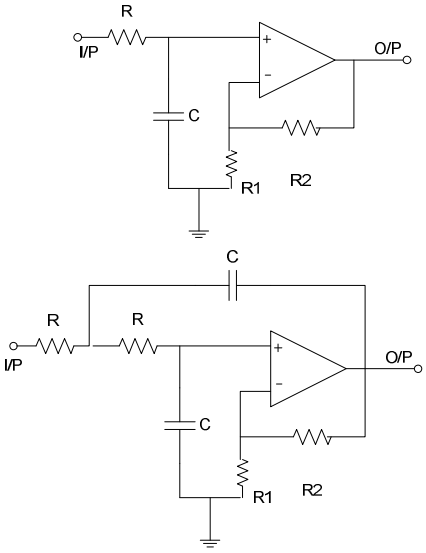


Fig. 7 First and Second Order Filter (resp.) [5]

R and C, as shown in Figure 6, determine the Cut-off frequency as $f_c = \frac{1}{2\pi RC}$ -equation (3) [5]

The gain for 1st Order Stage is given by

$$A_v = \frac{R2}{R1} \qquad \text{- equation (4) [5]}$$

The gain for 2nd Order Stage is given by

$$A_v = 1 + \frac{R2}{R1} \qquad \text{- equation (5) [5]}$$

Therefore, with all the parameters available we proceed to the Butterworth simulation of the 8th order Filter.

D. Butterworth Filter Schematic

The 8th Order Filter is formed by connecting four 2nd order stages, as shown in Figure 6.

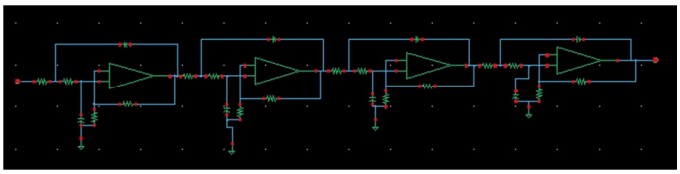


Fig. 8 8th Order Butterworth filter in Schematic View

Step1: We feed in the calculated values for R & C (determining the cut-off frequency) and R1 & R2 determining the Gain, in the Schematic and check for its ac analysis response.

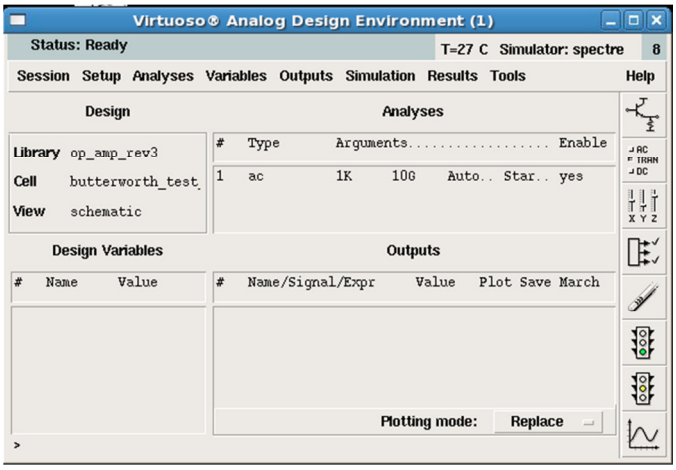


Fig. 8 Virtuoso Analaog Design Environment. Performing AC frequency sweep from 1e+3 to 1e+10

The output can be plotted in terms of the Output 20dB Gain. However the outputs can be seen in multiple ways depending on the type of analysis, such as AC Gain vs. Phase, AC Magnitude, 10 dB and so on.

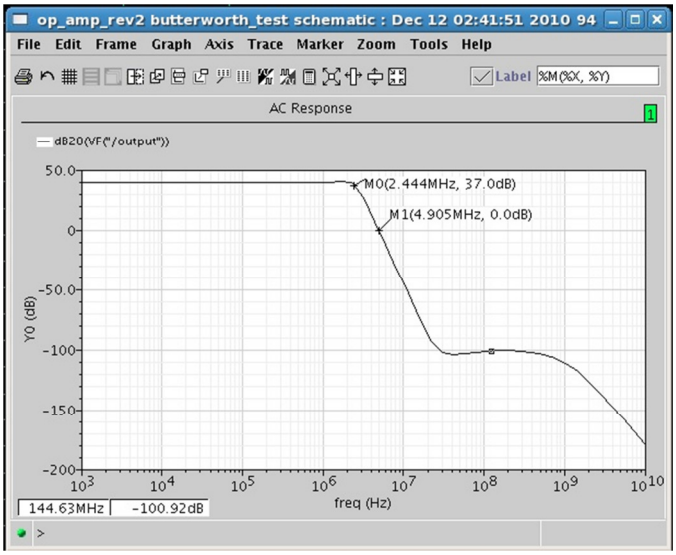


Fig. 9 Virtuoso Analaog Design Environment. Frequency analysis from 1e+3 to 1e+10

Marker M0: 2.444 MHz at 37 dB, and M1: 4.905MHz at 0.0dB

Note: I have used *Res* and *Cap* from *Primlib* in the first simulation irrespective of its practical feasibility. Advantage with using *res* and *cap* is that the user gets the freedom to assign any value to them to achieve the desired value. This is particularly useful when we are considering tuning the circuit frequency upto 4th least significant digit. Once the values for various resistances and capacitances are optimized, it is mandatory to replace it with *rpolyh* and *cploy* (from the *analoglib*) to the nearest values before Layout. Else the layout will not include its physical component.

Parameter passing feature is used to see for which values of Resistances the output wave form is closest to the required curve. Capacitor is set to 10p F and resistance R, is assigned a pPar ("res") variable so as to later sweep the value in a given interval and its response to the system. Tables must be numbered using uppercase Roman numerals. Table captions must be centred and in 8 pt Regular font with Small Caps. Every word in a table caption must be capitalized except for short minor words as listed in Section III-B. Captions with table numbers must be placed before their associated tables, as shown in Table 1.

Figure 10 shows the Output waveforms of a sweep of 10 Resistance values for the Resistor R, in equation (3). The graph is a zoomed in version for us to clearly see the difference in the output.

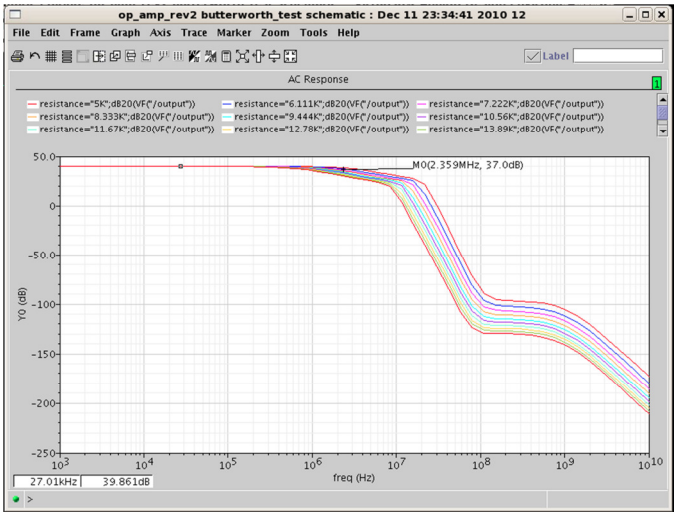


Fig. 10 Virtuoso Analaog Design Environment. Frequency analysis by using Parameter Passing for "R" from 1e+3 to 1e+10

The Marker M0 shows a frequency of 2.35 MHz at 37 dB. A rough estimate of the resistance value can be established from analysing the graph. Multiple paths of the output graph are due to the resistance sweep of R as "res". Therefore, we begin to approach closer to the Output frequency.

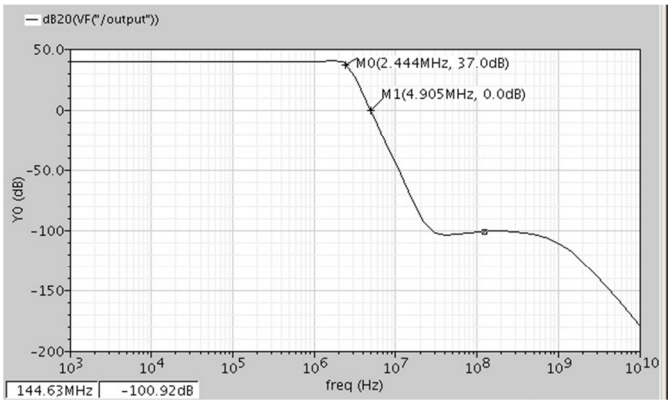


Fig. 11 Virtuoso Analaog Design Environment. Frequency analysis by using Parameter Passing for "R" from 1e+3 to 1e+10

After few sweeps, it becomes apparent when the output is going to be stabilized.

Throughout the simulation, both the parameters are to be checked for their approximations. No one device, either R or Capacitor should be too large.

Note: The larger capacitates, > 10 pF are very large physically, even larger than the whole Op-Amp in dimensions. Therefore it is advisable not to cross that limit in this particular exercise.

After running a few Parametric analysis at the Resistance value of the 1st stage was almost fixed since the resultant frequency response almost matches the desired level.

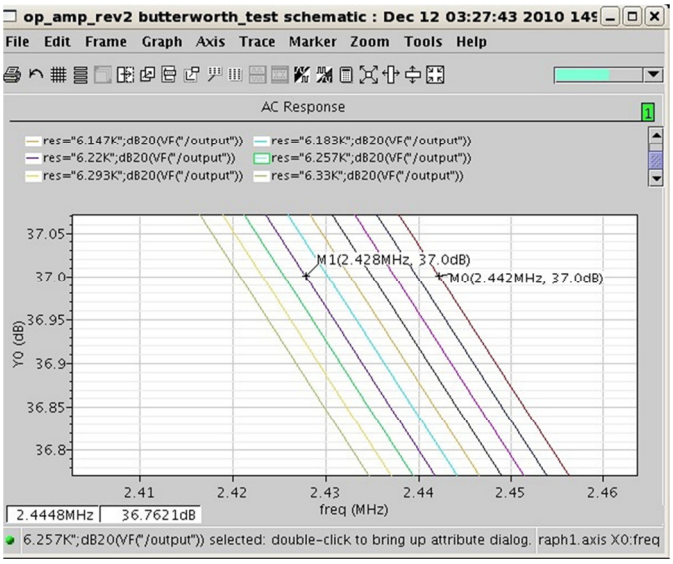


Fig. 12 Virtuoso Analaog Design Environment. Frequency analysis by using Parameter Passing for "R" from 1e+3 to 1e+10

$f_c = 2.428$ MHz is appropriate cut-off frequency.

After fixing the Capacitor and Resistor so as to achieve the Cut off frequency at 2.428 MHZ, we move to the stop band frequency, and try to achieve the closest result possible.

Figure 13 shows the final Butterworth simulation for our design.

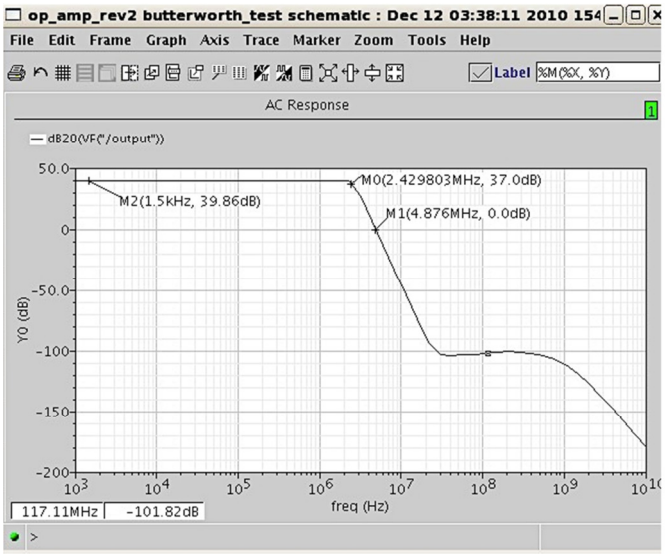


Fig. 13 Virtuoso Analaog Design Environment. Frequency analysis from 1e+3 to 1e+10

M1 Marker: 0dB at frequency $2 \times fc$

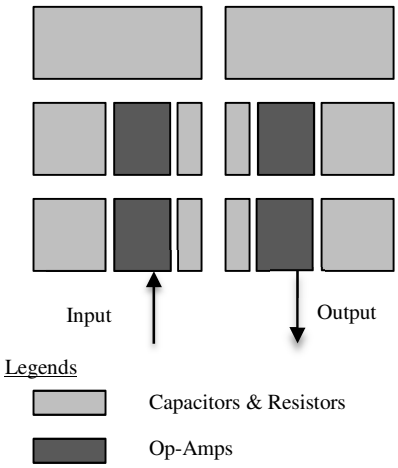
M2 Marker: 39.86 dB at frequency $< fc$

Markers M0, M1 and M2 clearly show the required characteristics are met.

At this point we can proceed to the Layout of the Butterworth Filter.

E. Butterworth Filter Layout

The floor plan for Butterworth layout is implemented first. Defining a floor plan is critical since it plays an important part in checking parasitics. If parasitic capacitances become large, the frequency response might fail.



The floor plan, seen in Figure 14 was based on the following assumption:

Fig. 14 Floor Plan for Butter worth filter Layout

1. Since there are larger Capacitors, and they are double the number of Op-Amps, it is placed at the outer periphery of the IC layout so that it doesn't interfere with the Data Path.
2. Another purpose of keep in Capacitors at the output is to protect the circuit from noise. For further immunity to the noise, a Guard Ring across the whole design is used connected to GND (Global) .Similar approach was used when designing individual Op-Amps
3. The Data path is concentrated in the centre of the Design, shown in figure 14.

Since including the floor plan design as an Image in this document might not serve the purpose, a Cadence file is supplied along with this report. However, a low-res image of the extracted plan can be seen in the appendix-1

The output after the extraction of DRC passed Layout, Figure 15, is considerably different from the expected result. The Error is however lower than 2 %.

AC analysis is carried out with varying Resistance and Capacitance values. The values of Capacitances are found to be equally sensitive to the output as the resistance values, but the change in their physical area for small change of capacitance is much higher when compared to a change in

resistances. The current Butterworth Filter design is therefore frozen at this state.

Further scope of improvement remains by using the parametric analysis, as was the case in Op-Amp design, and based on past results in op-Amp simulation the error can be expected be reduced to almost 0.5 % or less.

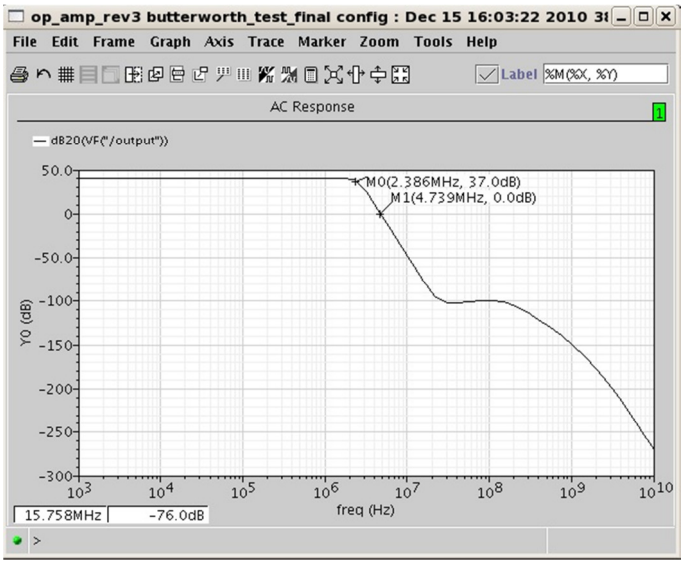


Fig. 9. Frequency analysis of the extracted Filter with parasitics (using "capall" in Extraction)

The final Output, Figure 15, is not as exact as the pre-extracted version, shows the effect of parasitics and various Metal-1 and Metal-2 path lengths in routing on the performance of a Filter.

LEARNING OUTCOMES & CONCLUSIONS

Cadence is a very useful tool for Electronics Engineers. We have used it in bottom-up approach in this exercise starting from Transistor level implementation in Individual Op-Amps to finally simulating the Filter in its extracted with parasitics form. Such an approach teaches not only about the basic building blocks of Electronics, but also lets the user explore immense functionality of the Cadence software itself. Throughout this design process I had kept a log of notes which can be used to improve the performance of this fabricated Butterworth filter IC:

A. *Observations*

1. There are a number *current mirror* stages/pairs in an Op-Amp. By implementing Inter-Digitization and Common Centroid techniques the individual matching of transistors can be improved [6].
2. The use of Metal Layers in this assignment is purposely restricted to METAL-2. However, the effect of Metal routing over Capacitors and various transistors needs to be investigated.
3. The IC implemented comprises of a lot of spaces, as can be seen in appendix-1, which were kept for accommodating any changes made in Resistance and capacitance values to optimize the filter response. Therefore, for fabrication, the overall area of the IC can be further reduced by 10 to 15 % by eliminating spaces in between.

A. *Learning Outcomes*

As little as I have worked on Cadence, I can still point out to some features those, which have been extremely beneficial

1. The *Design Rule Chec*k feature is an extremely exhaustive from of checking. Currently we checked our designs with a less stringent - "no_coverage" option.
2. *Parameter Passing* is particularly useful in large circuits, with multiple variables. The final Plot has a calculator to further simplify the analysis after using parameter passing feature.
3. The sequence of schematic entry – symbol generation – test bench – Layout - Extraction – and finally LVS results in a comprehensively tested and full proof unit/design.

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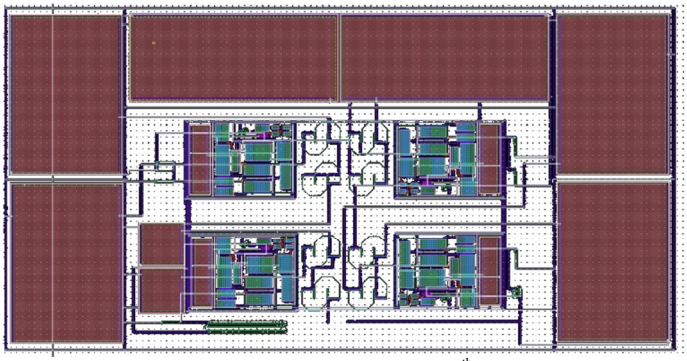
APPENDIX-1



Low-res image of the overall Butterworth 8th Order filter.
Dimensions 558 µm x 287 µm