A 5 Gbps Low Noise Receiver in 0.13μm CMOS For Wireless Optical Communications

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***Abstract*— A wideband, high gain, and low noise optical receiver targeting imaging architectures for optical wireless communications is presented. For line of sight tracking in optical wireless communications, a switching matrix is employed between the pixel/photodetctor array and the transimpedance amplifier. The optical receiver consists of a low noise wideband TIA, where noise and stability are optimized in the presence of the switch, using a series inductor at the input. The TIA is followed by a limiter with offset cancellation and 50 Ω output buffer capable of 900 mv p-p differential output swing over the 50 Ω resistance of measurement equipment. The receiver implemented in IBM 130nm CMOS technology achieves a bit error rate of 10^{-12} at 5 Gbps corresponding to 2.8 μA current at the input, in presence of 1 pF input capacitance representing the photodiode. The total power consumption including the on chip 50 Ω differential output buffer is 68 mW from 1.5V DC supply, while the die area including bonding pads and output buffer is 1106 $\times$ 895 μm^2.**

***Index Terms*— Optical receivers, CMOS image sensors, Low-noise amplifiers**

I. Introduction

Wireless optical communication is a promising technology to address the increasing demand for higher data rates, while providing secure communication. Possible applications range from short range parallel chip to chip wireless buses, static point to point last mile huge aggregate data rate links, to high speed indoor portable scenarios such as future Gigabit wireless LANs [1]. Despite its advantages, wireless optical communication suffers from several drawbacks such as line-of-sight (LOS) requirement and eye safety regulations which limit the communication distance. For LOS scenarios, a tracked receiver/transmitter architecture is typically needed to prevent link interruption. Nearly all tracking architectures use arrays of photodiodes in the receiver and LED or LASER diodes in transmit side. Such receiver as shown in Fig. 1 is called an imaging receiver [2] [3].

Several implementations for silicon imagers have been proposed in the literature [3] [4] [5]. However, they have mostly been limited to low data rate communications. The lower communication speed can be attributed to the time required for processing the complete image and locating the target as well as the low speed of photodetector in the imager. Other fundamental issues include the gain and noise requirements of the front end optical receiver which receives relatively weak signal from the small area of the PD, specially in array architectures. The front end of the optical receiver in the imager has to provide enough gain to amplify such signal while having minimum input referred current noise to achieve a reasonable bit error rate. In this paper, we present a design methodology for addressing wideband, high gain and low noise receiver front-end for silicon imagers targeting high data rate optical wireless communications. To minimize the overhead required to process the complete image and locate or track the target, a switch matrix is added to the imager as shown in Fig.1. The switch matrix is controlled by a digital controller that scans the different pixels or photodetectors and locates the pixel in LOS with the transmitter as proposed in [6]. The addition of the switching matrix changes the stability and noise analysis of the transimpedance stage following the switch and the PD as will be outlined in the following sections. The paper is organized as follows. Section II presents the circuit design, highlighting noise and stability optimization. Measurement results for a prototype chip is discussed in section III. Conclusions are drawn in Section IV.

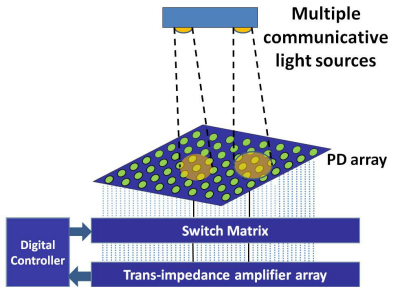


Fig. 1. Block diagram of an imaging receiver for optical wireless communication.

II. Circuit Design

A. Noise Optimized TIA For Imaging Receivers

Imaging receivers consist of arrays of photodiodes (PDs) as shown in Fig. 1. To control steering the current of different PDs towards a fast and high gain TIA, switches between PDs and TIA input need to be considered. Once the switch is added to the signal path, the PD becomes biased with a voltage other than the input bias of the TIA as shown in Fig. 2. The biasing resistor of the PD has to be large enough to lower its noise contribution. In the presented design for the front end optical receiver, shunt feedback TIAs are selected for their high gain and low noise. To account for the effect of the photodiode, a capacitance of 1pF is considered at the input of the TIA, based on device level simulations using 130nm process technology parameters, and prior work [7]. The added switch not only changes the input referred noise, but also has a high impact

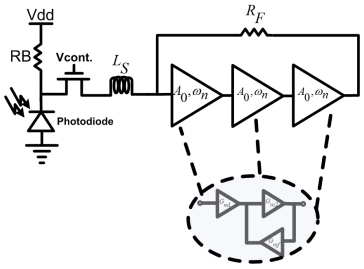


Fig. 2. Switched TIA in an imaging optical receiver.

on the stability of the TIA. For a target transimpedance gain Z_{TIA}, bandwidth BW and input capacitance C_{PD}, the gain of the core amplifier in the TIA A_v can be readily calculated as $A_v = 2\pi.BW.Z_{TIA}.C_{PD}$ and the DC gain of the core amplifier $A_{v0} = |A_0|^3$ as seen in Fig. 2. To ensure stability, the bandwidth of the core amplifier must be significantly wider than the target bandwidth. A series inductor is used to partially relax such high bandwidth requirement in the core amplifier by introducing a pair of complex conjugate poles in the transfer function. Fig. 2 shows the schematic of the front end circuit including the switch and the series inductor.

To quantify the noise contribution of different components in the receiver, we will assume an average input referred voltage noise $V_{n,A}$ for the core amplifier such that

$$V_{n,A} = \sqrt{\left(\frac{V^2{}_{n,out,tot,core}}{A^2{}_{v0}BW_{core}}\right)} \quad (1)$$

Ignoring the noise of the switch due to its low transconductance, the output noise spectrum of the circuit in Fig. 2 can be derived as:

$$V_{n,out} =$$
$$V_{n,R_F}\frac{A_v(L_sC_{PD}S^2 + SR_sC_{PD} + 1)}{(A_v+1)L_sC_{PD}S^2 + SC_{PD}(A_vR_s + R_F) + A_v + 1}$$
$$+ V_{n,A}\frac{A_v(L_sC_{PD}S^2 + SC_{PD}R_F + 1)}{A_vL_sC_{PD}S^2 + SC_{PD}(R_F + A_vR_s) + A_v} \quad (2)$$

Where R_s is the on-resistance of the switch and V_{n,R_F} is the voltage noise spectral density of the feedback resistor given by $\sqrt{4KTR_F}$. Given the two main noise sources originating from the feedback resistor and the core amplifier are uncorrelated, their noise contribution can be calculated separately over the bandwidth of the TIA, and their power densities added up. Fig. 3 shows the coefficients of the two noise components after integrating from (2) and referring back to the input, assuming a DC gain of 250 for the core amplifier, 25 $K\Omega$ for the feedback resistor, and 3 GHz bandwidth for the TIA.

As shown in Fig. 3(a) and (b), the two noise components decrease by increasing the value of the series inductor. Unlike noise matching techniques in RF amplifiers which tend to operate in a narrow bandwidth, the added series inductance tends to minimize the total integrated noise in the wide bandwidth of the TIA. It is worth noting that in one of the best reported sensitivities in the literature and with the

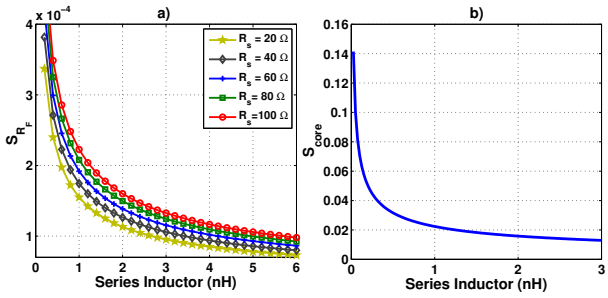


Fig. 3. Average input-referred current noise contribution scaling factors ($\frac{pA}{\sqrt{Hz}}$) of (a) the feedback resistance, and (b) the core amplifier, versus inductor and switch resistance values. S_{RF} corresponds to the first fraction in (2), while S_{core} is for the second fraction.

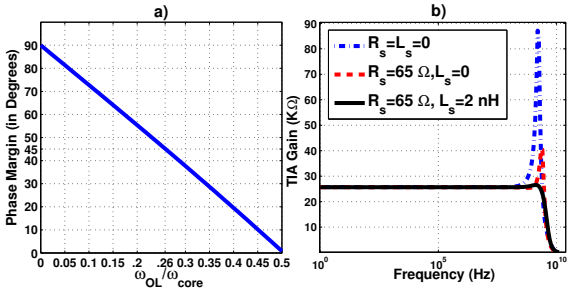


Fig. 4. (a) Phase margin of the shunt feedback TIA without considering the effect of the switch and inductance, (b) frequency response showing the effect of the series switch and inductance,R_s is the switch's on resistance.

low responsivity of the integrated photodiode (5mA/W), large devices were needed in the first stage of the core (420 μm) [7]. In this work, a comparable sensitivity is obtained with devices as small as 40 μm.

B. Stability Analysis Of The Switched TIA

To decrease the input referred current noise, a high gain TIA is required. The core amplifier consists of 3 identical cascaded stages as shown in Fig. 2. To derive the phase margin of the TIA, a maximally flat second order response for each stage of the core amplifier is assumed. Without the effect of the series switch and inductance L_s, the phase margin of the shunt feedback TIA shown in Fig. 2 can be given by:

$$PM = \pi - 3\arctan\frac{2\omega_{core}\omega_{OL}}{2\omega^2_{core} - \omega^2_{OL}} - \arctan\frac{|A_0|^3}{1 + \frac{R_E}{R_B}} \quad (3)$$

Where $\omega_{core} = 2\pi BW_{core} = \omega_n\sqrt[4]{\sqrt[3]{2} - 1}$ is the overall bandwidth of the core, ω_n is the natural frequency of each stage in the core, and $\omega_{OL} = \frac{|A_0|^3}{R_FC_{PD}}$ is the open loop unity gain frequency. The phase margin from (3) is shown in Fig 4(a) for $|A_v| = 250$, a feedback resistor of $25K\Omega$ and photodiode capacitance of 1 PF.

For typical values of the gain of the core amplifier and assuming a large bias resistor R_B, the third term in (3) nearly contributes -90 degrees to the total phase margin. Referring

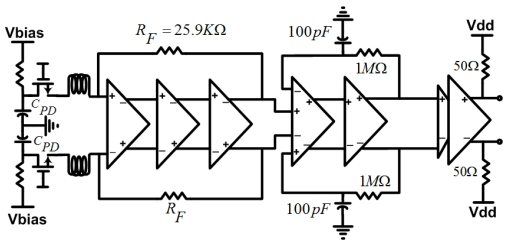


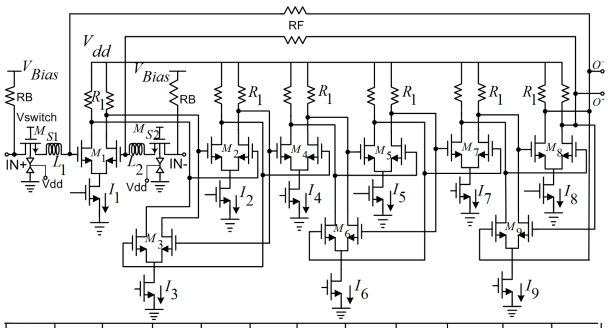
Fig. 5. Block diagram of the optical receiver.

to Fig. 4(a), to have a phase margin of $45°$, the bandwidth of the core amplifier has to be almost 4 times that of the open loop bandwidth and almost a factor of 6 for a $60°$ phase margin. Such high bandwidth is challenging to realize while still delivering high gain for the core amplifier. When including the effect of the switch between the PD and the TIA, a zero in loop transfer function is created which partially increases the phase margin and consequently reduces the gain peaking as shown in Fig. 4(b). However, as can be seen in the figure, this improvement in phase margin is still far from removing the peaking in the frequency response of the amplifier. Adding the inductance L_s creates a pair of complex conjugate poles in the open loop transfer function as well as a pair of complex conjugate zeros considering the series resistance of the switch. Fig. 4(b) shows progressive improvement in the phase margin after adding the switch and the series inductance.

C. Complete Receiver

The block diagram of the complete receiver is shown in Fig. 5, where C_{PD} represents the capacitance of the PD. Because of having the switch at the input, the PD must be biased with a voltage other than the common mode voltage at the input of the TIA. To minimize the current noise contribution of this resistor, its value must be maximized. A 100 $K\Omega$ resistor is selected for biasing and implemented using a series of smaller resistances to minimize its capacitive loading at the input node that will interface with the PD. In addition, smaller resistances have lower tolerance, which decreases the offset at the input of the TIA. Precision poly resistors have been used for realizing the biasing resistor.

For the switch, a triple-well NMOS device is selected for the following reasons. First, a triple well transistor is more isolated from substrate and thus less noise is coupled back from the substrate to the input node. Second, as the source can be connected to the bulk in this device, its series resistor is more linear compared to regular transistors, and hence potentially reduces inter-symbol interference ISI. Finally, because this transistor doesn't suffer from the body effect, it can be designed with smaller width, which directly reduces its parasitic capacitance at the input node. The spiral inductor is implemented using the top metal layer in the technology. Fig. 6 shows the detailed schematic of the TIA. The high gain of the TIA (25 $K\Omega$) reduces the gain requirements of the limiting amplifier, which directly reduces the power consumption of the receiver, a critical issue in the array implementation shown in



$M_{1a,b}$	$M_{2a,b}$	$M_{3a,b}$	$M_{4a,b}$	$M_{5a,b}$	$M_{6a,b}$	$M_{7a,b}$	$M_{8a,b}$	$M_{9a,b}$	$M_{S1,2}$	R_1	$L_{1,2}$
$40\mu m$ / $120nm$	$30\mu m$ / $120nm$	$5\mu m$ / $120nm$	$40\mu m$ / $120nm$	$30\mu m$ / $120nm$	$5\mu m$ / $120nm$	$40\mu m$ / $120nm$	$30\mu m$ / $120nm$	$5\mu m$ / $120nm$	$30\mu m$ / $120nm$	498Ω	2nH

R_B	R_F	I_1 1.8mA	I_2 1.85mA	I_3 148μA	I_4 2.63mA	I_5 1.65mA	I_6 152μA	I_7 1.94mA	I_8 2.5mA	I_9 241μA
$100K\Omega$	$25.9K\Omega$	$30\mu m$ / $120nm$	$30\mu m$ / $120nm$	$7\mu m$ / $120nm$	$30\mu m$ / $120nm$	$30\mu m$ / $120nm$	$7\mu m$ / $120nm$	$30\mu m$ / $120nm$	$30\mu m$ / $120nm$	$7\mu m$ / $120nm$

V_{Bias}	V_{dd}	$V_{Switch,On}$
1.2V	1.5V	1.5V

Fig. 6. Schematic of the TIA.

Fig. 1. A 2-stage limiting amplifier with similar amplification stages to the TIA is employed. For the offset cancellation stage, a low pass filter implemented using a distributed 1 $M\Omega$ resistor, and 100 pF on chip capacitor was considered on chip, which creates a high pass corner frequency of 79 KHz for the complete receiver. Finally, for the sake of measurements, a 2 stage 50 Ω buffer with f_T doubler architecture is used, which can steer maximum 20 mA current to each branch of its differential output.

III. Measurement Results

The design shown in Fig. 5 is implemented in 130 nm IBM technology. For electrical measurements, a series resistor is added on chip to convert the output voltage of the PRBS generator to current, emulating the function of the PD to be integrated in future phases of this work. The value of the the added series resistance must be maximized to lower its noise contribution and the noise contribution of on chip 50 Ω input resistor, while taking its effect on the bandwidth into consideration. A resistance of 12.3 KΩ was selected as a trade of between noise and the bandwidth degradation. The effect of the capacitance of the PD is also included on chip using a 1pF capacitance. The measurement setup is depicted in Fig. 7. The die is wirebonded to a PCB for testing purposes. The differential output of the PRBS generator goes through 20dB attenuators and then is ac coupled to the chip.

Fig. 8(a) shows the die photo of the chip while Fig. 8(b,c,d) show measured 2Gbps, 4Gbps and 5Gbps eye diagrams at the output of the receiver as a result of $2.8\mu A$ input current. As can be seen, a peak to peak amplitude of around 900 mV is measured at the output. Fig. 9 shows the measured BER versus the input current for the 3 data rates of 2, 4 and 5 Gbps. Table 1 compares the performance of recently published optical receivers with this work. To be consistent

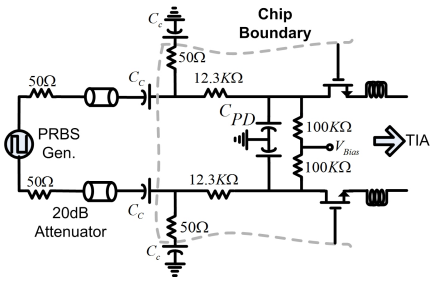


Fig. 7. Measurement setup.

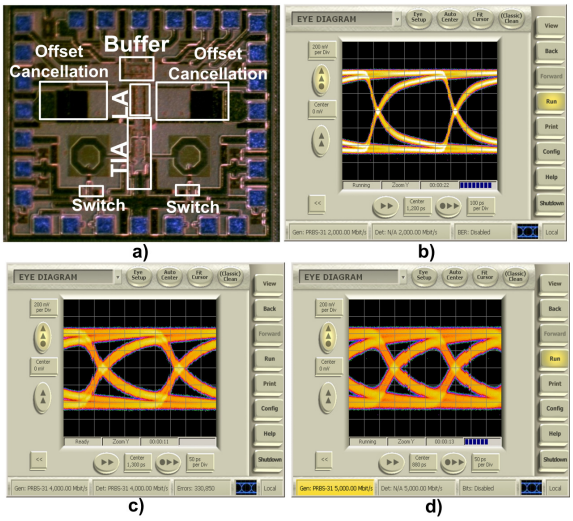


Fig. 8. (a) Die photo, (b)-(d) measured differential eye diagrams at the output of the receiver, corresponding to 2.8 μA input current for 2 Gbps, 4 Gbps, and 5 Gbps input data rate.

with electrical measurement done in this work, the sensitivity of all designs are reported as the input current, calculated using the published responsivity of the integrated photodiode in each design.

IV. Conclusion

The imaging receiver architecture is a possible solution for line of sight (LOS) tracking in high data rate wireless optical communication. Imaging receivers require arrays of small size PDs, which increases the sensitivity requirements of the following front end receiver. In this paper, a design methodology for noise and stability optimization of high gain TIAs is introduced which is specially applicable to low power imaging receivers. A prototype chip is implemented in IBM8RF 130 nm CMOS technology. Measurement results for data rates of 2, 4 and 5 Gbps are reported. The receiver consumes 68.6 mW from 1.5 volts power supply, of which 36.6 mW is consumed in output buffer. The optical receiver provides 2.8 μA input current sensitivity at 5Gbps, which is in the order of the best reported sensitivity to date, while occupying approximately around half of the area. The total die area including bond pads and 50 Ω output buffer is 1106 $\times$ 895 μm^2.

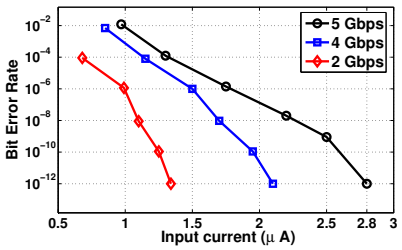


Fig. 9. Measured BER versus input current.

TABLE I
Comparison of performance parameters of some recently published optical receivers.

Design	Tech. μm	C_{PD} pF	Sen. μA	P_{Loss} mW	D.R. Gbps	P-P out mV	Area mm^2
[7]	.13	1	2.3	74.16	4.5	900	1.77[1]
[8]	.18	.5	25	183	5	200	.72[1,2]
[9]	.18	.206	7.3[3]	145	10	800	.76[1]
This work	.13	1	2.8	68.6	5	900	.98

[1] Die area includes the equalizer and photodiode
[2] Die area without pads
[3] Measured BER= 10^{-11}

Acknowledgment

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