Low-Cost High Gain Planar Antenna Array for 60-GHz Band Applications

Xiao-Ping Chen, Ke Wu, Liang Han, and Fanfan He

***Abstract*—An effective development of a class of low-cost planar antenna arrays having a high reproducibility is presented for 60-GHz band system applications. The proposed antenna arrays, based on the substrate integrated waveguide (SIW) scheme, consists of one compact SIW 12-way power divider and 12 radiating SIWs each supporting 12 radiating slots. A 50-Ω conductor-backed coplanar waveguide (CBCPW) integrated with CBCPW-to-SIW transition is directly used as the input of the antenna array, thus allowing to accommodate other circuits or MMICs at a minimum cost. An antenna array prototype was implemented on Rogers RT/Duroid 6002 substrate with thickness of 20 mils by our standard PCB process. Measured gain is about 22 dBi with a side lobe suppression of 25 dB in the H-plane and 15 dB in the E-Plane while the bandwidth for the 10-dB return loss is 2.5 GHz.**

***Index Terms*—Planar antenna array, power divider, substrate integrated waveguide (SIW), 60-GHz band.**

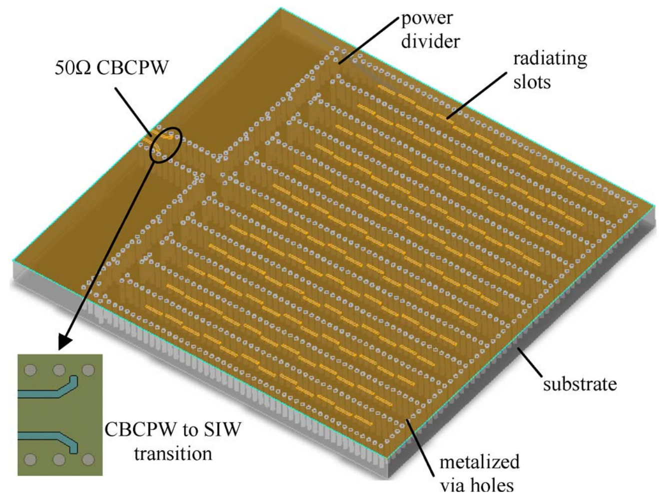

Fig. 1. Geometric configuration of the proposed 60 GHz SIW slot antenna.

I. Introduction

60-GHz band wireless applications have recently received much attention because the allocated unlicensed bandwidth of 7 GHz enables attractive gigabit-per-second applications, including high definition multimedia interface, uncompressed high definition video streaming, high-speed internet, wireless gigabit Ethernet, and close-range automotive radar sensor. One of the most important parts of such systems is the antenna since it strongly influences the overall receiver sensitivity and the link budget. With the consideration on the higher path loss and oxygen absorption of 15 dB/km around 60 GHz band, high-gain and mass-reproducible planar arrays have strongly been desired. High radiation efficiency is also important for the system cost reduction as well as the system performance enhancement [1].

To date, a vast amount of different planar antennas have been studied for millimeter-wave radio and radar applications. Although high gain operations have been demonstrated with microstrip patch antenna arrays, these configurations suffer from serious loss in the millimetre-wave band; the efficiency decreases as the gain and/or frequency becomes higher even though those antenna design techniques are basically mature. It was roughly estimated that the efficiency of microstrip arrays with gain of 35 dBi would be lower than 20% in the 60 GHz band [2]. On-chip antennas also have other drawbacks. Their radiation efficiency on conductive high-permittivity silicon is poor and in spite of the short wavelength, they still occupy a non-negligible area on an MMIC chip, which is an important cost factor. The situation is even worse if arrays need to be realized to achieve necessary gain of about 15 to 20 dBi in order to bridge intended distances of up to 10 meters in a WPAN environment [3].

On the other hand, waveguide slot antenna arrays are the most attractive candidates for high-gain planar antennas, having the smallest conductor loss among all the planar feeding structures [4]. However, the complicated 3D waveguide structure has prevented its use in cost-sensitive commercial applications with few exceptions of military or professional applications. A drastic reduction of manufacturing cost of the waveguide arrays to the level of microstrip counterparts has been desired for a long time. Single-layer waveguides for a mass reproducible planar array were presented in [5], [6]. All the waveguides consist of two parts, which are the top plate with slots and the bottom plate. Several types of single-layer waveguide arrays over 12-GHz and 20-GHz bands intended for high efficiency and manufacturability were developed and extended to higher frequencies up to 60-GHz. Nevertheless, costly mechanical manufacturing is still required for single-layer waveguide arrays and special transition structure should be used for the integration with other planar circuits. Substrate integrated waveguide (SIW), also called post-wall waveguide or laminated waveguide in some publications, is realized with two rows of metallised via-holes in a metal-clad dielectric substrate by standard print-circuit-board fabrication technique at low cost. The antenna based on the SIW scheme can easily be integrated with other circuits, which leads to the cost-effective subsystem. Some SIW slot antenna arrays and beam forming networks have been developed [7]–[10].

This communication extends the design of SIW antennas to 60-GHz band and a high-gain 60-GHz SIW slot antenna which can be directly integrated with other planar circuits was prototyped by our standard PCB process and experimentally demonstrated for its performance.

II. Design of the Proposed Antenna

Fig. 1 shows the geometric configuration of the proposed 60 GHz SIW slot array. With consideration on the dielectric properties and temperature properties of dielectric substrate, Rogers/duroid 6002 with 0.5 oz. rolled copper foil is used in this work. Generally, a thick substrate should be used to reduce the losses in connection with the top and bottom conductors and obtain appropriate offset for the design of radiating slots. In this context, 50 Ω conductor-backed coplanar waveguide (CBCPW) with metalized via holes on both sides for the suppression of unexpected modes should be used as the input of antenna by using a transition between CBCPW and SIW. A 12-way SIW power divider is deployed to feed 12 linear SIW slot arrays, and each of them carries 12 radiation slots etched on the broad wall of SIW. The SIW structure is terminated with a short-circuit three-quarter guided wavelength beyond the centre of the last radiation slot. In order to allocate the slots at the

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standing wave peaks and excite all the slots with the same phase condition (in-phase), the slots in a linear array are placed half a guided wavelength at the required centre frequency and the adjacent slots have the opposite offset with respect to the SIW centre line. The width of radiation slot should be much smaller than the slot length, usually between one tenth and one twentieth of slot length. This, of course, depends on the bandwidth requirements. The detailed design procedure similar to that presented in [11] is as follows.

A. Parameter Extraction of Isolated Radiation Slot

When a longitudinal slot in the broad wall of SIW is designed around resonance and slot offset is not very big or very small, the forward and backward wave scatterings from the slot are symmetrical in SIW and then the slot can be equivalent to shunt admittance on transmission line. According to the Stegen's factorization [12], the equivalent shunt admittance can be given as follows

$$\frac{Y(x,y)}{G_0}=\frac{G_r}{G_0}\cdot\frac{G+jB}{G_r}=g(x)h(y)=g(x)\left[h_1(y)+jh_2(y)\right]$$

where x is the offset of slot, $g(x) = G_r/G_0$ is the resonant conductance normalized to the conductance G_0 of SIW, $h(y) = h_1(y) + jh_2(y) = (G + jB)/G_r$ is the ratio of slot admittance to resonant conductance, $y = l/l(x, f)$ is the ratio of length to resonant length, $l(x, f) = \lambda \cdot v(x)/2\pi = c_0 \cdot v(x)/2\pi f$ is the resonant length. In this way, the calculation of the equivalent slot admittance is reduced to the calculation of three single variable functions $g(x)$, $v(x)$, and $h(y)$. Commercial full-wave simulator package HFSS is used to extract $g(x)$, $v(x)$, and $h(y)$ of the isolated longitudinal slot. In our work, slot width is 0.18 mm and SIW width a is 2.56 mm. Fig. 2(a) and (b) show $g(x/a)$ and $v(x/a)$ for a discrete number of relative offsets x/a in the range 0.03–0.1. Curve fitting has been applied to approximate $g(x/a)$ and $v(x/a)$ in a continuum which can be directly used in the design of the slot array by the classical iteration procedure [13]. For each offset, the function $h(y)$ as shown in Fig. 2(c) has also been extracted for y in the range 0.82–1.18. A table-look method for $h(y)$ is used in the design procedure of the slot array. It is clear that $h_1(y)$ and $h_2(y)$ rapidly change with the change of y around the matching point $y = 1$, which shows that the bandwidth of the SIW slot array is smaller than the bandwidth of conventional rectangular waveguide slot array [14].

B. Design of Antenna Array

Based on the classical pattern synthesis procedure, the excitation voltage of slots can be obtained by using Taylor distribution for H-plane pattern with 25 dB first side lobe level and uniform distribution for E-plane pattern. Elliott's method [13] is used to obtain the length and offset of each slot for a given aperture distribution by considering the internal and external mutual couplings. In this method, active input admittance Y^a of each radiating SIW includes both self admittance and mutual coupling effects with the remaining slots. A set of initial values for slot lengths and offsets are assumed, and the mutual coupling between slots is estimated according to the required slot voltage distribution. An optimization routine is then used to identify a new set of slot lengths and offsets such that all the slots are resonant and the matching conditions are satisfied for each subarray. Afterwards, a new set of mutual coupling terms are evaluated again. The procedure is iterated until a convergence is reached and the final slot lengths and offsets are obtained.

As for the SIW slot array, the slot offset in SIW may be very small due to the dielectric-filling and height-reduced effects of SIW. Therefore, a fine-tuning procedure may be needed to modify the slot length and slot offset obtained by using the Elliot's method. Some practical design aspects are considered in this work, for example, slot width and

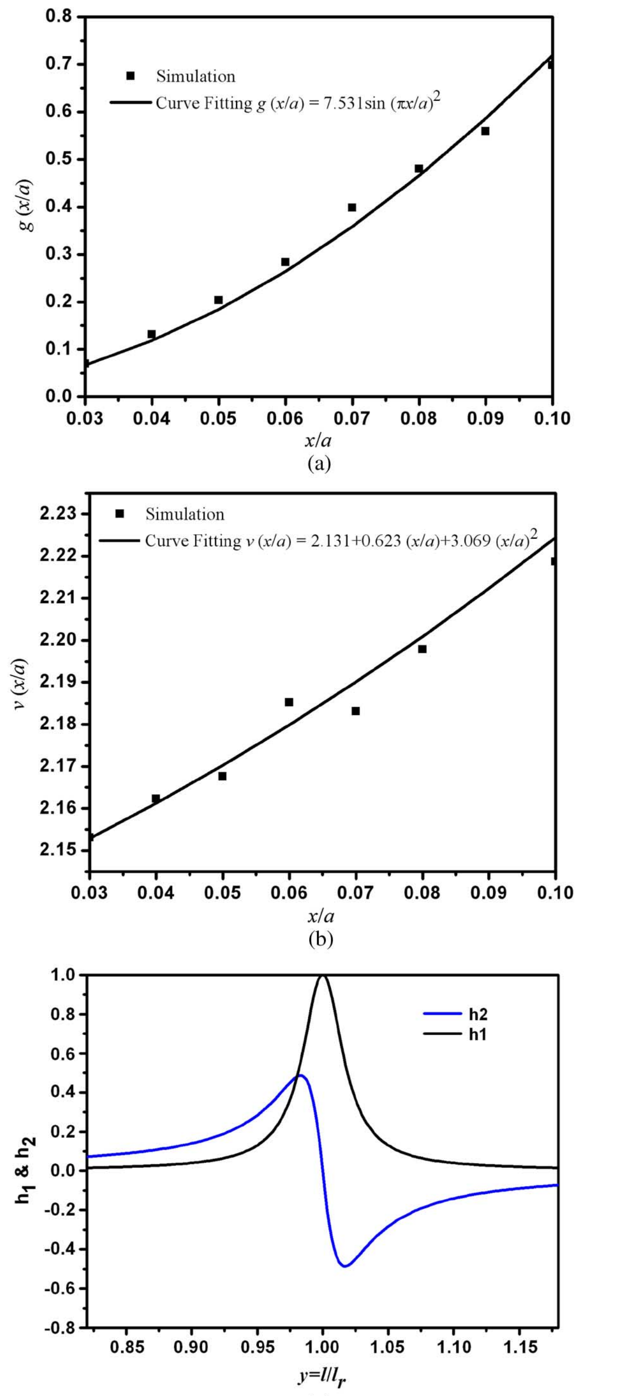
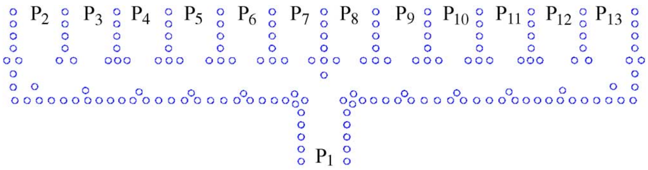


Fig. 2. (a) $g(x)$, (b) $v(x)$, and (c) $h(y)$, of isolated longitudinal slot with slot width 0.18 mm in the broad wall of SIW with width of 2.56 mm.

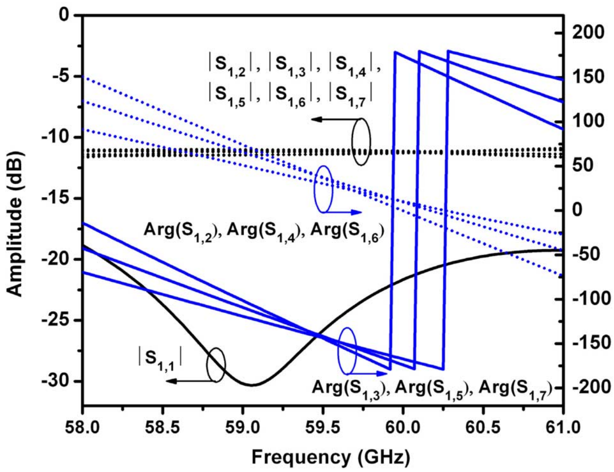
length due to the over-etching and rectangular-end slot will be changed to rounded-end slot in the etching process. Fig. 5 shows the simulated radiation pattern.

C. Design of Feeding Network

A 12-way power divider similar to that in [2] is used to feed the radiating SIWs. With consideration on the symmetry of feeding network, the feeding network shown in Fig. 3(a) consists of one CBCPW-to-SIW transition, SIW bends and five SIW T-junctions. The method presented in [15] is used to accurately design the transition



(a)



(b)

Fig. 3. (a) Configuration, (b) simulated frequency characteristics, of feeding network.

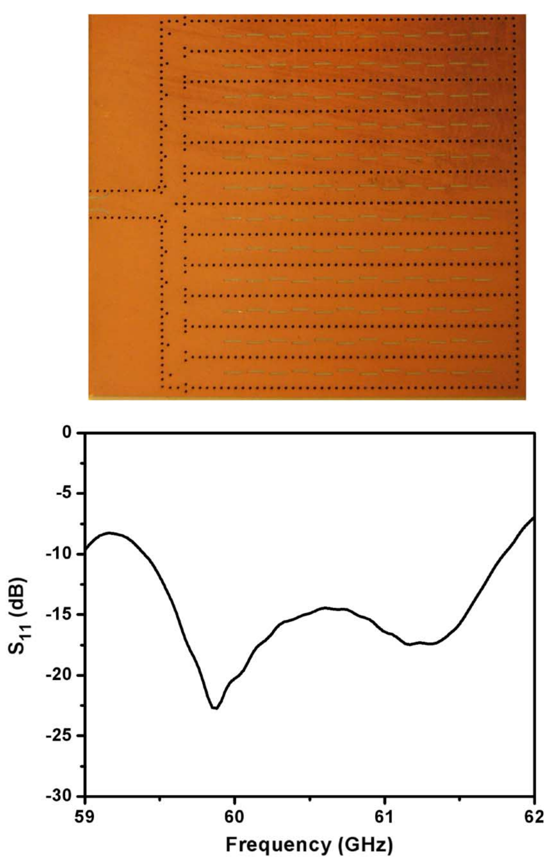
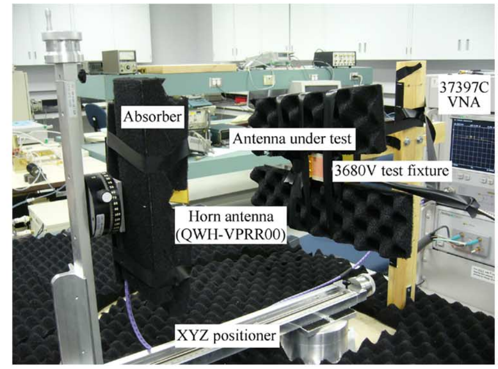
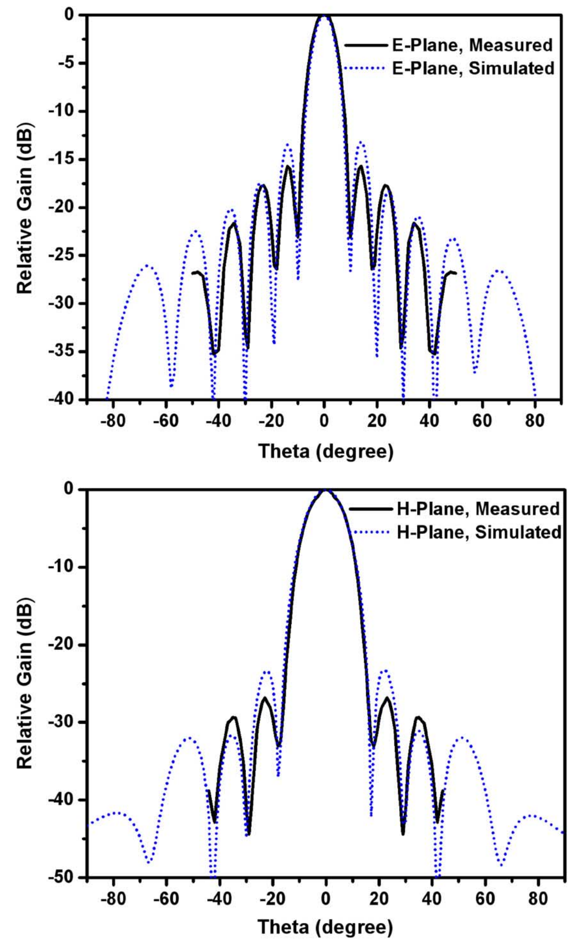


Fig. 4. Photograph and measured reflection coefficient of the proposed antenna.

between 50-Ω CBCPW and SIW. Usually, the slots in the CBCPW and transition structure should be placed on the opposite side to reduce the spurious radiation. In this work, the CBCPW slots are etched on the same side as the radiating slots to facilitate measurements. For the design of T-junctions, the size of coupling post-wall window is determined by the power dividing ratio while the position of metalized via hole is used to obtain good input matching. The adjacent radiating SIWs are spaced by a half guided wavelength in the feeding SIW. Therefore, the radiating SIWs are excited with alternating-phase of 180 degree by an incident travelling wave from the input port. Finally, the overall feeding network is analyzed and optimized to compensate the mutual coupling effect from adjacent discontinuities. Fig. 3(b) depicts the simulated frequency characteristics of the overall feeding network. Over the simulation frequency band, the magnitude difference of the



(a)



(b)

Fig. 5. (a) Experimental setup, (b) simulated and measured radiation patterns in both E-plane and H-Plane at 60.5 GHz.

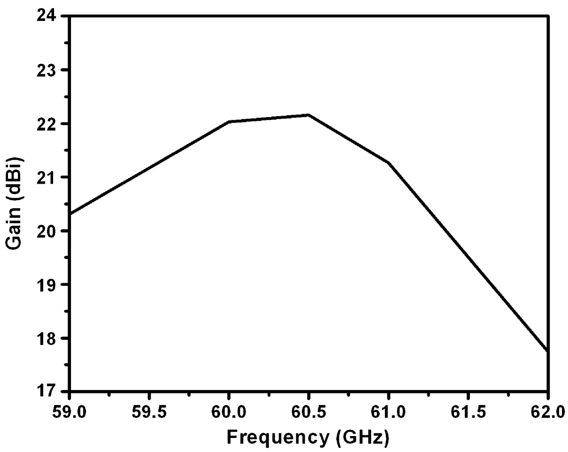


Fig. 6. Gain at different frequency points for the proposed antenna.

input power between adjacent radiating SIWs is smaller than 0.5 dB, while the input reflection of the feeding network is better than 18 dB. The phase difference of the input power between adjacent radiating SIWs is within the range of 180 $\pm$ 15 degree over the simulation frequency band, which may reduce the gain bandwidth of the SIW slot array antenna.

III. Fabrication and Measurement

The proposed antenna array was implemented by using linear arrays of metallized via hole having the diameter of 0.3 mm and the center-to-center pitch of 0.6 mm, which can be made with our laboratory's standard PCB process. The photograph of the developed antenna is displayed in Fig. 4. Anritsu 37397C vector network analyzer and Anritsu Wiltron 3680 V test fixture are used to measure the reflection coefficient that is depicted in Fig. 4. The measured bandwidth for 10 dB return loss is 2.5 GHz from 59.3 GHz to 61.8 GHz. Fig. 5 shows the experimental setup for the measurement of radiation patterns, and the measured and simulated E-plane and H-plane patterns which very well agree with each other. Due to the restriction of absorbers surrounding the antenna under test, the measurement was operated in the range from -50 degree to 50 degree. The measured side lobe level is better than 15 dB in the E-plane while better than 26 dB in the H-Plane. The gain shown in Fig. 6 was calculated from the Friis transmission equation for different frequency points. The maximum gain is about 22 dBi, which corresponds to the efficiency of about 68% estimated from the gain and directivity.

IV. Conclusion

Planar antenna array based on the substrate integrated waveguide (SIW) scheme is designed and realized on a standard dielectric substrate by a low cost PCB process. Simulated and measured results show that the proposed antenna has good efficiency and side lobe level, and it can be used as a potential candidate for 60-GHz-band applications at low cost.

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