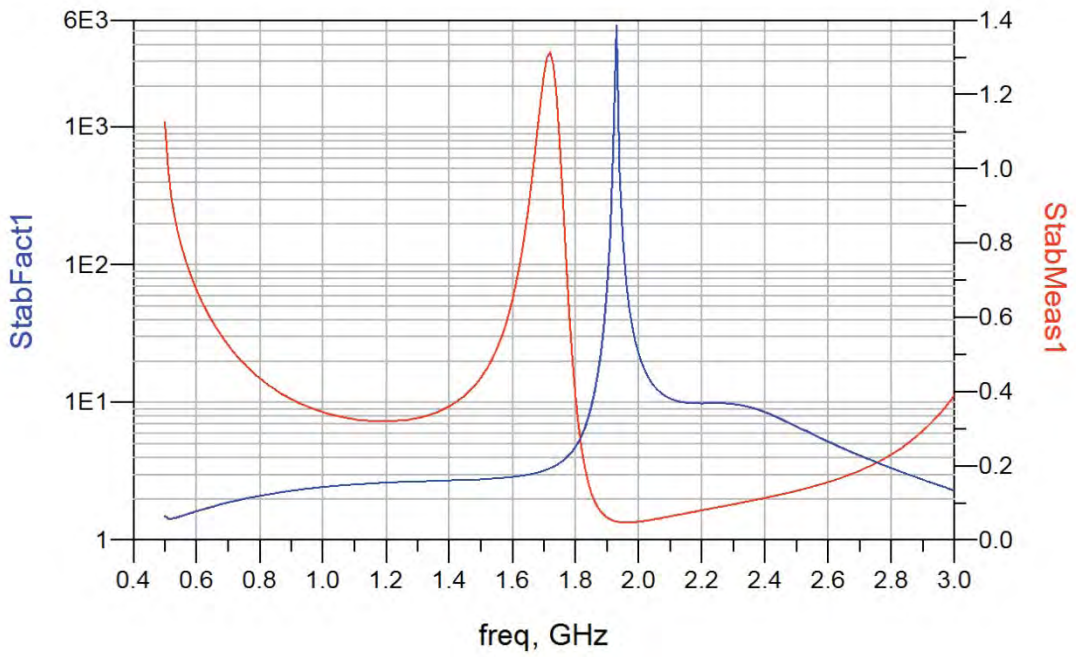


In the graph shown here, stability factor is plotted on the left-Y axis with log scale and Stability Measure is plotted on the right-Y axis. It can be seen Stability Factor is more than 1 and Stability Measure is greater than 0 over the entire frequency range hence our device is stable with the help of stability resistors inside subnetwork and we can begin our actual PA analysis as outlined in next few sections.

Step 4: Load Pull Analysis

Load Pull is a very commonly used and preferred analysis for PA design applications. Load Pull is the technique during which we keep source impedance and source power is kept constant at certain level and then sweep impedance / reflection coefficient of load over certain section in smith chart to characterize Output Power, PAE, IMD (with 2-tone LoadPull) etc to find out our optimum impedance to be presented to device and then accordingly perform impedance matching network design.

Critical things to determine while performing Load Pull simulation are:

a. Which section of the Smith Chart to use for load impedance?
b. What source impedance to keep while performing load pull simulations?
c. How much should be the source power for load pull simulation?

Now there are no straight answers to these questions but one can follow simple guidelines as given here to work through them in an iterative manner before final Load Pull analysis.

Tip 1: How to select area in Smith Chart for Load Pull?

For finding out which section of smith chart is to be used can be obtained from device datasheet which sometime can provide certain information or one can decide to define a section and then go around various parts in Smith Chart to finalize the optimum location. Usually power devices work at lower impedances so sections near periphery are the best guess to start with and designers can start to divide Smith on four quadrants and work their way to reach right area to zoom in and perform load pull simulations.

Tip 2: What Source Impedance to keep during Load Pull?

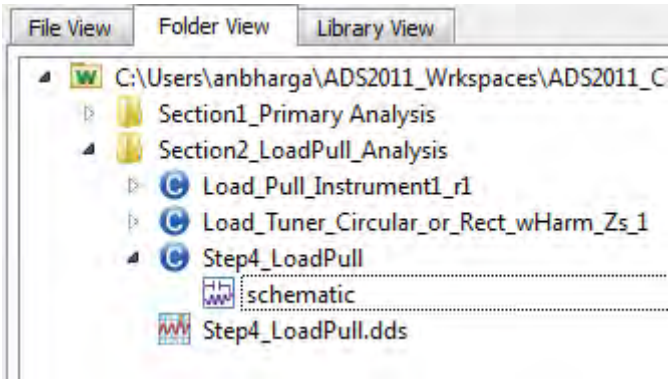
Usually power devices have lower impedances so keeping source impedance as 5 or 10 Ohms offers good starting point for a designer and then this can be tweaked to arrive at good number. After successful load pull simulation ADS provides pretty good estimate of optimum source impedance or designers can perform Source Pull Analysis to find optimum source impedance for maximum gain hence reducing the compression level while extracting required amount of output power from the device. For example, in our case we have used 10Ohm resistor in series with Gate hence we shall keep 15 Ohm as our starting point for Source Impedance during our LoadPull simulations.

Tip 3: How much should be the Source Power for Load Pull Analysis?

Good estimate of the source power to be kept can come from the device datasheet which provides the gain of the device at certain frequency. Good way to calculate required input power required is by formula = **(output power required – gain as mentioned in datasheet) + 3dB** and then it can be reduced or increased in couple of iterations and final value of source power can be decided.

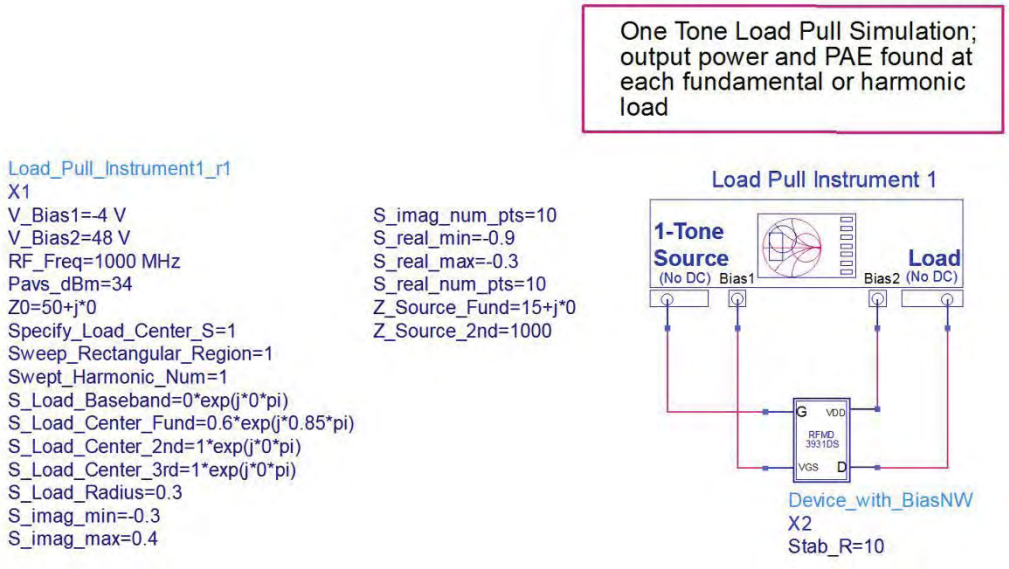
Load Pull Simulation for our Amplifier:

1. Click on **Designguide->LoadPull->One Tone, Constant Available Source Power Load Pull** and this shall copy few schematics and one data display onto the workspace tree….rename HB1Tone_LoadPull to **Step4_LoadPull** and HB1Tone_LoadPull.dds to **Step4_LoadPull.dds** as shown here

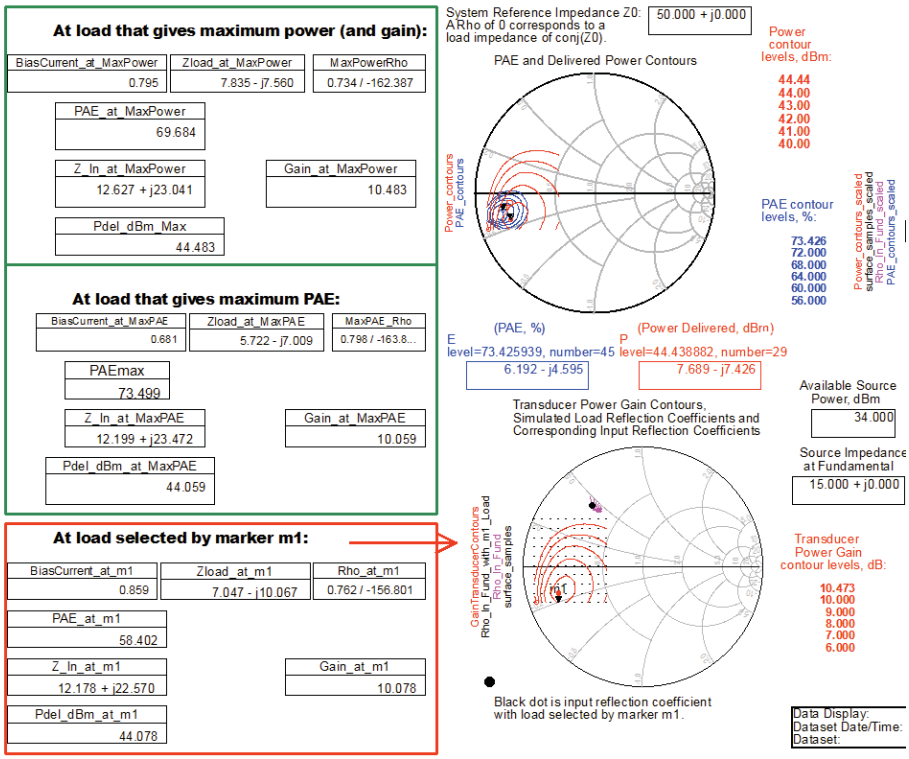


2. Open the schematic of Step4_LoadPull and you shall see a LoadPull instrument with a default device, delete the device and its connections and drag and drop “Device_with_BiasNW” onto this schematic and change **Stab_R = 10** and make connections to the Load Pull Instrument. Make following changes on the parameters by double clicking on the LoadPull Instrument:
    a. V_Bias1 = -4 V
    b. V_Bias2 = 48 V
    c. RF_Freq = 1000 MHz
    d. Pavs_dBm = 34
    e. S_imag_min = -0.3
    f. S_imag_max = 0.4
    g. S_imag_num_pts=10
    h. S_real_min = -0.9
    i. S_real_max = -0.3
    j. S_real_num_pts = 10
    k. Z_Source_Fund = 15+j*0

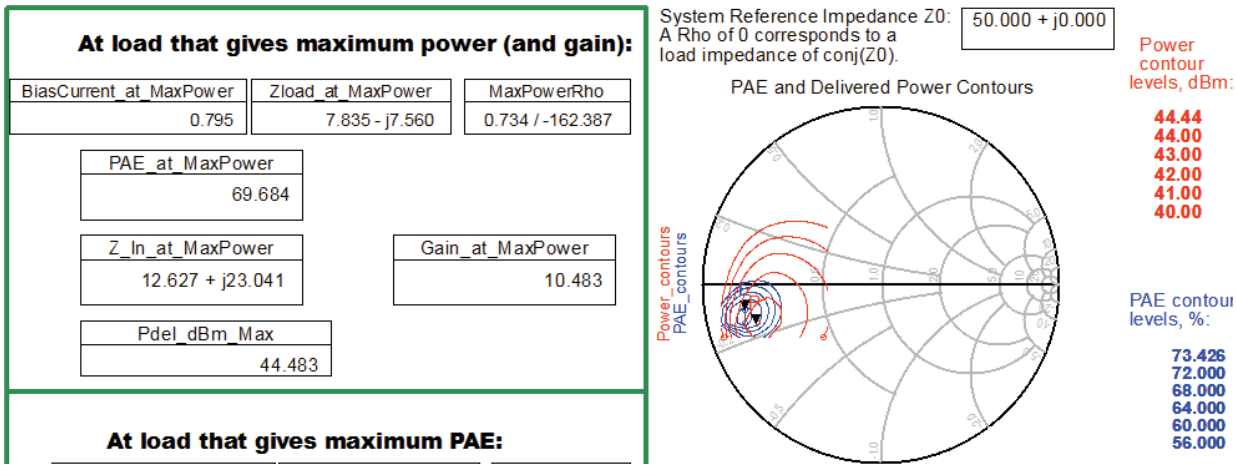
Once finished schematic will look as shown here:



Perform simulation by clicking on Simulate icon or press F7. Observe the data display which provides all the useful information



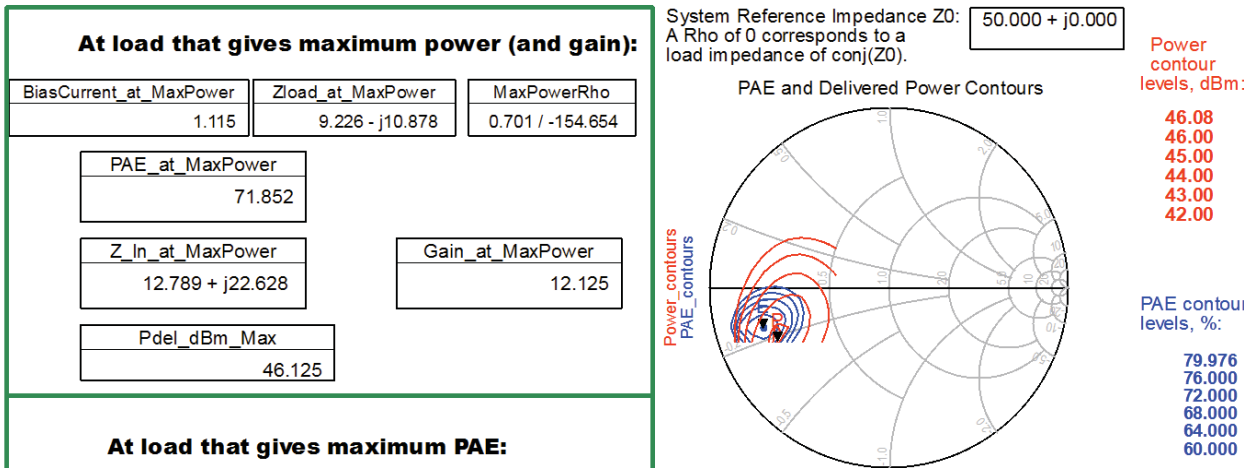
Zoom to the section which shows **"At load that gives maximum power (and gain)"**



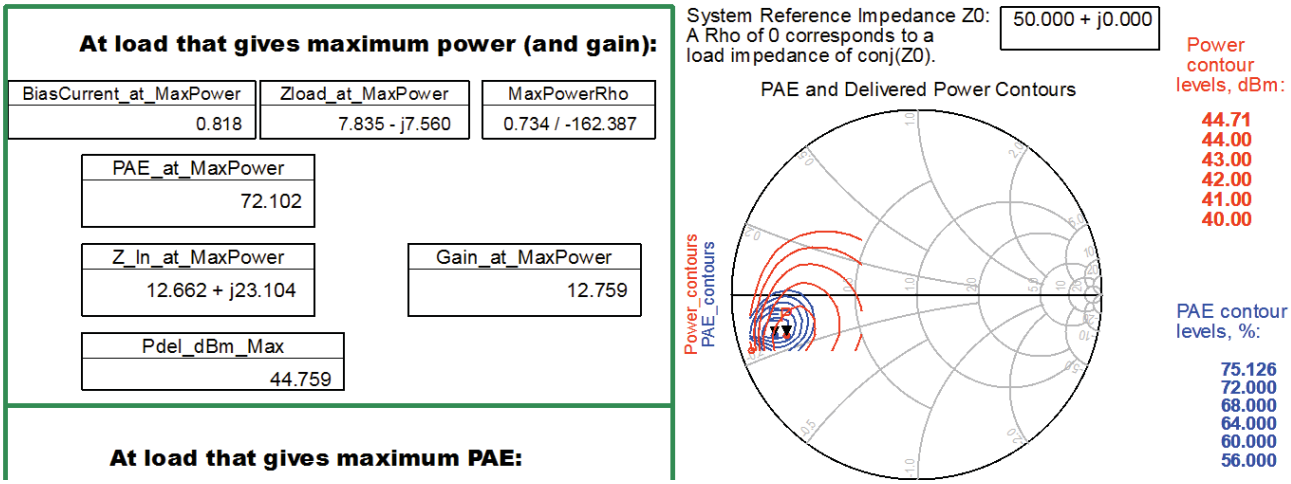
Notice that we are able to achieve the required output power of 44dBm (25Watts) but gain seems to be lower than what is mentioned in the datasheet which should be more than 12 or so and that is because we have not yet terminated source in its optimum impedance for maximizing the gain. We can note the optimum load impedance which is shown as 7.835-j*7.56 Ohm and if we match our device to this load impedance we shall obtain 44dBm of output power.

Go to schematic and modify the Z_Source_Fund = 12.6 –j*23 (complex conjugate) as predicted by Load Pull simulation which is the right termination for the source. For more sophisticated simulation designers can use the Source Pull template provided in Load Pull designguide whereby we shall terminate the load using the impedance of 7.835-j*7.56 and then vary the source impedance to find out the termination which provides the maximum gain from the device. For this exercise we shall use the source impedance as computed by the load pull simulation.

Perform load pull simulation again and observe the Pdel_dBm_Max and Gain_at_MaxPower as shown below



We can observe that the output power has risen to 46dBm and Gain has gone up to 12dB indicating that we can reduce the input power level by 2dB or so to achieve 44 dBm output power. Modify the source power Pavs_dBm to 32 and resimulate the design and observe the data display to note that we obtain output power of 44.75 dBm and Gain of 12.75 with a PAE = 72%



Take away from our Load Pull analysis:

Input Source Power = 32dBm
Input Impedance = 12.6 + j*23 Ohm
Output Impedance = 7.835 –j*7.56 Ohm

Step 5: Impedance Matching Network Design

ADS offers variety of choices to perform Impedance Matching network design and designers can choose any of the options as listed below:

a. Tools->Smith Chart: This allows users to perform Lumped Element and transmission line based matching network design using an interactive Smith Chart tool.
b. Tools->Impedance Matching: This is smart component based impedance matching network synthesis which also allows users to perform broadband based matching network using Lowpass, Highpass or Bandpass topologies. Default synthesized network is always lumped components and using the lumped to transmission line transformation one can transform lumped components to equivalent transmission lines.
c. Designguide->Passive Circuit: This designguide can be used to synthesize single stub or double stub transmission line based matching networks.

Output Matching Network Design:
For the present case of our Power Amplifier matching network, we shall use Smith Chart tool in ADS which provides greater control on the impedance matching network design.

1. Click on Tools->Smith Chart to see a pop up window of Smith Chart opening up.