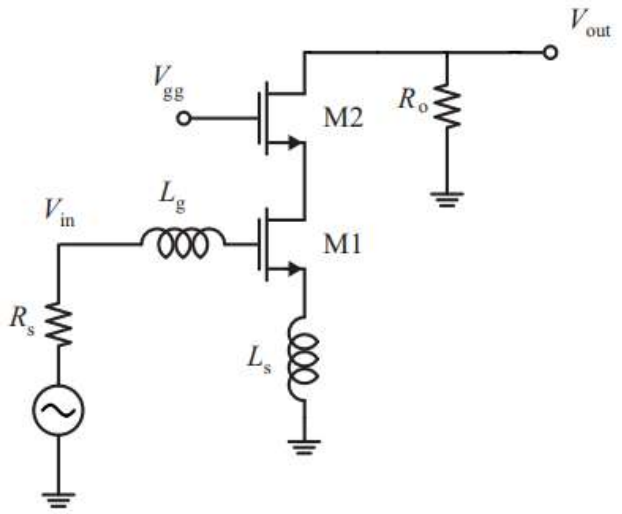
1. Show your design computation and schematic.

- The cascode inductor source degeneration was chosen because it has the most advantages that outweigh the disadvantages. The basic schematic of the topology is seen below.

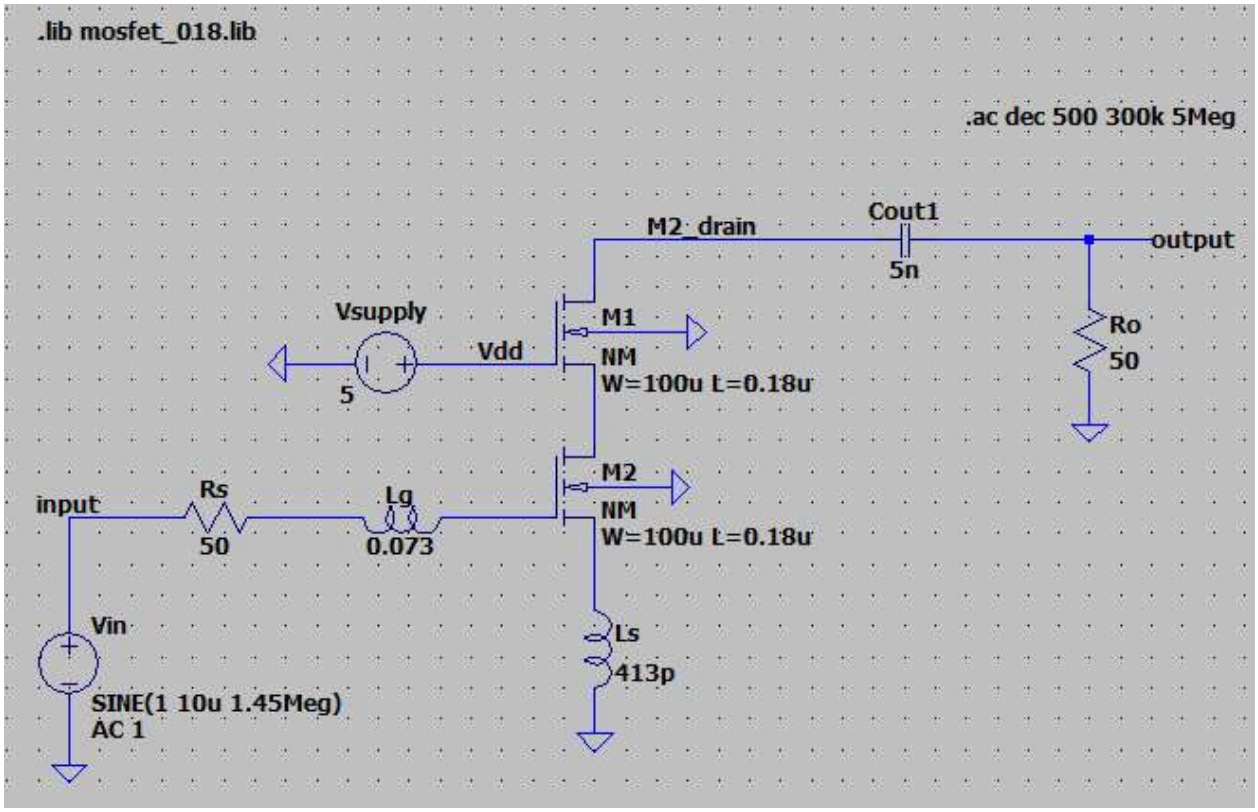


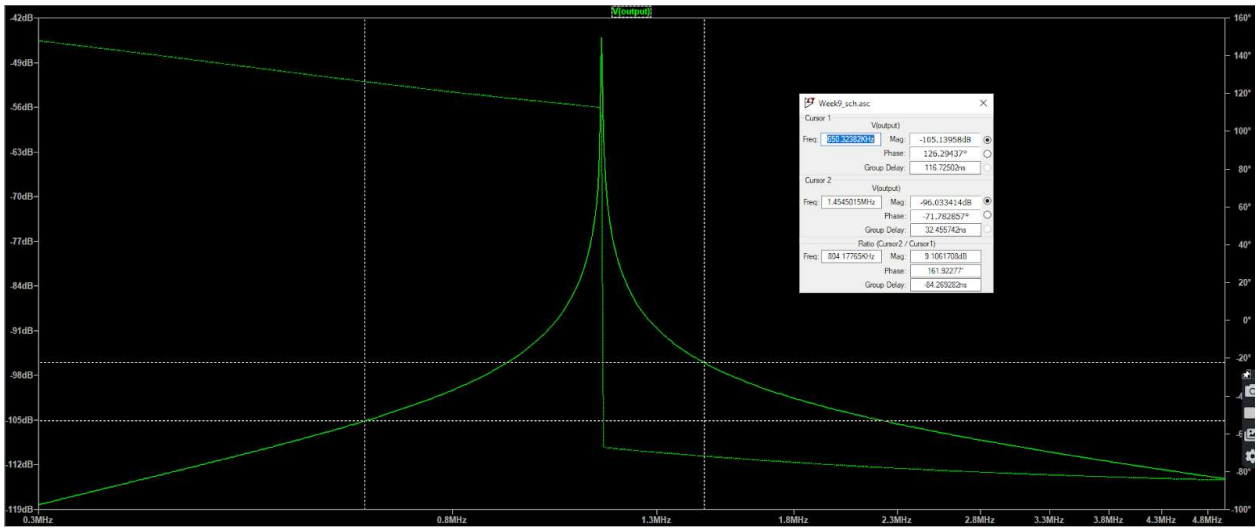
- The CMOS parameters were first computed. This design is based on a 180nm CMOS technology. Assuming $I_{bias} = 1mA$, $V_{D,SAT} = 100mV$, and $K_n' = 380\mu A/V^2$:
  - $(W/L)_{in} = \frac{2I_{bias}}{K_n'(V_{D,SAT})^2} = \frac{2\times 1mA}{380\mu A/V^2 \times 100mV^2} \approx 550$
  - From this computed ratio, it can be approximated that $(W/L)_{in} = \frac{100\mu}{0.18\mu}$, where $W = 100\mu m$ and $L = 0.18\mu m$
  - To compute for the capacitances of the device:
    - $C_{gs} \approx \frac{2}{3} C_{OX} \times W \times L = \frac{2}{3} \times 8.58fF/\mu m^2 \times 100\mu m \times 0.18\mu m \approx 105fF$
    - $C_{ds} \approx 0.3fF/\mu m^2 \times 100\mu m = 30fF$
    - $C = C_{gs} + 2C_{ds} = 165fF$
- First order estimation of inductor values. Assuming $g_m = 20ms$:
  - Real part of impedance $50\Omega = g_m \frac{L_s}{C}$
  - Isolate from above $L_s = \frac{50\Omega \times C}{g_m} = \frac{50\Omega \times 165fF}{20ms} = 413pF$
  - Calculate L_g from operating frequency

$$f_o = 1.45MHz = \frac{1}{2\pi\sqrt{(L_g+L_s)C}} = \frac{1}{2\pi\sqrt{(L_g+412.5pF)165fF}}$$

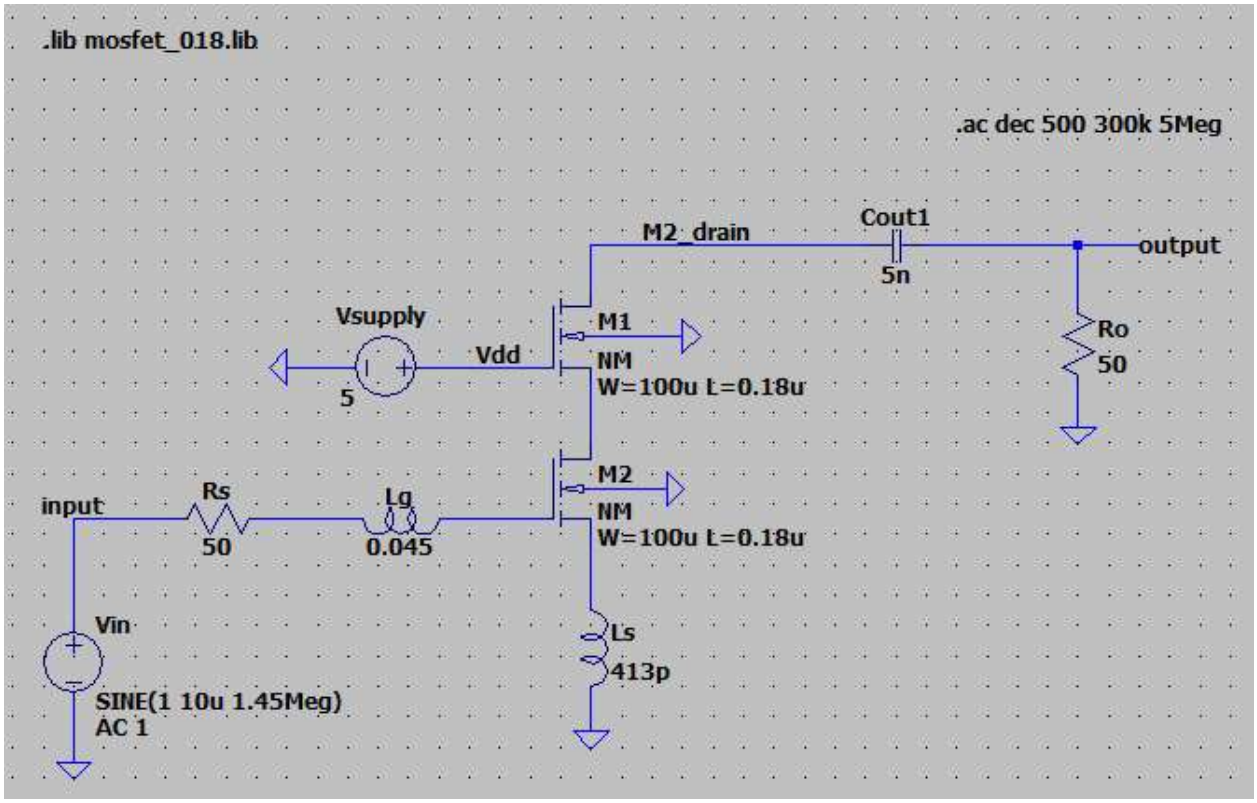
    - Isolate and solve $L_g \approx 0.073\ F$

- Using the CMOS parameters $W = 100\mu m$ and , and inductances $L_s = 413pF$ and $L_g \approx 0.073\ F$, the LTSpice simulation and schematic looks like:





- The desired response is slightly off from the frequency band we need. This might be due to approximation errors. So the value of L_g was adjusted until the peak is around 1.45MHz, which resulted in the final value $L_g \approx 0.045\ F$.
- The **final schematic** looks like this:



AC Analysis