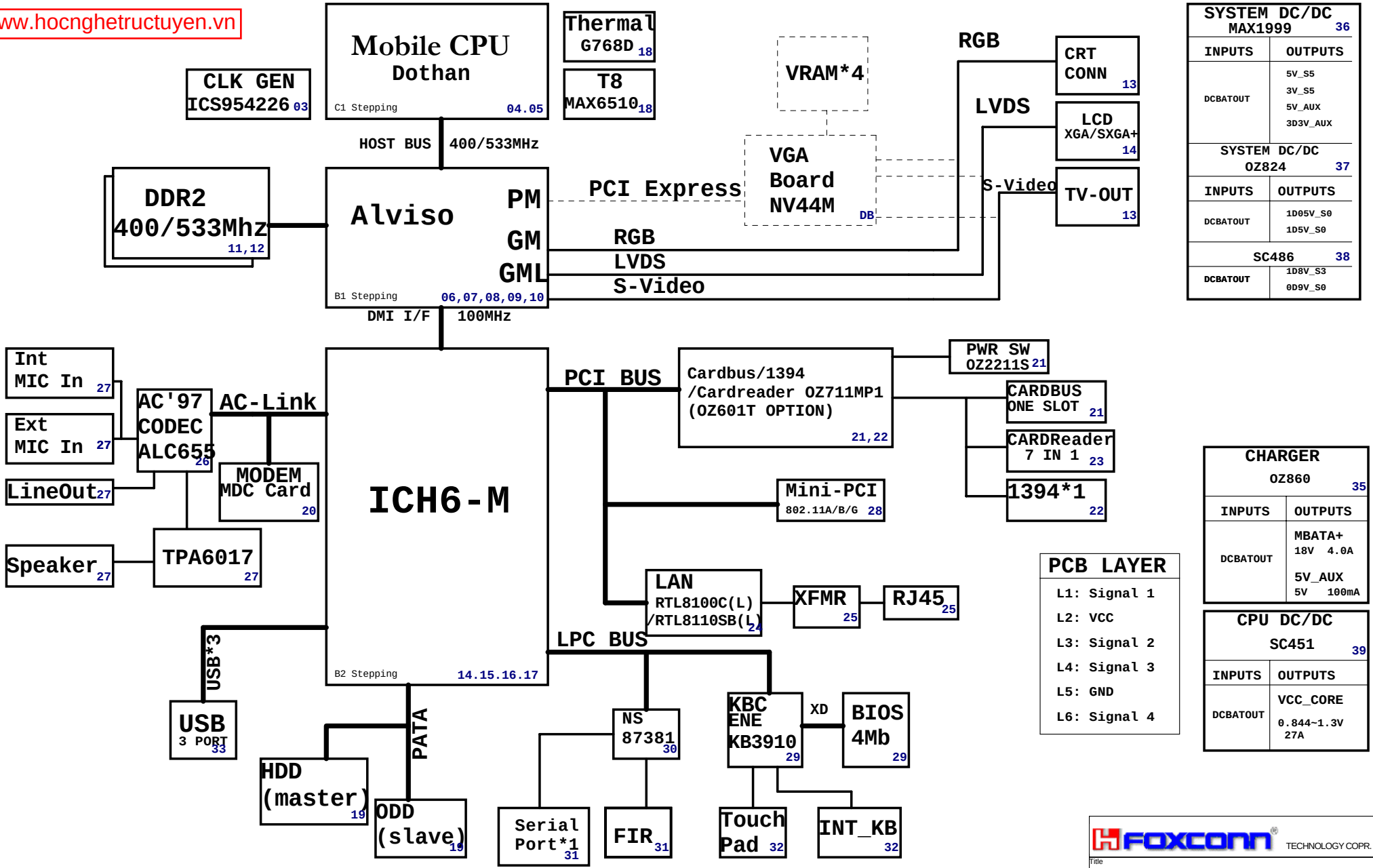
S06/S07 System Block Diagram



SYSTEM DC/DC MAX1999 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 5V_AUX 3D3V_AUX

SYSTEM DC/DC OZ824 37	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S0

SC486 38	
DCBATOUT	1D8V_S3 0D9V_S0

CHARGER OZ860 35	
INPUTS	OUTPUTS
DCBATOUT	MBATA+ 18V 4.0A 5V_AUX 5V 100mA

CPU DC/DC SC451 39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER
L1: Signal 1
L2: VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

FOXCONN TECHNOLOGY COPR.

Title: Block Diagram

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 1 of 45

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 101 = FSB400 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	**0 = DDR II** (Default) 1 = DDR I
CFG7	CPU Strap	0= Reserved **1=Dothan** (Default)
CFG8	Reversed	
CFG9	PCI Express Graphics Lane reverse option for layout convenience	0=Reverse Lanes 1=Normal Operation (Default)
CFG10	Reversed	
CFG11	Reversed	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVO CRTL_DATA	SDVO Present	**0 = No SDVO device present (Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

KBC Hardware Strap

PinNumber	PinName	Function
125	A1	High:Enable the internal pull-up resistors on XIOCS [F:0] pins Low:Disable the internal pull-up resistors on XIOCS [F:0]
128	A4	High: Diasble DMPP(Recommended) Low : Enable DMPP
131	A5	High:Enable EMWB(Recommended for application using shared BIOS Low:Disable EMWB
11	GPIO05	High:Test Mode Low:32KHz clock in normal running(Recommend)
12	GPIO06	High:Test Mode(KSOUT0~15 become DPLL internal data outputs, KSO16 becomes internal power-on reset output Low:Normal operation(Recommended)
105	GPIO20	High:Normal operation(Recommended) Low:Enable ISP mode during which the RD#,WR#,MEMSEL#,A[20:0] andD[7:0}will be controlled by ISP COntroller

ICS954226 Spread Spectrum Select

page 3

Byte 6b7	Byte 6b6	byte 6b5	Byte 6b4	Spread Mode	Spread Amount%	Pin17/18 Mhz	
1	0	0	0	Down	0.8	100	
1	0	0	1	Down	1.25	100	
1	0	1	0	Down	1.75	100	
1	0	1	1	Down	2.5	100	
1	1	0	0	Center	+-0.3	100	(Default)
1	1	0	1	Center	+-0.5	100	
1	1	1	0	Center	+-0.8	100	
1	1	1	1	Center	+-1.25	100	

PCI Routing

	IDSEL	IRQ	REQ/GNT
OZ711MP1 1394	25	E	0
MiniPCI	21	C	1
LAN	23	C	2

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 15851 1.5V1

EE_DIN,EE_DOUT, GNT[3:0] GNT[4]#/GPO[48], GNT[5]#/GPO[17], GNT[6]#/GPO[16], GPIO[25] LAD[3:0]#/FB[3:0]#, LAN_RXD[2:0], LDRQ[0], LDRQ[1]/GPI[41],PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
ACZ_BITCLK,ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSTP# DPRSLPVR, EE_CS, SPKR,	ICH6 internal 20K pull-downs
USB[7:0][P,N] SATALED#	ICH6 internal 15K pull-downs
DD[7], DDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

Super I/O (PC87381) Strapping Options

PinNumber	PinName	Function
2	BADDR	**Base Address.** No pull down(default) - the Index-Data pair at 164Eh-164Fh 10 K external pull-down resistor - the Index-Data pair at 2Eh-2Fh1
47	TRIS	**TRI-STATE Device** No pull-down resistor (default) - normal pin operation 10 K external pull-down resistor - floating device pins TRIS is set to 0 (by an external pull-down resistor), TEST must be 1
48	TEST	**XOR Tree Test Mode.** No pull-down resistor (default) - normal pin operation 10 K external pull-down resistor - pins configured as XOR tree. When TEST is set to 0 (by an external pull-down resistor), TRIS must be 1

FOXCONN TECHNOLOGY COPR.

Title: Table of content

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 2 of 45

ITP_EN 0=PCIEX_6 1=CPU_2_ITP
SS_SEL 0=LCDCLK 1=PCIEX/free running
3.3V PCI clock output

*internal Pull-Up resistors
**internal Pull-Down resistor

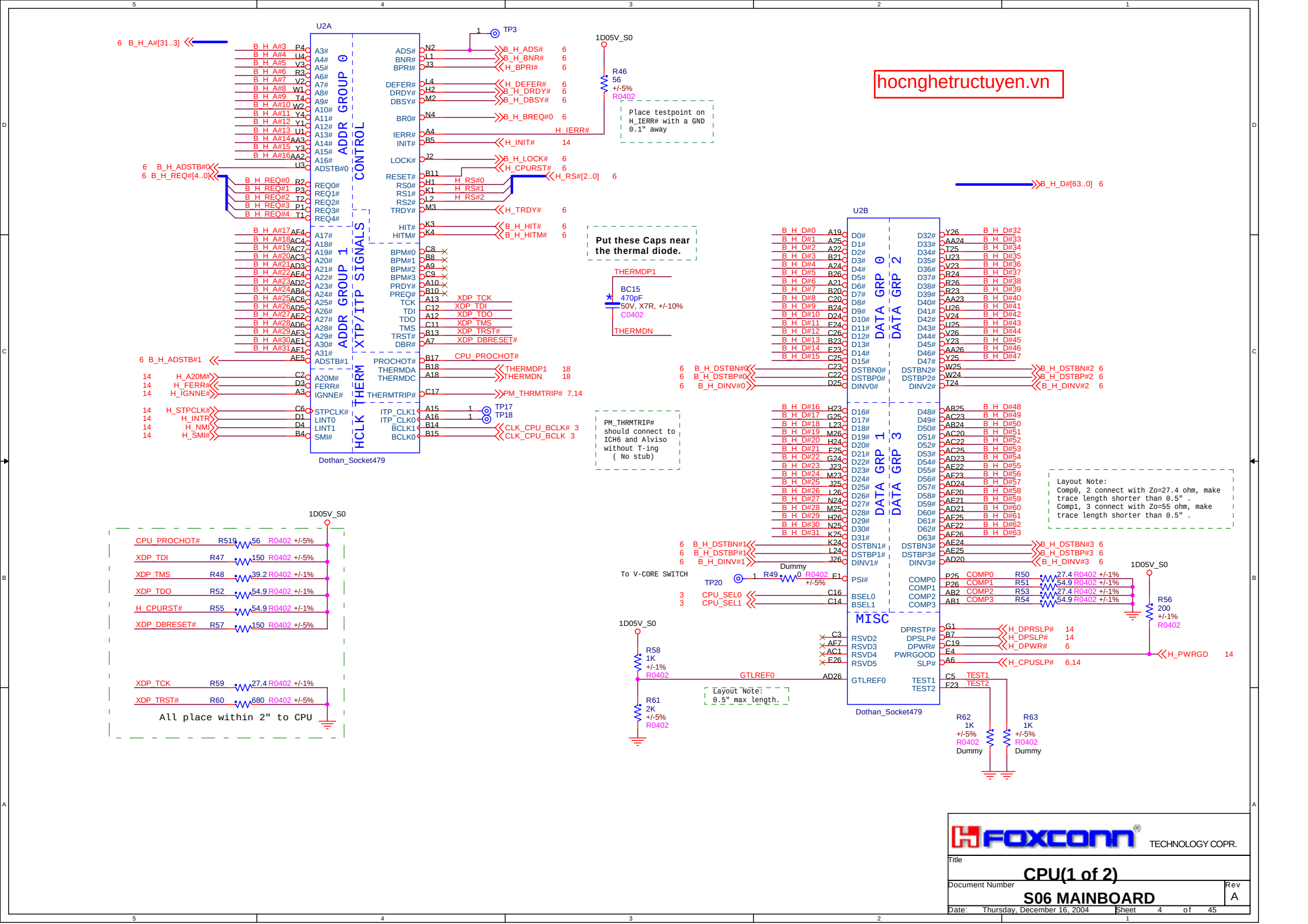
To external AC'97 CLK

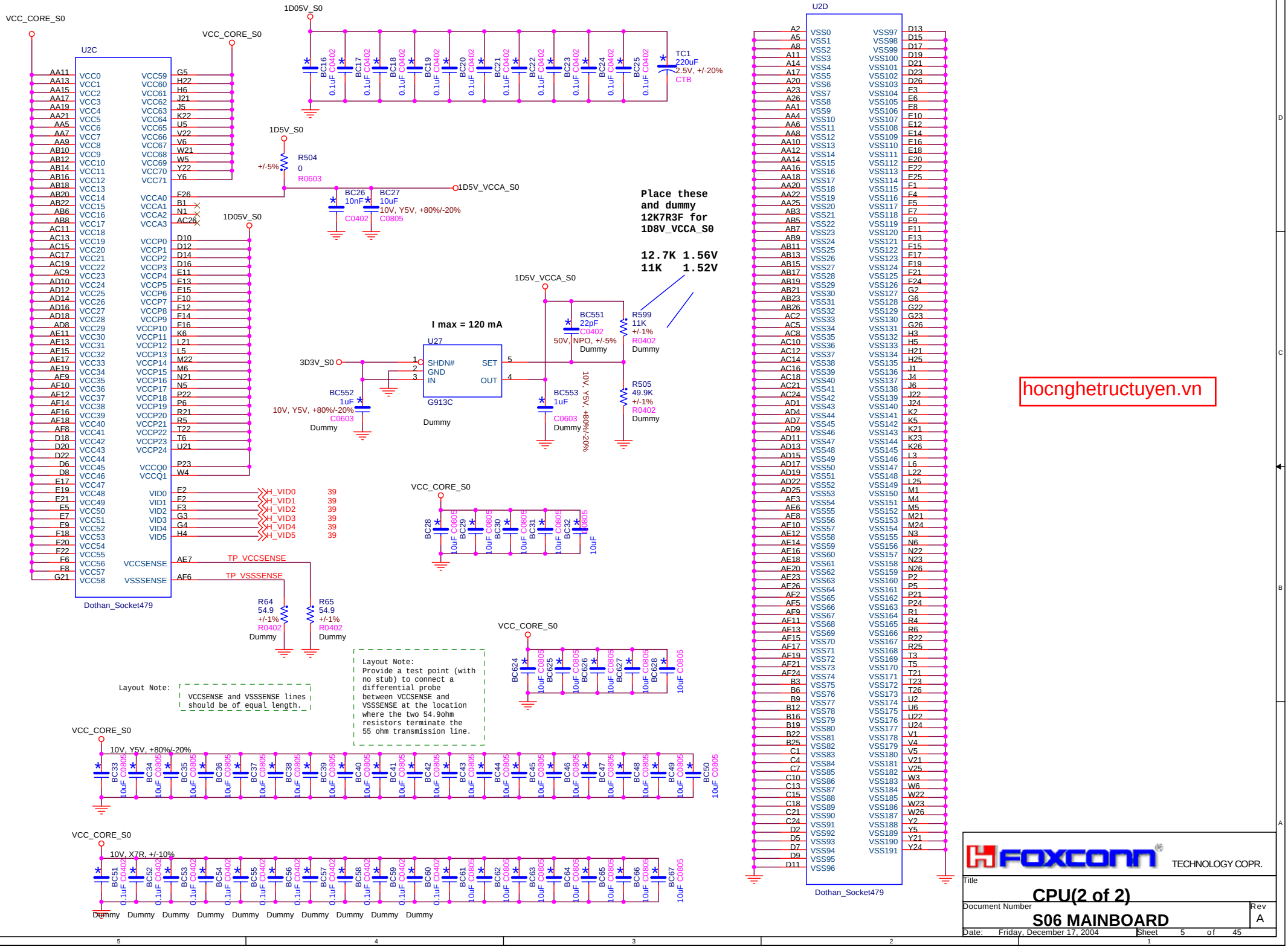
EMI capacitor

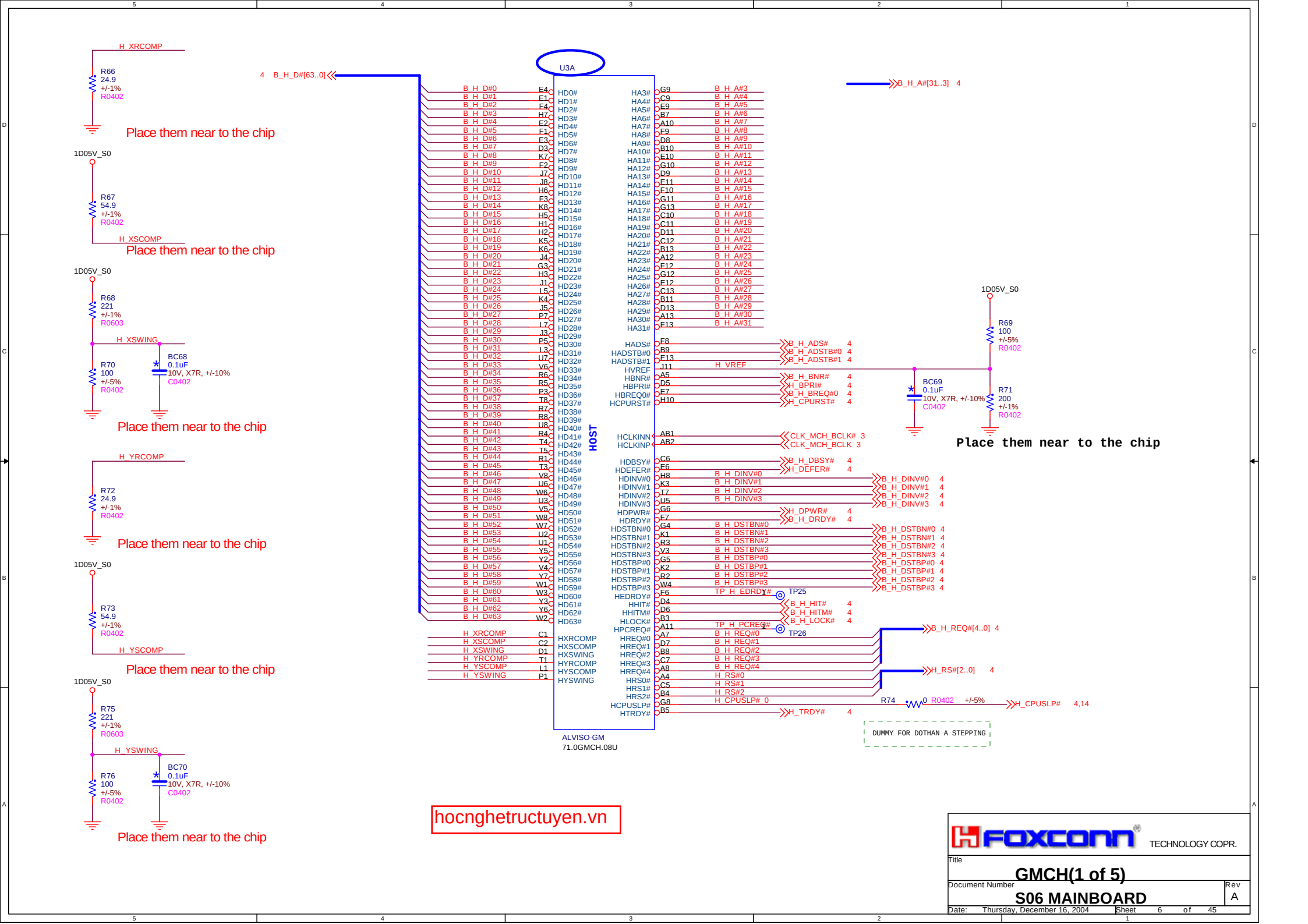
FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M (Default)
1	1	0	400M

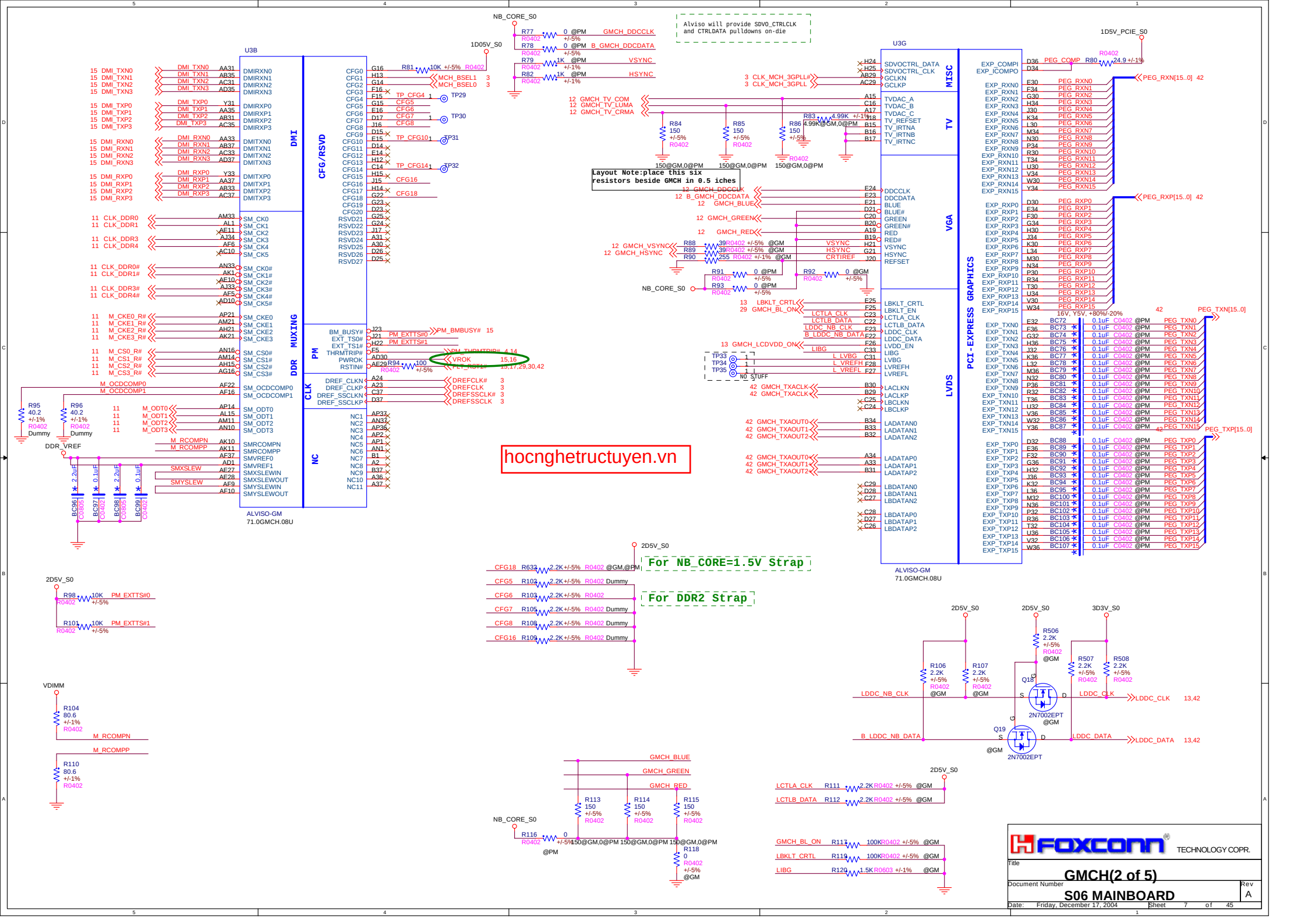
FOXCONN TECHNOLOGY COPR.

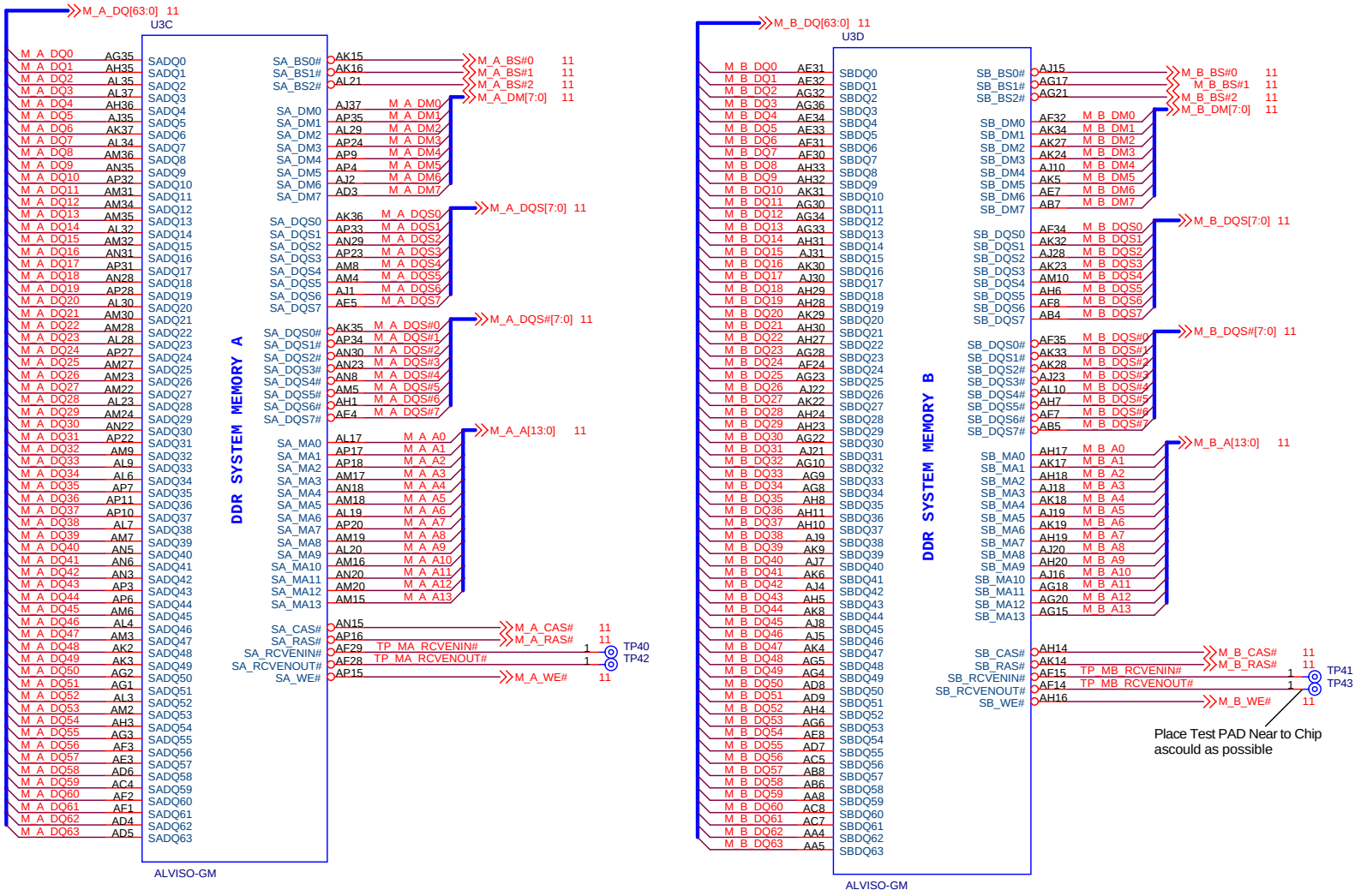
Title: Clock Generator
Document Number: S06 MAINBOARD
Rev: A
Date: Friday, December 17, 2004 Sheet 3 of 45


U2A
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
HCLK THERM CONTROL
Dothan_Socket479
U2B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Dothan_Socket479
hocnghetructuyen.vn
Place testpoint on H_IERR# with a GND 0.1" away
Put these Caps near the thermal diode.
THERMDP1
BC15
470pF
50V, X7R, +/-10%
C0402
THERMDN
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
To V-CORE SWITCH
Dummy
Layout Note: 0.5" max length.
All place within 2" to CPU
1D05V_S0
TECHNOLOGY COPR.
Title
CPU(1 of 2)
Document Number
S06 MAINBOARD
Rev
A
Date: Thursday, December 16, 2004
Sheet 4 of 45


U2C
Dothan_Socket479
U2D
Dothan_Socket479
U27
G913C
SHDN#
GND
IN
SET
OUT
1D05V_S0
VCC_CORE_S0
1D05V_VCCA_S0
3D3V_S0
R504
0
R0603
+/-5%
BC26
10nF
C0402
BC27
10uF
10V, Y5V, +80%/-20%
C0805
Place these
and dummy
12K7R3F for
1D8V_VCCA_S0
12.7K 1.56V
11K 1.52V
I max = 120 mA
BC551
22pF
C0402
50V, NPO, +/-5%
Dummy
R599
11K
+/-1%
R0402
Dummy
BC552
1uF
10V, Y5V, +80%/-20%
C0603
Dummy
BC553
1uF
10V, Y5V, +80%/-20%
C0603
Dummy
R505
49.9K
+/-1%
R0402
Dummy
TC1
220uF
2.5V, +/-20%
CTB
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
39
TP_VCCSENSE
TP_VSSSENSE
R64
54.9
+/-1%
R0402
Dummy
R65
54.9
+/-1%
R0402
Dummy
Layout Note:
VCCSENSE and VSSSENSE lines
should be of equal length.
Layout Note:
Provide a test point (with
no stub) to connect a
differential probe
between VCCSENSE and
VSSSENSE at the location
where the two 54.9ohm
resistors terminate the
55 ohm transmission line.
10V, Y5V, +80%/-20%
10V, X7R, +/-10%
Dummy
hocnghetructuyen.vn
FOXCONN
TECHNOLOGY COPR.
Title
CPU(2 of 2)
Document Number
S06 MAINBOARD
Rev
A
Date: Friday, December 17, 2004
Sheet 5 of 45


H_XRCOMP
R66
24.9
+/-1%
R0402
Place them near to the chip
1D05V_S0
R67
54.9
+/-1%
R0402
H_XSCOMP
Place them near to the chip
1D05V_S0
R68
221
+/-1%
R0603
H_XSWING
R70
100
+/-5%
R0402
BC68
0.1uF
10V, X7R, +/-10%
C0402
Place them near to the chip
H_YRCOMP
R72
24.9
+/-1%
R0402
Place them near to the chip
1D05V_S0
R73
54.9
+/-1%
R0402
H_YSCOMP
Place them near to the chip
1D05V_S0
R75
221
+/-1%
R0603
H_YSWING
R76
100
+/-5%
R0402
BC70
0.1uF
10V, X7R, +/-10%
C0402
Place them near to the chip
4 B_H_D#[63..0]
U3A
HOST
B_H_D#0 E4
B_H_D#1 E1
B_H_D#2 F4
B_H_D#3 H7
B_H_D#4 E2
B_H_D#5 F1
B_H_D#6 E3
B_H_D#7 D3
B_H_D#8 K7
B_H_D#9 F2
B_H_D#10 J7
B_H_D#11 J8
B_H_D#12 H6
B_H_D#13 F3
B_H_D#14 K8
B_H_D#15 H5
B_H_D#16 H1
B_H_D#17 H2
B_H_D#18 K5
B_H_D#19 K6
B_H_D#20 J4
B_H_D#21 G3
B_H_D#22 H3
B_H_D#23 J1
B_H_D#24 L5
B_H_D#25 K4
B_H_D#26 J5
B_H_D#27 P7
B_H_D#28 L7
B_H_D#29 J3
B_H_D#30 P5
B_H_D#31 L3
B_H_D#32 U7
B_H_D#33 V6
B_H_D#34 R6
B_H_D#35 R5
B_H_D#36 P3
B_H_D#37 T8
B_H_D#38 R7
B_H_D#39 R8
B_H_D#40 U8
B_H_D#41 R4
B_H_D#42 T4
B_H_D#43 T5
B_H_D#44 R1
B_H_D#45 T3
B_H_D#46 V8
B_H_D#47 U6
B_H_D#48 W6
B_H_D#49 U3
B_H_D#50 V5
B_H_D#51 W8
B_H_D#52 W7
B_H_D#53 U2
B_H_D#54 U1
B_H_D#55 Y5
B_H_D#56 Y2
B_H_D#57 V4
B_H_D#58 Y7
B_H_D#59 W1
B_H_D#60 W3
B_H_D#61 Y3
B_H_D#62 Y6
B_H_D#63 W2
HD0# HD1# HD2# HD3# HD4# HD5# HD6# HD7# HD8# HD9# HD10# HD11# HD12# HD13# HD14# HD15# HD16# HD17# HD18# HD19# HD20# HD21# HD22# HD23# HD24# HD25# HD26# HD27# HD28# HD29# HD30# HD31# HD32# HD33# HD34# HD35# HD36# HD37# HD38# HD39# HD40# HD41# HD42# HD43# HD44# HD45# HD46# HD47# HD48# HD49# HD50# HD51# HD52# HD53# HD54# HD55# HD56# HD57# HD58# HD59# HD60# HD61# HD62# HD63#
H_XRCOMP C1
H_XSCOMP C2
H_XSWING D1
H_YRCOMP T1
H_YSCOMP L1
H_YSWING P1
HXRCOMP HXSCOMP HXSWING HYRCOMP HYSCOMP HYSWING
ALVISO-GM
71.0GMCH.08U
HA3# G9 B_H_A#3
HA4# C9 B_H_A#4
HA5# E9 B_H_A#5
HA6# B7 B_H_A#6
HA7# A10 B_H_A#7
HA8# F9 B_H_A#8
HA9# D8 B_H_A#9
HA10# B10 B_H_A#10
HA11# E10 B_H_A#11
HA12# G10 B_H_A#12
HA13# D9 B_H_A#13
HA14# E11 B_H_A#14
HA15# F10 B_H_A#15
HA16# G11 B_H_A#16
HA17# G13 B_H_A#17
HA18# C10 B_H_A#18
HA19# C11 B_H_A#19
HA20# D11 B_H_A#20
HA21# C12 B_H_A#21
HA22# B13 B_H_A#22
HA23# A12 B_H_A#23
HA24# F12 B_H_A#24
HA25# G12 B_H_A#25
HA26# E12 B_H_A#26
HA27# C13 B_H_A#27
HA28# B11 B_H_A#28
HA29# D13 B_H_A#29
HA30# A13 B_H_A#30
HA31# F13 B_H_A#31
B_H_A#[31..3] 4
HADS# F8 B_H_ADS# 4
HADSTB#0 B9 B_H_ADSTB#0 4
HADSTB#1 E13 B_H_ADSTB#1 4
HVREF J11 H_VREF
HBNR# A5 B_H_BNR# 4
HBPRI# D5 H_BPRI# 4
HBREQ#0 E7 B_H_BREQ#0 4
HCPURST# H10 H_CPURST# 4
1D05V_S0
R69
100
+/-5%
R0402
BC69
0.1uF
10V, X7R, +/-10%
C0402
R71
200
+/-1%
R0402
Place them near to the chip
HCLKINN AB1 CLK_MCH_BCLK# 3
HCLKINP AB2 CLK_MCH_BCLK 3
HDBSY# C6 B_H_DBSY# 4
HDEFER# E6 H_DEFER# 4
HDINV#0 H8 B_H_DINV#0 B_H_DINV#0 4
HDINV#1 K3 B_H_DINV#1 B_H_DINV#1 4
HDINV#2 T7 B_H_DINV#2 B_H_DINV#2 4
HDINV#3 U5 B_H_DINV#3 B_H_DINV#3 4
HDPWR# G6 H_DPWR# 4
HDRDY# F7 B_H_DRDY# 4
HDSTBN#0 G4 B_H_DSTBN#0 B_H_DSTBN#0 4
HDSTBN#1 K1 B_H_DSTBN#1 B_H_DSTBN#1 4
HDSTBN#2 R3 B_H_DSTBN#2 B_H_DSTBN#2 4
HDSTBN#3 V3 B_H_DSTBN#3 B_H_DSTBN#3 4
HDSTBP#0 G5 B_H_DSTBP#0 B_H_DSTBP#0 4
HDSTBP#1 K2 B_H_DSTBP#1 B_H_DSTBP#1 4
HDSTBP#2 R2 B_H_DSTBP#2 B_H_DSTBP#2 4
HDSTBP#3 W4 B_H_DSTBP#3 B_H_DSTBP#3 4
HEDRDY# F6 TP_H_EDRDY# TP25
HHIT# D4 B_H_HIT# 4
HHITM# D6 B_H_HITM# 4
HLOCK# B3 B_H_LOCK# 4
HPCREQ# A11 TP_H_PCREQ# TP26
HREQ#0 A7 B_H_REQ#0 B_H_REQ#[4..0] 4
HREQ#1 D7 B_H_REQ#1
HREQ#2 B8 B_H_REQ#2
HREQ#3 C7 B_H_REQ#3
HREQ#4 A8 B_H_REQ#4
HRS0# A4 H_RS#0 H_RS#[2..0] 4
HRS1# C5 H_RS#1
HRS2# B4 H_RS#2
HCPUSLP# G8 H_CPUSLP# 0 R74 0 R0402 +/-5% H_CPUSLP# 4,14
HTRDY# B5 H_TRDY# 4
DUMMY FOR DOTHAN A STEPPING
hocnghetructuyen.vn
FOXCONN TECHNOLOGY COPR.
Title
GMCH(1 of 5)
Document Number
S06 MAINBOARD
Rev
A
Date: Thursday, December 16, 2004
Sheet 6 of 45


U3B
DMI
CFG/RSVD
MUXING
DDR
PM
CLK
NC
ALVISO-GM
71.0GMCH.08U
U3G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO-GM
71.0GMCH.08U
Alviso will provide SDVO_CTRLCLK
and CTRLDATA pulldowns on-die
Layout Note:place this six
resistors beside GMCH in 0.5 iches
hocnghetructuyen.vn
For NB_CORE=1.5V Strap
For DDR2 Strap
DDR_VREF
VDIMM
2N7002EPT
2N7002EPT
FOXCONN
TECHNOLOGY COPR.
Title
GMCH(2 of 5)
Document Number
S06 MAINBOARD
Rev
A
Date: Friday, December 17, 2004
Sheet 7 of 45



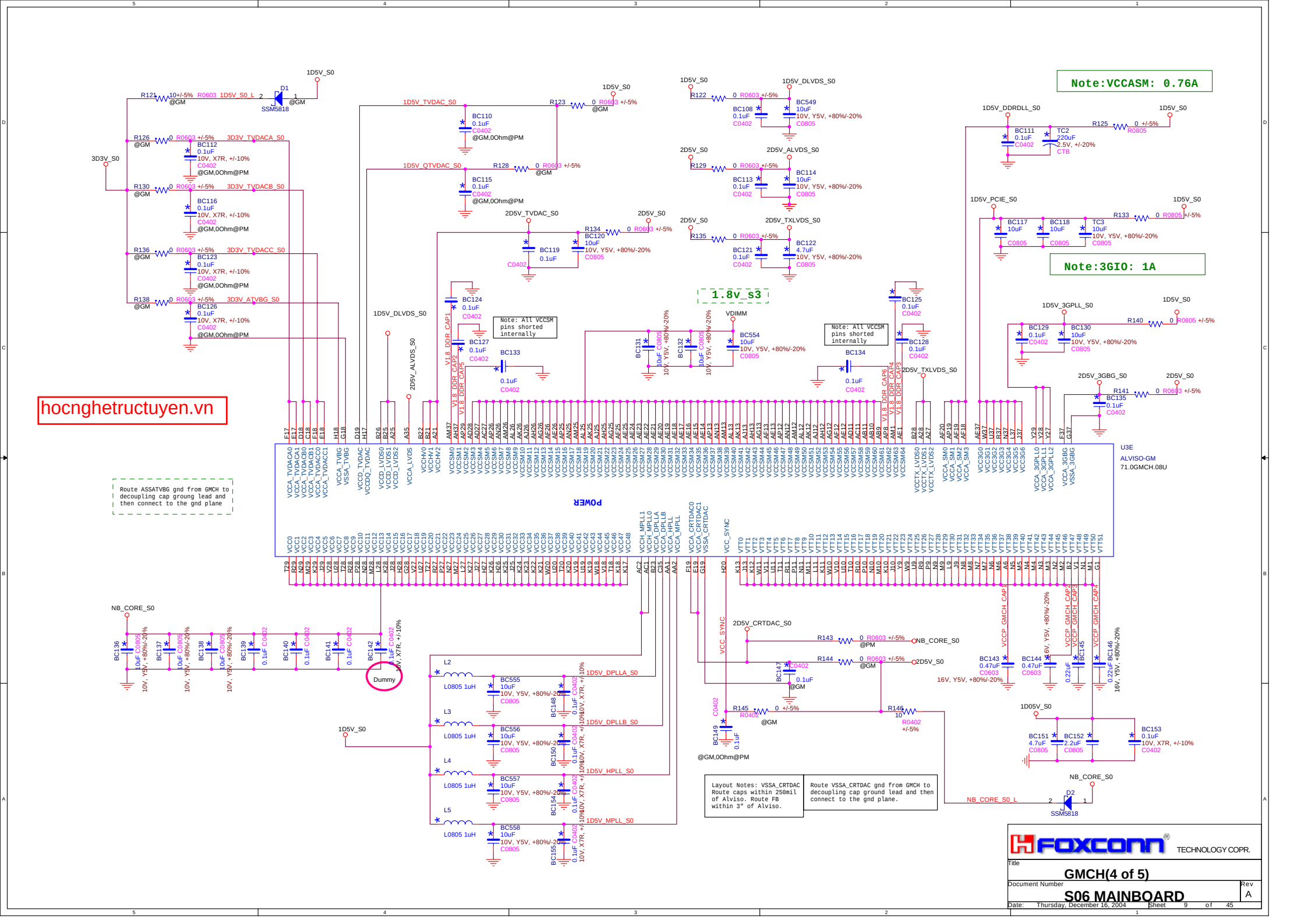
FOXCONN TECHNOLOGY COPR.

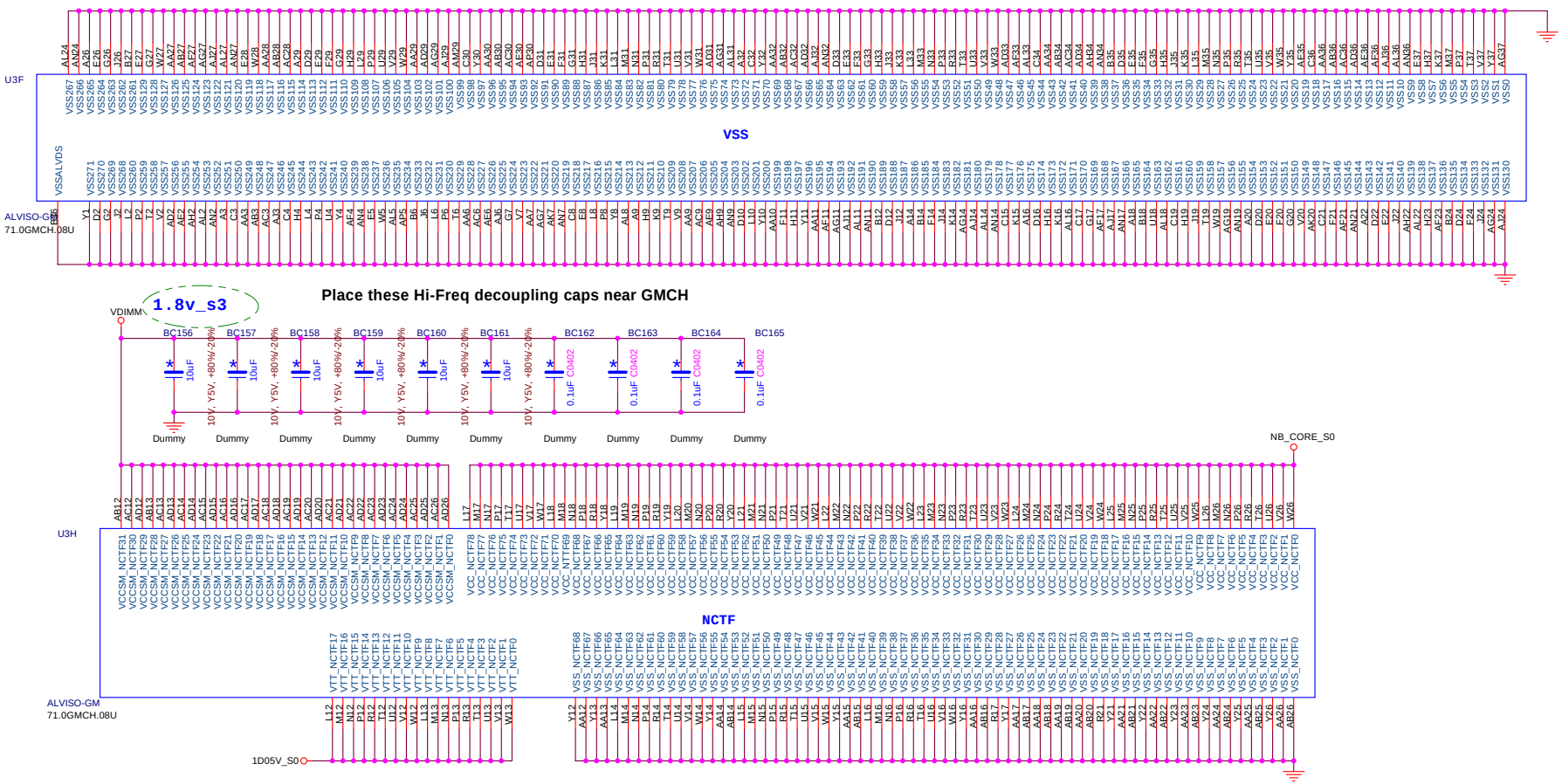
Title: GMCH(3 of 5)

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 8 of 45


Note:VCCASM: 0.76A
Note:3GIO: 1A
1.8v_S3
POWER
U3E
ALVISO-GM
71.0GMCH.08U
Note: All VCCSM pins shorted internally
Route ASSATVBG gnd from GMCH to decoupling cap grounge lead and then connect to the gnd plane
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
hocnghetructuyen.vn
FOXCONN TECHNOLOGY COPR.
Title
GMCH(4 of 5)
Document Number
S06 MAINBOARD
Rev
A
Date: Thursday, December 16, 2004
Sheet 9 of 45



GML: NB_CORE=1.05V
GM/PM: NB_CORE=1.5V

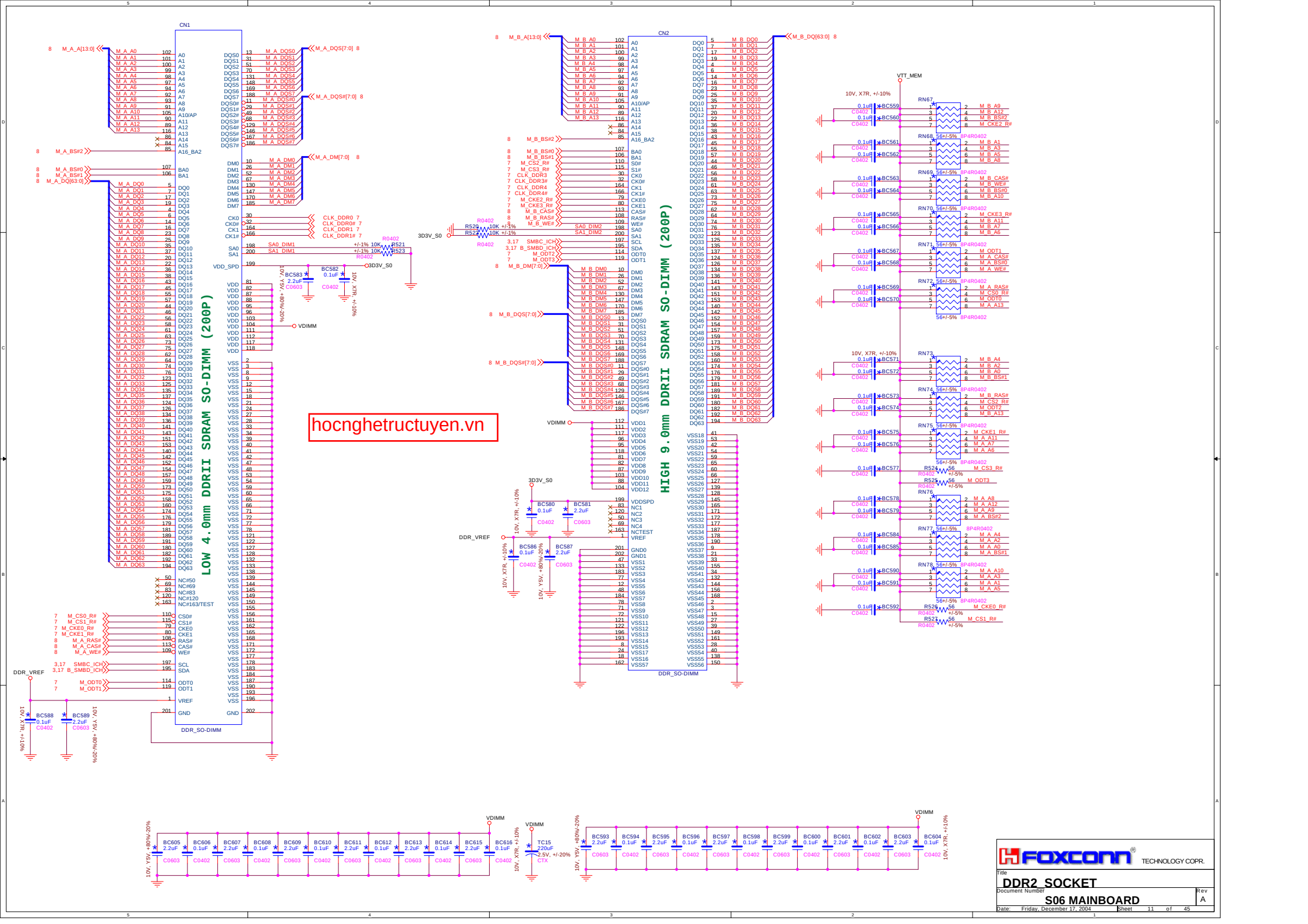
FOXCONN TECHNOLOGY COPR.

Title: GMCH(5 of 5)

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 10 of 45



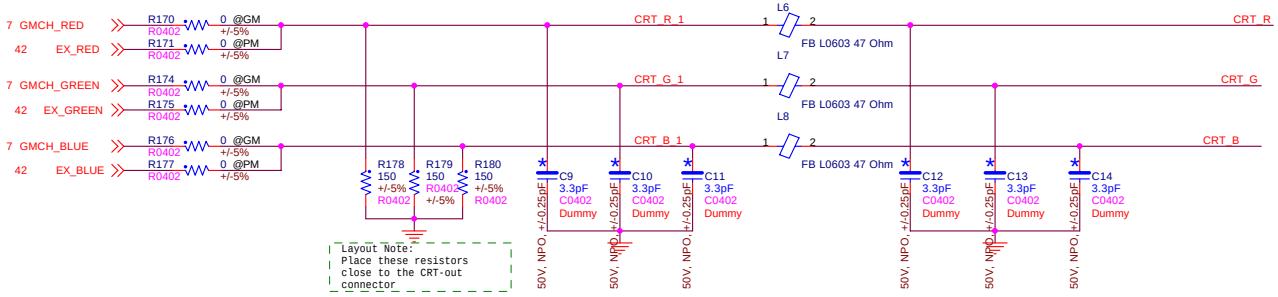
Title	DDR2 SOCKET
Document Number	S06 MAINBOARD
Rev	A
Date:	Friday, December 17, 2004
Sheet	11 of 45

FOXCONN TECHNOLOGY COPR.

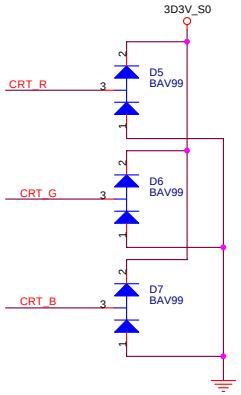
This page
Modified by Ke-Cheng 0923 am

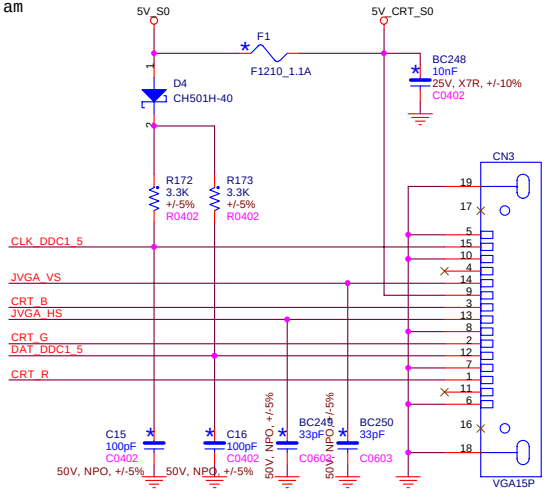
CRT I/F & CONNECTOR

Ferrite bead impedance: 47ohm@100MHz

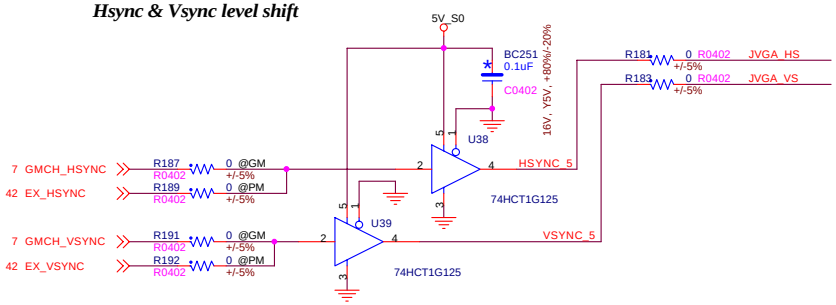


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



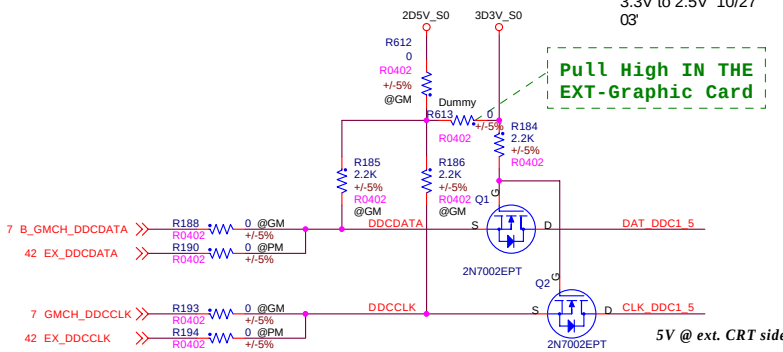


Hsync & Vsync level shift

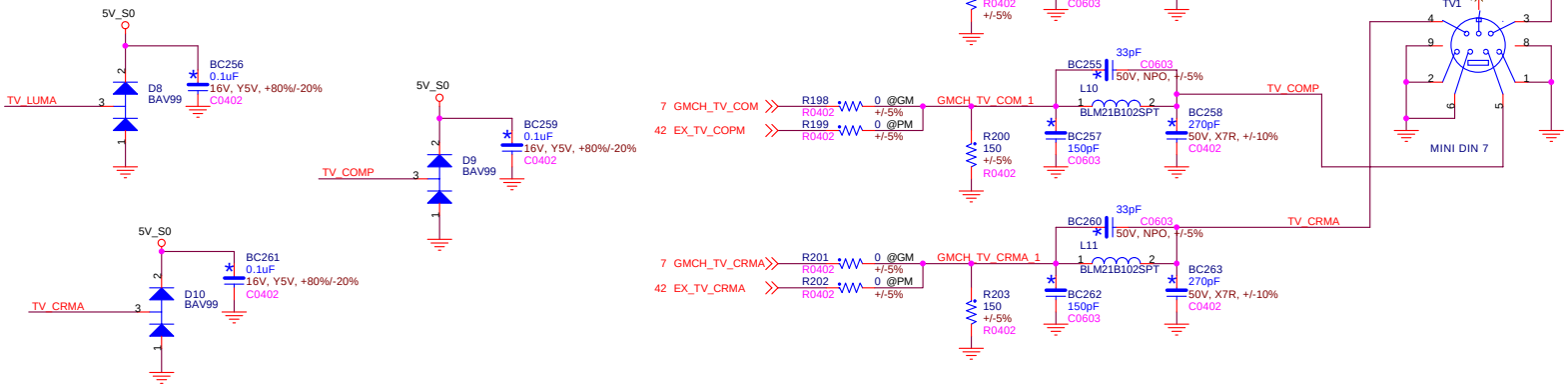


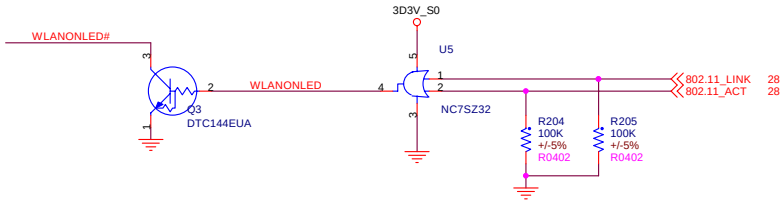
DDC_CLK & DATA level shift

Change VCC from 3.3V to 2.5V 10/27 03'

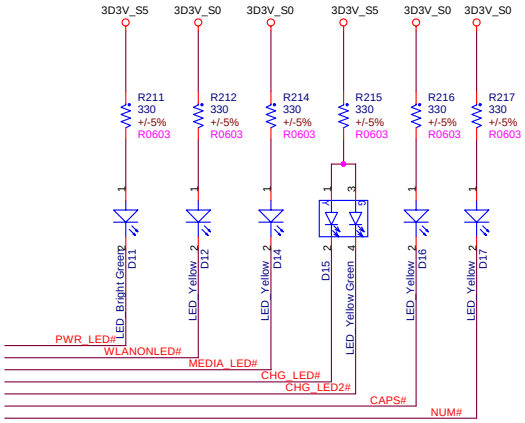


TV OUT CONN





LED

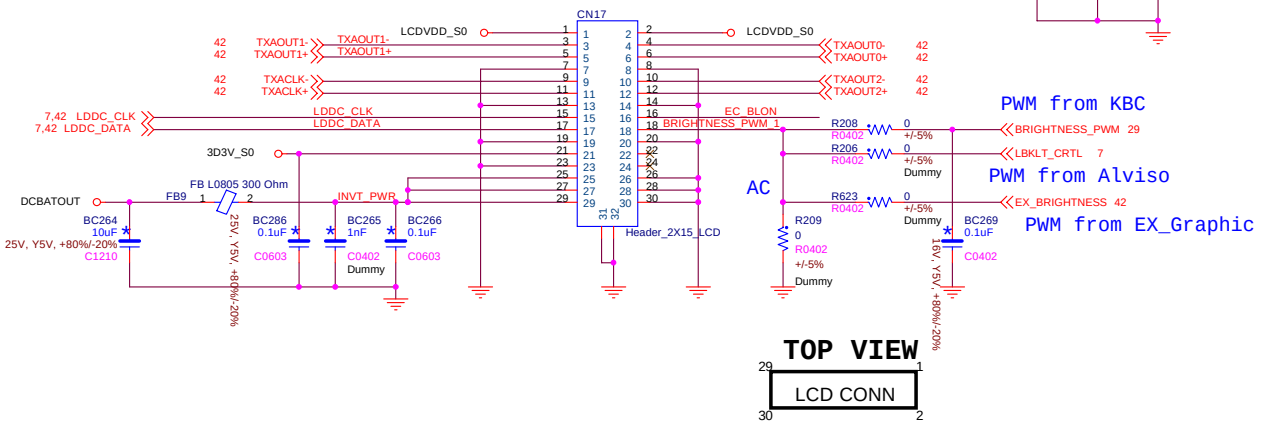


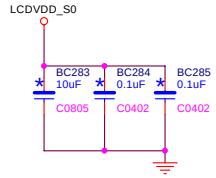
PWR: Green,KPT-1608SGC
CHG_LED#: Orang/Green KPTB-1615YSGC
Other: Yellow, KPT-1608YC

LED Status Table

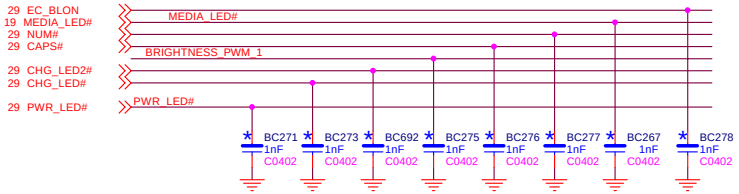
Power/Suspend LED	S0/S3				S4 Enter/Resume			
	Stay On(Green)				Need blinking			
Power LED	AC MODE				Battery Only			
	Full Charging	Discharging	Charging	Critical Low	Full Charging	Discharging	Charging	Critical Low
	Green	X	Orange	X	X	X	X	Orange Flash
Storage Access LED	Yellow							
Caps Lock LED	Yellow							
Number Lock LED	Yellow							
WirelessLAN LED	Yellow(Stay On when Enable)							

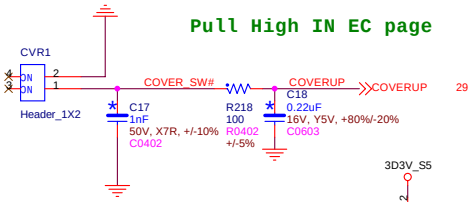
LCD / INVERTER

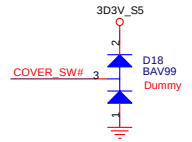


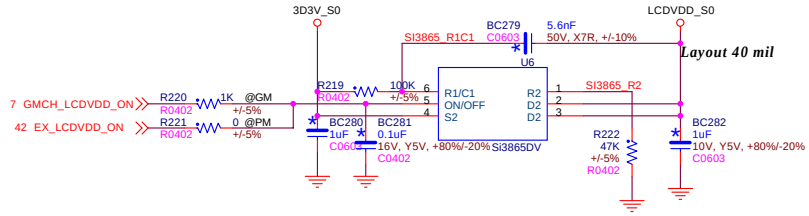


TOP VIEW









FOXCONN TECHNOLOGY COPR.

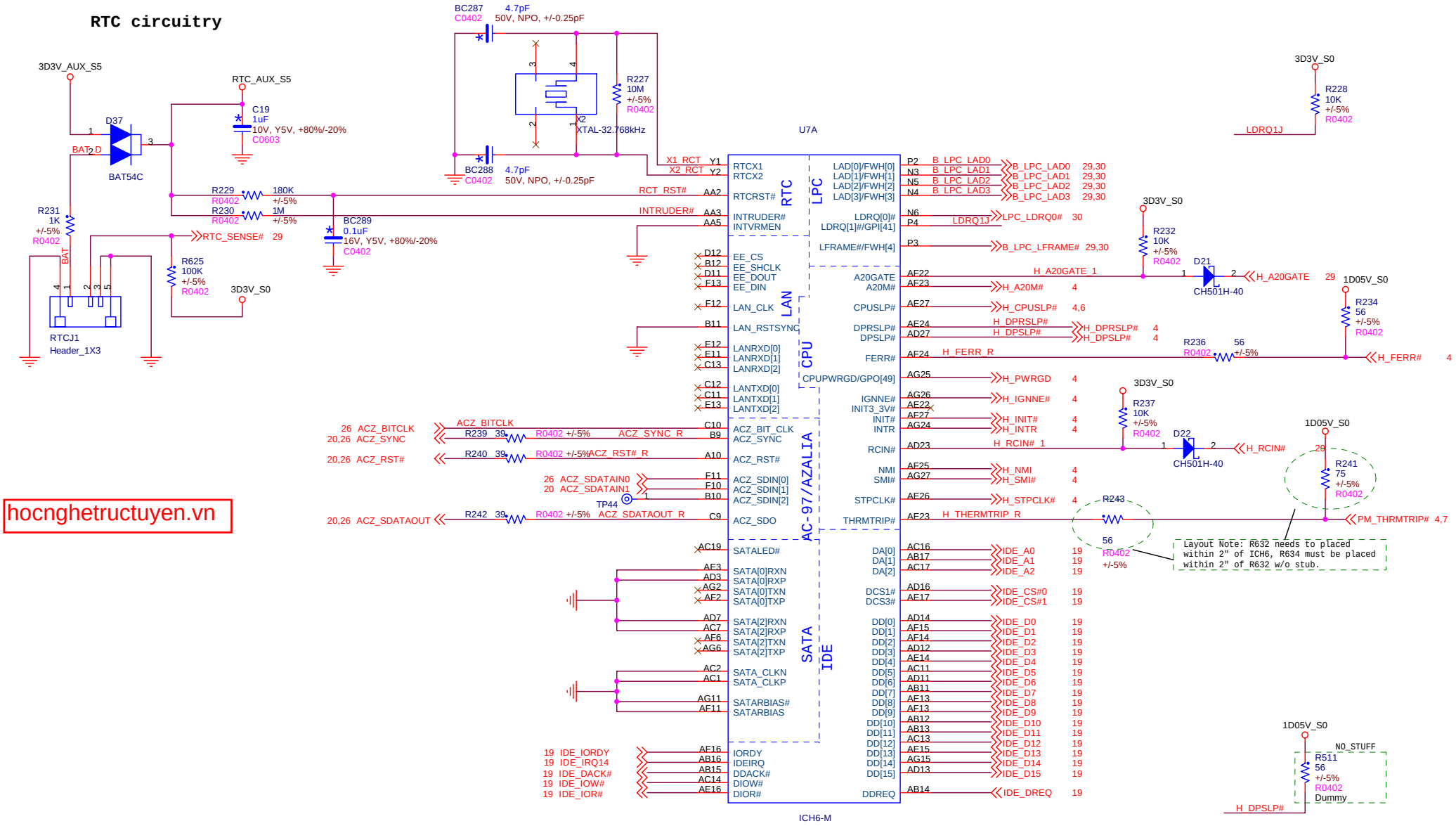
Title: LCD/Inverter

Document Number: S06 MAINBOARD

Rev: A

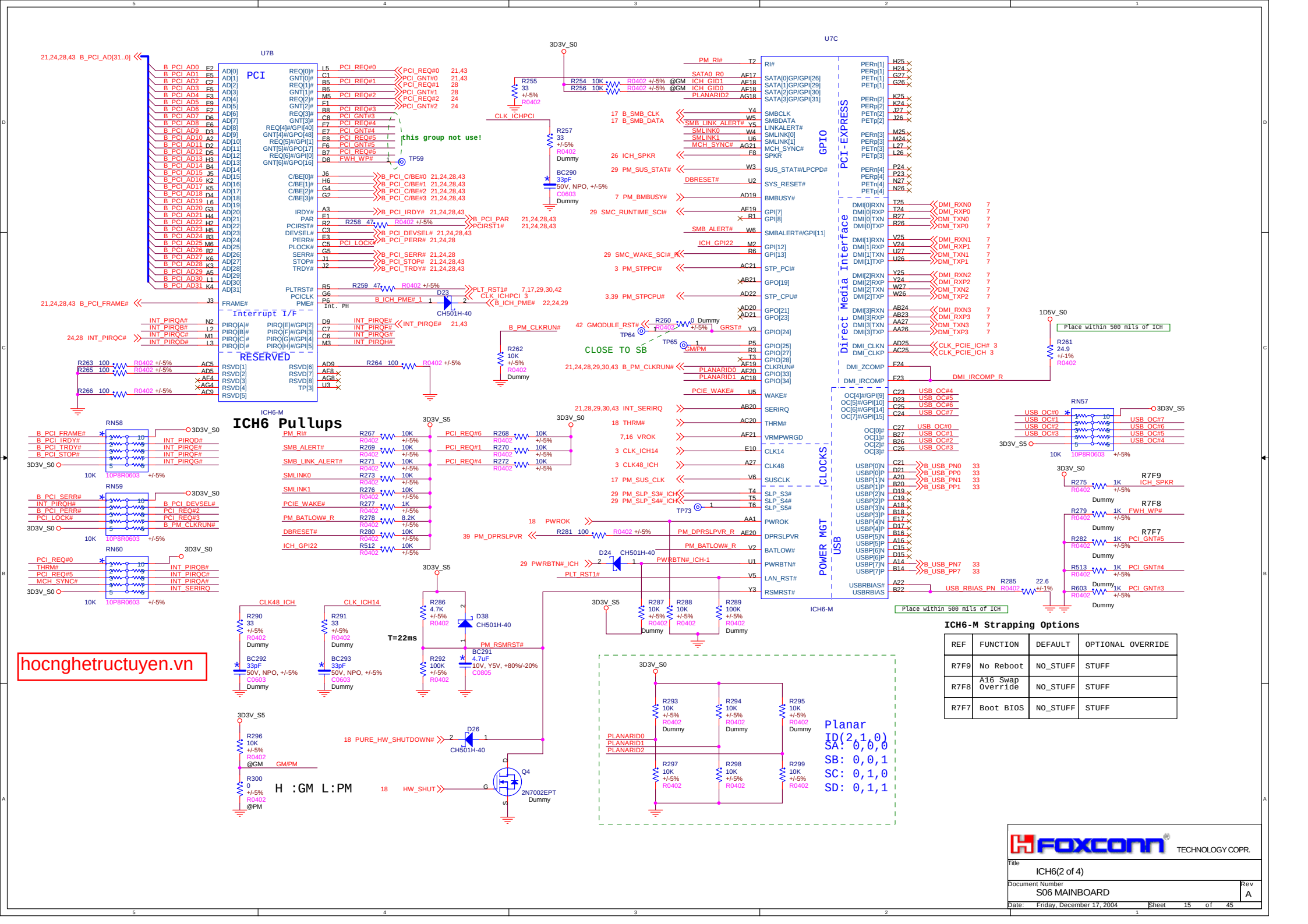
Date: Thursday, December 16, 2004 Sheet 13 of 45

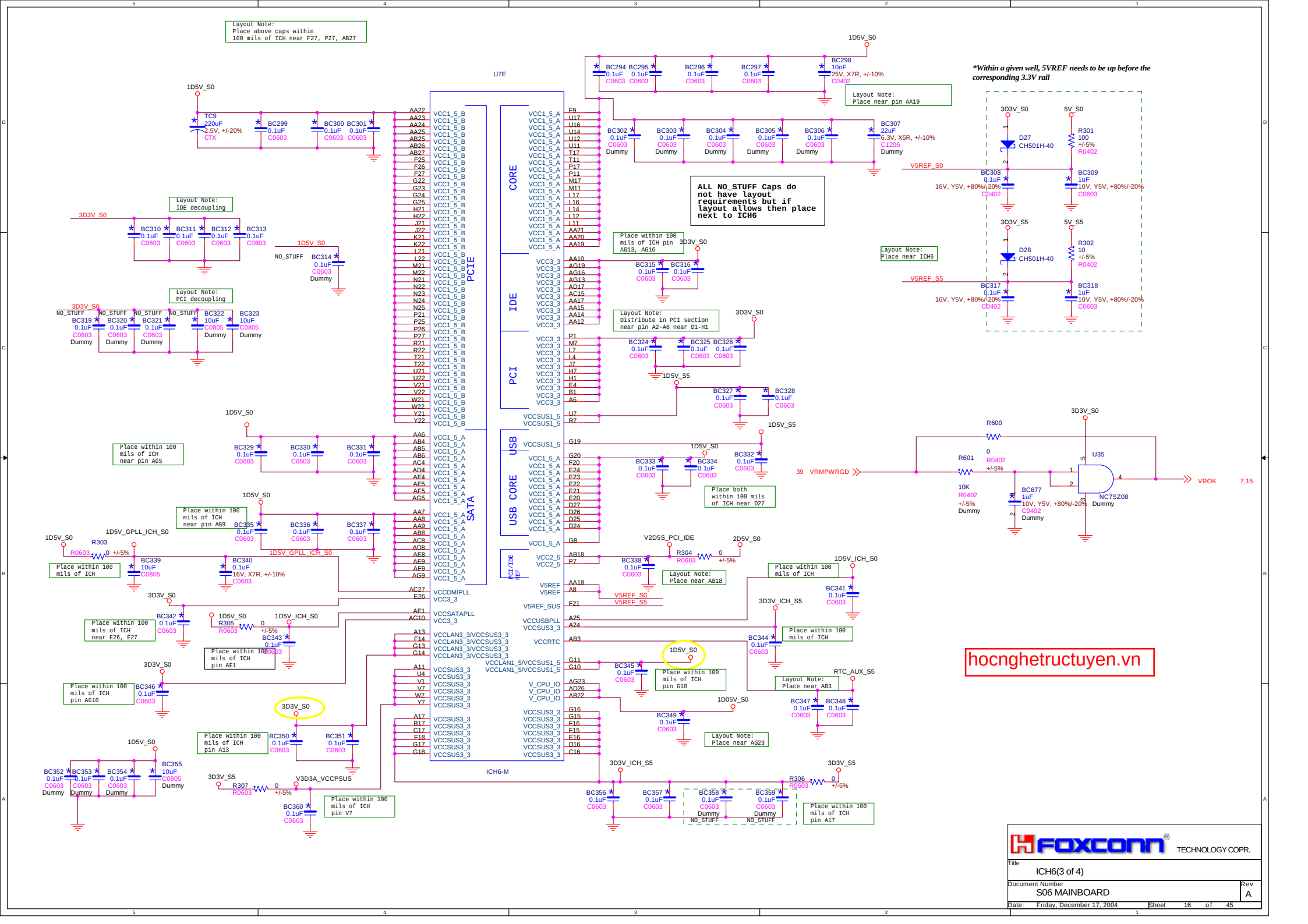
RTC circuitry

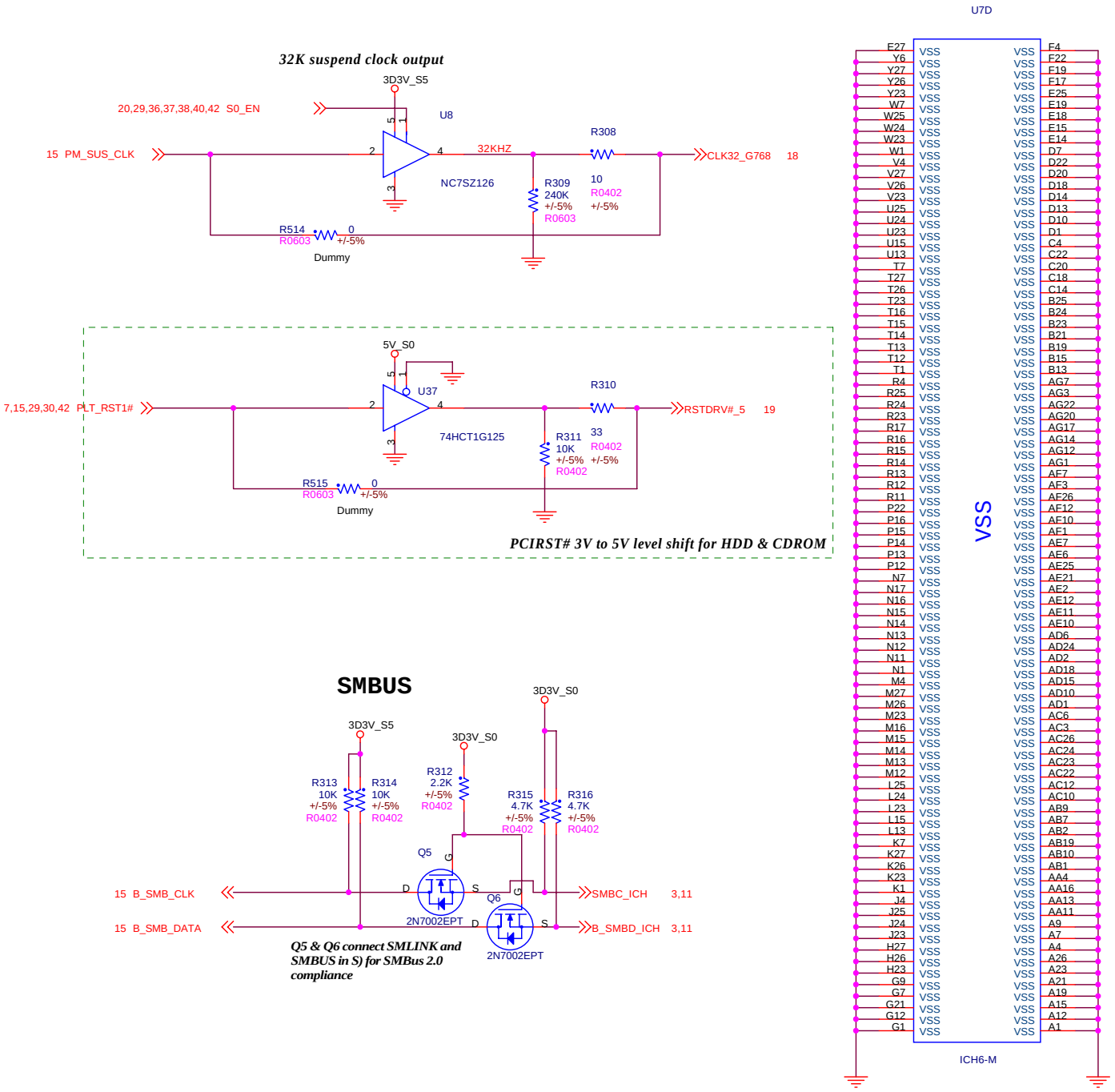


FOXCONN TECHNOLOGY COPR.

Title	ICH6(1 of 4)
Document Number	S06 MAINBOARD
Rev	A
Date:	Friday, December 17, 2004
Sheet	14 of 45


U7B
PCI
this group not use!
Interrupt I/F
RESERVED
ICH6-M
ICH6 Pullups
U7C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
POWER MGT
USB
CLOSE TO SB
T=22ms
H :GM L:PM
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
ICH6-M Strapping Options
REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE
R7F9 | No Reboot | NO_STUFF | STUFF
R7F8 | A16 Swap Override | NO_STUFF | STUFF
R7F7 | Boot BIOS | NO_STUFF | STUFF
hocnghetructuyen.vn
FOXCONN TECHNOLOGY COPR.
Title
ICH6(2 of 4)
Document Number
S06 MAINBOARD
Rev
A
Date: Friday, December 17, 2004
Sheet 15 of 45

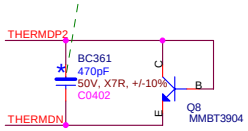

Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27
U7E
ICH6-M
CORE
PCIE
IDE
PCI
USB
USB CORE
SATA
PCI/IDE REF
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Layout Note: Place near pin AA19
Layout Note: Place near ICH6
Layout Note: Place near AB18
Layout Note: Place near AB3
Layout Note: Place near AG23
Place within 100 mils of ICH pin AG13, AG16
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin A17
Place both within 100 mils of ICH near D27
1D5V_S0
3D3V_S0
5V_S0
1D5V_S5
3D3V_S5
5V_S5
2D5V_S0
1D05V_S0
1D5V_GPLL_ICH_S0
1D5V_ICH_S0
3D3V_ICH_S5
3D3V_S5
V5REF_S0
V5REF_S5
V2D5S_PCI_IDE
V3D3A_VCCPSUS
RTC_AUX_S5
39 VRMPWRGD
VROK 7,15
TECHNOLOGY COPR.
Title
ICH6(3 of 4)
Document Number
S06 MAINBOARD
Rev
A
Date: Friday, December 17, 2004
Sheet 16 of 45
hocnghetructuyen.vn



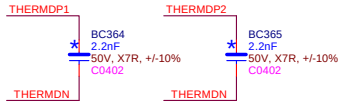
FOXCONN TECHNOLOGY COPR.

Title	ICH6(4 of 4)
Document Number	S06 MAINBOARD
Rev	A
Date:	Thursday, December 16, 2004
Sheet	17 of 45

Put these two Caps near the thermal diode.



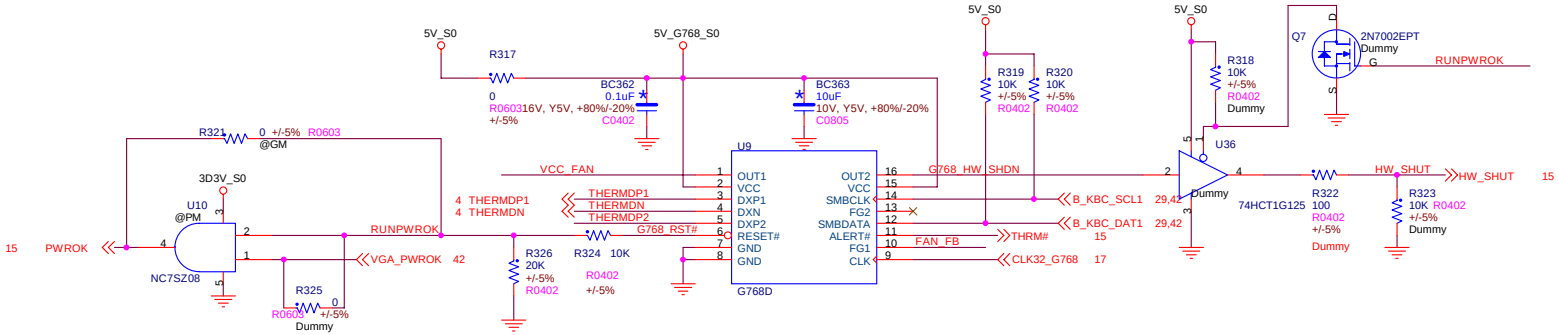
SYSTEM SENSOR

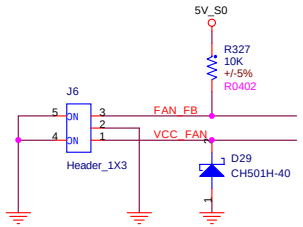


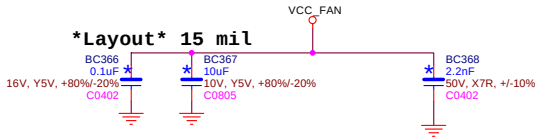
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

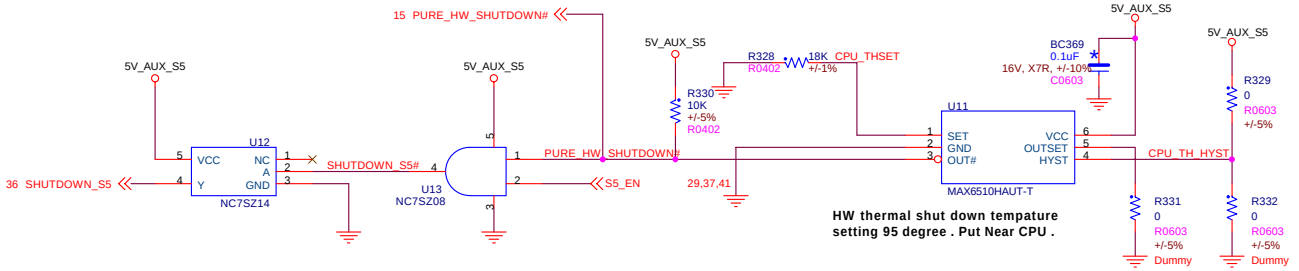
HW thermal shut down tempature
setting 95 degree . Put Near CPU .

Reserve for G768B
works at High
Speed







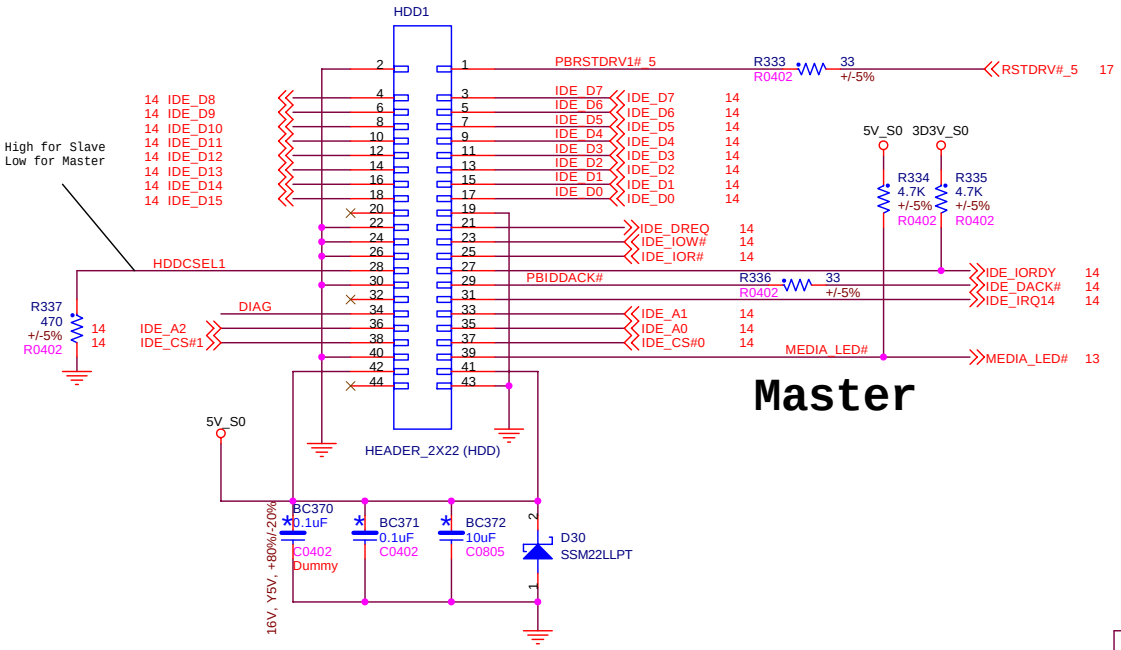


HW thermal shut down tempature
setting 95 degree . Put Near CPU .

FOXCONN TECHNOLOGY COPR.

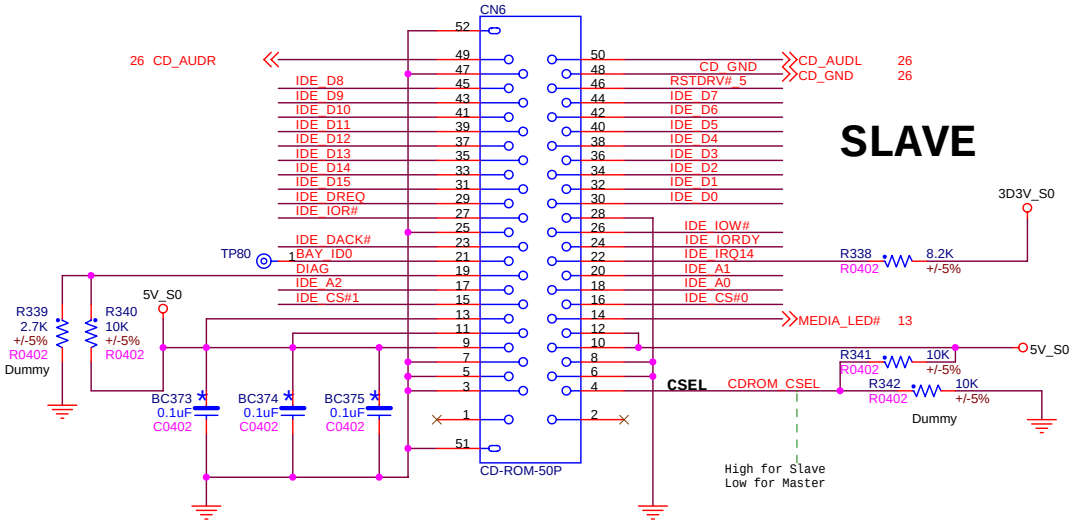
Title	THERMAL G768
Document Number	S06 MAINBOARD
Rev	A
Date:	Friday, December 17, 2004
Sheet	18 of 45

HDD Connector

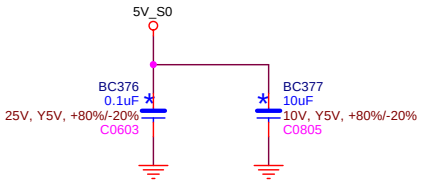


Master

CDROM

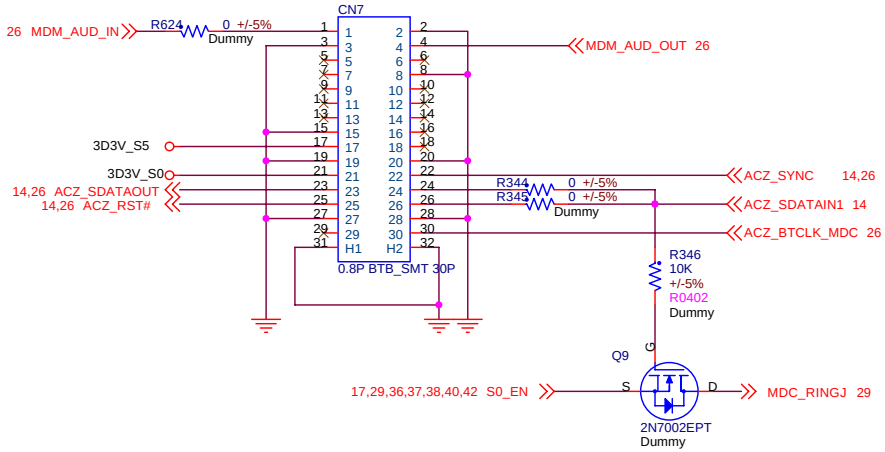


SLAVE



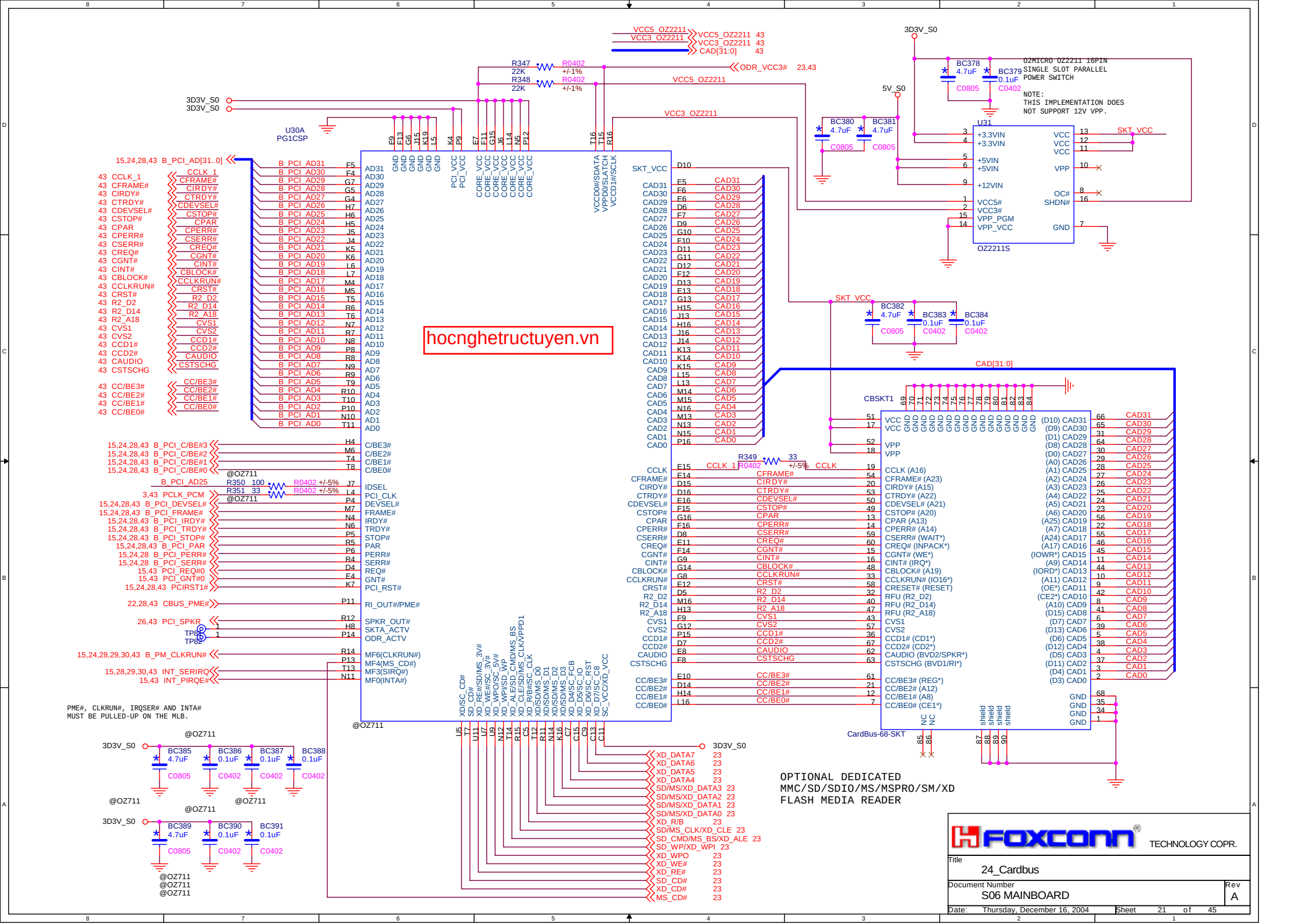
FOXCONN TECHNOLOGY COPR.

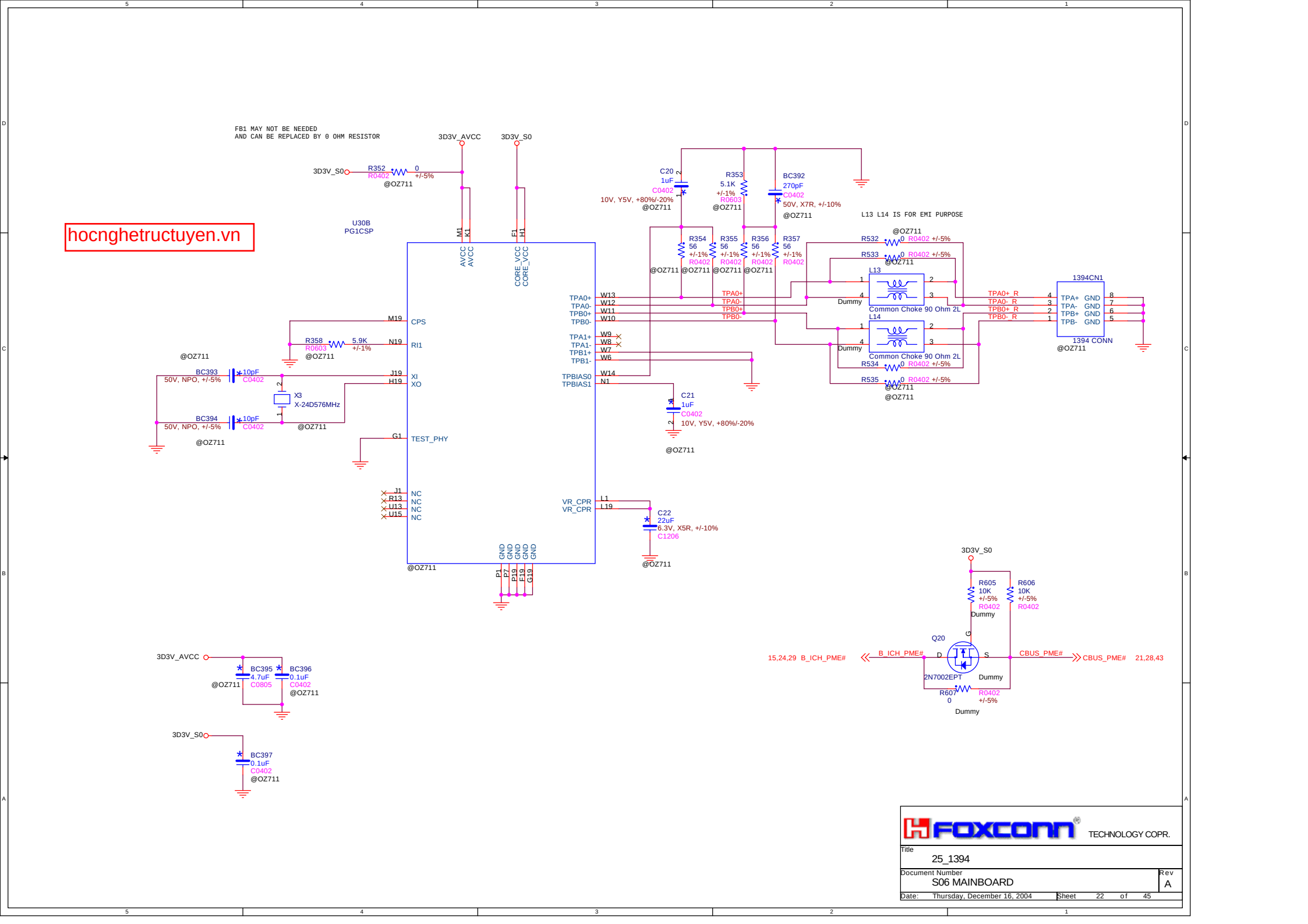
Title	HDD/CDROM	
Document Number	S06 MAINBOARD	Rev A
Date: Thursday, December 16, 2004	Sheet 19 of 45	

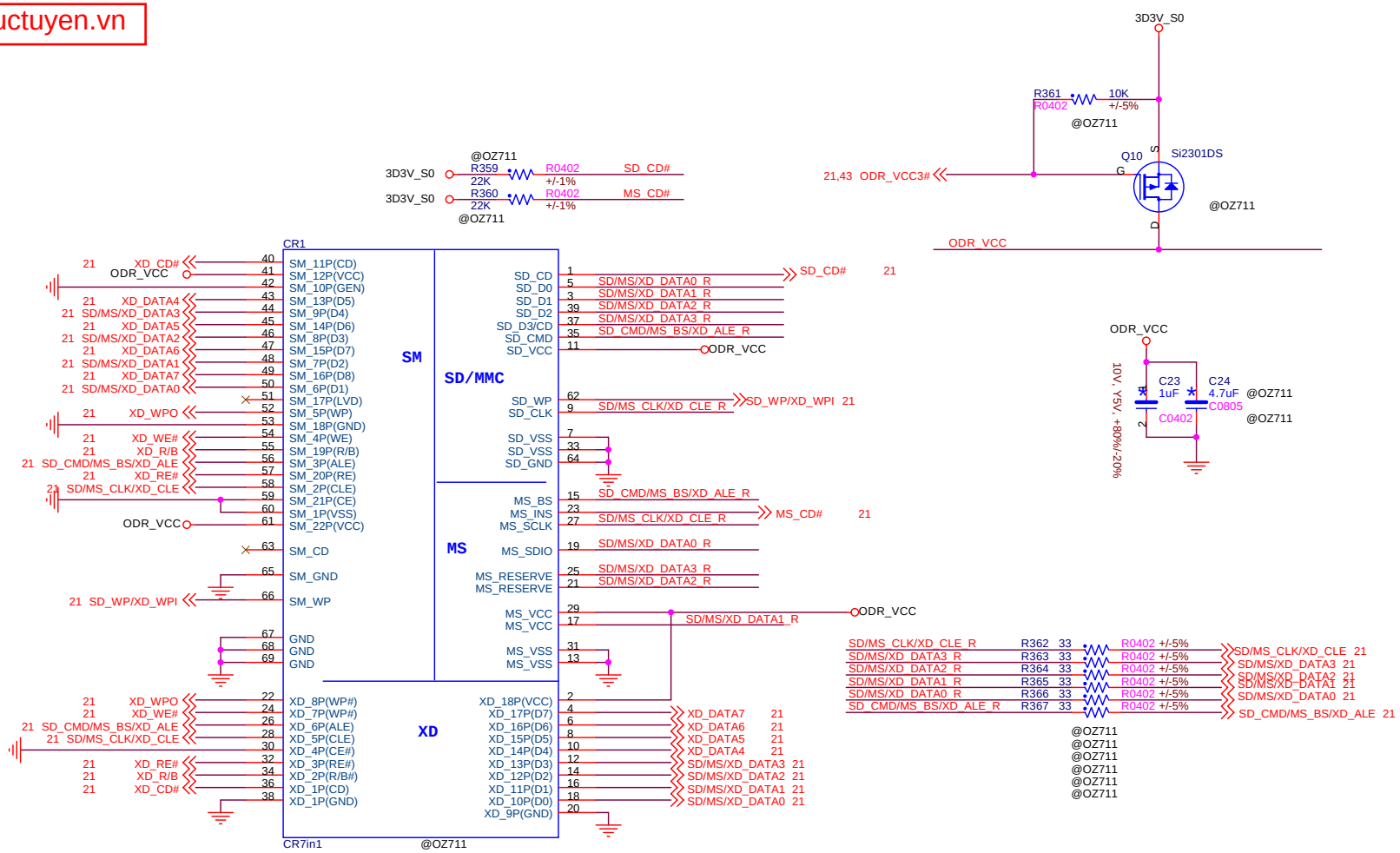


FOXCONN TECHNOLOGY COPR.

Title	MDC
Document Number	S06 MAINBOARD
Rev	A
Date: Thursday, December 16, 2004	Sheet 20 of 45

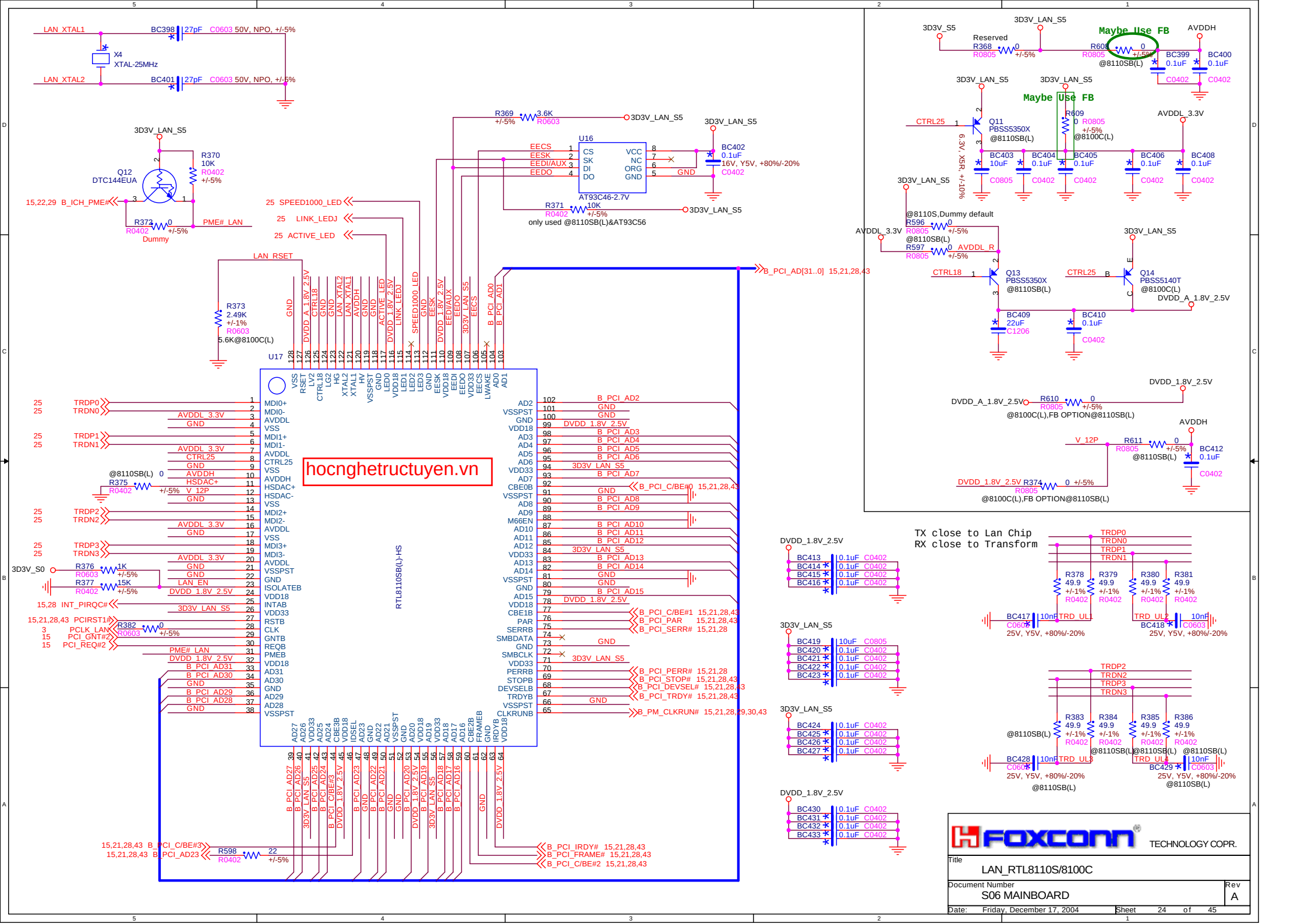

U30A
PG1CSP
U31
OZ2211S
CBSKT1
CardBus-68-SKT
@OZ711
hocnghetructuyen.vn
OPTIONAL DEDICATED
MMC/SD/SDIO/MS/MSPRO/SM/XD
FLASH MEDIA READER
PME#, CLKRUN#, IRQSER# AND INTA#
MUST BE PULLED-UP ON THE MLB.
O2MICRO OZ2211 16PIN
SINGLE SLOT PARALLEL
POWER SWITCH
NOTE:
THIS IMPLEMENTATION DOES
NOT SUPPORT 12V VPP.
FOXCONN
TECHNOLOGY COPR.
Title
24_Cardbus
Document Number
S06 MAINBOARD
Rev
A
Date: Thursday, December 16, 2004
Sheet 21 of 45

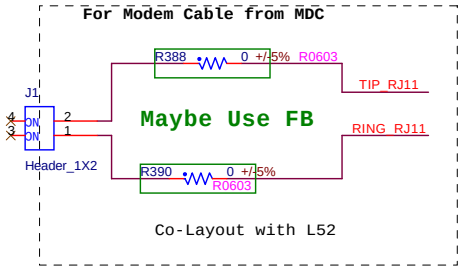


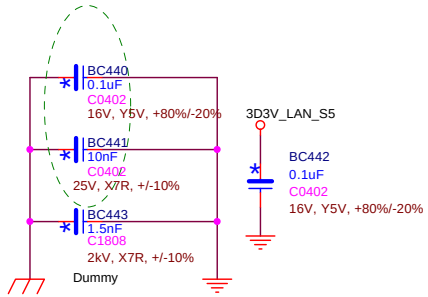


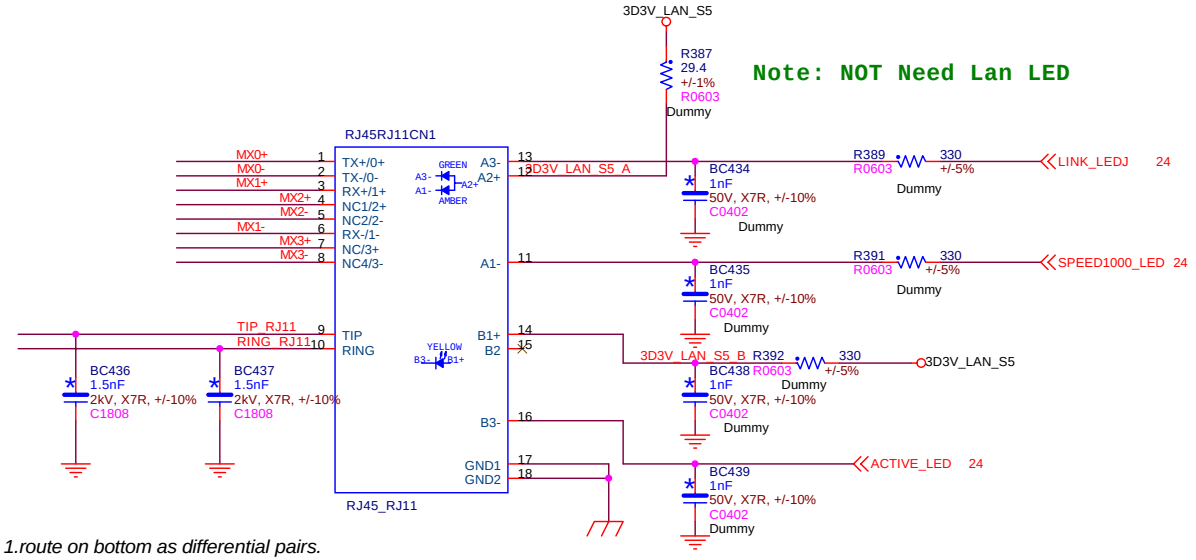
FOXCONN TECHNOLOGY COPR.

Title	26_CardReader
Document Number	S06 MAINBOARD
Rev	A
Date:	Friday, December 17, 2004
Sheet	23 of 45

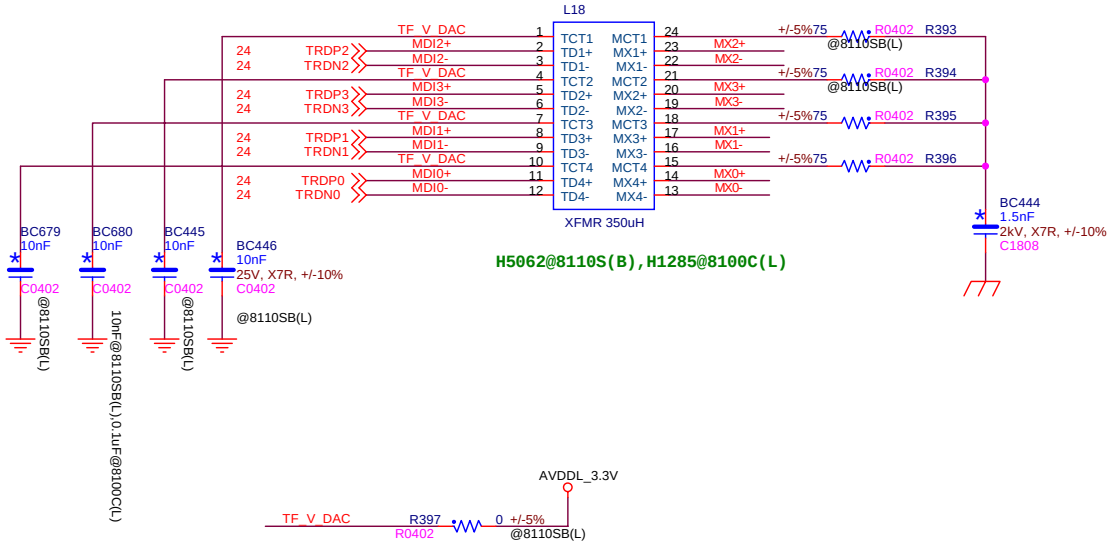

LAN_XTAL1
BC398 27pF C0603 50V, NPO, +/-5%
X4
XTAL-25MHz
LAN_XTAL2
BC401 27pF C0603 50V, NPO, +/-5%
3D3V_LAN_S5
Q12
DTC144EUA
R370 10K R0402 +/-5%
15,22,29 B_ICH_PME#
R372 0 R0402 +/-5%
Dummy
PME# LAN
R369 3.6K +/-5% R0603
3D3V_LAN_S5
U16
EECS
EESK
EEDI/AUX
EEDO
CS
SK
DI
DO
VCC
NC
ORG
GND
AT93C46-2.7V
BC402 0.1uF 16V, Y5V, +80%/-20% C0402
R371 10K R0402 +/-5%
3D3V_LAN_S5
only used @8110SB(L)&AT93C56
25 SPEED1000_LED
25 LINK_LEDJ
25 ACTIVE_LED
LAN_RSET
R373 2.49K +/-1% R0603
5.6K@8100C(L)
U17
RTL8110SB(L)-HS
hocnghetructuyen.vn
B_PCI_AD[31..0] 15,21,28,43
25 TRDP0
25 TRDN0
25 TRDP1
25 TRDN1
25 TRDP2
25 TRDN2
25 TRDP3
25 TRDN3
AVDDL_3.3V
GND
CTRL25
AVDDH
HSDAC+
HSDAC-
@8110SB(L) 0
R375 R0402 +/-5% V_12P
3D3V_S0
R376 1K R0603 +/-5%
R377 15K R0402 +/-5%
LAN_EN
DVDD_1.8V_2.5V
15,28 INT_PIRQC#
3D3V_LAN_S5
15,21,28,43 PCIRST1#
3 PCLK_LAN
15 PCI_GNT#2
15 PCI_REQ#2
R382 0 R0603 +/-5%
PME# LAN
B_PCI_AD31
B_PCI_AD30
B_PCI_AD29
B_PCI_AD28
B_PCI_C/BE#3
B_PCI_AD23
B_PCI_AD22
B_PCI_AD21
B_PCI_AD20
B_PCI_AD19
B_PCI_AD18
B_PCI_AD17
B_PCI_AD16
B_PCI_C/BE#2
B_PCI_FRAME#
B_PCI_IRDY#
B_PCI_AD0
B_PCI_AD1
B_PCI_AD2
B_PCI_AD3
B_PCI_AD4
B_PCI_AD5
B_PCI_AD6
B_PCI_AD7
B_PCI_C/BE#0 15,21,28,43
B_PCI_AD8
B_PCI_AD9
B_PCI_AD10
B_PCI_AD11
B_PCI_AD12
B_PCI_AD13
B_PCI_AD14
B_PCI_AD15
B_PCI_C/BE#1 15,21,28,43
B_PCI_PAR 15,21,28,43
B_PCI_SERR# 15,21,28
B_PCI_PERR# 15,21,28
B_PCI_STOP# 15,21,28,43
B_PCI_DEVSEL# 15,21,28,43
B_PCI_TRDY# 15,21,28,43
B_PM_CLKRUN# 15,21,28,29,30,43
R598 22 R0402 +/-5%
15,21,28,43 B_PCI_C/BE#3
15,21,28,43 B_PCI_AD23
3D3V_LAN_S5
Reserved
R368 0 R0805 +/-5%
Maybe Use FB
R608 0 R0805 +/-5% @8110SB(L)
AVDDH
BC399 0.1uF C0402
BC400 0.1uF C0402
R609 0 R0805 +/-5% @8100C(L)
AVDDL_3.3V
Q11
PBSS5350X
@8110SB(L)
6.3V, X5R, +/-10%
BC403 10uF C0805
BC404 0.1uF C0402
BC405 0.1uF C0402
BC406 0.1uF C0402
BC408 0.1uF C0402
@8110S,Dummy default
R596 0 R0805 +/-5% @8110SB(L)
R597 0 AVDDL_R R0805 +/-5%
Q13
PBSS5350X
@8110SB(L)
Q14
PBSS5140T
@8100C(L)
DVDD_A_1.8V_2.5V
BC409 22uF C1206
BC410 0.1uF C0402
DVDD_1.8V_2.5V
R610 0 R0805 +/-5%
@8100C(L),FB OPTION@8110SB(L)
V_12P
R611 0 R0805 +/-5% @8110SB(L)
BC412 0.1uF C0402
DVDD_1.8V_2.5V R374 0 +/-5% R0805
@8100C(L),FB OPTION@8110SB(L)
TX close to Lan Chip
RX close to Transform
BC413 0.1uF C0402
BC414 0.1uF C0402
BC415 0.1uF C0402
BC416 0.1uF C0402
BC419 10uF C0805
BC420 0.1uF C0402
BC421 0.1uF C0402
BC422 0.1uF C0402
BC423 0.1uF C0402
BC424 0.1uF C0402
BC425 0.1uF C0402
BC426 0.1uF C0402
BC427 0.1uF C0402
BC430 0.1uF C0402
BC431 0.1uF C0402
BC432 0.1uF C0402
BC433 0.1uF C0402
TRDP0
TRDN0
TRDP1
TRDN1
R378 49.9 +/-1% R0402
R379 49.9 +/-1% R0402
R380 49.9 +/-1% R0402
R381 49.9 +/-1% R0402
BC417 10nF C0603 25V, Y5V, +80%/-20%
BC418 10nF C0603 25V, Y5V, +80%/-20%
TRD_UL1
TRD_UL2
TRDP2
TRDN2
TRDP3
TRDN3
R383 49.9 +/-1% R0402
R384 49.9 +/-1% R0402
R385 49.9 +/-1% R0402
R386 49.9 +/-1% R0402
@8110SB(L)
BC428 10nF C0603 25V, Y5V, +80%/-20%
BC429 10nF C0603 25V, Y5V, +80%/-20%
TRD_UL3
TRD_UL4
FOXCONN
TECHNOLOGY COPR.
Title
LAN_RTL8110S/8100C
Document Number
S06 MAINBOARD
Rev
A
Date: Friday, December 17, 2004
Sheet 24 of 45







1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



FOXCONN TECHNOLOGY COPR.

Title	RJ45/RJ11 & Transformer
Document Number	S06 MAINBOARD
Rev	A
Date:	Thursday, December 16, 2004
Sheet	25 of 45

FAE suggest
Layout close to Pin6

Layout
40 mil

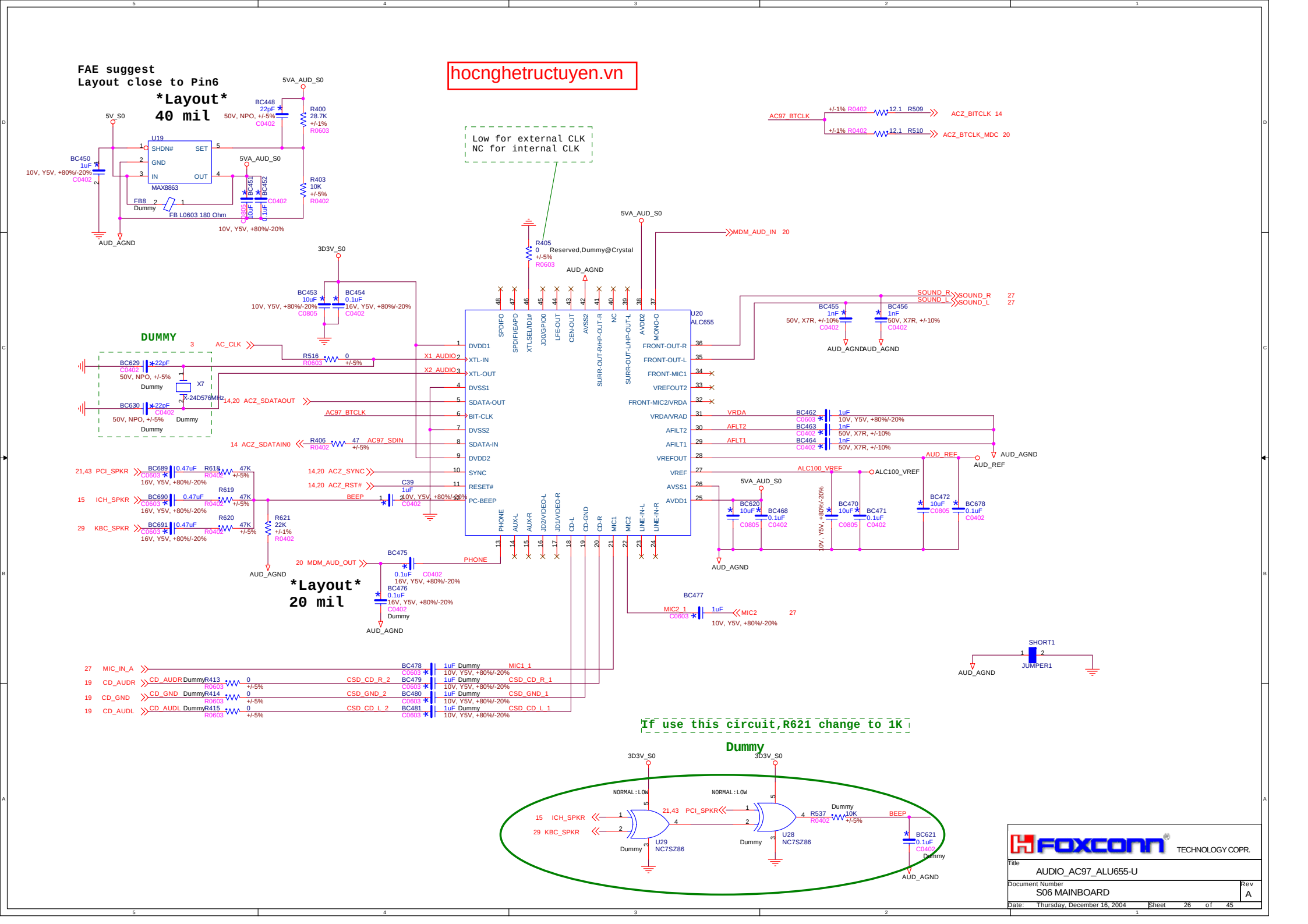
Layout
20 mil

Low for external CLK
NC for internal CLK

DUMMY

If use this circuit,R621 change to 1K

Dummy



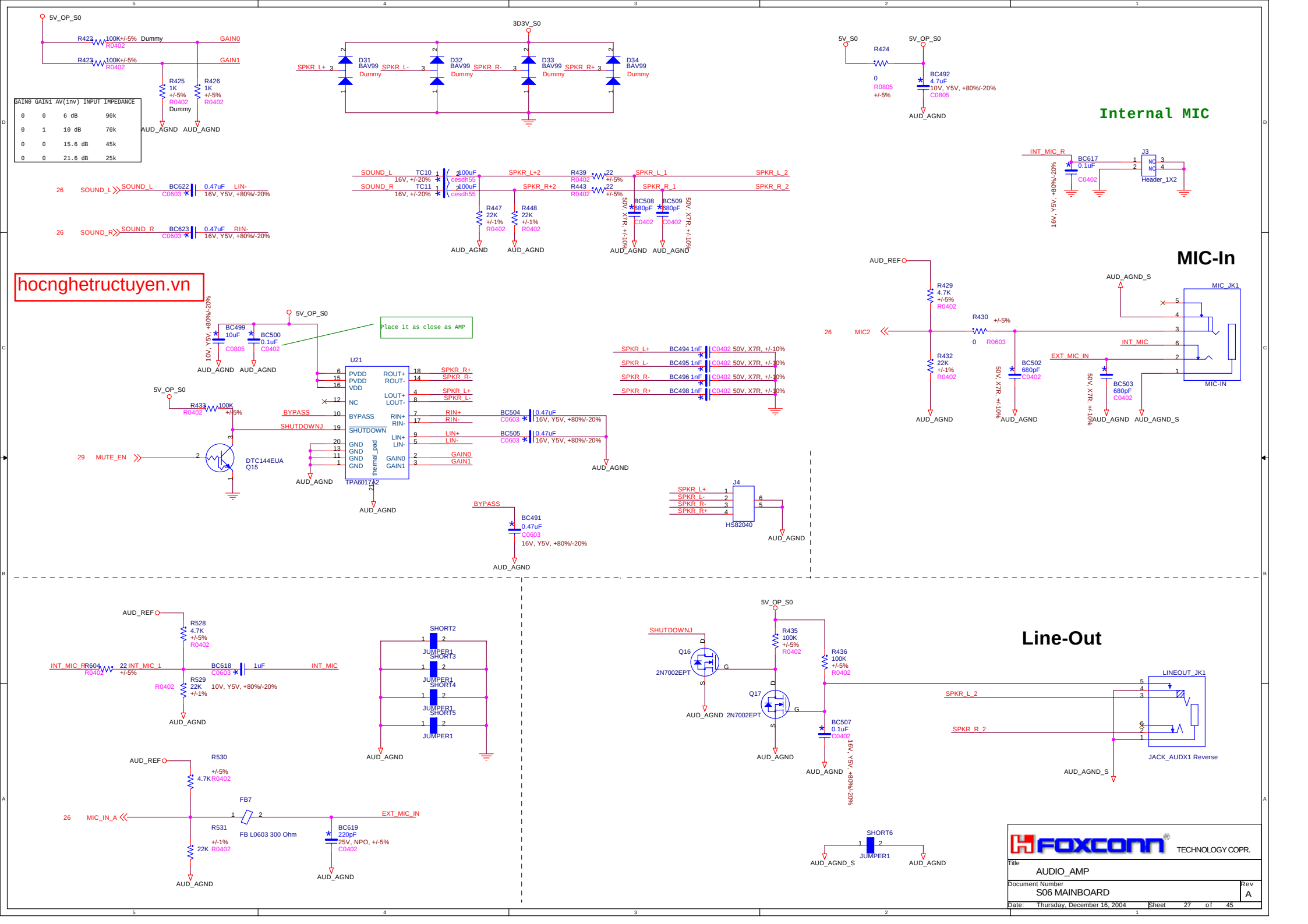
FOXCONN TECHNOLOGY COPR.

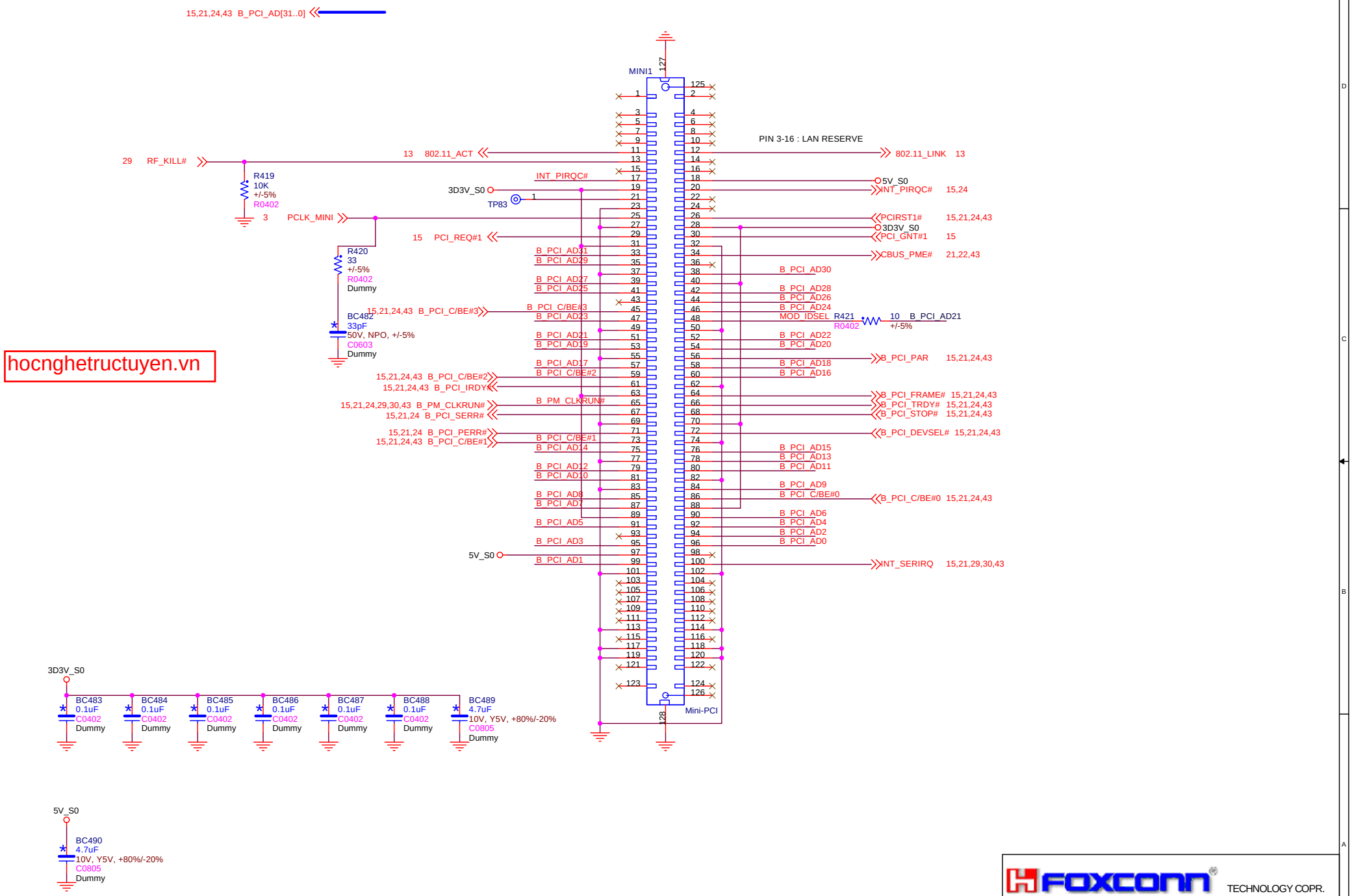
Title: AUDIO_AC97_ALU655-U

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 26 of 45


5V_OP_S0
R422 100K+/-5% Dummy R0402
GAIN0
R423 100K+/-5% R0402
GAIN1
R425 1K +/-5% R0402 Dummy
R426 1K +/-5% R0402
AUD_AGND AUD_AGND
GAIN0 GAIN1 AV(inv) INPUT IMPEDANCE
0 0 6 dB 90k
0 1 10 dB 70k
0 0 15.6 dB 45k
0 0 21.6 dB 25k
3D3V_S0
SPKR_L+ D31 BAV99 SPKR_L- Dummy
D32 BAV99 SPKR_R- Dummy
D33 BAV99 SPKR_R+ Dummy
D34 BAV99 Dummy
5V_S0
R424 0 R0805 +/-5%
5V_OP_S0
BC492 4.7uF 10V, Y5V, +80%/-20% C0805
AUD_AGND
Internal MIC
INT_MIC_R
BC617 0.1uF C0402
J3 NC NC Header_1X2
16V, Y5V, +80%/-20%
26 SOUND_L
SOUND_L BC622 C0603 0.47uF LIN- 16V, Y5V, +80%/-20%
26 SOUND_R
SOUND_R BC623 C0603 0.47uF RIN- 16V, Y5V, +80%/-20%
SOUND_L TC10 16V, +/-20% 100uF cesdh55
SOUND_R TC11 16V, +/-20% 100uF cesdh55
SPKR_L+2 R439 R0402 22 +/-5% SPKR_L_1 SPKR_L_2
SPKR_R+2 R443 R0402 22 +/-5% SPKR_R_1 SPKR_R_2
R447 22K +/-1% R0402
R448 22K +/-1% R0402
BC508 680pF C0402 50V, X7R, +/-10%
BC509 680pF C0402 50V, X7R, +/-10%
AUD_AGND AUD_AGND AUD_AGND AUD_AGND
MIC-In
hocnghetructuyen.vn
AUD_REF
R429 4.7K +/-5% R0402
26 MIC2
R430 +/-5% 0 R0603
R432 22K +/-1% R0402
AUD_AGND
BC502 680pF C0402 50V, X7R, +/-10%
AUD_AGND
AUD_AGND_S
MIC_JK1
INT_MIC
EXT_MIC_IN
BC503 680pF C0402 50V, X7R, +/-10%
MIC-IN
AUD_AGND AUD_AGND_S
BC499 10uF C0805 10V, Y5V, +80%/-20%
BC500 0.1uF C0402
AUD_AGND AUD_AGND
5V_OP_S0
Place it as close as AMP
U21
PVDD PVDD VDD NC BYPASS SHUTDOWN GND GND GND GND thermal_pad
ROUT+ ROUT- LOUT+ LOUT- RIN+ RIN- LIN+ LIN- GAIN0 GAIN1
SPKR_R+ SPKR_R- SPKR_L+ SPKR_L-
TPA6017A2
5V_OP_S0
R433 100K +/-5% R0402
BYPASS
SHUTDOWNJ
29 MUTE_EN
DTC144EUA Q15
AUD_AGND
SPKR_L+ BC494 1nF C0402 50V, X7R, +/-10%
SPKR_L- BC495 1nF C0402 50V, X7R, +/-10%
SPKR_R- BC496 1nF C0402 50V, X7R, +/-10%
SPKR_R+ BC498 1nF C0402 50V, X7R, +/-10%
BC504 C0603 0.47uF 16V, Y5V, +80%/-20%
BC505 C0603 0.47uF 16V, Y5V, +80%/-20%
AUD_AGND
BYPASS
BC491 0.47uF C0603 16V, Y5V, +80%/-20%
AUD_AGND
SPKR_L+ SPKR_L- SPKR_R- SPKR_R+
J4 HS82040
AUD_AGND
AUD_REF
R528 4.7K +/-5% R0402
INT_MIC_R R604 R0402 22 +/-5%
INT_MIC_1
BC618 C0603 1uF INT_MIC
R529 22K +/-1% R0402
10V, Y5V, +80%/-20%
AUD_AGND
SHORT2 JUMPER1
SHORT3 JUMPER1
SHORT4 JUMPER1
SHORT5 JUMPER1
AUD_AGND
AUD_REF
R530 4.7K +/-5% R0402
26 MIC_IN_A
FB7 FB L0603 300 Ohm
EXT_MIC_IN
R531 22K +/-1% R0402
BC619 220pF 25V, NPO, +/-5% C0402
AUD_AGND AUD_AGND
SHUTDOWNJ
Q16 2N7002EPT
5V_OP_S0
R435 100K +/-5% R0402
R436 100K +/-5% R0402
Q17 2N7002EPT
AUD_AGND AUD_AGND
BC507 0.1uF C0402
16V, Y5V, +80%/-20%
AUD_AGND
Line-Out
LINEOUT_JK1
SPKR_L_2
SPKR_R_2
JACK_AUDX1 Reverse
AUD_AGND_S
SHORT6 JUMPER1
AUD_AGND_S AUD_AGND
FOXCONN TECHNOLOGY COPR.
Title AUDIO_AMP
Document Number S06 MAINBOARD
Rev A
Date: Thursday, December 16, 2004
Sheet 27 of 45



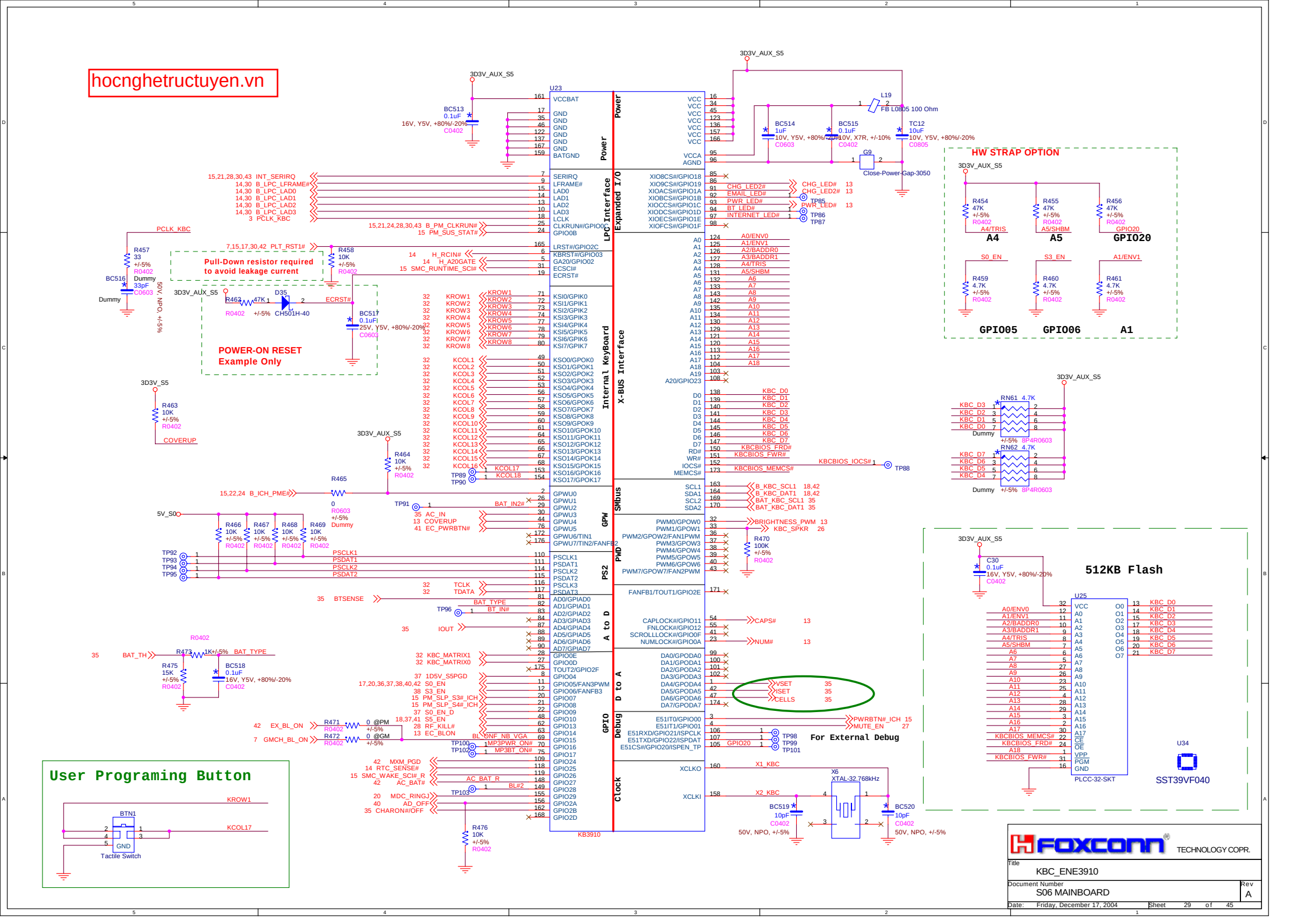
FOXCONN TECHNOLOGY COPR.

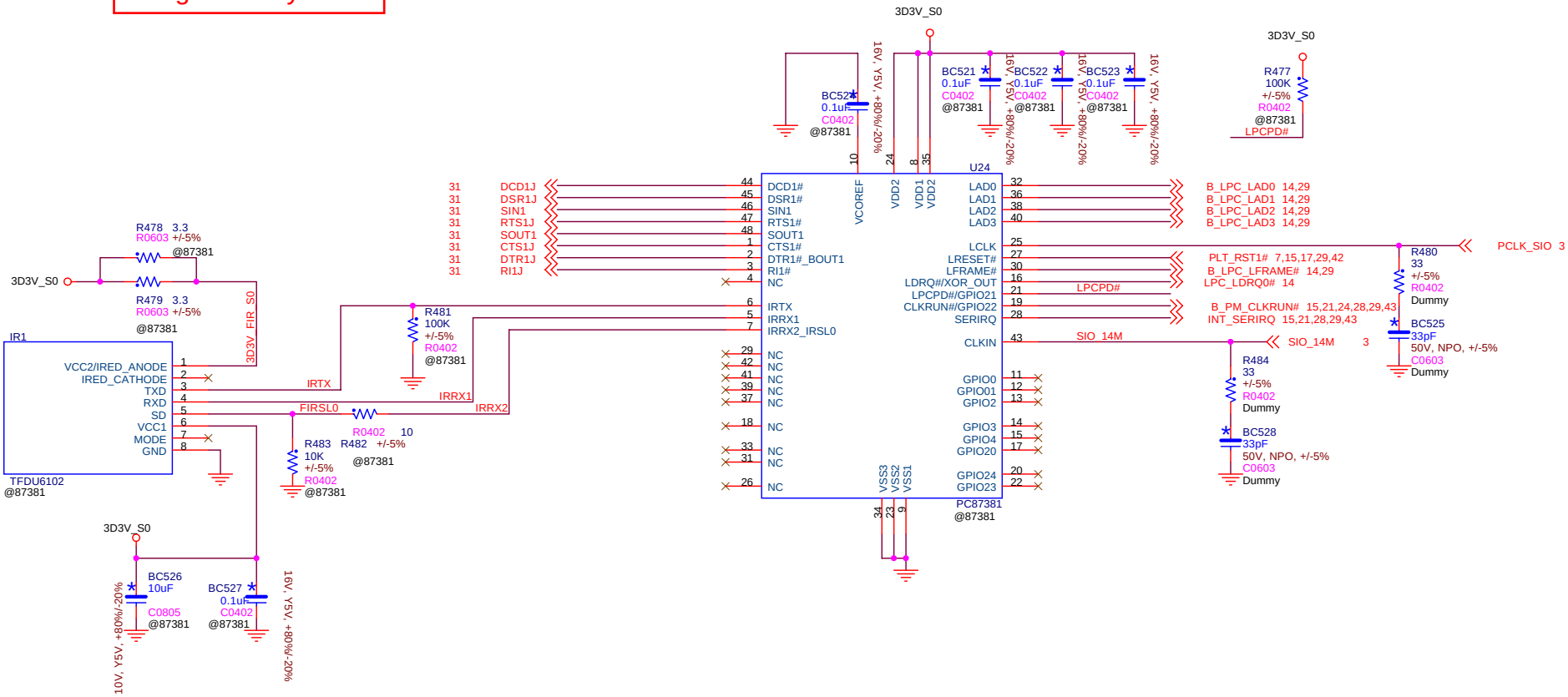
Title: MINI-PCI

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 28 of 45

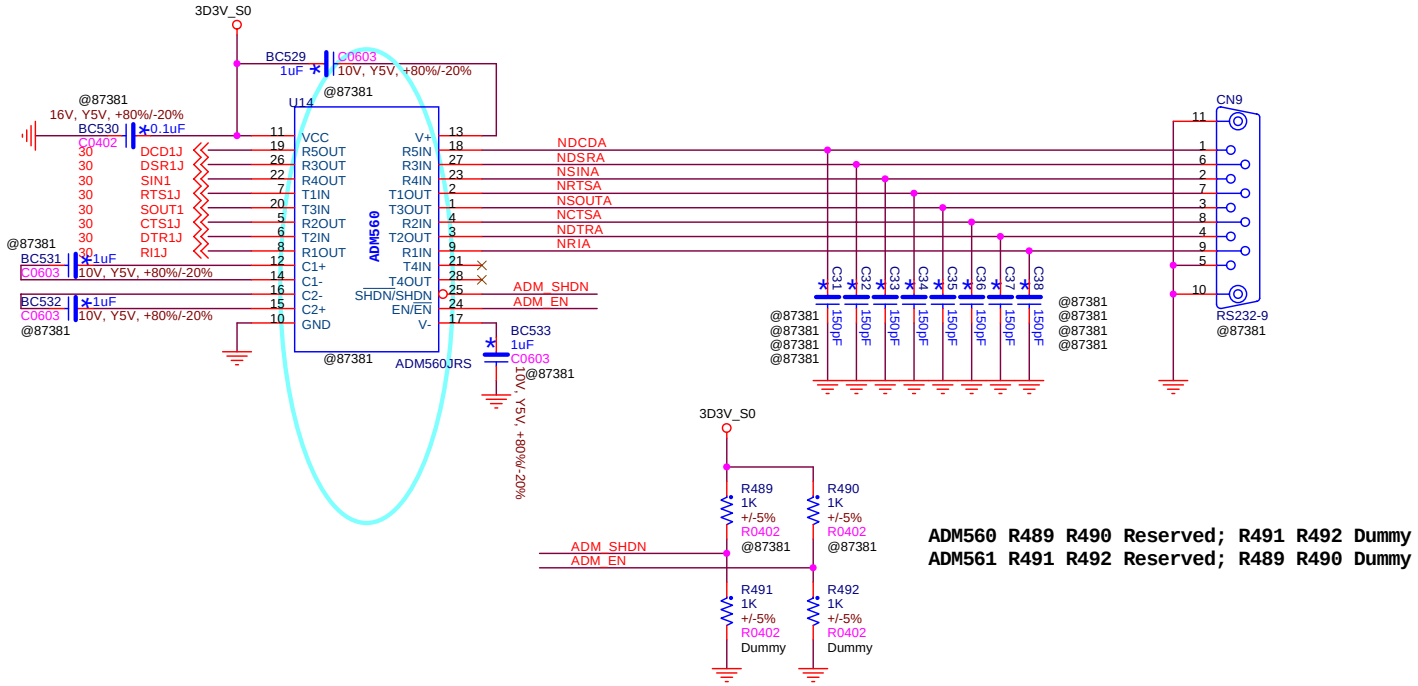




FOXCONN TECHNOLOGY COPR.

Title	SIO_FIR NS87381
Document Number	S06 MAINBOARD
Rev	A
Date:	Thursday, December 16, 2004
Sheet	30 of 45

SERIAL PORT1



ADM560 R489 R490 Reserved; R491 R492 Dummy
ADM561 R491 R492 Reserved; R489 R490 Dummy

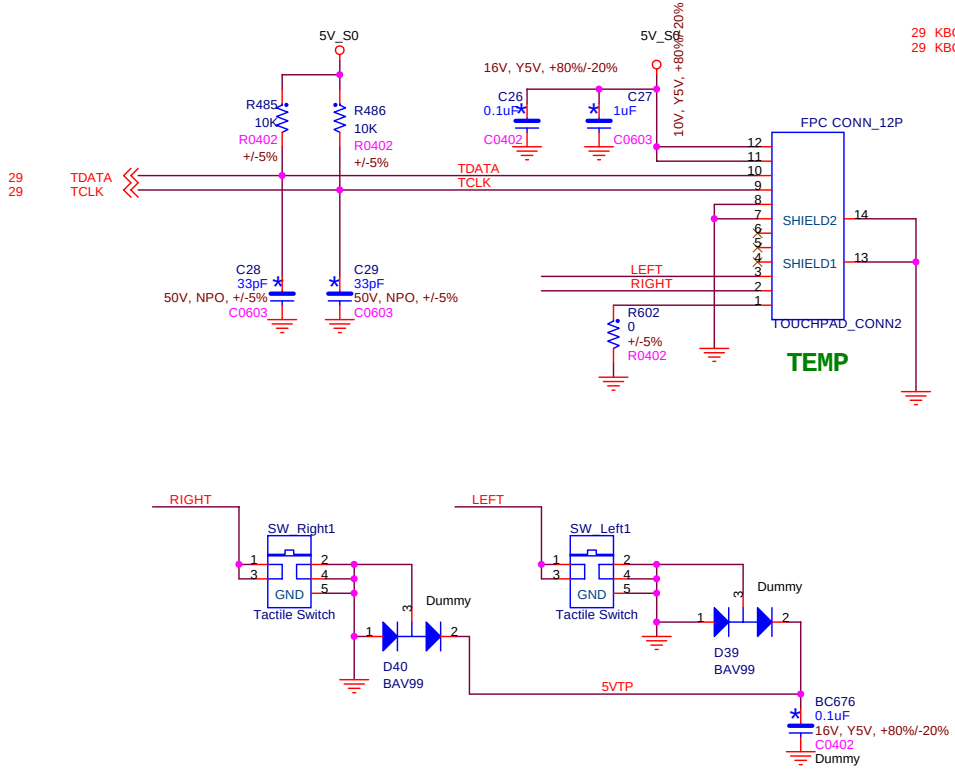
FOXCONN TECHNOLOGY COPR.

Title	FWH&DEBUG&COM	
Document Number	S06 MAINBOARD	Rev A
Date: Thursday, December 16, 2004	Sheet 31 of 45	

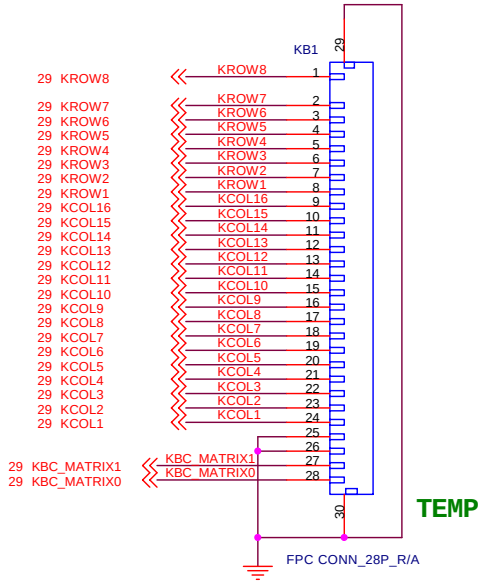
TouchPad Strap

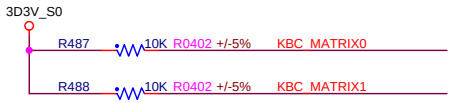
PIN Number	PH/PL	NOTES
1	NC	**0 Degree Connector Downtoward**
	0	**180 Degree Connector Uptoward**
6	NC	**For Two Buttons**
	0	**For Four Buttons**

TouchPad Connector



Internal KeyBoard Connector





Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID1#	1	0	1	0
MATRIXID2#	1	1	0	0

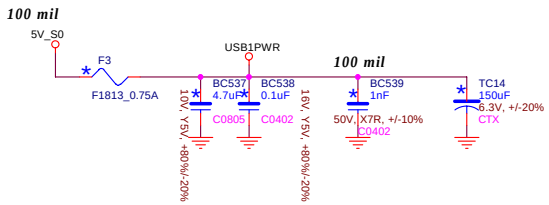
FOXCONN TECHNOLOGY COPR.

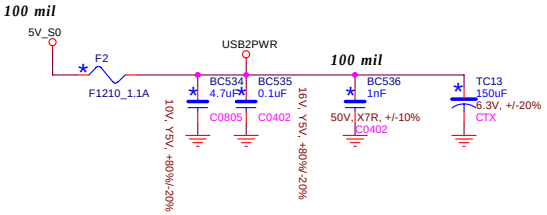
Title: KBC CONN

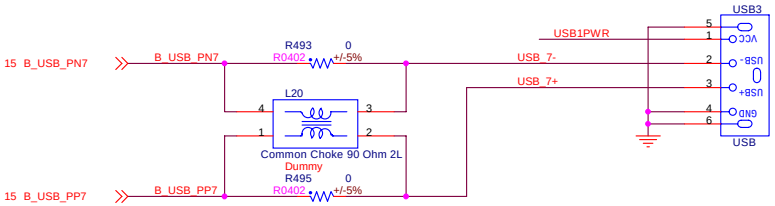
Document Number: S06 MAINBOARD

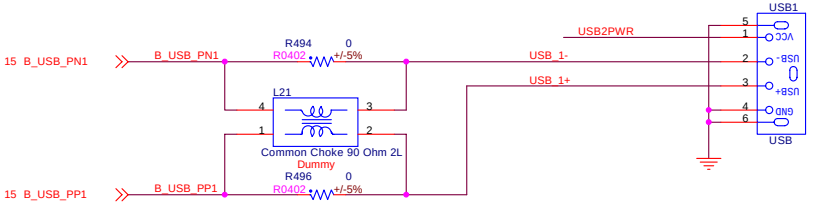
Rev: A

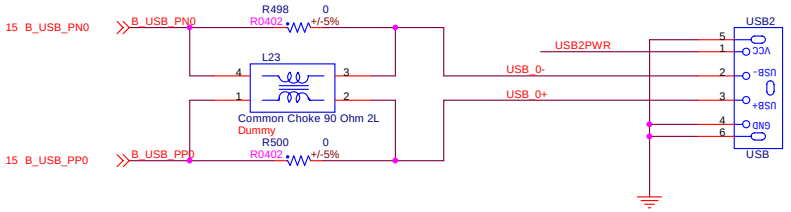
Date: Thursday, December 16, 2004 Sheet 32 of 45











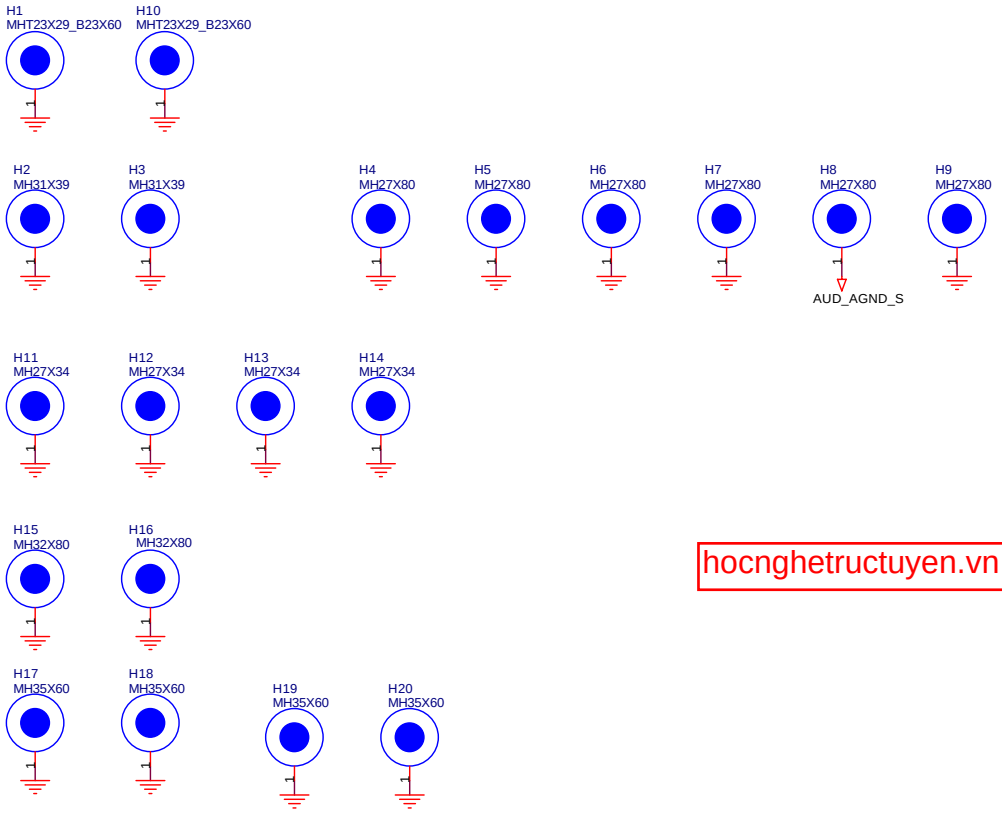
FOXCONN TECHNOLOGY COPR.

Title
USB*2*2/POWERSWITCH

Document Number
S06 MAINBOARD

Rev
A

Date: Thursday, December 16, 2004 Sheet 33 of 45



FOXCONN TECHNOLOGY COPR.

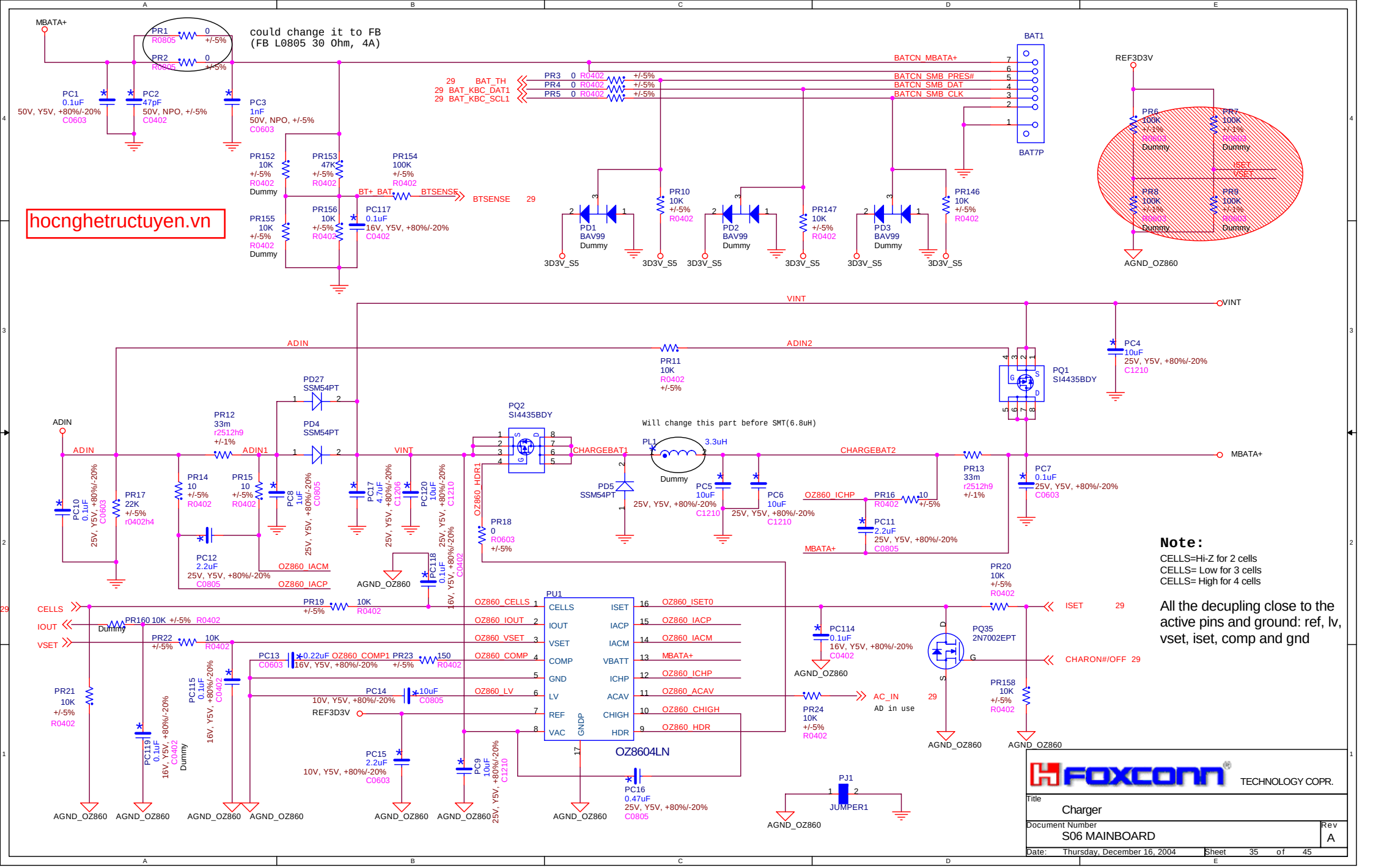
Title: HOLE/UNUSED PARTS

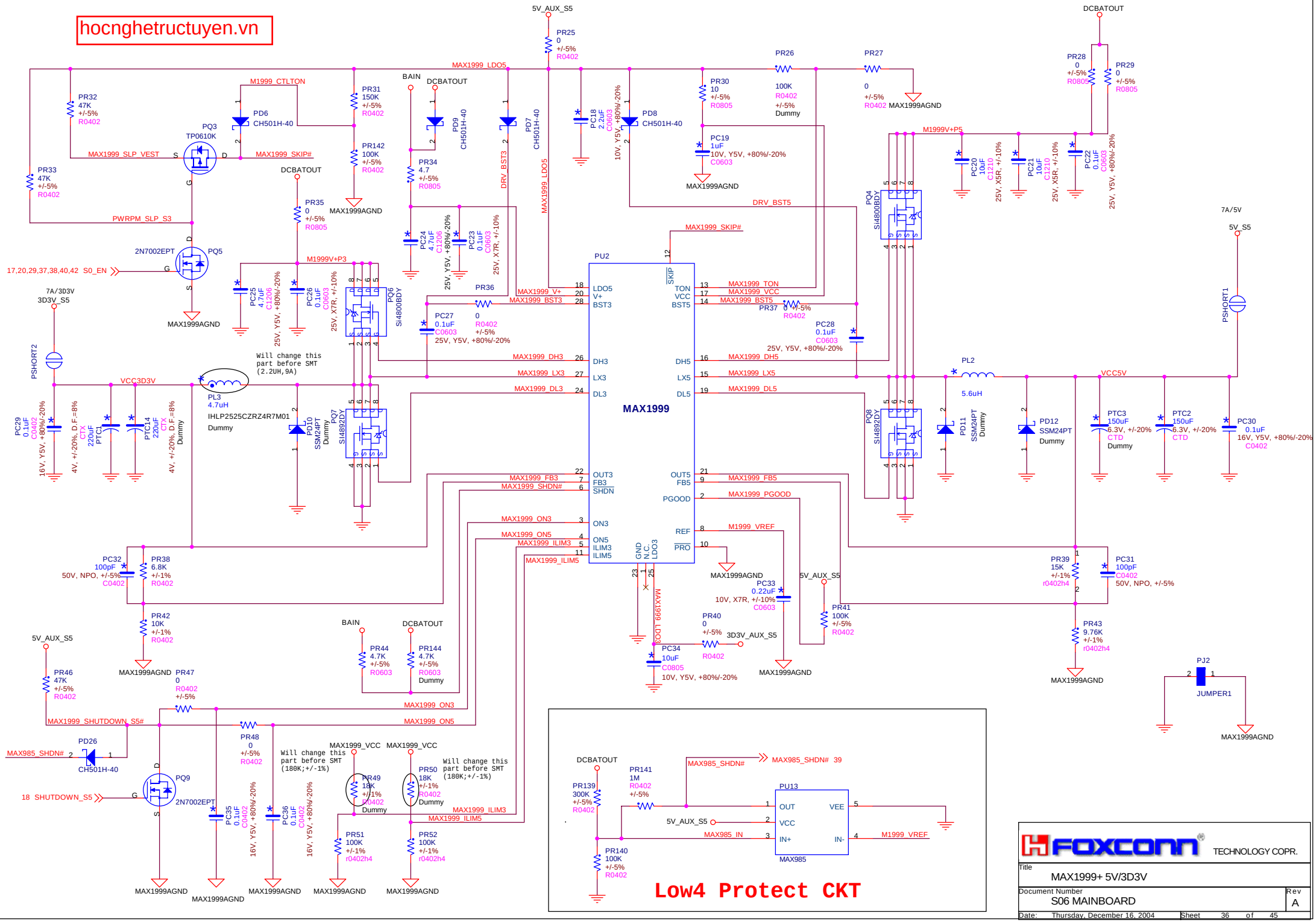
Document Number: S06 MAINBOARD

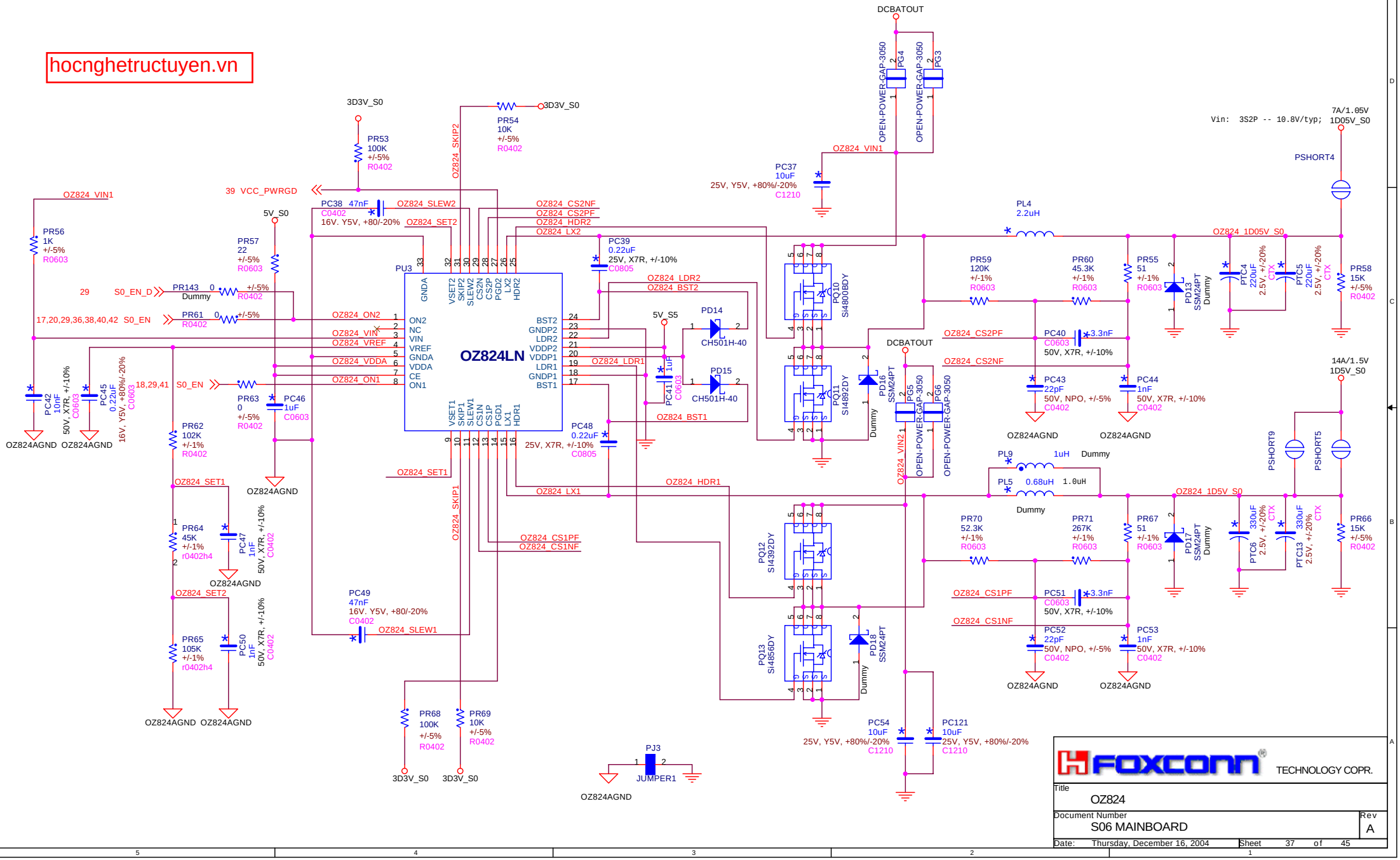
Rev: A

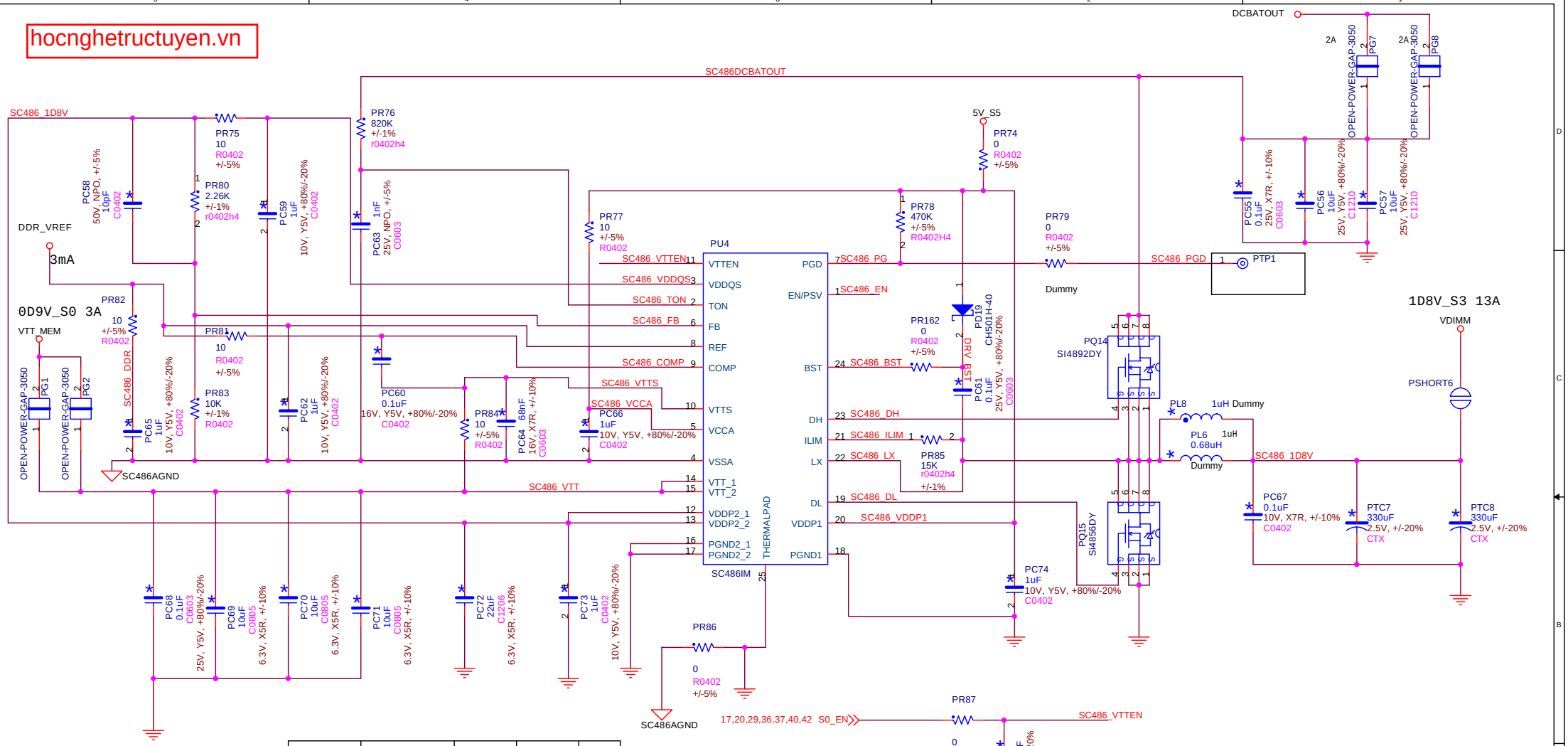
Date: Thursday, December 16, 2004

Sheet 34 of 45


could change it to FB
(FB L0805 30 Ohm, 4A)
hocnghetructuyen.vn
Will change this part before SMT(6.8uH)
OZ8604LN
Note:
CELLS=Hi-Z for 2 cells
CELLS= Low for 3 cells
CELLS= High for 4 cells
All the decupling close to the active pins and ground: ref, lv, vset, iset, comp and gnd
FOXCONN TECHNOLOGY COPR.
Title
Charger
Document Number
S06 MAINBOARD
Rev
A
Date: Thursday, December 16, 2004
Sheet 35 of 45



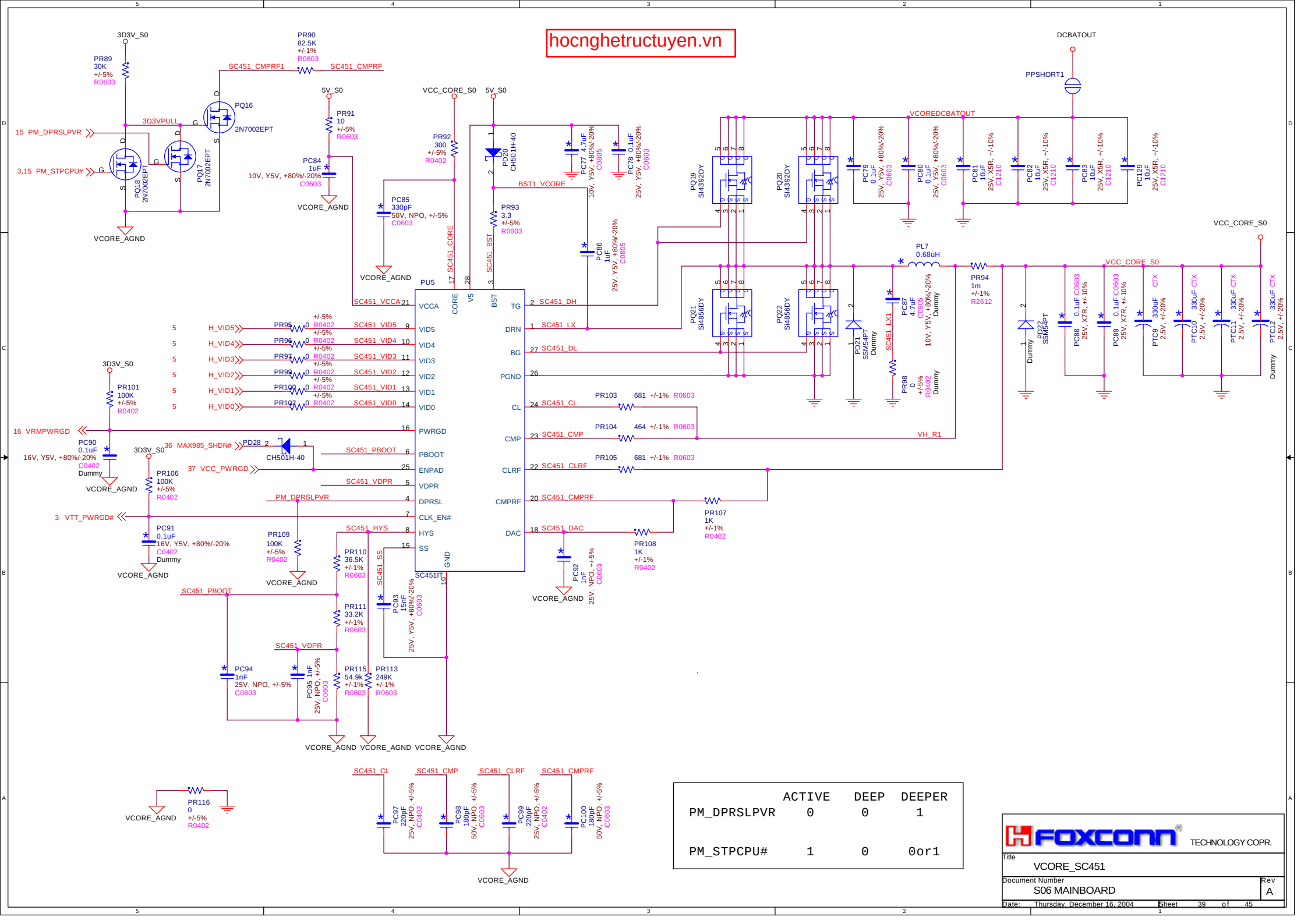




VDIMM/EN	VTT_MEM/EN	VDIMM	VTT_MEM	VREF
0	0	X	X	X
0	1	X	X	X
1	0	1.8	X	0.9
1	1	1.8	0.9	0.9

FOXCONN TECHNOLOGY COPR.

Title	SC486(1D8V-S3&0D9V-S0)
Document Number	S06 MAINBOARD
Rev	A
Date:	Friday, December 17, 2004
Sheet	38 of 45



	ACTIVE	DEEP	DEEPER
PM_DPRSLPVR	0	0	1
PM_STPCPU#	1	0	0or1

FOXCONN TECHNOLOGY COPR.

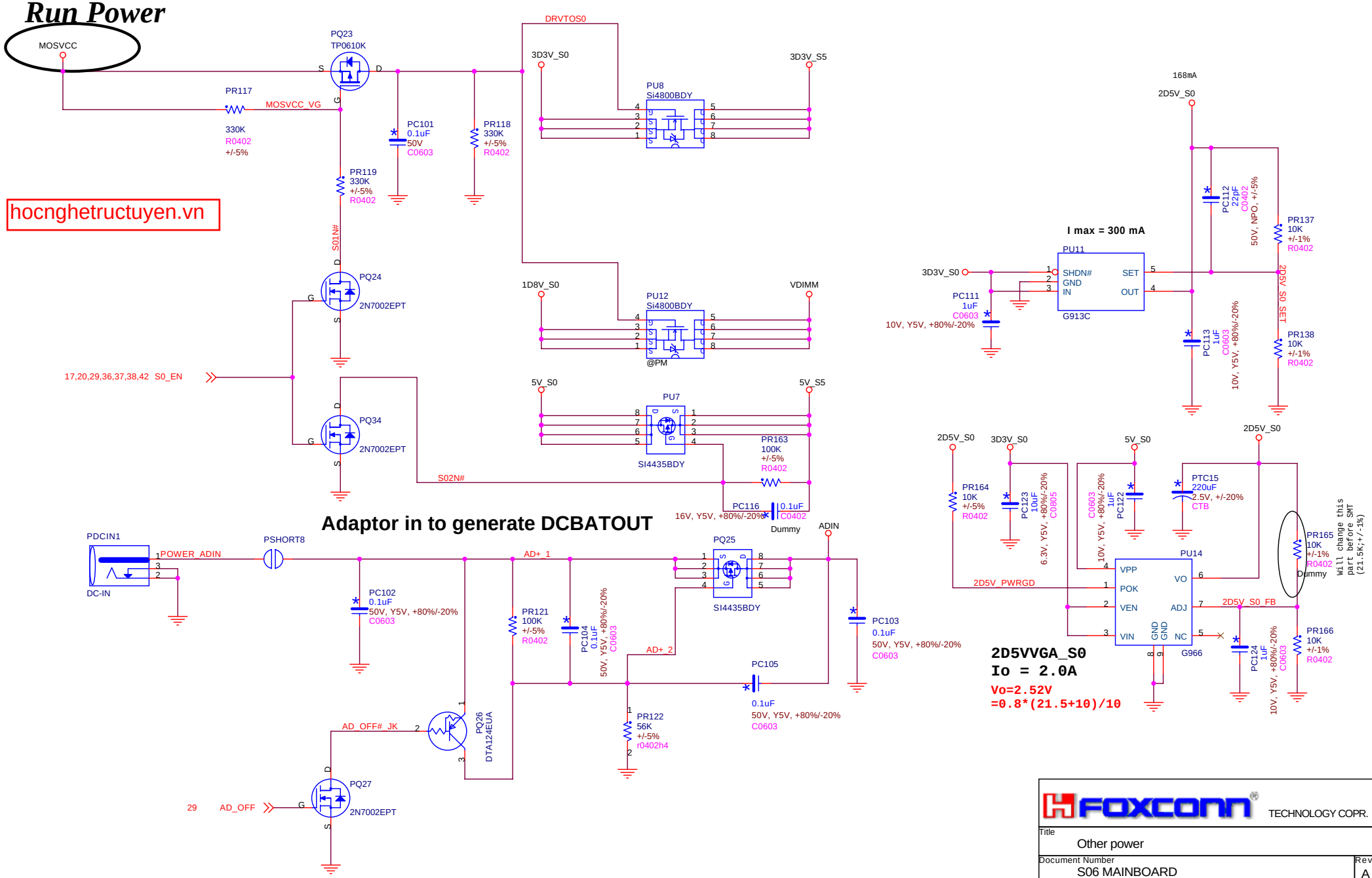
Title: VCORE_SC451

Document Number: S06 MAINBOARD

Rev: A

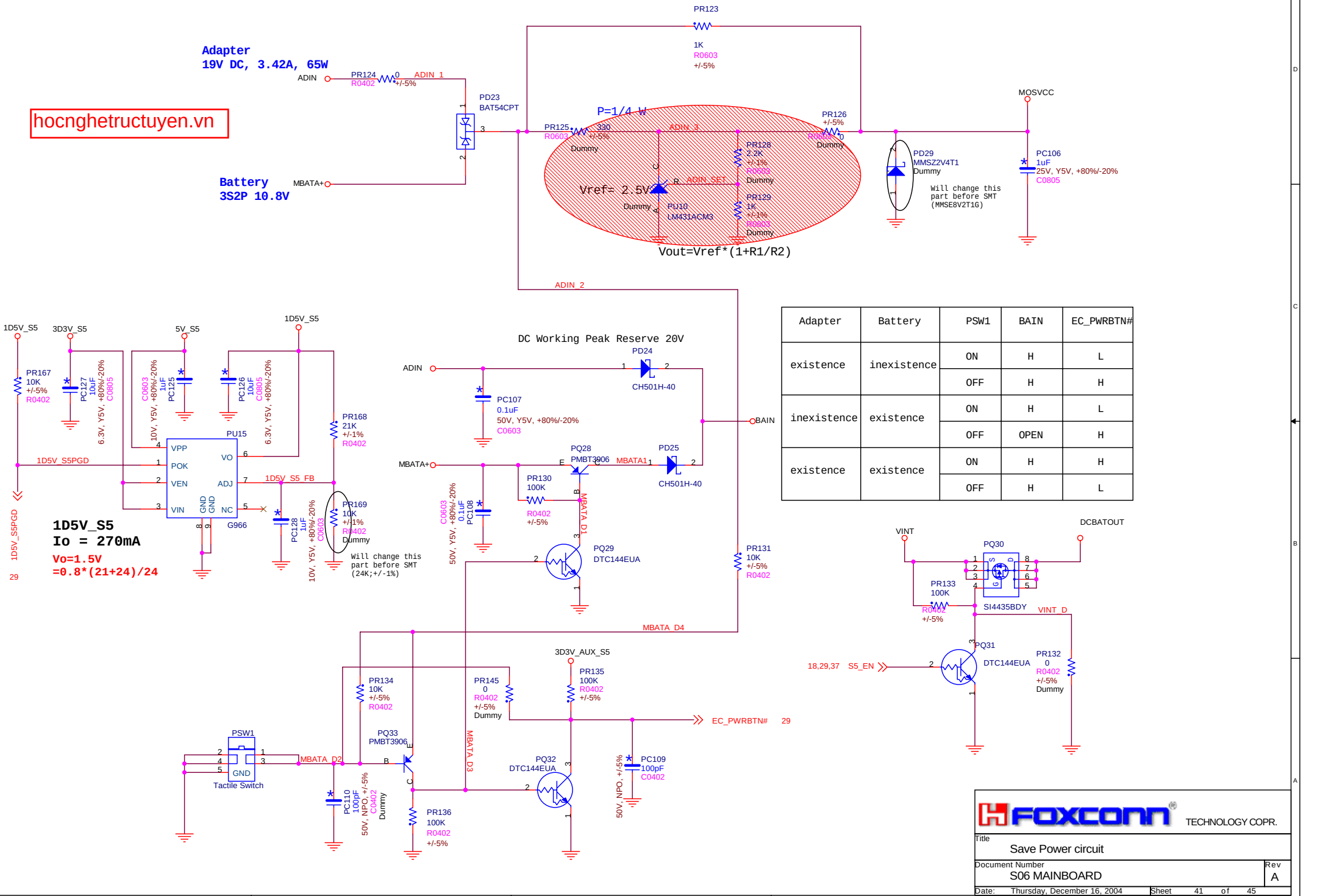
Date: Thursday, December 16, 2004 Sheet 39 of 45

Run Power



FOXCONN TECHNOLOGY COPR.

Title	Other power
Document Number	S06 MAINBOARD
Rev	A
Date:	Friday, December 17, 2004
Sheet	40 of 45



Adapter	Battery	PSW1	BAIN	EC_PWRBTN#
existence	inexistence	ON	H	L
		OFF	H	H
inexistence	existence	ON	H	L
		OFF	OPEN	H
existence	existence	ON	H	H
		OFF	H	L

FOXCONN TECHNOLOGY COPR.

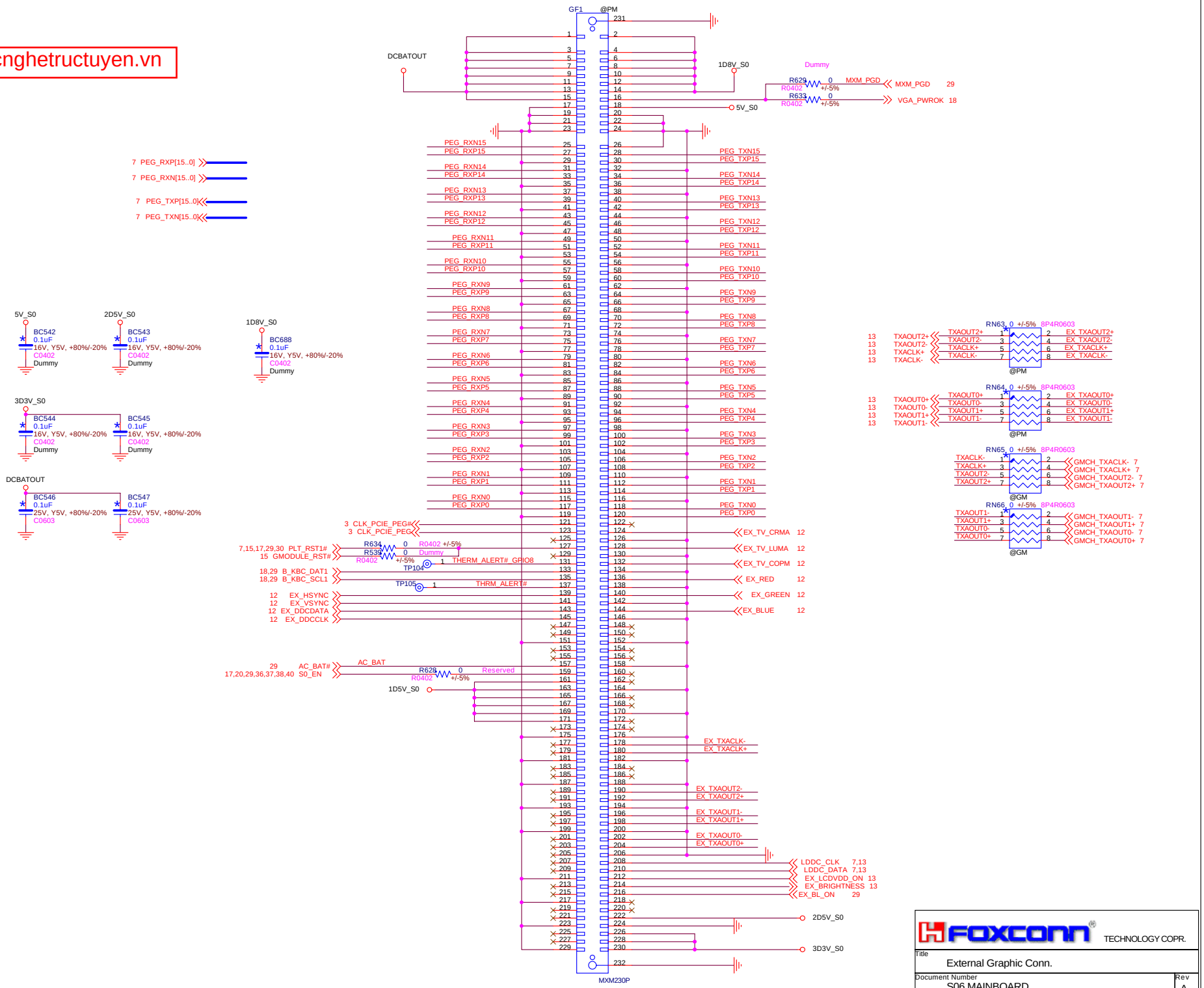
Title: Save Power circuit

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004

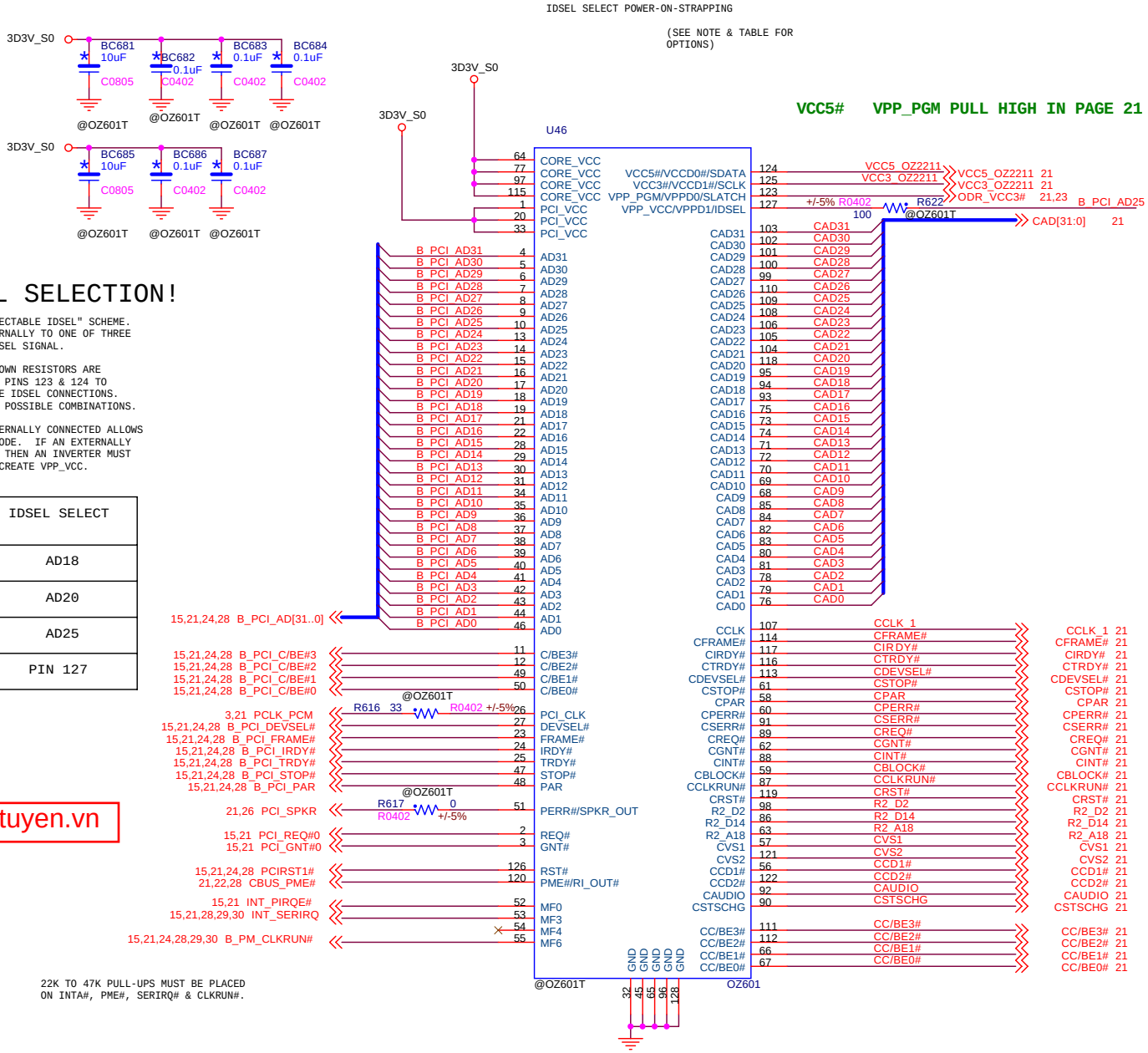
Sheet 41 of 45



Title	External Graphic Conn.
Document Number	S06 MAINBOARD
Rev	A
Date:	Thursday, December 16, 2004
Sheet	42 of 45

FOXCONN TECHNOLOGY COPR.

NOTE:
THIS PAGE SHOWS THE OZ601T CONFIGURED WITH
EXTERNAL IDSEL AND WITHOUT 12V VPP SUPPORT.



NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

FOXCONN TECHNOLOGY COPR.

Title: OZ601T(DUAL LAYOUT)

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004 Sheet 43 of 45

11_09.MOVE VRMPGD BUFFER FROM PAGE 39(VCORE) TO PAGE 16(ICH 3 OF 4)
11_10.Modify T/P Connector Circuit for Material Change
11_10.Modify Parts to Combine BOM
R241 R0402 +/-1% TO R0402 +/-5%
R48 R0603 +/- 1% TO R0402 +/-5%
R47,R57,R84,R85,R86,R113,R114,R115,R178,R179,R180,R197,R200,R203 TO R0402 +/-5%
BC3,BC27,PC69,PC70,PC71,BC283,BC322,BC323,BC339,BC355,BC620,BC472,TC12 TO +80%/-20%, Y5V, 10V, SMD0805 CC0805ZRY5V6BB106
BC450,BC462,BC477,BC478,BC479,BC480,BC481,C19,BC499,BC500,BC501,BC529,BC531,BC532,BC533,BC618,BC622,BC623,BC636,BC514 TO CC0603ZRY5V6BB105 CAP, 1uF, +80%/-20%, Y5V, 10V, SMD0603
BC619,BC637 FROM CAP, 220pF, +/-5%, NPO, 50V, SMD0603 TO CAP, 220pF, +/-5%, NPO, 25V, SMD0402
Q1,Q2,Q4,Q5,PQ5,Q6,Q7,Q18,Q19,Q20,Q21,Q9 FROM MOS N, 2N7002, 7.5 Ohm@Vgs=10V, SOT-23-3P, SMD TO MOS N, 2N7002, 5.3 Ohm@Vgs=4.5V, SOT-23-3P, SMD
BC1,BC534,BC537 FROM CAP, 4.7uF, +/-10%, X5R, 10V, SMD0805 TO CAP, 4.7uF, +80%/-20%, Y5V, 10V, SMD0805
Change CarBus Controler From CB810 to OZ711MP1
11_10. change Q10 TO P-CHANNEL MOS
11_11. Change MDC Suspend Power from 3D3V_Lan_s5 to 3D3v_S5
11_11. Add R604,L13,L14 use TDK
11_11. chang MOS 2N7002 TO VENDOR CHEMKO
change USB to use 0,1,6,7 four Ports
11_12. Modify Parts to combine BOM
change BC12,PC13,C24,C25,C26,BC373,BC374,BC375 from CAP, 0.1uF, +80%/-20%, Y5V, 16V, SMD0603 CC0603ZRY5V7BB104 TO CAP, 0.1uF, +80%/-20%, Y5V, 16V, SMD0402 CC0402ZRY5V7BB104
BC76 FROM CAP, 1uF, +80%/-20%, Y5V, 6.3V, SMD0402 CC0402ZRY5V5BB105 TO CAP, 1uF, +80%/-20%, Y5V, 10V, SMD040 CC0402ZRY5V6BB105
BC581,BC583,BC587,BC589,BC593,BC595,BC597,BC599,BC601,BC603,BC605,BC607,BC609,BC611,BC613,BC615 FROM CAP, 2.2uF, +80%/-20%, Y5V, 16V, SMD0805 CC0805ZRY5V7BB225 TO CAP, 2.2uF, +80%/-20%, Y5V, 10
BC409,BC307 FROM CAP, 22uF, +80%/-20%, Y5V, 10V, SMD1206 CC1206ZRY5V6BB226 TO CAP, 22uF, +/-10%, X5R, 6.3V, SMD1206 CC1206KRX5R5BB226
BC378,BC380,BC381,BC382,BC385,BC389,BC395 FROM CAP, 4.7uF, +/-10%, X5R, 6.3V, SMD0805 CC0805KRX5R5BB475 TO CAP, 4.7uF, +80%/-20%, Y5V, 10V, SMD0805 CC0805ZRY5V6BB475
11_12. Modefy CR1 S_VCC Pin CONNECT to SD/MS/XD_DATA1
11_13. Page21, add CarBus PME# signal connection to ICH6
11_13. Page 20 change R345 Dummy
11_13. Change U4A,U4B,U4C to 74HCT1G125GW U36,U37,U38
11_13.Change R352,R353,R354,R355 R493,R494,R495,R496,R497,R498,R499,R500 TO 0402 0 ohm
11_14.Page 7 Modefy the Level Shift circuit,change R507,R508 Reserved,Q18,Q19,R506 @GM
11_14. Replace LAN FB with 0 Ohm,include FB3,4,5,6,7
11_14.Change R352,353,354,355 to 1% tolerence
11_15.Change R34,R40 Reserved
11_15.change R133,R140 to R0805
11_15 add R612,R613
11_15 chang Page 25 Lan Transformer H5062@Giga and H1285@8100c
11_15. Add BC679,BC680
11_16 Change R260 Dummy,R539 Reserved
11_18 Change L13,L14 to TDK ACM2012-900-2P-T000
11_18 page 7 Del some CFG pins and TestPoints to meet Layout needs
11_22. change R368 Reserved
11_23. Updated connector accroding ME's request Audio Jack, RTC header, Battery CONN changed
11_24. UPDATED EXTERNAL GRAPHIC CARD, DEL GID SIGNALS

11_25 BC403 Change to 10u, del BC407,C25,BC411,R614,R615,DUMMY BC434,BC435,BC438,BC439,R389,R391,R392,R346,Q9
CHANGE BC417,BC418,BC428,BC429 TO Y5V 0603,CHANGE C23 TO 0402 Y5V,C24 TO 4.7U 0805 Y5V
DEL BC458,BC459,R434,R440,R444,R404,BC461,R434,R538,CHANGE BC530 TO Y5V,R489,R490,R491,R492,BC450 TO 0402
DUMMY U29,U28,R537,R538,BC621,RN61,RN62,R387,R413,R414,R405,BC478,BC479,BC480,BC481
ADD BC689,BC690,BC691,R618,R619,R620,R621,R622,R542,MOVE ISET,VSET TO DA4,DA5 CHANGE R326 TO 20K 0402
CHANGE BC403 TO TOLERANCE 10%,BC404 TO Y5V,

12_07 add R630 R631, DUMMY R95,R96,R613 DEL R474,R539,R147

11_26
ADD R623,R624,NET RTC SENSE, CHANGE OZ601T REMARK TO @OZ601T
MOVE R622 FOR IDSEL, MODIFIED IT TO 100OHM,ADD R623,R625,R626,
DUMMY R18,R26,CHANGE TC1,TC2,TC13,TC14,TC9,TC15,R447,R448

12_2 DEL SMBUS OF LAN,DEL R518,R542,ADD R627,R628,BC692,CHANGE R518 TO 22ohm, CHANGE D37,CORRECT AC'97 BIT CLOCK
CHANGE BC622,BC623 TO 0.47U,BC499 TO 10U, BC500 TO 0.1U,TC1,TC2 TO C2016M0100SD

12_3 ADD R629,R630,R631,DEL R540
DEL EC's 168 pin, DEL SMI# OF EC, ADD THERMAL ALERT TO EXT_GRAHPIC

12_4
1.change PR56 to 0603 1K (RC0603JR-071K)
2.PR18 change to 0603 0ohm (RC0603JR-070R)
3.OZ8604LN pin7 name change to REF3D3V
4.VSET ISET need pull low with 10K
5.ADD PD27 (SSM54PT)
6.ADD PR152-PR156 (RC0402JR-0710K)
7.ADD PR159 (RC0402JR-0733K)
8.ADD PC117,PC118 (CC0402ZRY5V7BB104)
9.CHANGE PC16 TO 0.47uF (CC0805ZRY5V8BB474)
10.CHANGE PR59,PR70 TO 120K (RC0603FR-07120K)
11.CHANGE PR60,PR71 TO 45.3K (RC0603FR-0745K3)

12_15 Change BC444 Reserved,R185,R186 @GM

1.PC1,PC3 CHANGE TO REQUEST
2.PC17 CHANGE TO 4.7uF
3.OZ860 Pin17:AGND
4.OZ824 PGD2 PULL HIGH 3D3V_S5
5.OZ824 SKIP2 CONNECT TO 3D3V_S5
6.OZ824 Pin6,7 VDDA,CE CONNECT TO 5V_S5
7.PC14,PC34 CHANGE TO REQUEST
8.PC39,PC48 PC33 PC42 PC67 CHANGE TO REQUEST
9.PQ24,PQ5,PQ9,PQ27 CHANGE TO 2N7002EPT
10.PQ3 CHANGE TO TP0610K
11.PD10,PD11,PD12 CHANGE TO SSM24PT
12.PD19 CHANGE TO CH501H-40
13.PTC1 CHANGE TO 4TPE220MIC
14.ADD ONE PU10:Si4800BDY
15.PR22 CHANGE TO REQUEST
16.ADD NETNAME

2004年11月13日
1.PC13(CC0603ZRY5V7BB104) CHANGE TO CC0603ZRY5V8BB104
2.PC15(CC0603ZRY5V5BB225) CHANGE TO CC0603ZRY5V6BB225
3.PC99(CC0402JRNPO9BN221) CHANGE TO CC0402JRNPO8BN221

2004年11月17日
1.PR115 (RC0603FR-0754K9) CHANGE TO RC0402FR-0754K9
2.PC27,PC28 (CC0603KRX7R8BB104) CHANGE TO CC0603ZRY5V8BB104
3.ADD TWO BY PASS CAP PC114,PC115 (CC0402ZRY5V7BB104) TO OZ860 PIN3&PIN16
4.MAX1999 ADD LOW4 PROTECT CKT
5.CHANGE PD13 (DUMMT) TO DUMMY
6.PC13 (CC0603ZRY5V8BB104) CHANGE TO CC0402ZRY5V7BB104

2004年11月19日
1.ADD PQ34 2N7002EPT
2.CHANGE PU7 TO SI4435BDY
3.ADD PR143 RC0402JR-07100K
4.ADD PC116 CC0402ZRY5V7BB104

2004年11月24日
1.ADD PR145（DUMMY） RCO4O2JR-070R
2.ADD PR144（DUMMY） RCO6O3JR-074K7
3.CHANGE PR139 TO RCO4O2JR-07300K
4.CHANGE PR140 TO RCO4O2JR-07100K

2004年11月25日
1.CHANGE PR12 PR13 TO 33m (WSL2512R0330FEK)
2.CHANGE PTC2 PTC3 TO (TLPSLV0J157M(18)12RE)

2004年11月29日
1.CHANGE PR56 TO 1K (RC0402JR-071K)
2.CHANGE PR64 TO 45K (RC0402FR-0745K)
3.CHANGE PR65 TO 105K (RC0402FR-07105K)
4.CHANGE PL5 TO 3.3uH (IHLP2525CZRZ3R3M01)
5.CHANGE PR17 TO (RC0402JR-0722K)

2004年12月1日
1.CHANGE PU1 TO OZ8604LN
2.P35:ADD FUNCTION:CHARON#/OFF,AND BTSENSE
3.ADD PR148,PR149,PR150,PD27,PQ35
4.CHANGE PR 62 (RC0402FR-07100K)

FOXCONN TECHNOLOGY COPR.

Title: HISTORY
Document Number: S06 MAINBOARD
Rev: A
Date: Thursday, December 16, 2004
Sheet 44 of 45

Device / Rails	CPU	GMCH	ICH6-M	ENE3910	DDRII	Audio	HDD	ODD	LCD	INV	USB2.0	LAN	SIO	OZ711	CLK GEN	EXT VGA
3D3V_AUX_S5				●												
5V_AUX_S5																
3D3V_S5			●									●				
5V_S5																
1D5V_S5			●													
VDIMM (1D8V_S3)		●			●											
VTT_MEM (0D9V_S0)					●											
3D3V_S0		●	●		●	●			●	●			●	●	●	●
5V_S0						●	●	●		●	●			●		
2D5V_S0		●	●													●
1D5V_S0	●	●	●													●
1D05V_S0	●	●	●													
VCC_CORE_S0	●															
1D8V_S0																●
DCBATOUT										●						●

FOXCONN TECHNOLOGY COPR.

Title: POWER PLANE

Document Number: S06 MAINBOARD

Rev: A

Date: Thursday, December 16, 2004

Sheet 45 of 45