LZ2 Block Diagram

Project code: 91.4K101.001 ZY LZ2
91.4J301.001 XR LX2
PCB P/N : 07260-SB
Revision : SA

CLK GEN. 3

Mobile CPU
Penryn SV 35W
4, 5

EMC2102 07

HOST BUS 800/1066MHz@1.05V

DDR3 socket 15 — 800/1066MHz

DDR3 socket 16 — 800/1066MHz

Cantiga 8,9,10,11,12,13,14
- AGTL+ CPU I/F
- DDR Memory I/F
- INTEGRATED GRAHPICS
- LVDS, CRT I/F

R.G.B → CRT 18

LVDS → 12"W LCD 17

X4 DMI 400MHz

C-Link0

ICH9M 19,20,21,22,23
- 6 PCIe ports
- PCI/PCI BRIDGE
- ACPI 1.1
- 4 SATA
- 12 USB
- High Definition Audio
- LPC I/F
- Serial Peripheral I/F

INT MIC

SPR x2

Codec ALC269 (include AMP) 25 — AZALIA

MIC In

HP

RJ11 — MODEM MDC Card 24

USB → Realtek RTS5158E Cardreader 28 → SD/MMC/MS 3 in 1 28

PCIe → LAN Boardcom 5906M 26 → RJ45 27

PCIe/ USB → Mini Card a/b/g/n 31

LPC BUS → KBC Winbond WPC776 29 (SPI I/F → BIOS 2M byte 34; G-sensor 30; Touch Pad 34; INT. KB 34)

LPC DEBUG CONN. 24

New card 31 — PCI Express / USB

Power switch 31

SATA → SATA-HDD 24

SATA → SATA-ODD 24

USB → Finger Print 32; BlueTooth 24; CAMERA 17; USB 3 Port 32

PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3

TPS51100 38

1D5V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
1D5V_S3	33 1D5V_S0

CHARGER BQ24740 39

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V UP+5V 5V 100mA

CPU DC/DC ADP3208 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

<Variant Name>

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Friday, April 11, 2008 | Sheet 1 of 41

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved Rising Edge of PWROK.	This signal has a weak internal pull-down. Note:This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap(Server Only) Rising edge of PWROK	Tying this strap low configures DMI for SIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server latforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG11 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1= The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE1	BroadCom LAN
LANE2	MiniCard WLAN
LANE4	NewCard

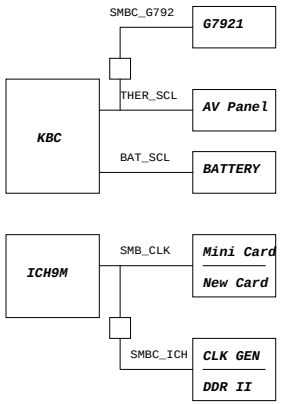
History:

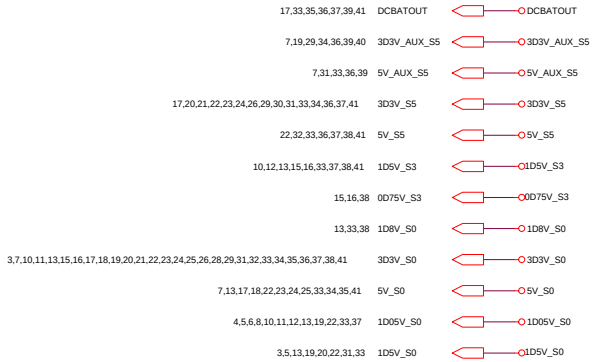
LAB: 2008/01/02

USB Table

USB	
Pair	Device
0	JACK0
1	NC
2	JACK2
3	NC
4	BLUETOOTH
5	JACK1
6	Fringer Print
7	Mini Card
8	CAMERA
9	NEW CARD
10	CARDREADER
11	NC

SMBus





<Variant Name>

Wistron Corporation
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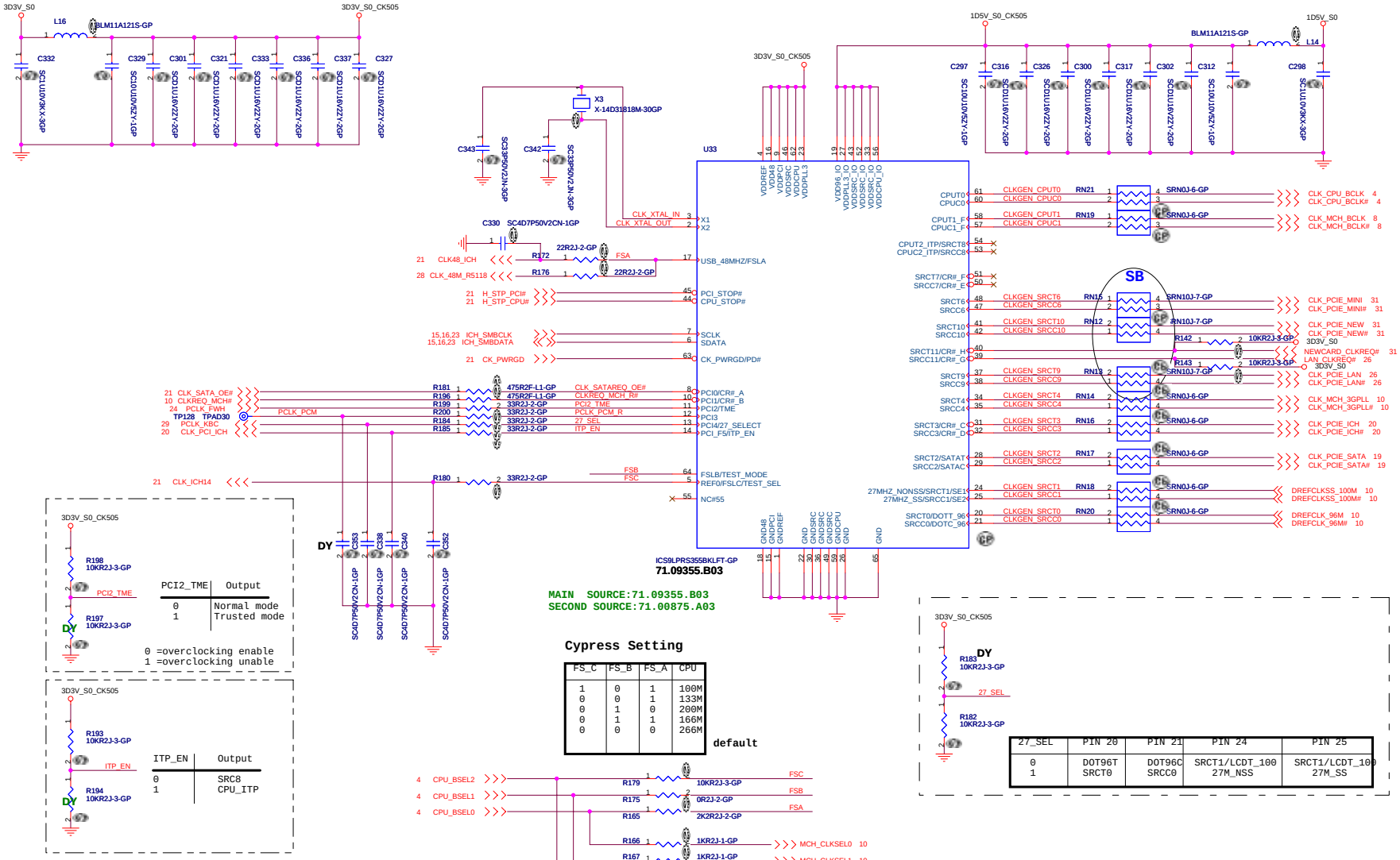
Title: Reference

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 2 of 41



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

Wistron Corporation
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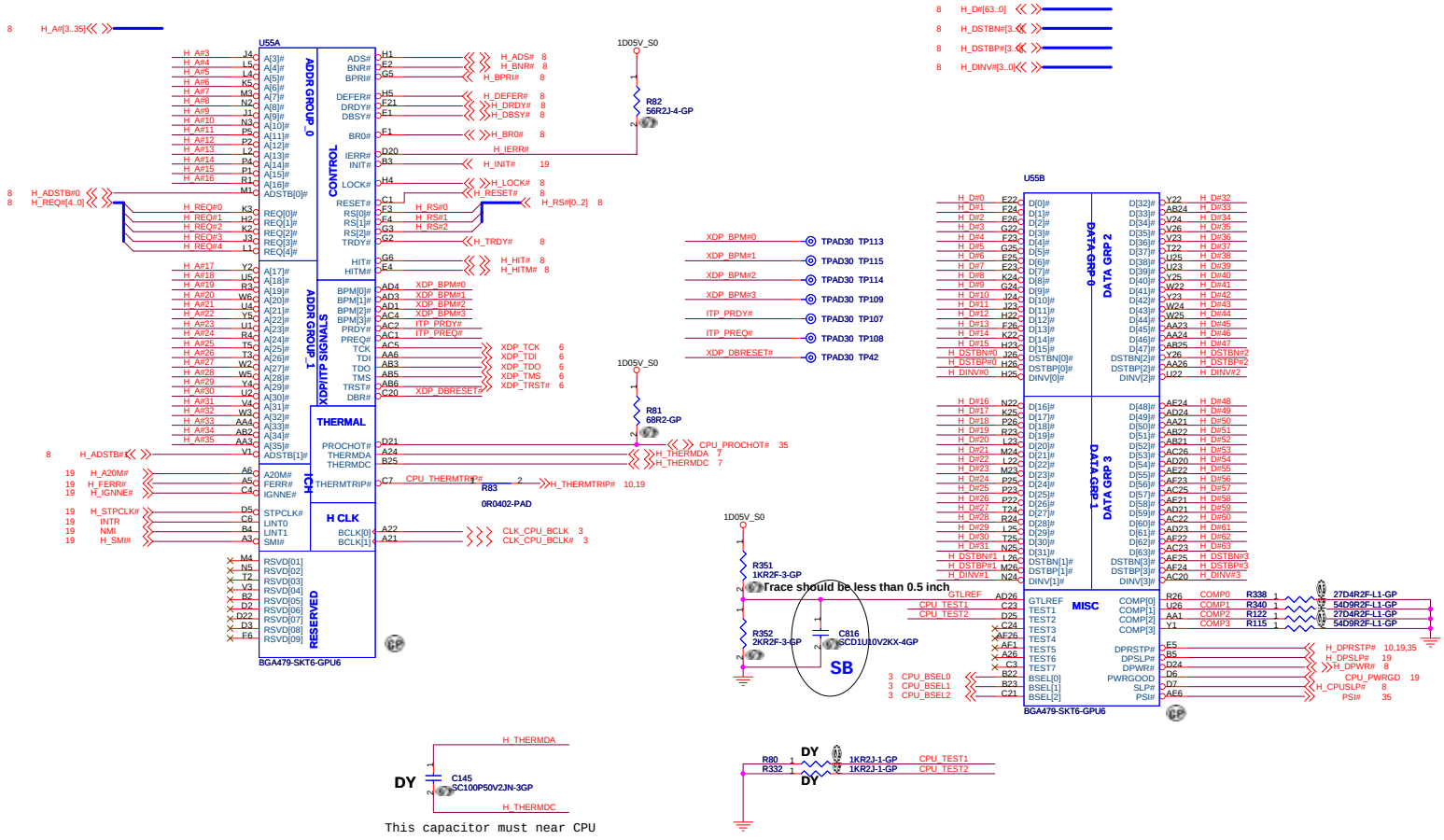
Title: Clock Generator

Size: | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 Sheet 3 of 41



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Wistron Corporation
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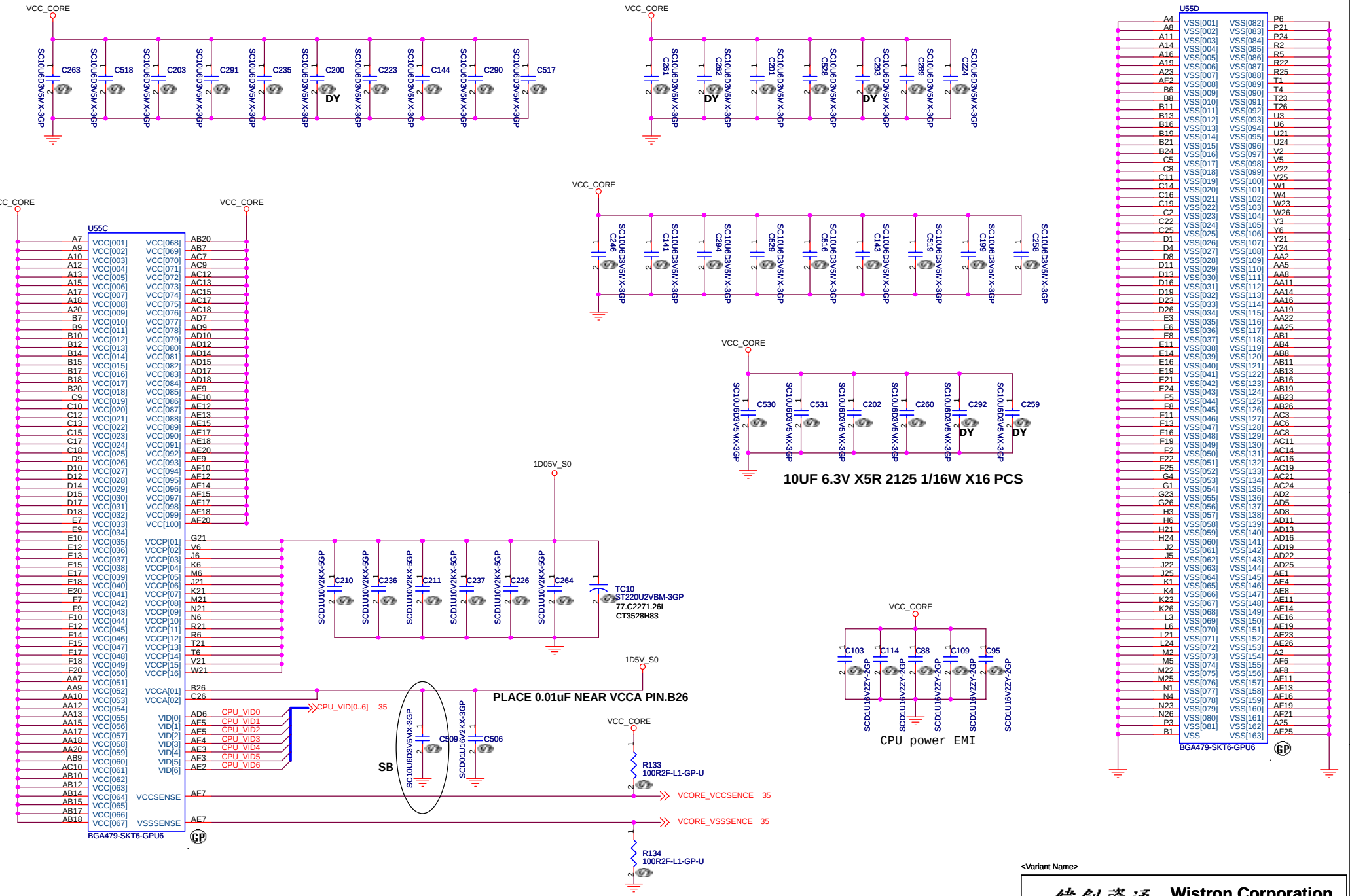
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Penryn CPU(1/2)**

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 4 of 41



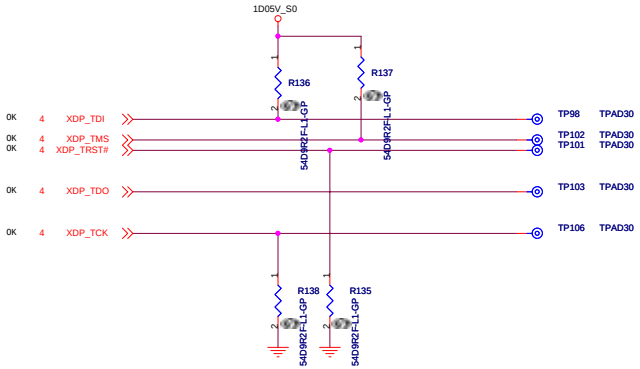
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(2/2)

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 5 of 41



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *ITP CONN*

Size	Document Number	Rev
C	LZ2	SB

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Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing

Layout notice :
Both H_THERMDA_1 and THERMDC_1 routing
10 mil trace width and 10 mil spacing

Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing

Layout 15 mil

Layout notice :
C809, C811, C812
close to chip side;

CPU0

SYSTEM

This cap should close to thermal diode.

EMC2102

EMC2102-DZK-GP
74.02102.A73

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

SC

U96
NC7SZ08P5-GP
73.7SZ08.AAH
220ms delay time after Power-on

Dummy when G792 enhanced T8 function

HW thermal shut down tempature
setting 95 degree . Put Near CPU .

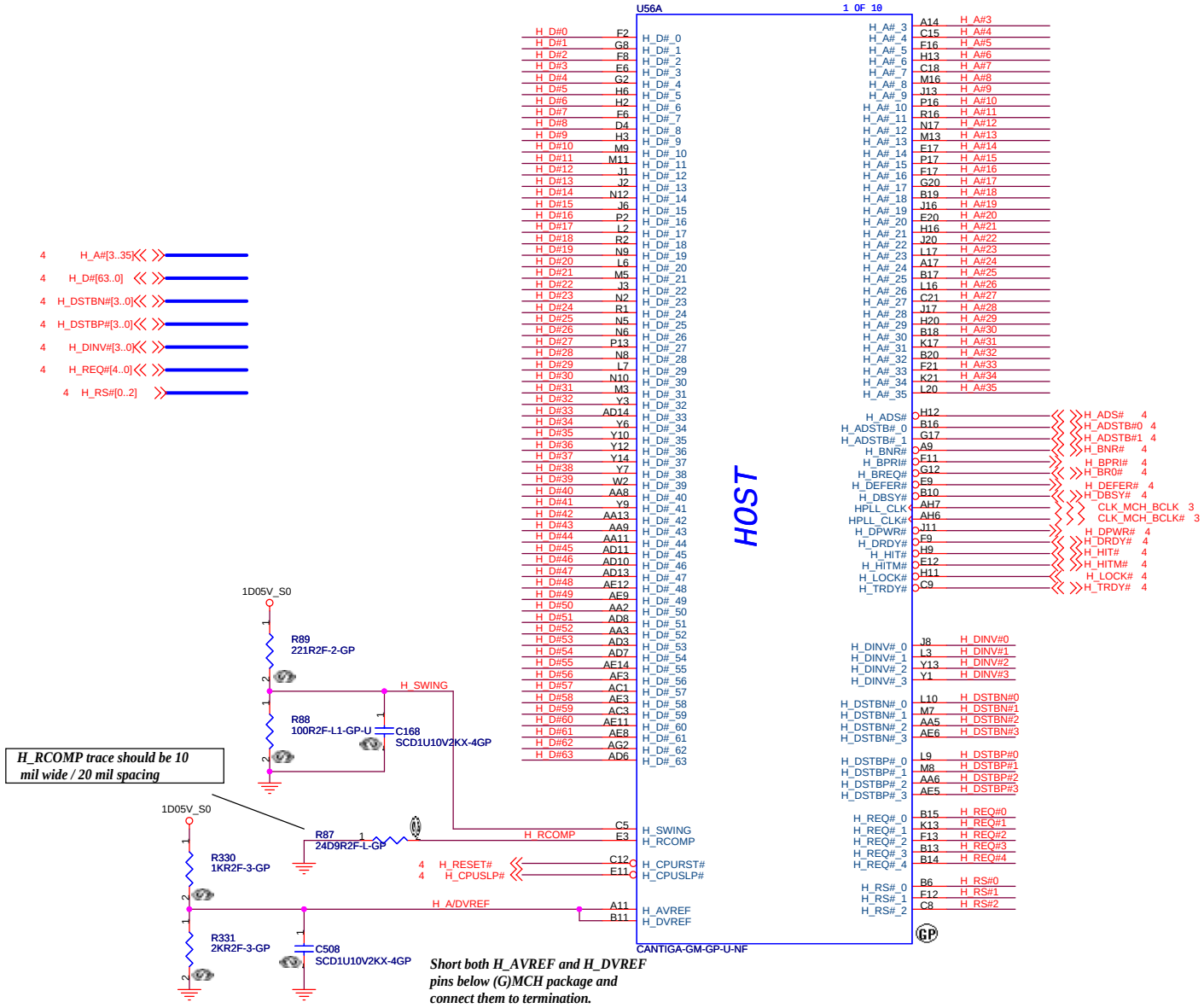
U28
G709T1UF-GP

Rset=0.0012*T^2-0.9308*T+96.147

D16
BAW56W-7-F-GP

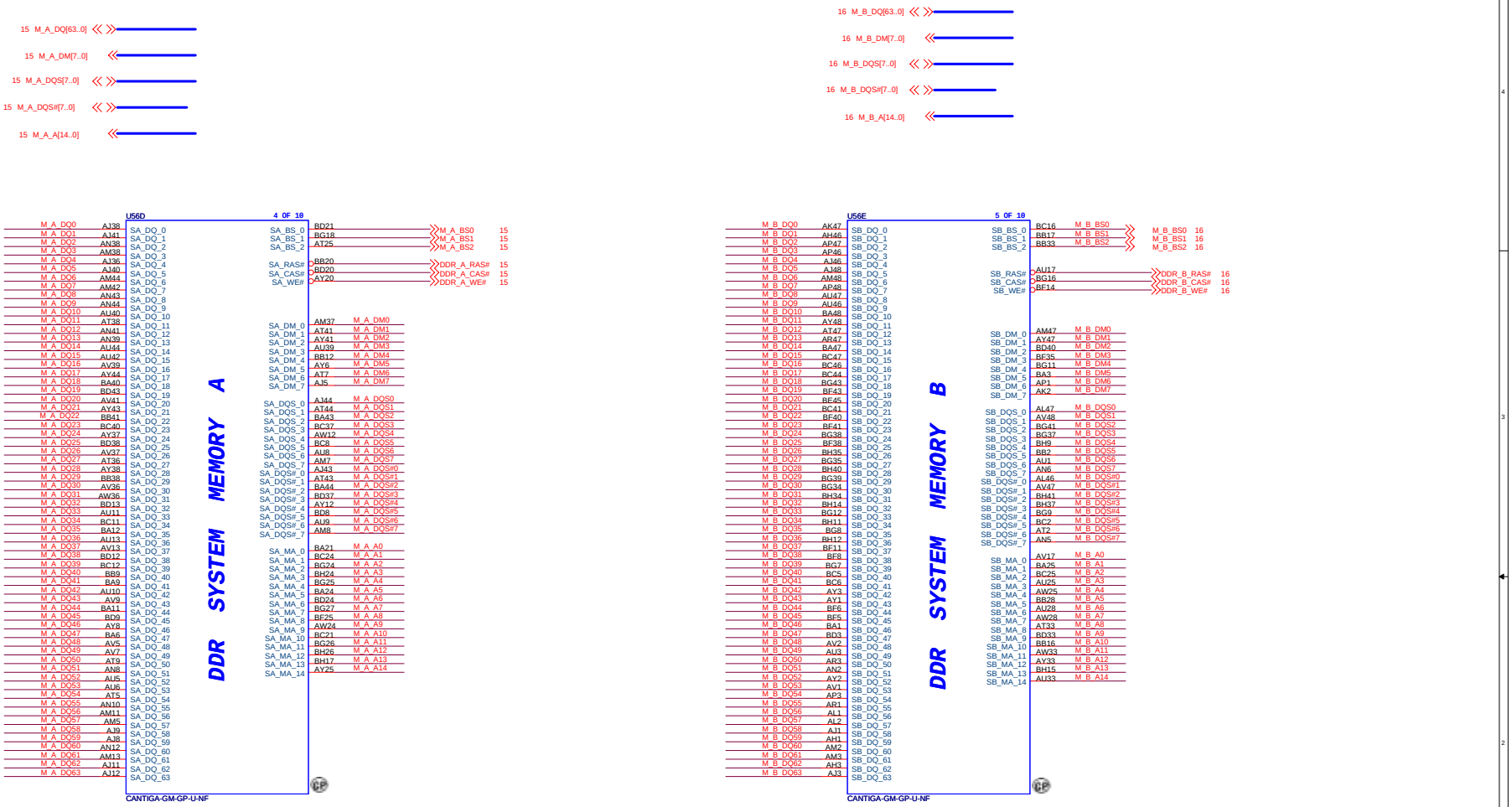
D23
BAT54-4-GP

BOM1	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thermal/Fan Controllor EMC2102
Size: Custom	Document Number: LZ2
Rev	SB
Date: Wednesday, April 16, 2008	Sheet 7 of 41



<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Cantiga(1/7):HOST I/F		
Size: A3	Document Number: LZ2	Rev: SB
Date: Wednesday, April 16, 2008	Sheet 8 of 41	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<variant_name>

Title: Cantiga(2/7):DDR3

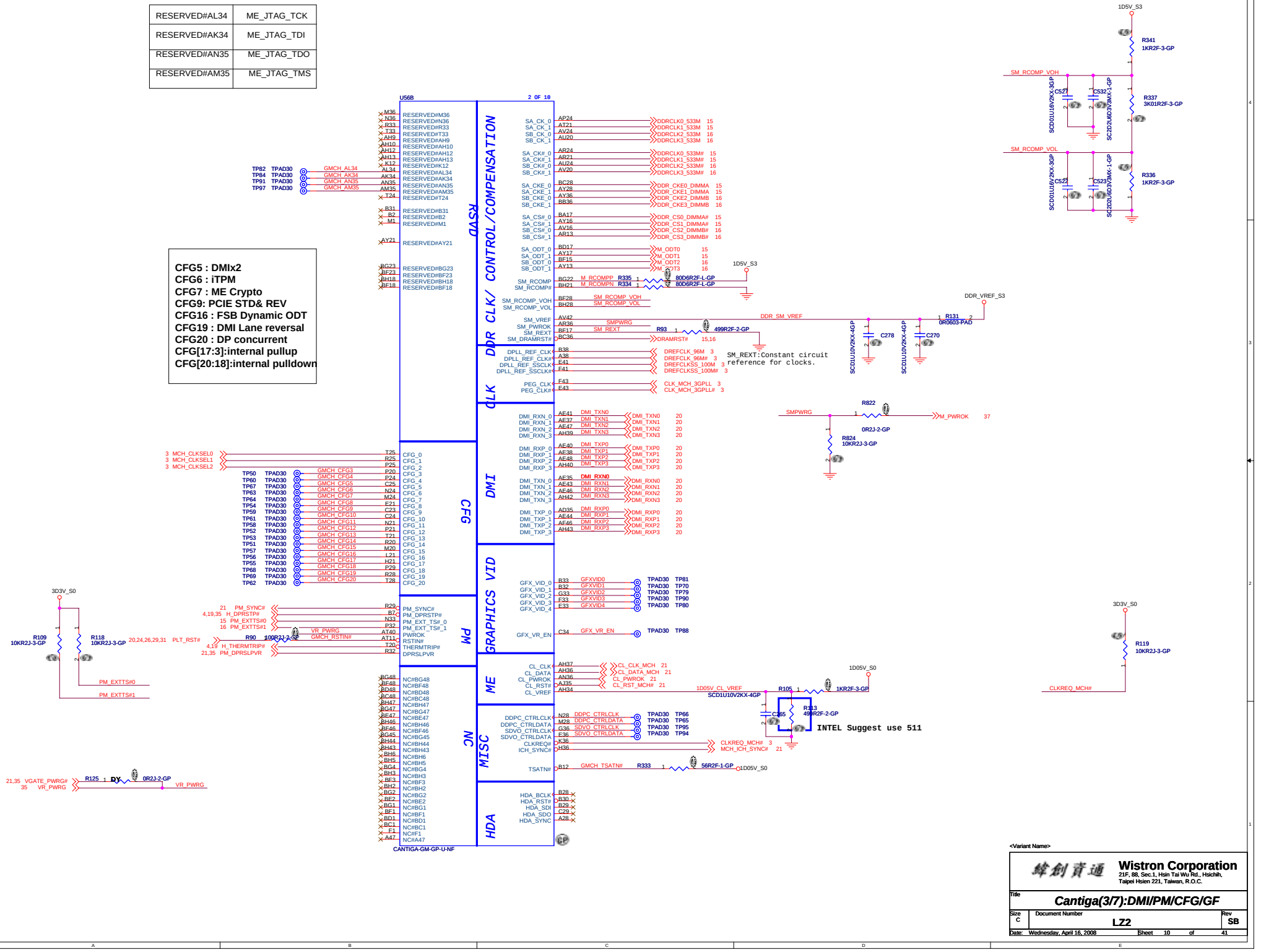
Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 9 of 41

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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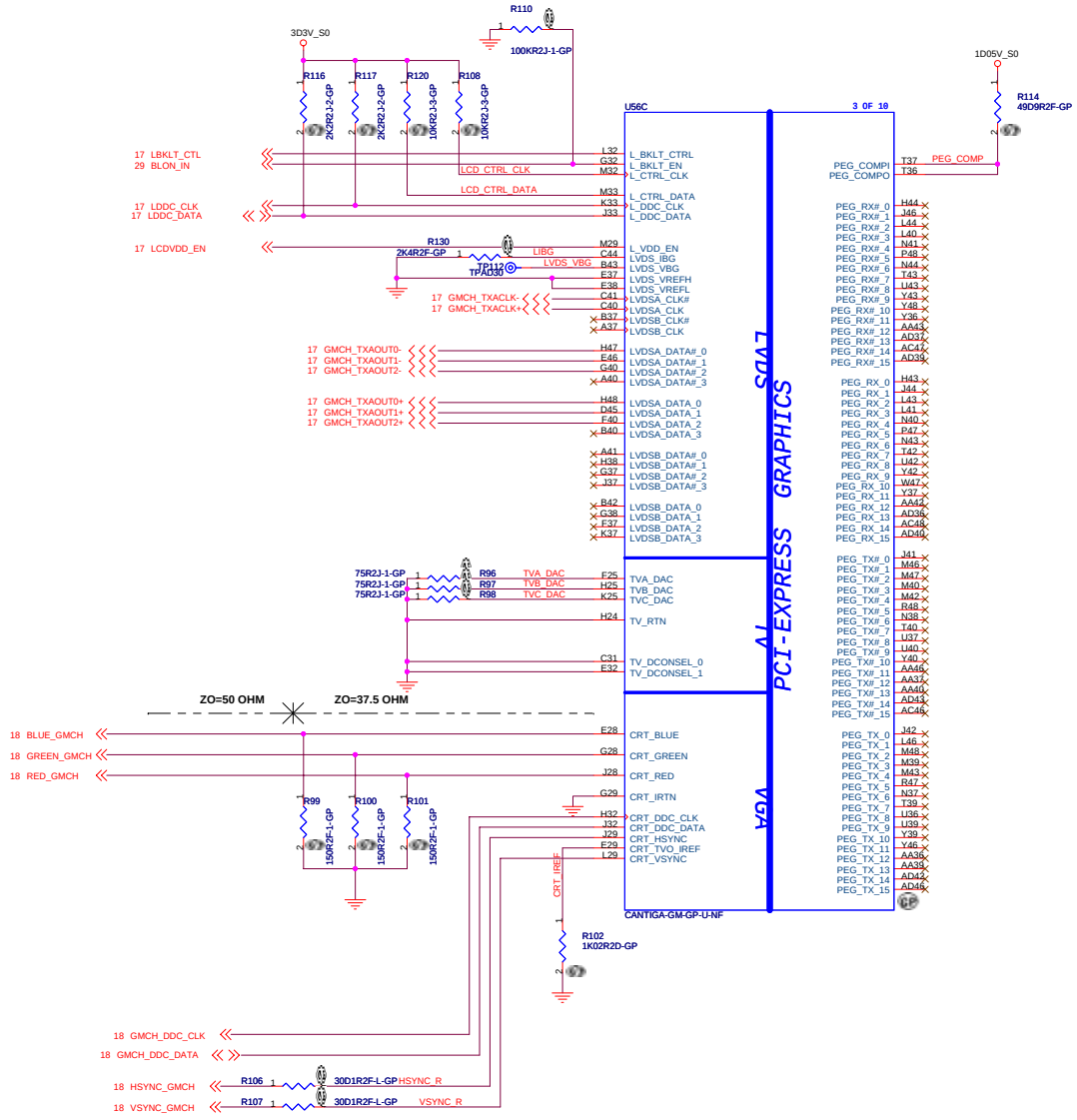
Title: Cantiga(3/7):DMI/PM/CFG/GF

Size: C | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 10 of 41



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Wistron Corporation
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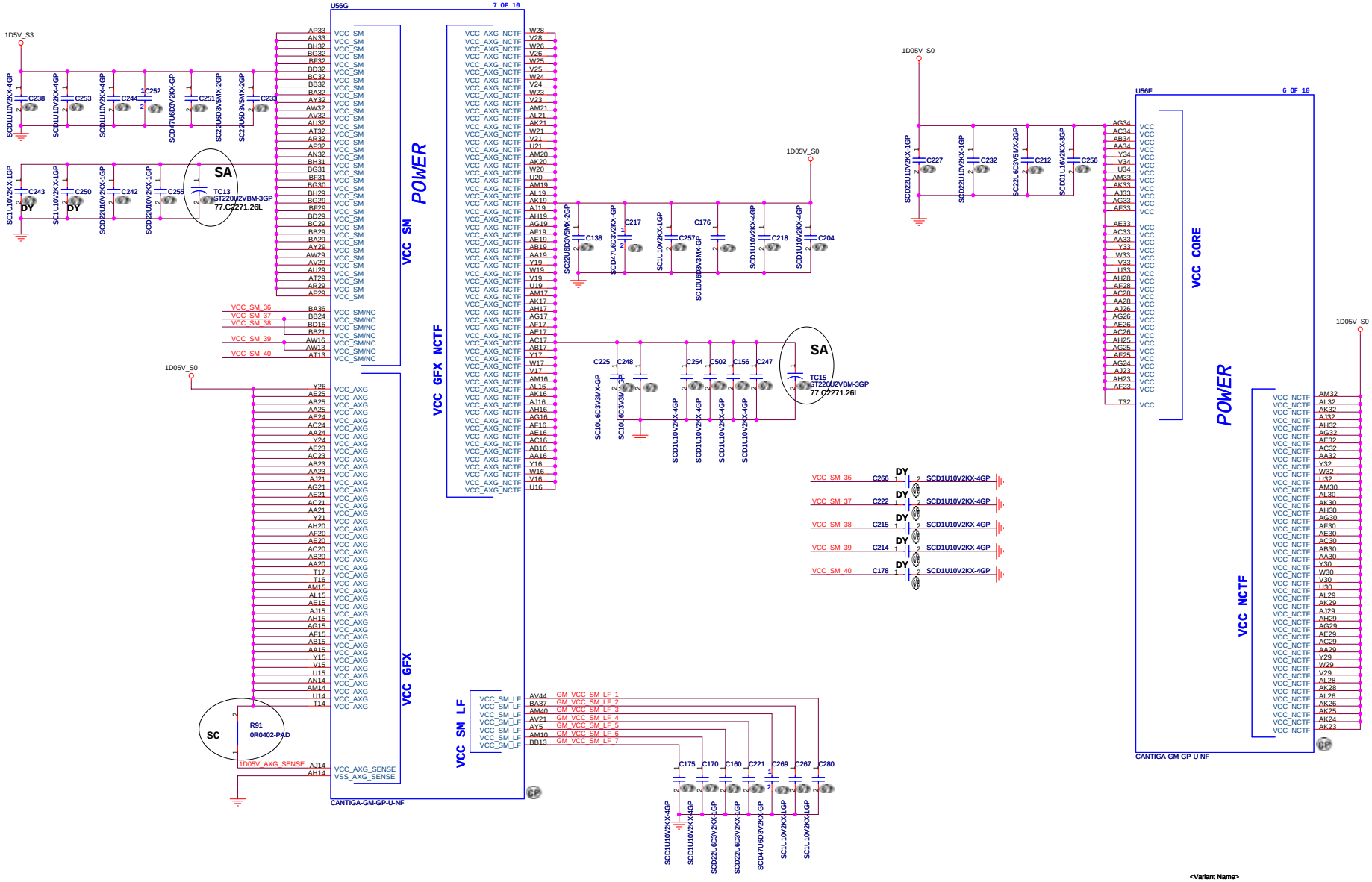
Title: CANTIGA(5/7)-VGA/LVDS

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 11 of 41



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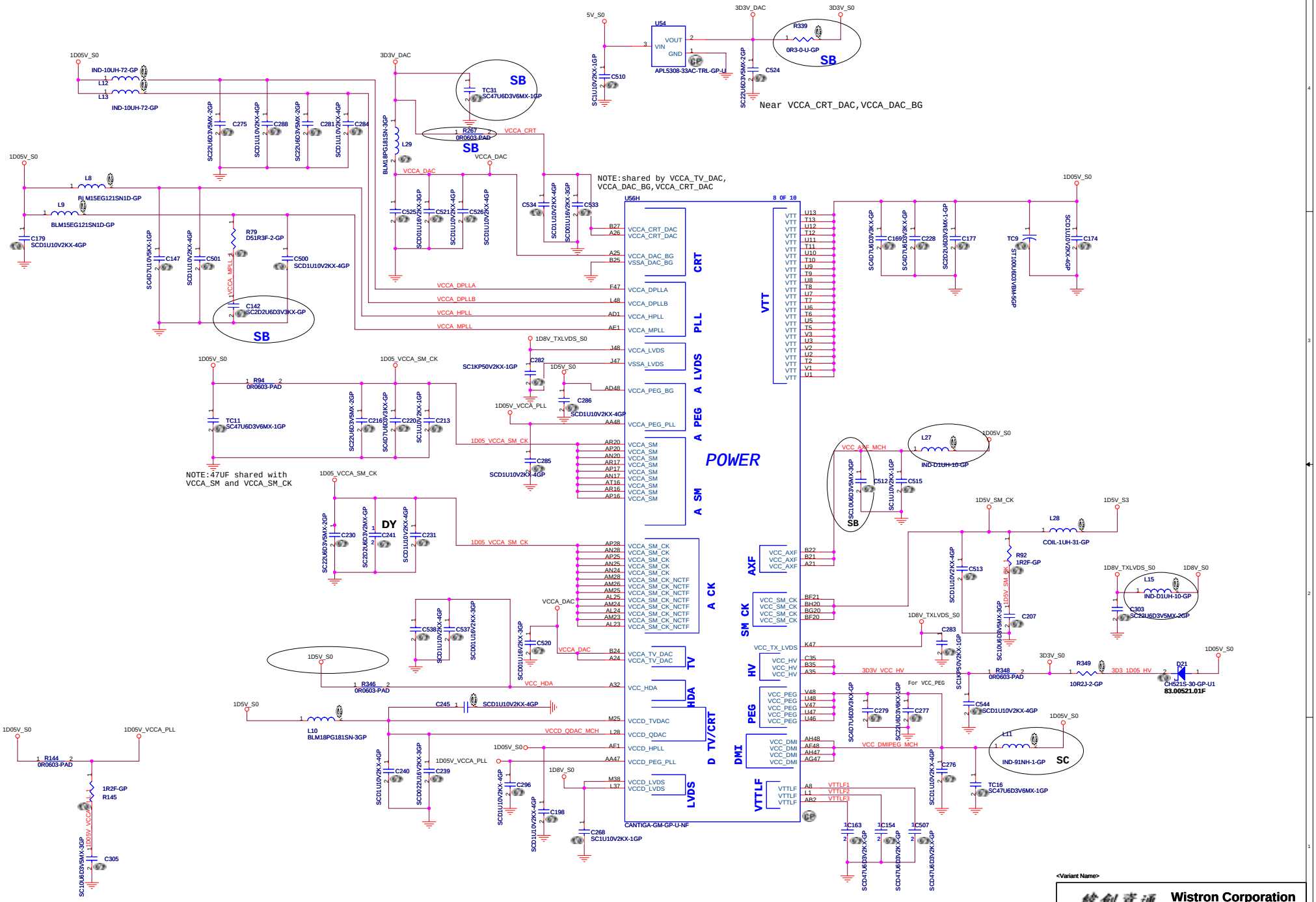
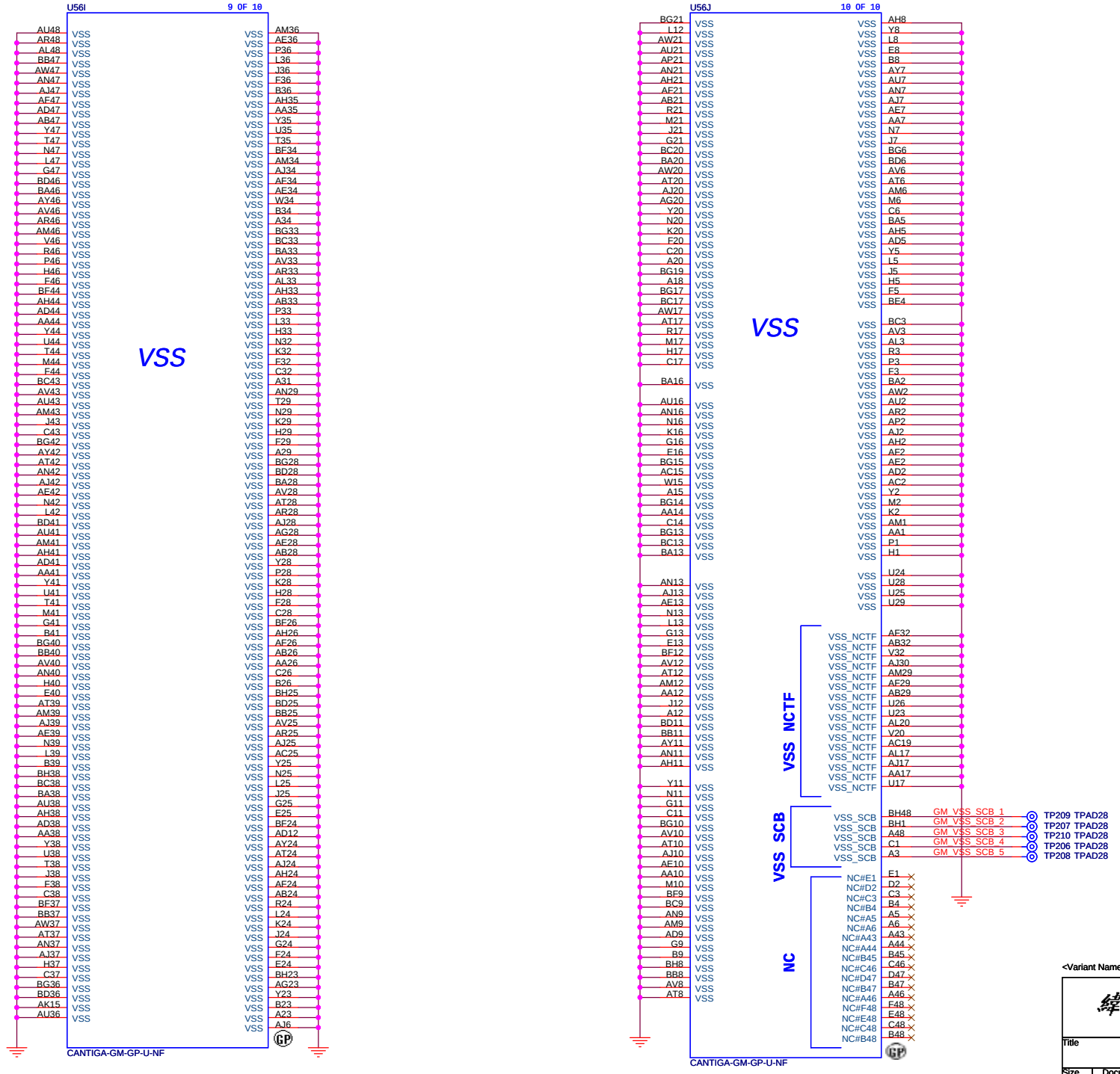
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(5/7):VCC

Size	Document Number	Rev
C	LZ2	SB

Date: Friday, April 11, 2008 Sheet 12 of 41


U56H
8 OF 10
POWER
CANTIGA-GM-GP-U-NF
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
NOTE:shared by VCCA_TV_DAC, VCCA_DAC_BG,VCCA_CRT_DAC
Near VCCA_CRT_DAC,VCCA_DAC_BG
NOTE:47UF shared with VCCA_SM and VCCA_SM_CK
SB
DY
1D05V_S0
3D3V_DAC
3D3V_S0
5V_S0
1D05V_VCCA_PLL
1D05_VCCA_SM_CK
1D8V_TXLVDS_S0
1D8V_S0
1D05_S3
1D05V_SM_CK
3D3V_VCC_HV
3D3_1D05_HV
VCC_DMIPEG_MCH
For VCC_PEG
VCCA_CRT
VCCA_DAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCC_HDA
VCCD_QDAC_MCH
VCC_AXF_MCH
U54
APL5308-33AC-TRL-GP-U
IND-10UH-72-GP
IND-D1UH-10-GP
IND-91NH-1-GP
COIL-1UH-31-GP
0R3-0-U-GP
0R0603-PAD
1R2F-GP
10R2J-2-GP
CH521S-30-GP-U1
83.00521.01F
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga(6/7):VCC
Size C
Document Number LZ2
Rev SB
Date: Friday, April 11, 2008
Sheet 13 of 41



<Variant Name>

緯創資通 **Wistron Corporation**
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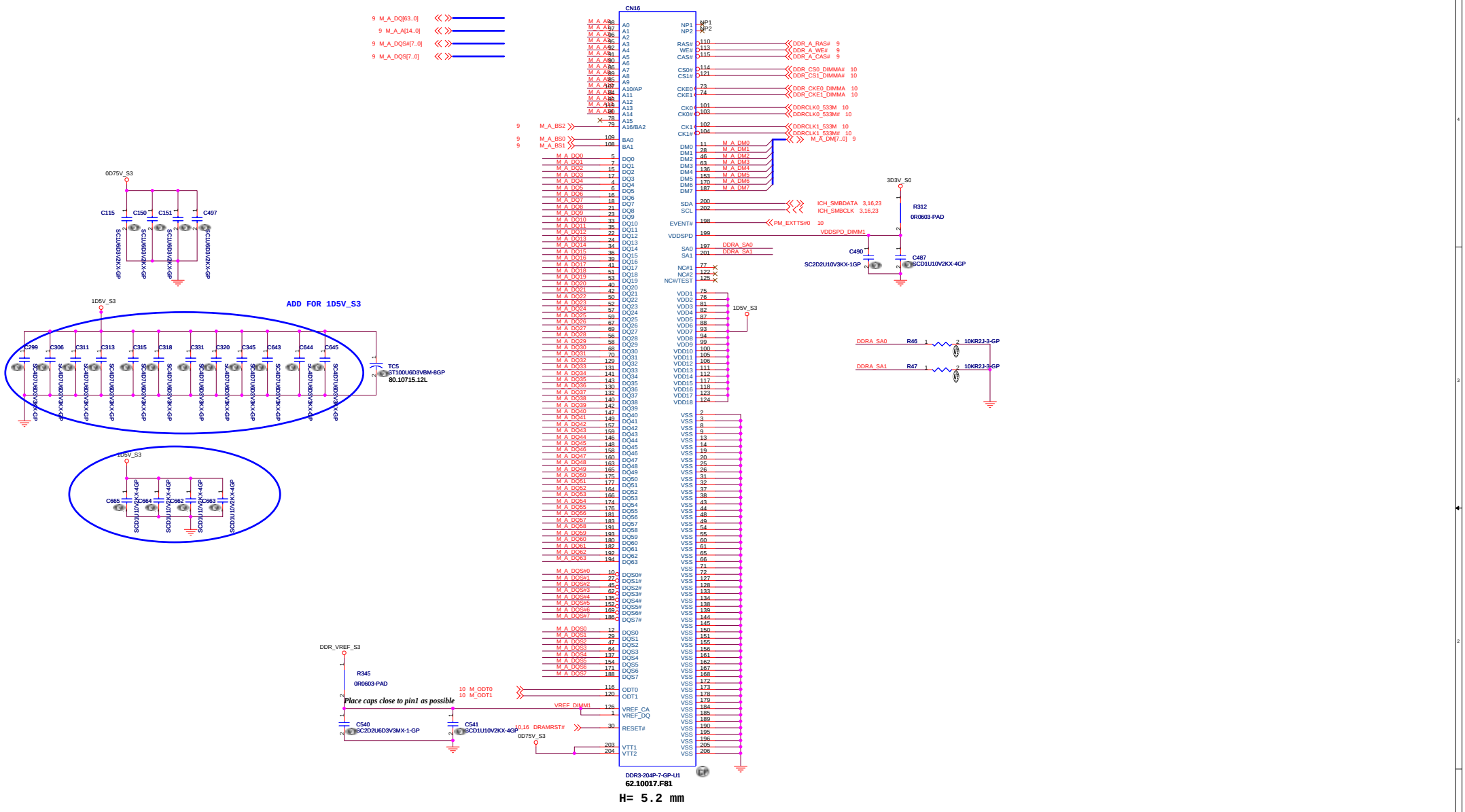
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga(8/7):GND**

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 09, 2008 Sheet 14 of 41



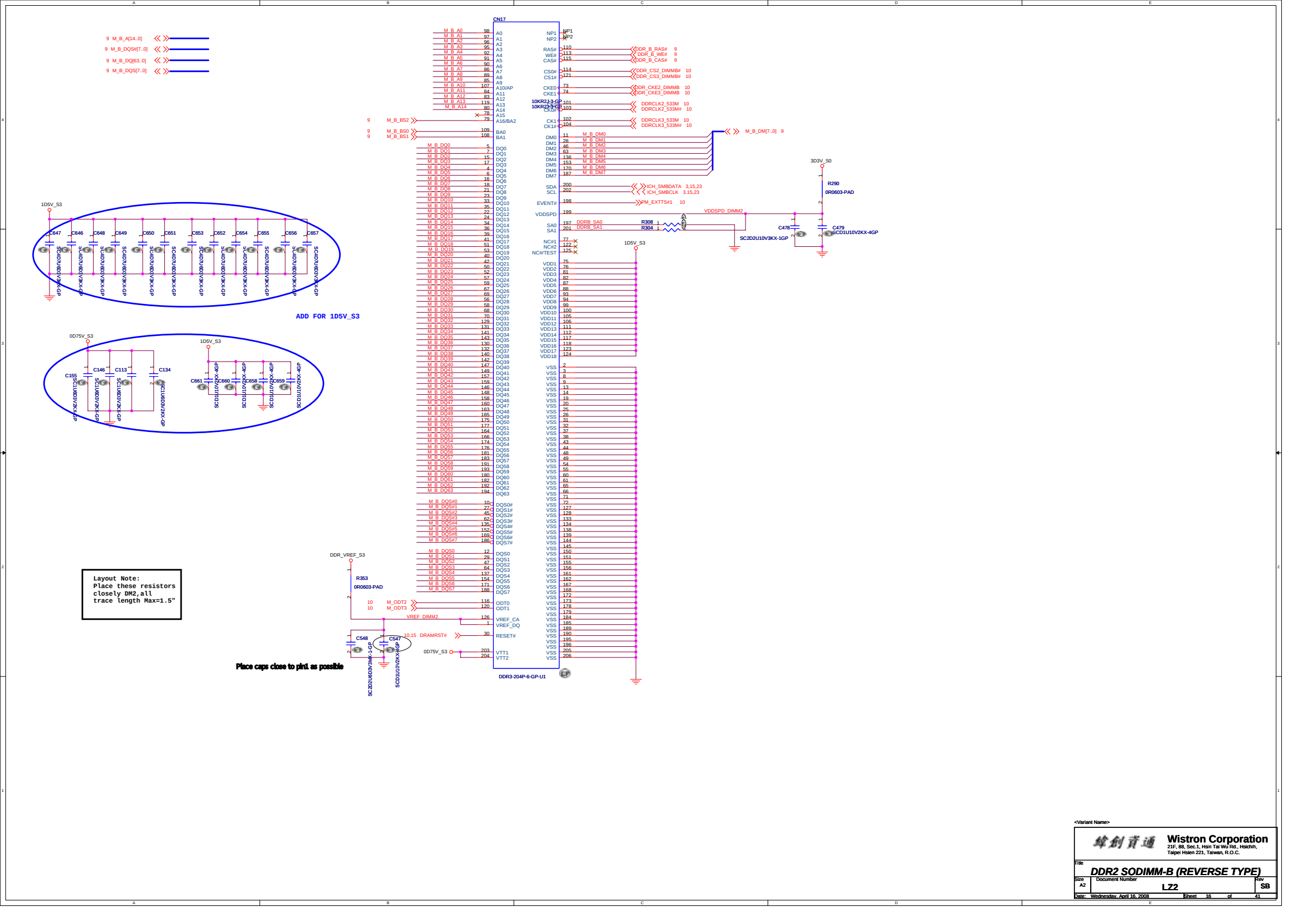
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-A (NORMAL TYPE)

Size: A2 | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 15 of 41



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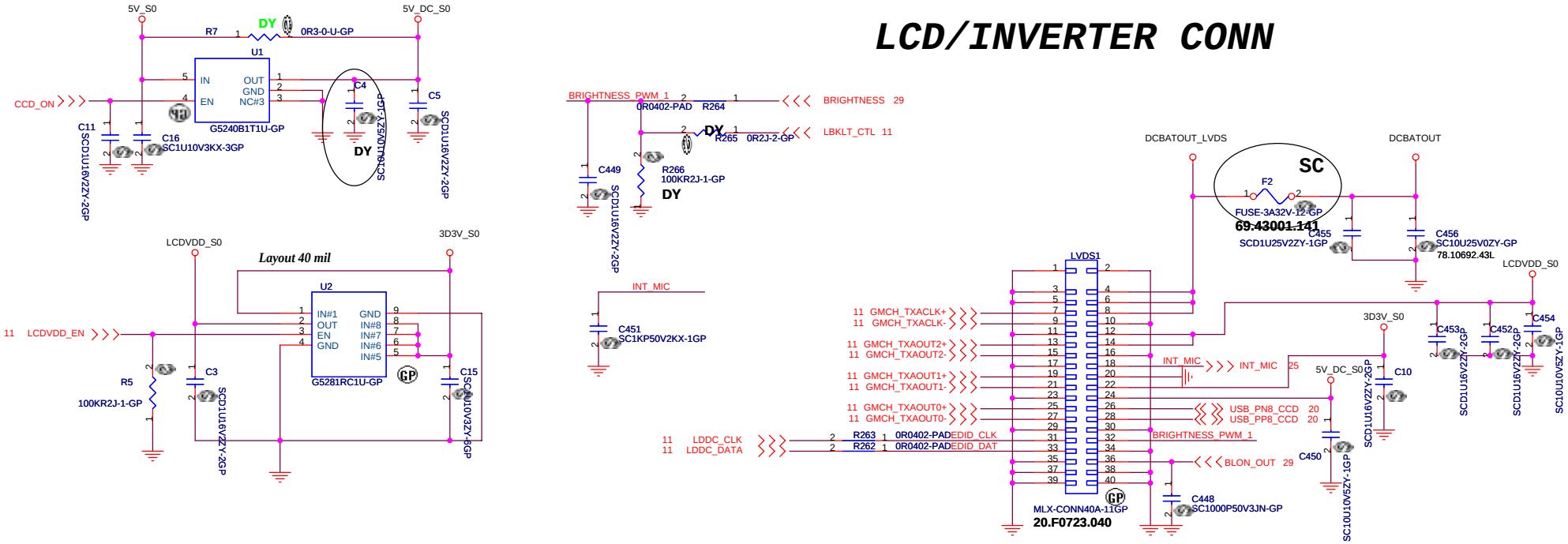
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-B (REVERSE TYPE)

Size: A2 | Document Number: LZ2 | Rev: SB

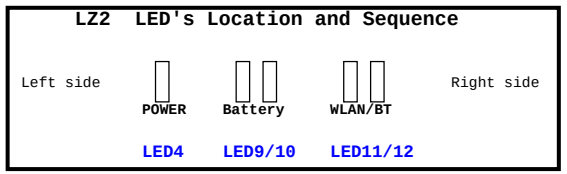
Date: Wednesday, April 16, 2008 | Sheet 16 of 41

LCD/INVERTER CONN



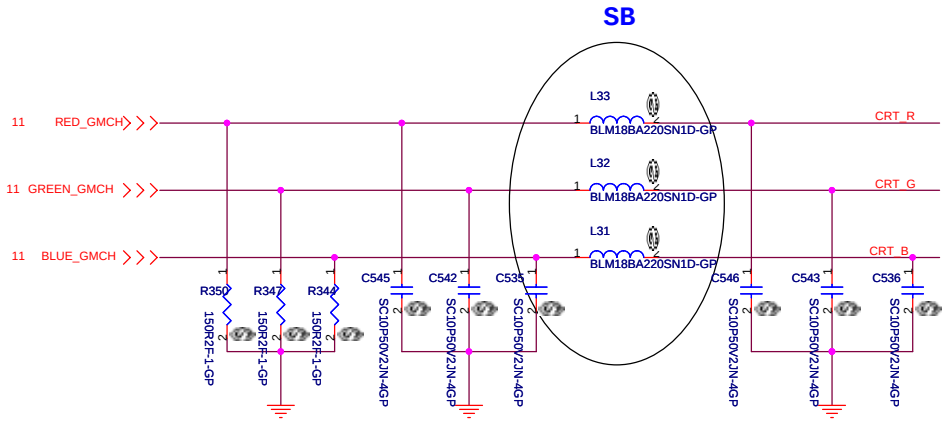
M/B LED

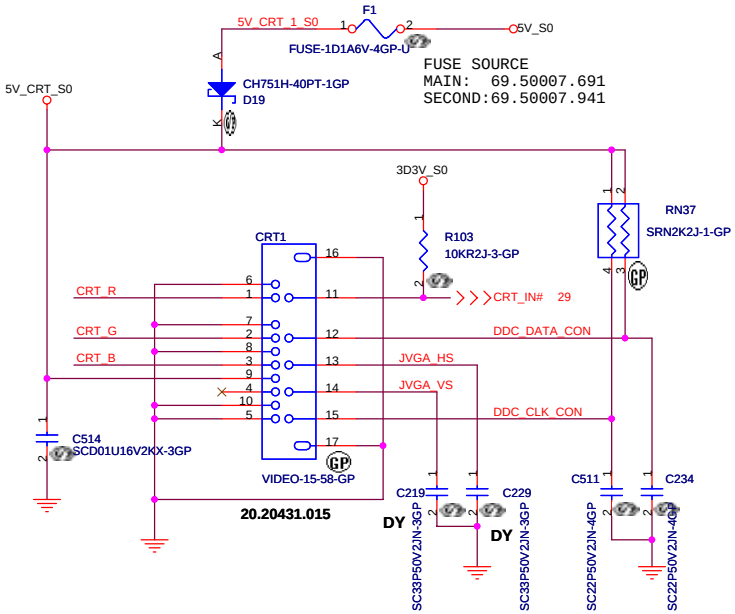
LZ2 LED's Location and Sequence

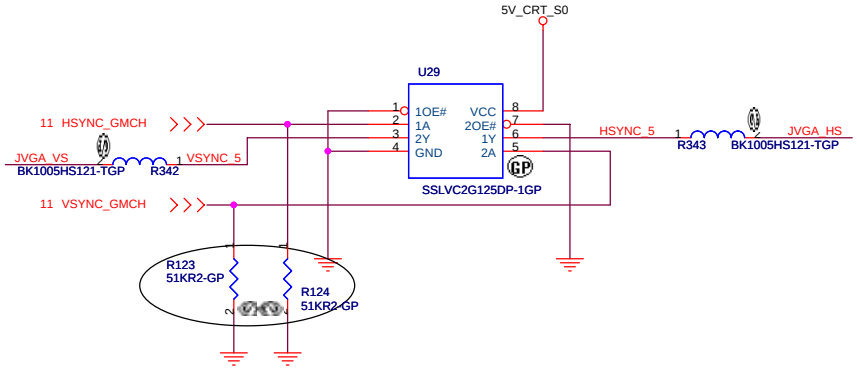


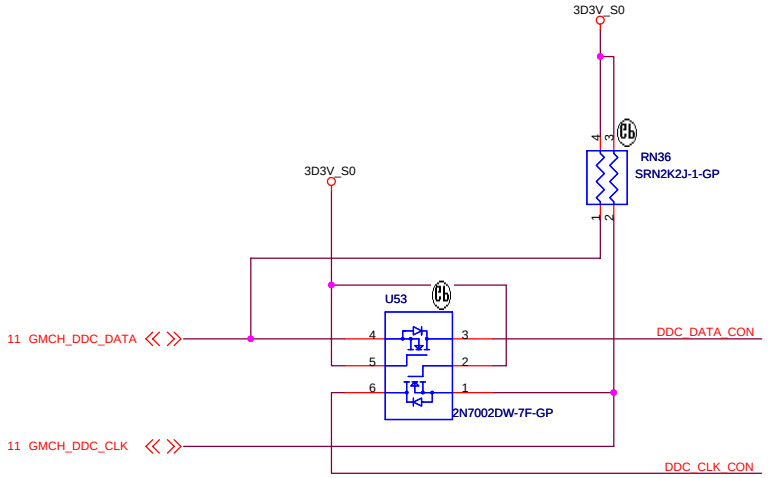
BOM1

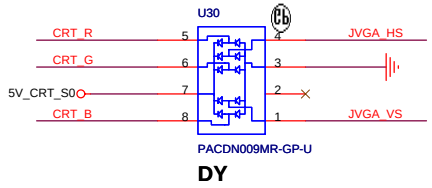
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD CONN & CAMERA & DIG-MIC	
Size	Document Number: LZ2	Rev: SB
Date: Wednesday, April 16, 2008	Sheet 17 of 41	

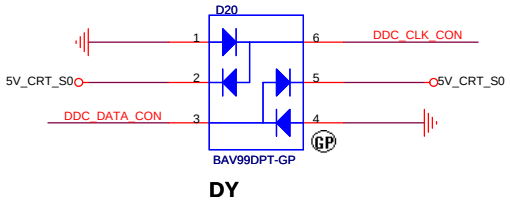












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Title: CRT/TV Connector

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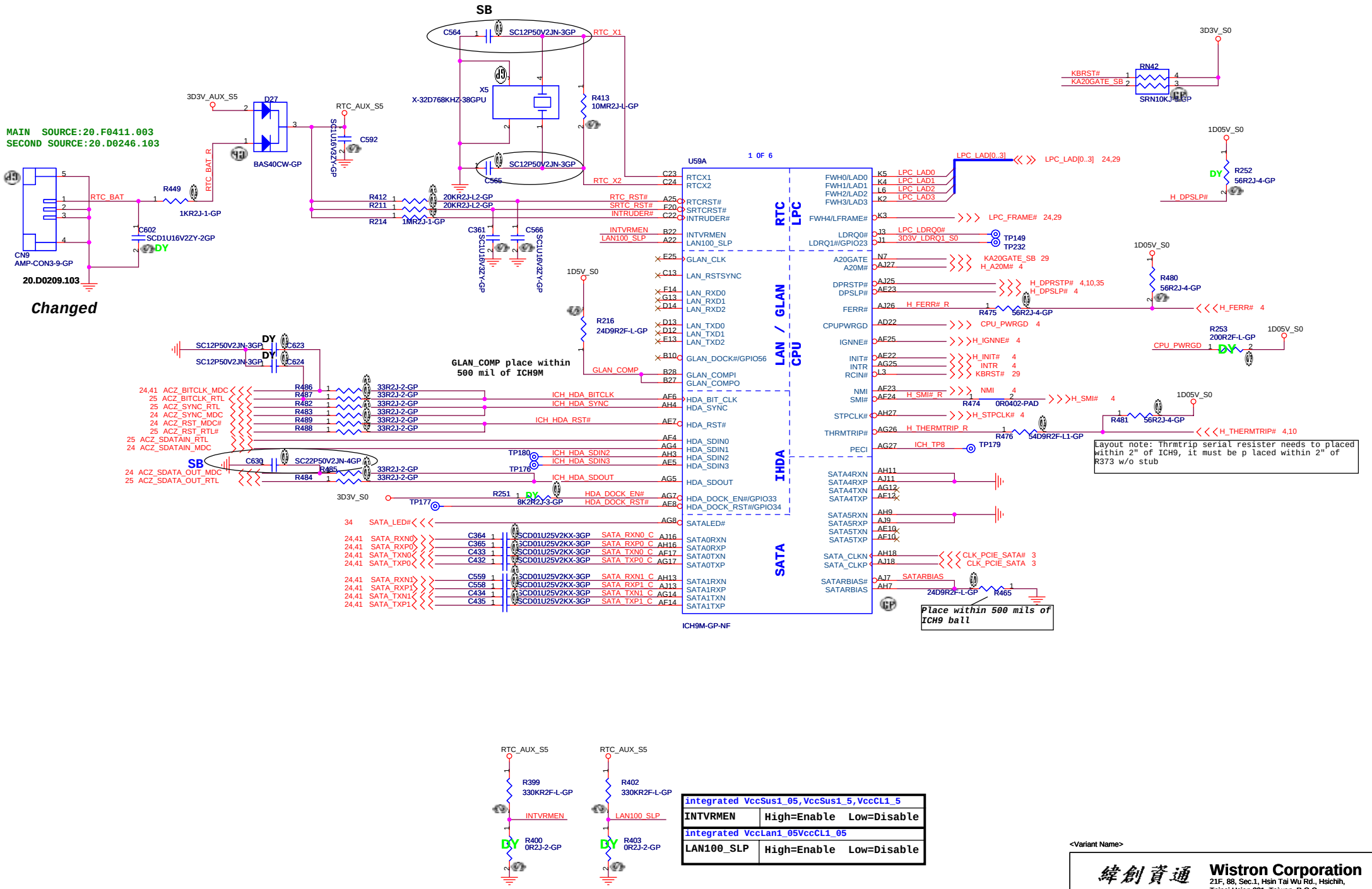
SB
MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103
20.D0209.103
Changed
U59A
1 OF 6
ICH9M-GP-NF
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: Thrmtrip serial resister needs to placed within 2" of ICH9, it must be p laced within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
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ICH9-M (1 of 4)
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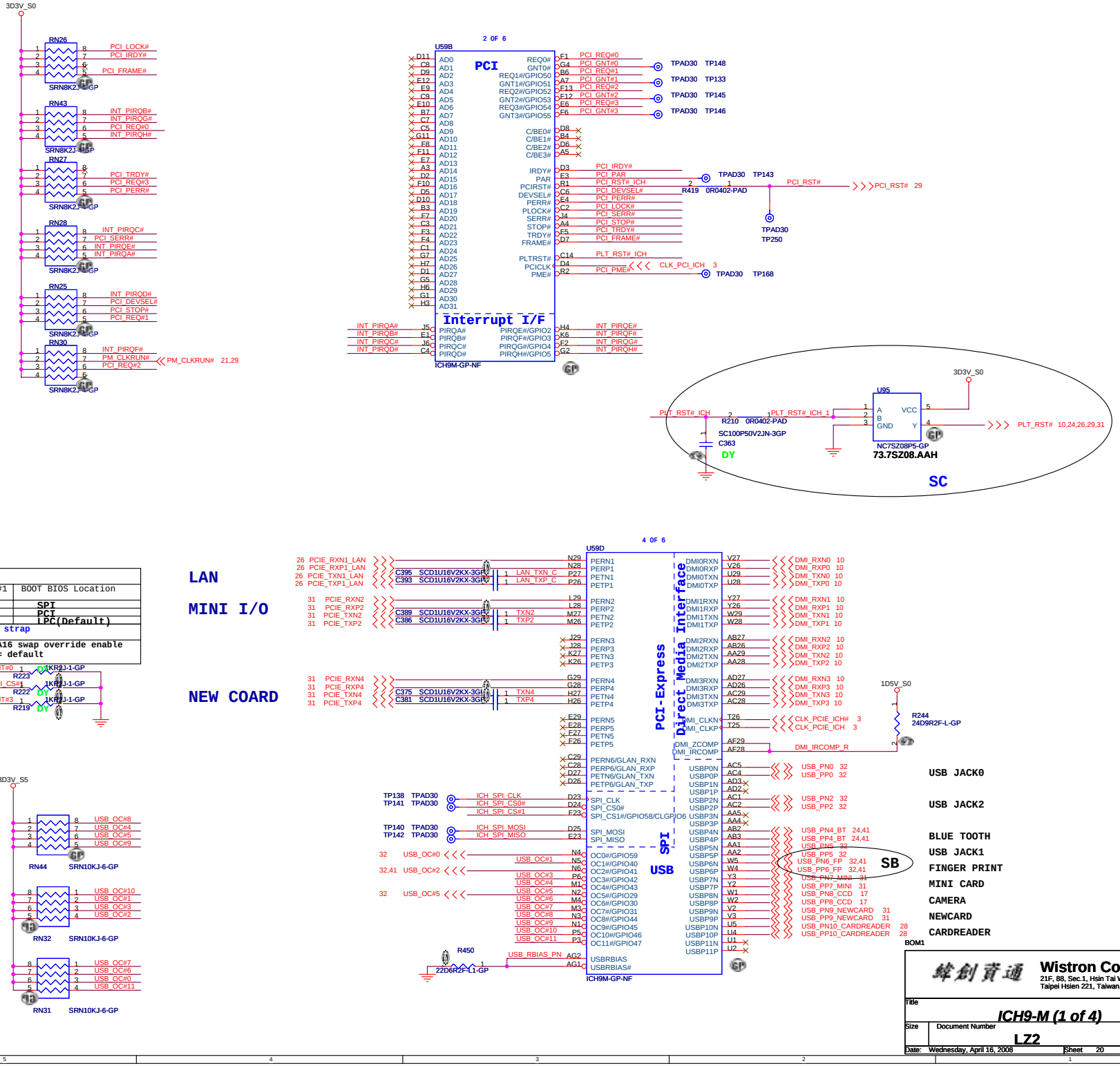
3D3V_S0
RN26
PCI_LOCK#
PCI_IRDY#
PCI_FRAME#
SRN8K2J-1-GP
RN43
INT_PIRQB#
INT_PIRQG#
PCI_REQ#0
INT_PIRQH#
RN27
PCI_TRDY#
PCI_REQ#3
PCI_PERR#
RN28
INT_PIRQC#
PCI_SERR#
INT_PIRQE#
INT_PIRQA#
RN25
INT_PIRQD#
PCI_DEVSEL#
PCI_STOP#
PCI_REQ#1
RN30
INT_PIRQF#
PM_CLKRUN#
PCI_REQ#2
PM_CLKRUN# 21,29
2 OF 6
U59B
PCI
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
REQ0#
GNT0#
REQ1#/GPIO50
GNT1#/GPIO51
REQ2#/GPIO52
GNT2#/GPIO53
REQ3#/GPIO54
GNT3#/GPIO55
C/BE0#
C/BE1#
C/BE2#
C/BE3#
IRDY#
PAR
PCIRST#
DEVSEL#
PERR#
PLOCK#
SERR#
STOP#
TRDY#
FRAME#
PLTRST#
PCICLK
PME#
PCI_REQ#0
PCI_GNT#0
PCI_REQ#1
PCI_GNT#1
PCI_REQ#2
PCI_GNT#2
PCI_REQ#3
PCI_GNT#3
TPAD30 TP148
TPAD30 TP133
TPAD30 TP145
TPAD30 TP146
PCI_IRDY#
PCI_PAR
PCI_RST# ICH
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
TPAD30 TP143
R419 0R0402-PAD
PCI_RST#
PCI_RST# 29
TPAD30 TP250
PLT_RST# ICH
CLK_PCI_ICH 3
PCI_PME#
TPAD30 TP168
Interrupt I/F
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
ICH9M-GP-NF
3D3V_S0
U95
PLT_RST# ICH
PLT_RST#_ICH_1
R210 0R0402-PAD
SC100P50V2JN-3GP
C363
DY
A
B
GND
VCC
Y
NC7SZ08P5-GP
73.7SZ08.AAH
PLT_RST# 10,24,26,29,31
SC
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable / high = default
PCI_GNT#0 R223 1KR2J-1-GP
ICH_SPI_CS#1 R222 DY 1KR2J-1-GP
PCI_GNT#3 R219 DY 1KR2J-1-GP
LAN
MINI I/O
NEW COARD
4 OF 6
U59D
PCI-Express
Direct Media Interface
SPI
USB
26 PCIE_RXN1_LAN
26 PCIE_RXP1_LAN
26 PCIE_TXN1_LAN
26 PCIE_TXP1_LAN
C395 SCD1U16V2KX-3GP
C393 SCD1U16V2KX-3GP
LAN_TXN_C
LAN_TXP_C
31 PCIE_RXN2
31 PCIE_RXP2
31 PCIE_TXN2
31 PCIE_TXP2
C389 SCD1U16V2KX-3GP
C386 SCD1U16V2KX-3GP
TXN2
TXP2
31 PCIE_RXN4
31 PCIE_RXP4
31 PCIE_TXN4
31 PCIE_TXP4
C375 SCD1U16V2KX-3GP
C381 SCD1U16V2KX-3GP
TXN4
TXP4
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_RXN0 10
DMI_RXP0 10
DMI_TXN0 10
DMI_TXP0 10
DMI_RXN1 10
DMI_RXP1 10
DMI_TXN1 10
DMI_TXP1 10
DMI_RXN2 10
DMI_RXP2 10
DMI_TXN2 10
DMI_TXP2 10
DMI_RXN3 10
DMI_RXP3 10
DMI_TXN3 10
DMI_TXP3 10
CLK_PCIE_ICH# 3
CLK_PCIE_ICH 3
DMI_IRCOMP_R
1D5V_S0
R244
24D9R2F-L-GP
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO
ICH_SPI_CLK
ICH_SPI_CS0#
ICH_SPI_CS1#
ICH_SPI_MOSI
ICH_SPI_MISO
TP138 TPAD30
TP141 TPAD30
TP140 TPAD30
TP142 TPAD30
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USB_PN0 32
USB_PP0 32
USB_PN2 32
USB_PP2 32
USB_PN4_BT 24,41
USB_PP4_BT 24,41
USB_PN5 32
USB_PP5 32
USB_PN6_FP 32,41
USB_PP6_FP 32,41
USB_PN7_MINI 31
USB_PP7_MINI 31
USB_PN8_CCD 17
USB_PP8_CCD 17
USB_PN9_NEWCARD 31
USB_PP9_NEWCARD 31
USB_PN10_CARDREADER 28
USB_PP10_CARDREADER 28
SB
USB JACK0
USB JACK2
BLUE TOOTH
USB JACK1
FINGER PRINT
MINI CARD
CAMERA
NEWCARD
CARDREADER
BOM1
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9
USB_OC#10
USB_OC#11
32 USB_OC#0
32,41 USB_OC#2
32 USB_OC#5
R450
22D6R2F-L1-GP
USB_RBIAS_PN
USB_RBIAS#
USBRBIAS
USBRBIAS#
ICH9M-GP-NF
3D3V_S5
RN44 SRN10KJ-6-GP
USB_OC#8
USB_OC#4
USB_OC#5
USB_OC#9
RN32 SRN10KJ-6-GP
USB_OC#10
USB_OC#1
USB_OC#3
USB_OC#2
RN31 SRN10KJ-6-GP
USB_OC#7
USB_OC#6
USB_OC#0
USB_OC#11
蜂創資通
Wistron Corporation
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Title
ICH9-M (1 of 4)
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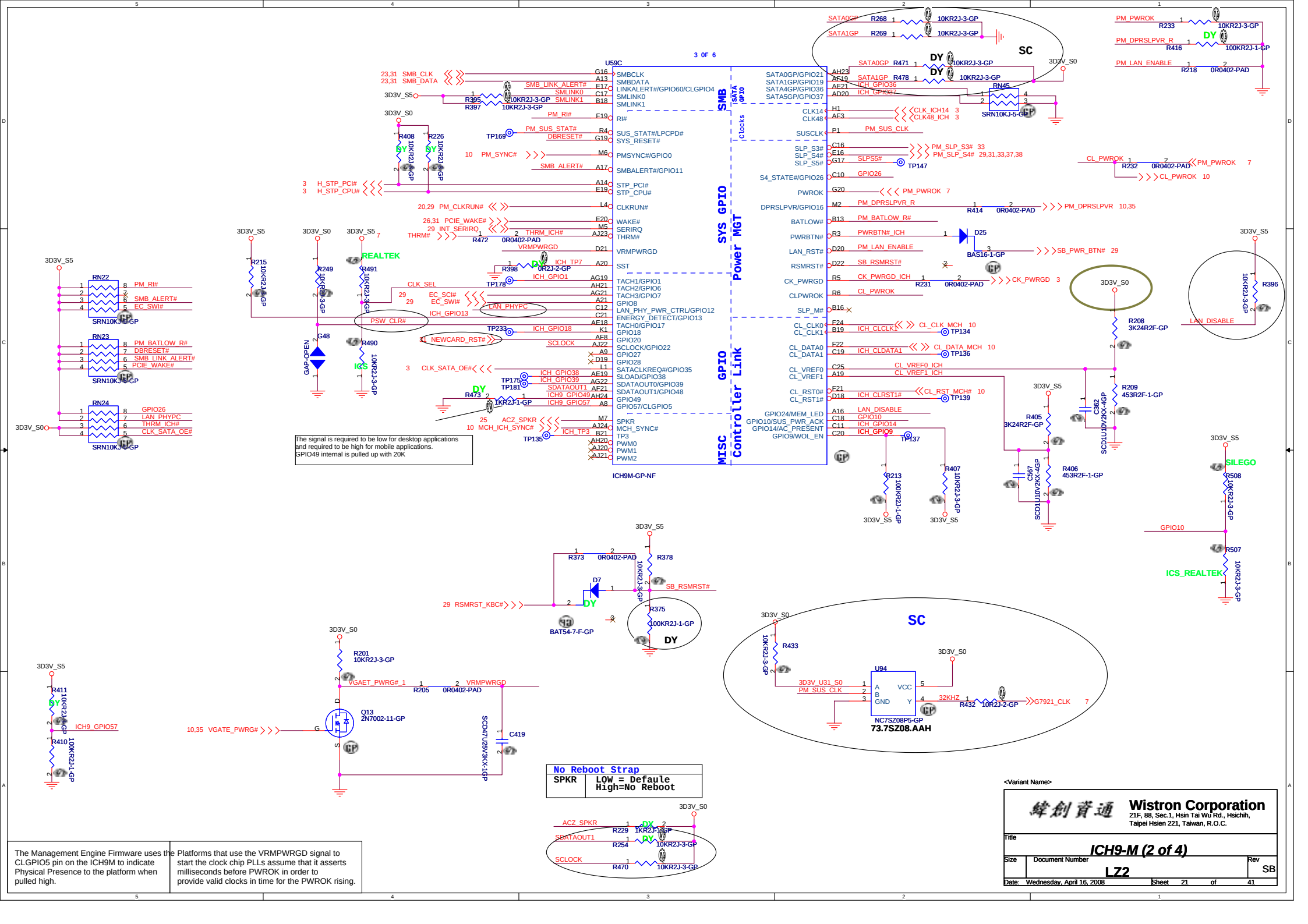
U59C
3 OF 6
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
SC
REALTEK
ICS
SILEGO
ICS_REALTEK
GAP-OPEN
DY
3D3V_S0
3D3V_S5
SMB_CLK
SMB_DATA
SMB_LINK_ALERT#
PM_RI#
PM_SUS_STAT#
DBRESET#
PM_SYNC#
SMB_ALERT#
H_STP_PCI#
H_STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
THRM#
THRM_ICH#
VRMPWRGD
ICH_TP7
ICH_GPIO1
CLK_SEL
EC_SCI#
EC_SWI#
LAN_PHYPC
PSW_CLR#
ICH_GPIO13
ICH_GPIO18
NEWCARD_RST#
SCLOCK
CLK_SATA_OE#
ICH_GPIO38
ICH_GPIO39
SDATAOUT1
ICH9_GPIO49
ICH9_GPIO57
ACZ_SPKR
MCH_ICH_SYNC#
ICH_TP3
SATA0GP
SATA1GP
ICH_GPIO36
ICH_GPIO37
CLK_ICH14
CLK48_ICH
PM_SUS_CLK
PM_SLP_S3#
PM_SLP_S4#
SLPS5#
GPIO26
PM_PWROK
PM_DPRSLPVR_R
PM_BATLOW_R#
PWRBTN#_ICH
PM_LAN_ENABLE
SB_PWR_BTN#
SB_RSMRST#
CK_PWRGD_ICH
CL_PWROK
CL_CLKICH
CL_CLK_MCH
ICH_CLCLK1
CL_DATA_MCH
ICH_CLDATA1
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST_MCH#
ICH_CLRST1#
LAN_DISABLE
GPIO10
ICH_GPIO14
ICH_GPIO9
CL_PWROK
PM_PWROK
PM_DPRSLPVR_R
PM_LAN_ENABLE
LAN_DISABLE
GPIO10
SB_RSMRST#
RSMRST_KBC#
VGATE_PWRG#
VRMPWRGD
ACZ_SPKR
SDATAOUT1
SCLOCK
G7921_CLK
32KHZ
3D3V_U31_S0
PM_SUS_CLK
RN22
RN23
RN24
SRN10KJ-5-GP
RN45
SRN10KJ-5-GP
R268
R269
R471
R478
R233
R416
R218
R232
R414
R231
R398
R472
R395
R397
R408
R226
R215
R249
R491
R490
R373
R378
R375
R201
R205
R411
R410
R213
R407
R405
R406
R208
R209
R396
R508
R507
R433
R432
R229
R254
R470
D25
BAS16-1-GP
D7
BAT54-7-F-GP
Q13
2N7002-11-GP
U94
NC7SZ08P5-GP
73.7SZ08.AAH
C362
C567
C419
SCD1U10V2KX-4GP
SCD47U25V8KX-1GP
TP134
TP136
TP139
TP137
TP135
TP147
TP169
TP178
TP233
TP175
TP181
TP3
0R0402-PAD
10KR2J-3-GP
100KR2J-1-GP
1KR2J-1-GP
10KR2J-2-GP
10KR2J-3-GP
3K24R2F-GP
453R2F-1-GP
The signal is required to be low for desktop applications and required to be high for mobile applications. GPIO49 internal is pulled up with 20K
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
The Management Engine Firmware uses the CLGPIO5 pin on the ICH9M to indicate Physical Presence to the platform when pulled high.
Platforms that use the VRMPWRGD signal to start the clock chip PLLs assume that it asserts milliseconds before PWROK in order to provide valid clocks in time for the PWROK rising.
<Variant Name>
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ICH9M-GP-NF

VccRTC=6uA in G3

Vcc1_5_B=646mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

V5REF=2mA

V5REF_Sus=2mA

VccSATAPLL=47mA

Vcc1_5_A=1.342A

USBPLL=11mA

VccLAN3_3=19mA

VccLAN3_3=19mA in S0;78mA in S3/S4/S5,The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.

VccGLANPLL=23mA

VccGLAN1_5=80mA

VccGLAN3_3=1mA

Vcc1_05=1.634A

Layout Note:Place near ICH9M

VccDMIPLL=23mA

VccDMI=48mA

V_CPU_IO=2mA

VCC3_3=308mA

VccHDA=11mA

VccSusHDA=11mA

VccSus3_3=212mA

VccCL3_3=19mA

Layout Note: Place near ICH9

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Title: ICH9-M (3 of 4)

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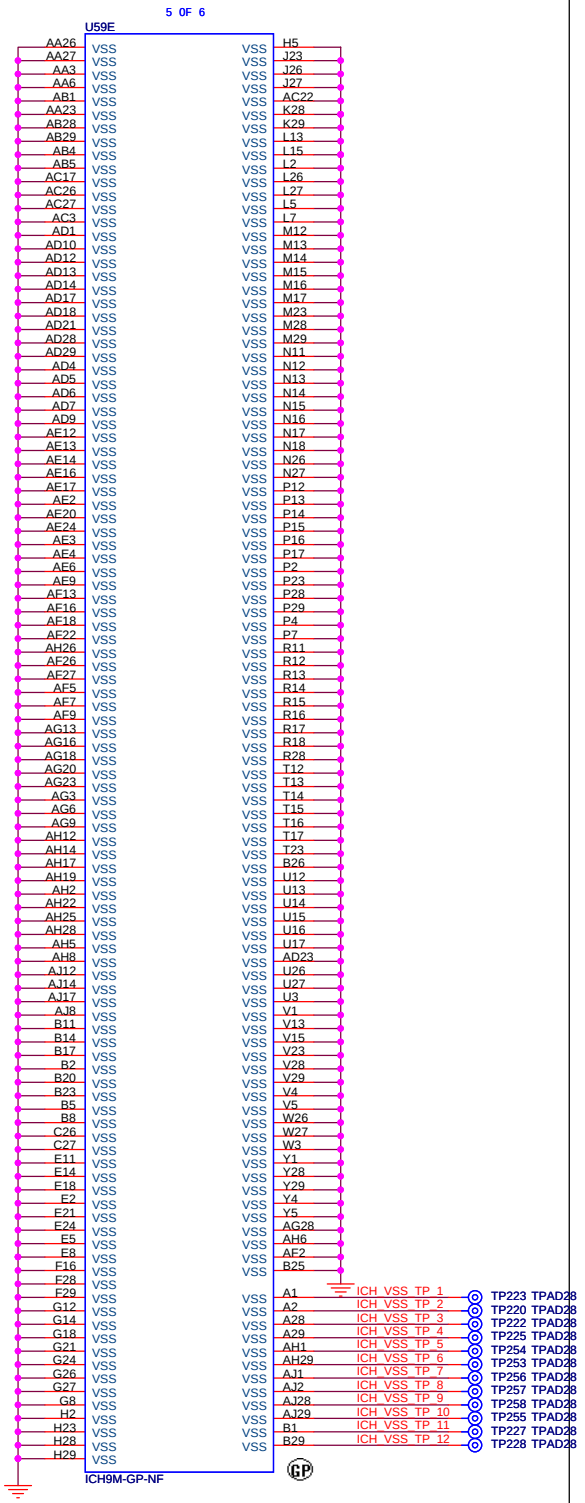

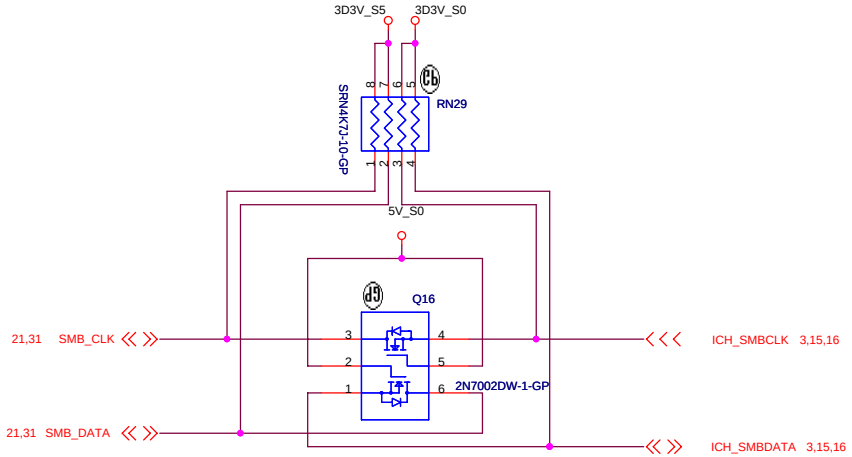

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ICH9-M (4 of 4)*		
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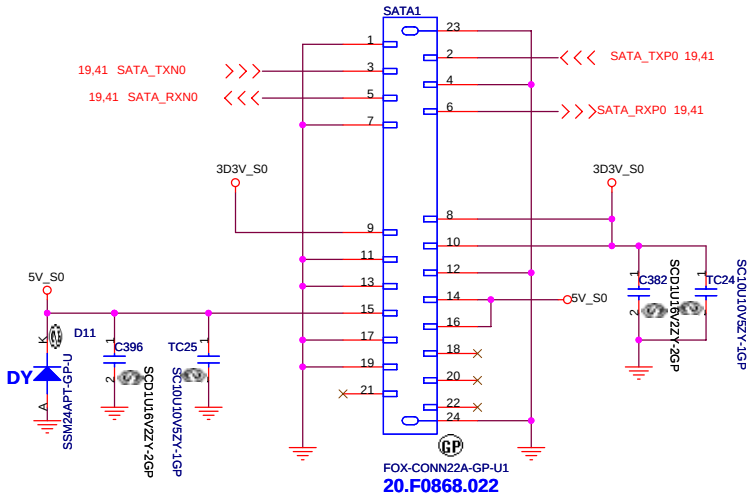
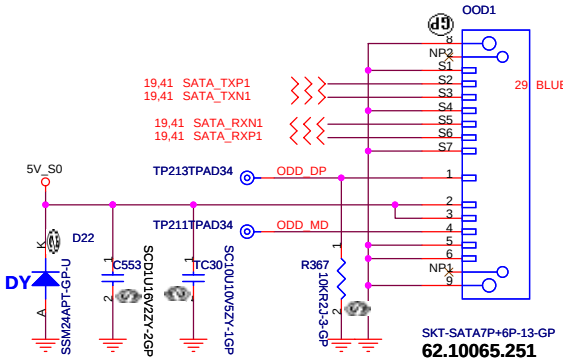
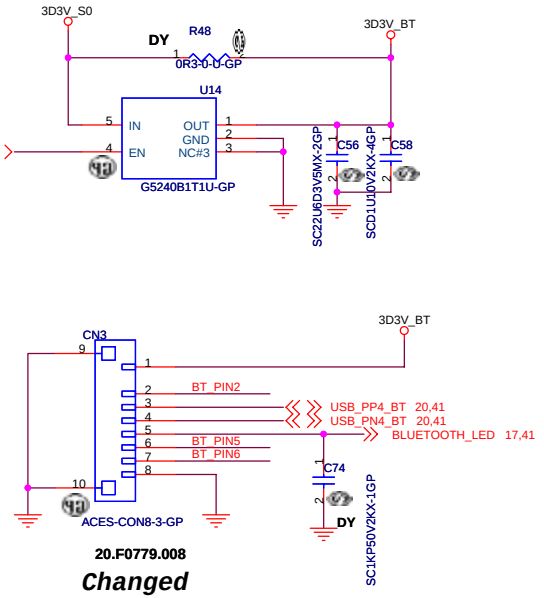
SATA HD Connector



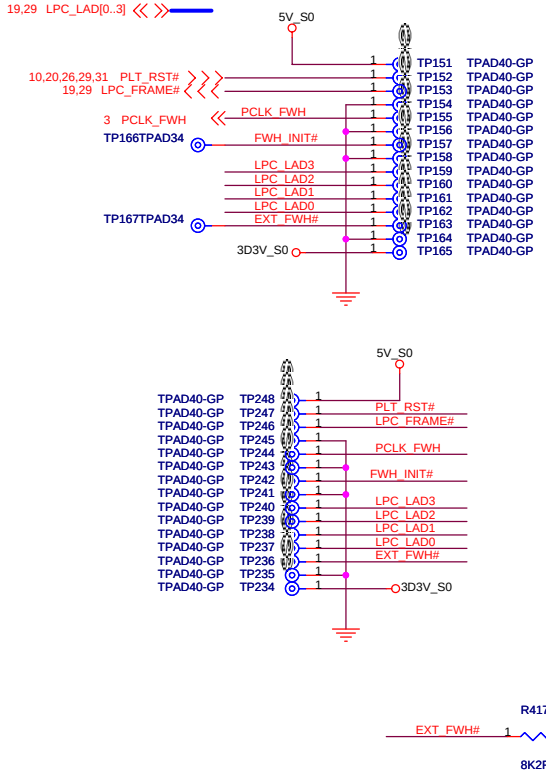
ODD Connector



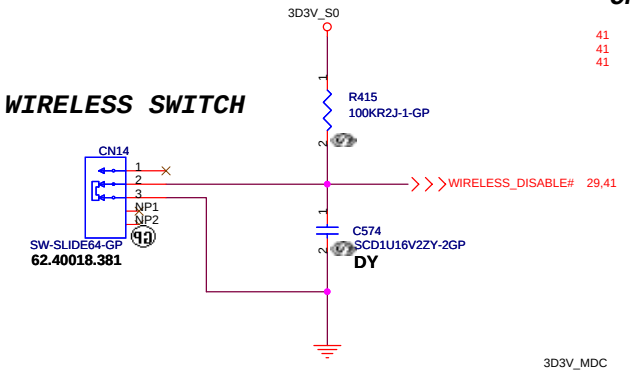
BT CONNECTOR



GOLDEN FINGER FOR DEBUG BOARD

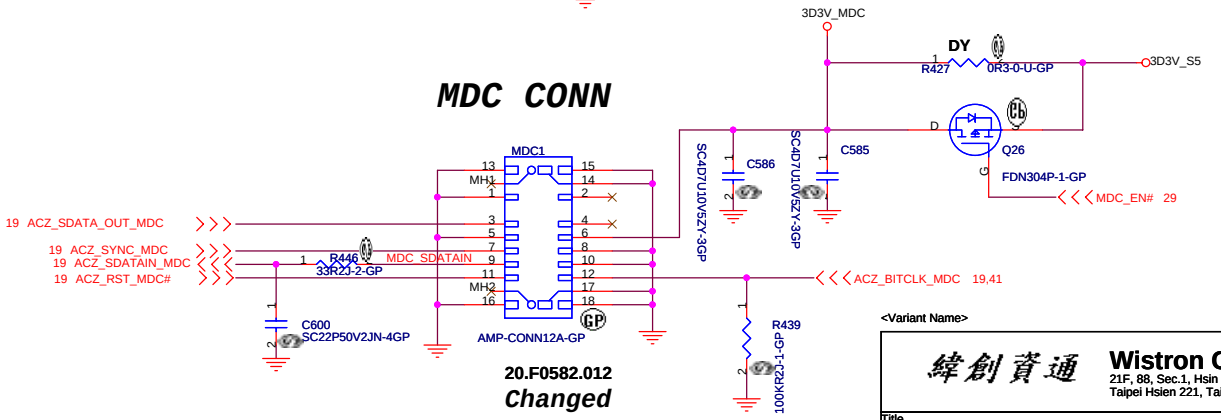


WIRELESS SWITCH



41 BT_PIN2 BT_PIN2
41 BT_PIN5 BT_PIN5
41 BT_PIN6 BT_PIN6

MDC CONN



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM/DEBUG /MODEM/WIRELESS SW/BT

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	LZ2	SB

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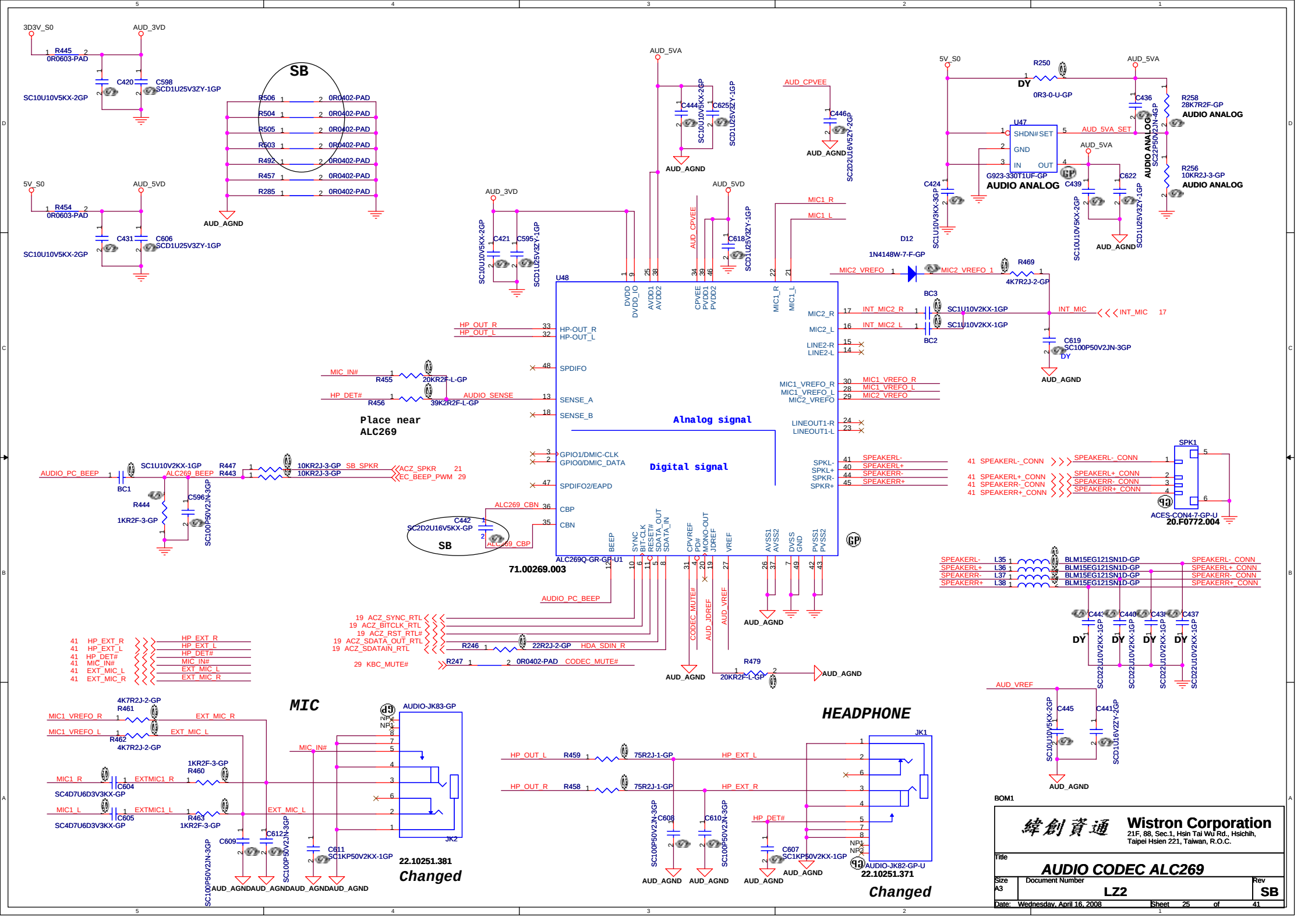
3D3V_S0
AUD_3VD
R445
0R0603-PAD
C420
SC10U10V5KX-2GP
C598
SCD1U25V3ZY-1GP
SB
R506
R504
R505
R503
R492
R457
R285
0R0402-PAD
AUD_AGND
5V_S0
AUD_5VD
R454
C431
C606
AUD_5VA
C444
C625
C446
SC2D2U16V5ZY-2GP
AUD_CPVEE
C618
MIC1_R
MIC1_L
AUD_3VD
C421
C595
U48
DVDD
DVDD_IO
AVDD1
AVDD2
CPVEE
PVDD1
PVDD2
HP-OUT_R
HP-OUT_L
SPDIFO
SENSE_A
SENSE_B
GPIO1/DMIC-CLK
GPIO0/DMIC_DATA
SPDIFO2/EAPD
CBP
CBN
MIC2_R
MIC2_L
LINE2-R
LINE2-L
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
LINEOUT1-R
LINEOUT1-L
SPKL-
SPKL+
SPKR-
SPKR+
BEEP
SYNC
BIT-CLK
RESET#
SDATA_OUT
SDATA_IN
CPVREF
PD#
MONO-OUT
JDREF
VREF
AVSS1
AVSS2
DVSS
GND
PVSS1
PVSS2
ALC269Q-GR-GP-U1
71.00269.003
Alnalog signal
Digital signal
Place near
ALC269
MIC_IN#
HP_DET#
R455
R456
20KR2F-L-GP
39K2R2F-L-GP
AUDIO_SENSE
HP_OUT_R
HP_OUT_L
ALC269_CBN
ALC269_CBP
C442
SC2D2U16V5KX-GP
SB
AUDIO_PC_BEEP
SC1U10V2KX-1GP
BC1
R444
1KR2F-3-GP
C596
SC100P50V2JN-3GP
R447
R443
10KR2J-3-GP
SB_SPKR
ACZ_SPKR
EC_BEEP_PWM
19 ACZ_SYNC_RTL
19 ACZ_BITCLK_RTL
19 ACZ_RST_RTL#
19 ACZ_SDATA_OUT_RTL
19 ACZ_SDATAIN_RTL
29 KBC_MUTE#
R246
22R2J-2-GP
HDA_SDIN_R
R247
0R0402-PAD
CODEC_MUTE#
AUD_JDREF
AUD_VREF
R479
20KR2F-L-GP
41 HP_EXT_R
41 HP_EXT_L
41 HP_DET#
41 MIC_IN#
41 EXT_MIC_L
41 EXT_MIC_R
MIC2_VREFO
D12
1N4148W-7-F-GP
MIC2_VREFO_1
R469
4K7R2J-2-GP
BC3
BC2
SC1U10V2KX-1GP
INT_MIC2_R
INT_MIC2_L
INT_MIC
C619
SC100P50V2JN-3GP
DY
5V_S0
R250
0R3-0-U-GP
U47
SHDN#
SET
GND
IN
OUT
G923-330T1UF-GP
AUDIO ANALOG
AUD_5VA_SET
C436
C424
SC1U10V3KX-3GP
C439
SC10U10V5KX-2GP
C622
SCD1U25V3ZY-1GP
R258
28K7R2F-GP
R256
10KR2J-3-GP
SC22P50V2JN-4GP
SPK1
ACES-CON4-7-GP-U
20.F0772.004
SPEAKERL-
SPEAKERL+
SPEAKERR-
SPEAKERR+
SPEAKERL-_CONN
SPEAKERL+_CONN
SPEAKERR-_CONN
SPEAKERR+_CONN
L35
L36
L37
L38
BLM15EG121SN1D-GP
C441
C440
C438
C437
SCD22U10V2KX-1GP
C445
SCD1U16V2ZY-2GP
SC10U10V5KX-2GP
MIC
AUDIO-JK83-GP
JK2
4K7R2J-2-GP
R461
R462
MIC1_VREFO_R
MIC1_VREFO_L
EXT_MIC_R
EXT_MIC_L
1KR2F-3-GP
R460
R463
C604
C605
SC4D7U6D3V3KX-GP
EXTMIC1_R
EXTMIC1_L
C609
C612
C611
SC1KP50V2KX-1GP
SC100P50V2JN-3GP
22.10251.381
Changed
HEADPHONE
JK1
AUDIO-JK82-GP-U
22.10251.371
Changed
HP_OUT_L
HP_OUT_R
R459
R458
75R2J-1-GP
HP_EXT_L
HP_EXT_R
C608
C610
C607
HP_DET#
AUD_AGND
BOM1
Wistron Corporation
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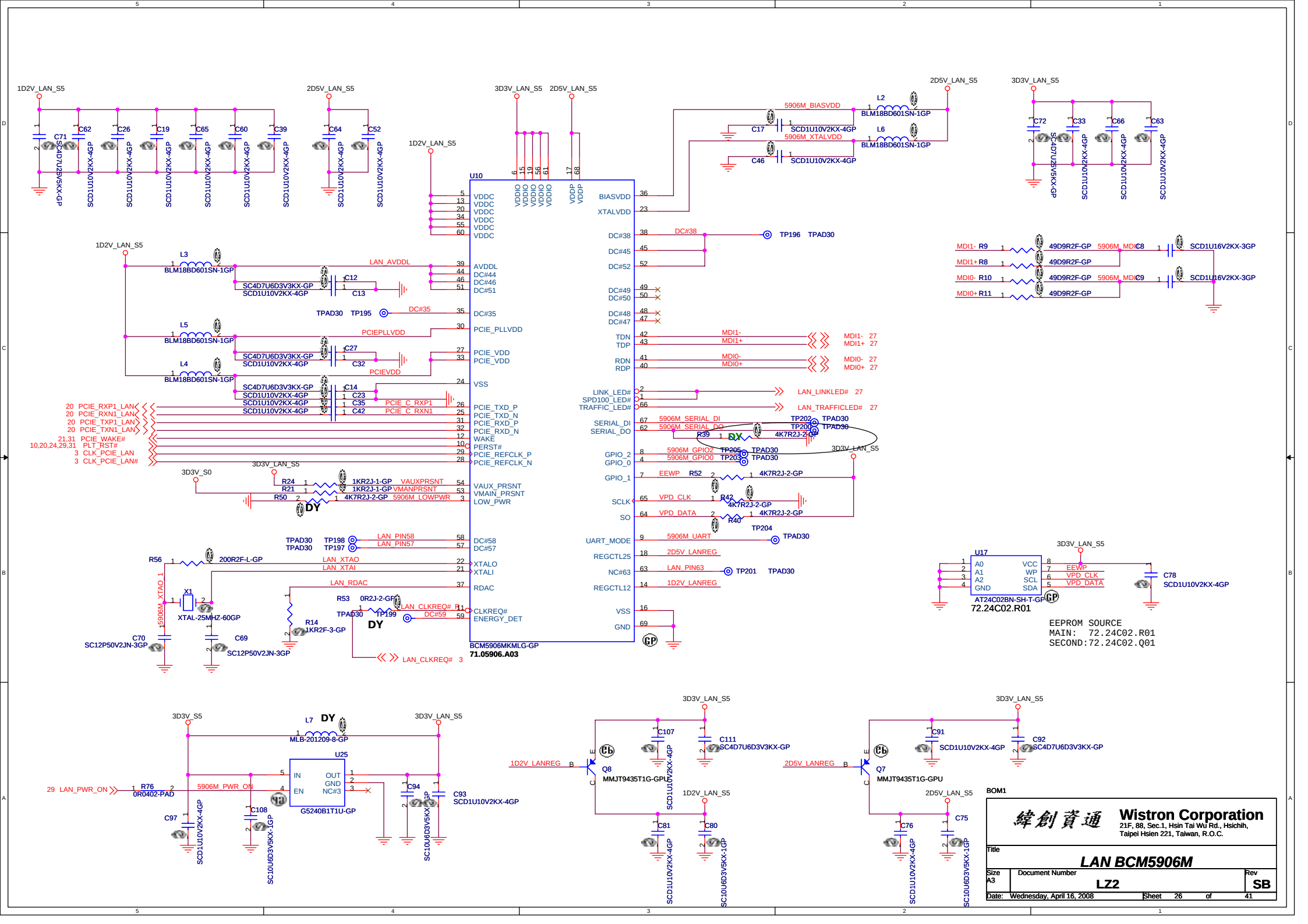
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC ALC269
Size
A3
Document Number
LZ2
Rev
SB
Date: Wednesday, April 16, 2008
Sheet 25 of 41


1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
U10
BCM5906MKMLG-GP
71.05906.A03
5906M_BIASVDD
5906M_XTALVDD
LAN_AVDDL
PCIEPLLVDD
PCIEVDD
PCIE_RXP1_LAN
PCIE_RXN1_LAN
PCIE_TXP1_LAN
PCIE_TXN1_LAN
PCIE_WAKE#
PLT_RST#
CLK_PCIE_LAN
CLK_PCIE_LAN#
LAN_XTAO
LAN_XTAI
LAN_RDAC
LAN_CLKREQ#
LAN_PIN58
LAN_PIN57
LAN_PIN63
LAN_LINKLED#
LAN_TRAFFICLED#
5906M_SERIAL_DI
5906M_SERIAL_DO
5906M_GPIO2
5906M_GPIO0
5906M_UART
2D5V_LANREG
1D2V_LANREG
MDI1-
MDI1+
MDI0-
MDI0+
VAUXPRSNT
VMANPRSNT
5906M_LOWPWR
DC#38
DC#35
DC#58
DC#59
EEWP
VPD_CLK
VPD_DATA
XTAL-25MHZ-60GP
AT24C02BN-SH-T-GP
72.24C02.R01
EEPROM SOURCE
MAIN: 72.24C02.R01
SECOND:72.24C02.Q01
MMJT9435T1G-GPU
G5240B1T1U-GP
LAN_PWR_ON
5906M_PWR_ON
Wistron Corporation
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LAN BCM5906M
LZ2
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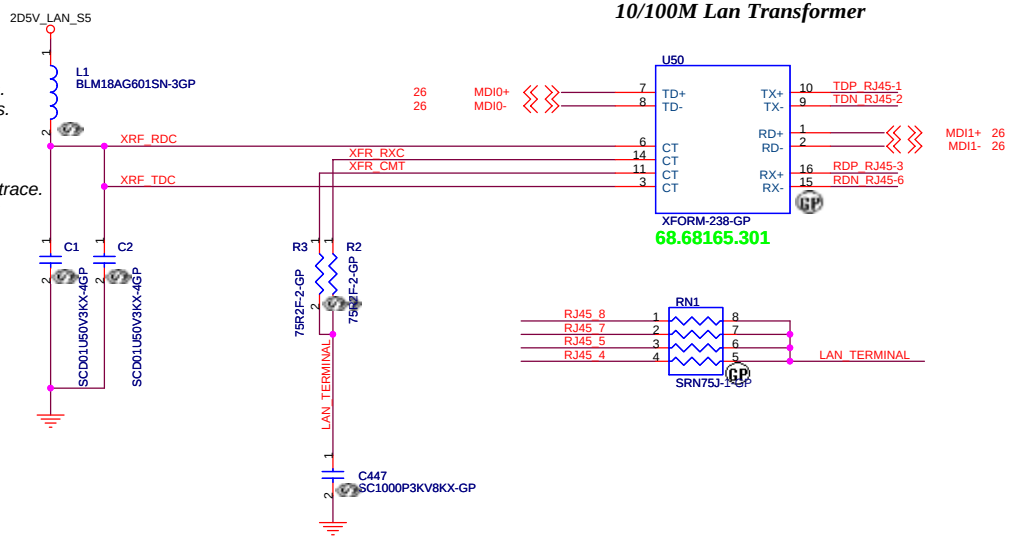
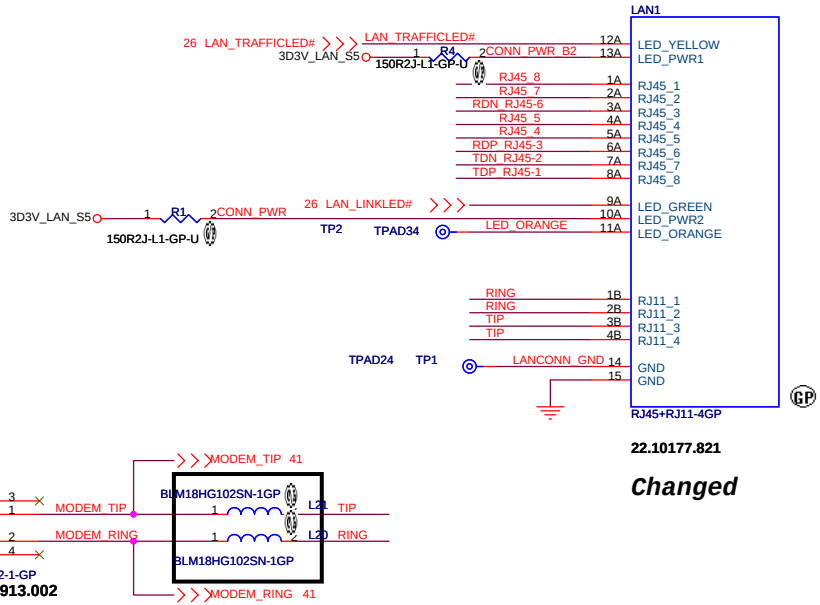
10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



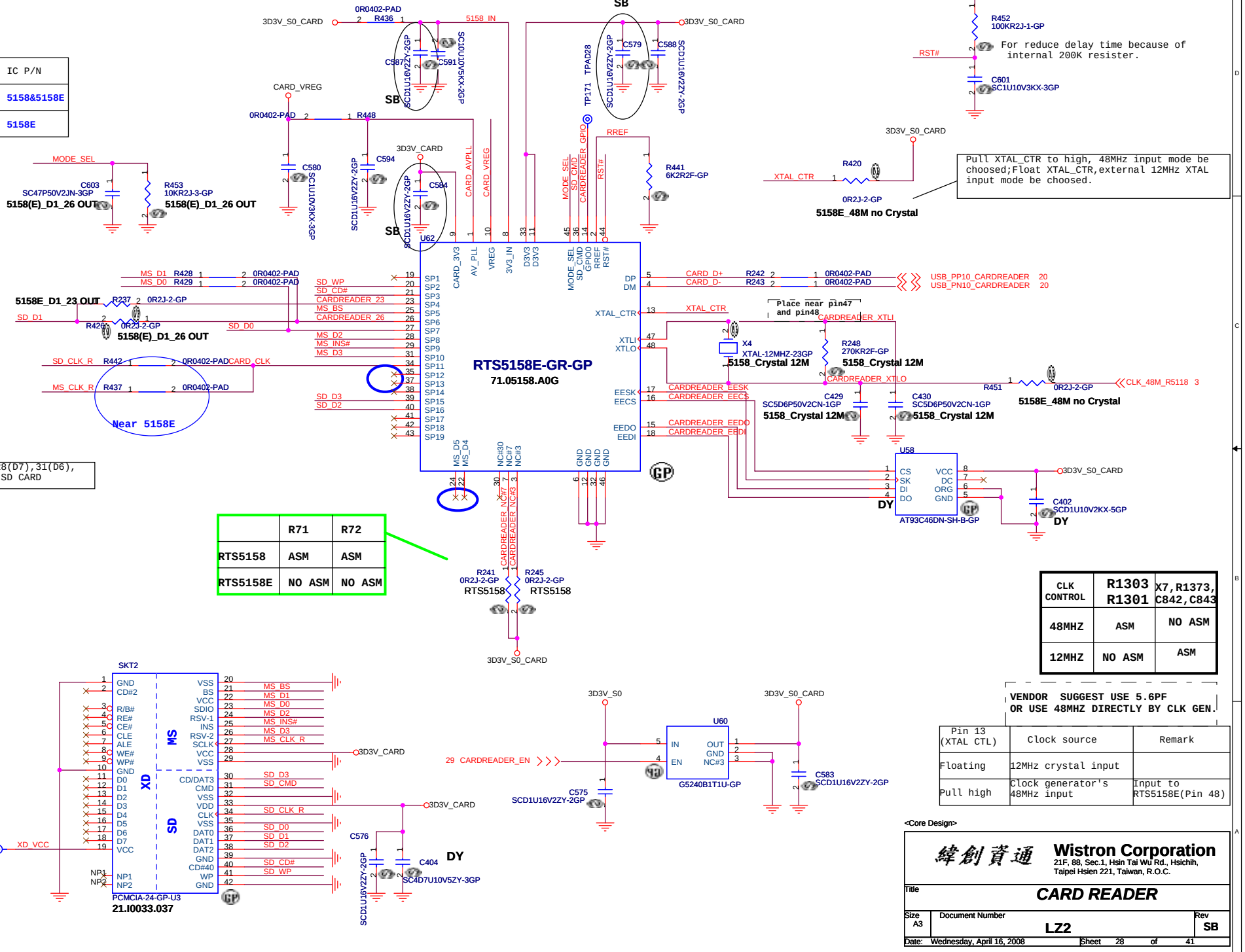


<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN connector/NEW CARD/SIM		
Size: A3	Document Number: LZ2	Rev: SB
Date: Wednesday, April 16, 2008	Sheet 27 of 41	

For 3in1 SD/MMC/MS CARD

R1302	C38	SD_D1 OUT FROM	IC P/N
10K	47 PF	PIN 26(MS_D1)	5158&5158E
NC	NC	PIN 23	5158E



	R71	R72
RTS5158	ASM	ASM
RTS5158E	NO ASM	NO ASM

CLK CONTROL	R1303 R1301	X7,R1373, C842,C843
48MHZ	ASM	NO ASM
12MHZ	NO ASM	ASM

Pin 13 (XTAL CTL)	Clock source	Remark
Floating	12MHz crystal input	
Pull high	Clock generator's 48MHz input	Input to RTS5158E(Pin 48)

<Core Design>

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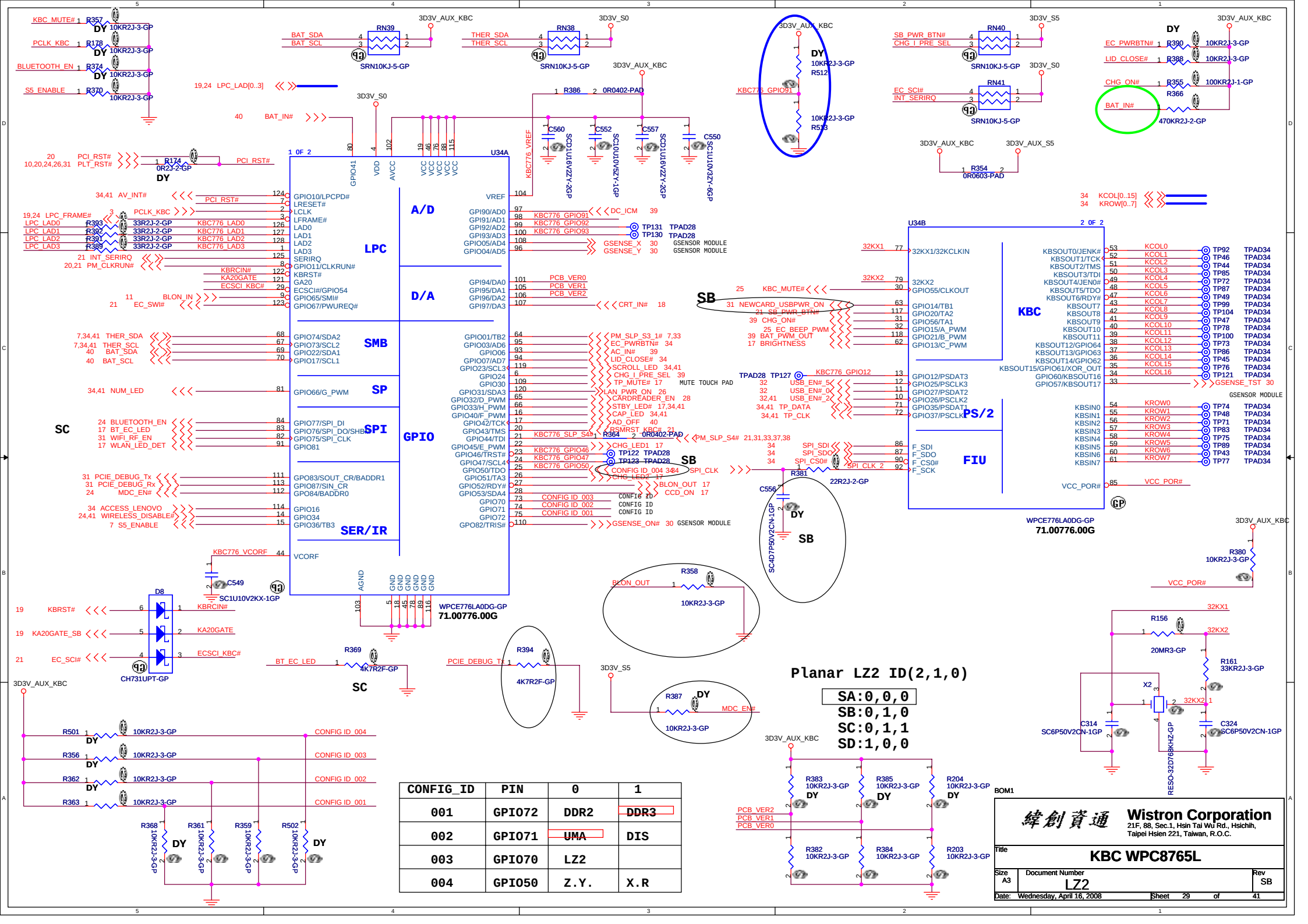
Title: CARD READER

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 28 of 41


U34A
1 0F 2
WPCE776LA0DG-GP
71.00776.00G
U34B
2 0F 2
WPCE776LA0DG-GP
71.00776.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
SB
KBC
PS/2
FIU
SC
Planar LZ2 ID(2,1,0)
SA:0,0,0
SB:0,1,0
SC:0,1,1
SD:1,0,0
CONFIG_ID | PIN | 0 | 1
001 | GPIO72 | DDR2 | DDR3
002 | GPIO71 | UMA | DIS
003 | GPIO70 | LZ2 |
004 | GPIO50 | Z.Y. | X.R
Wistron Corporation
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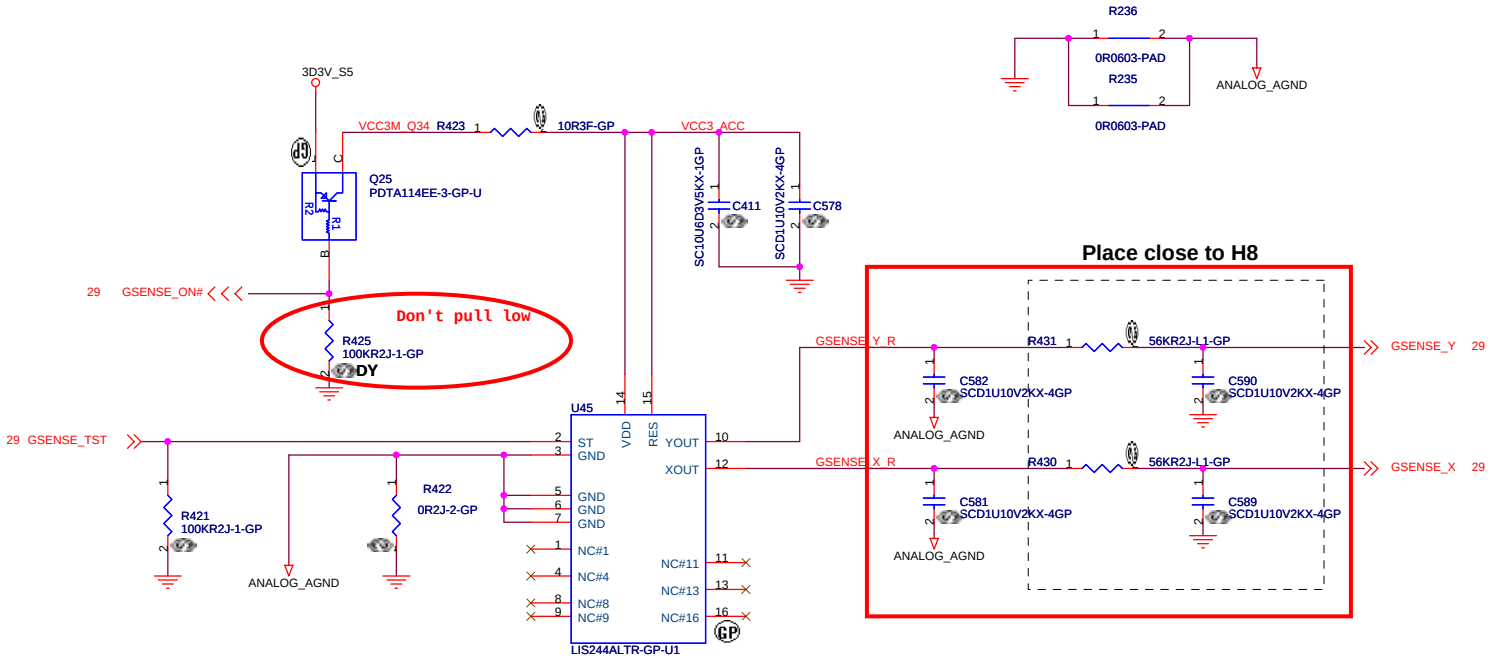
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8765L
Size A3
Document Number LZ2
Rev SB
Date: Wednesday, April 16, 2008
Sheet 29 of 41



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

BOM1

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Title: **GSENSOR**

Size	Document Number	Rev
	LZ2	SB

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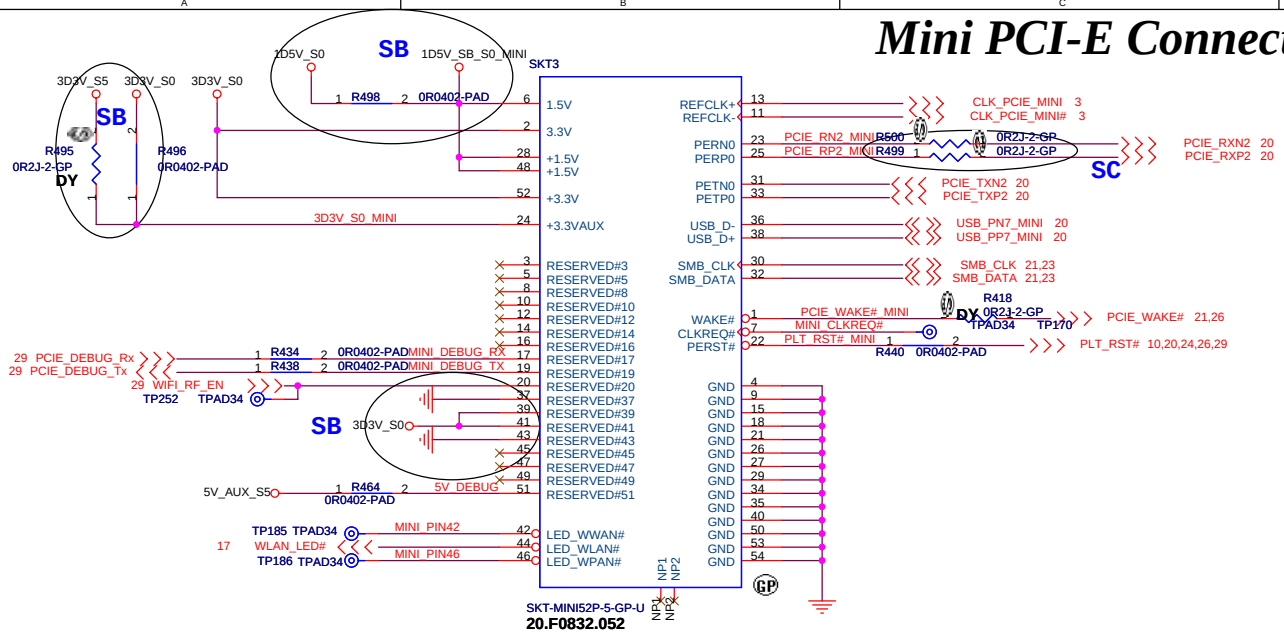
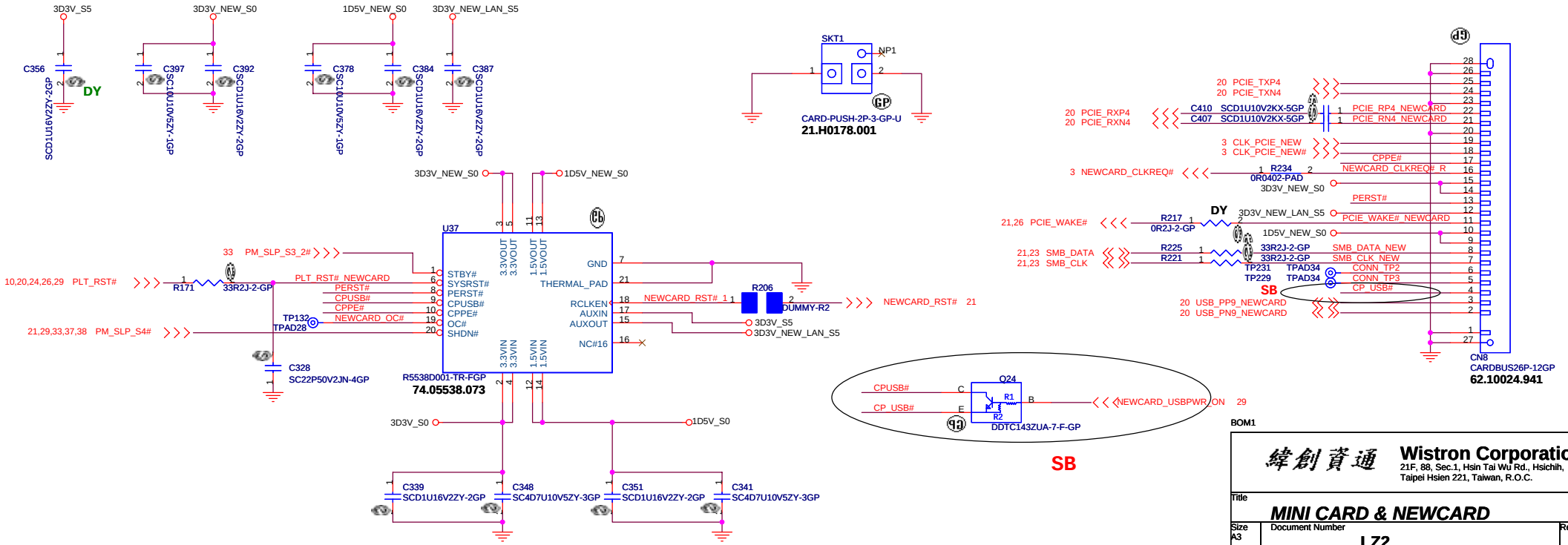
Mini PCI-E Connector



Place them Near to Chip

Place them Near to Connector

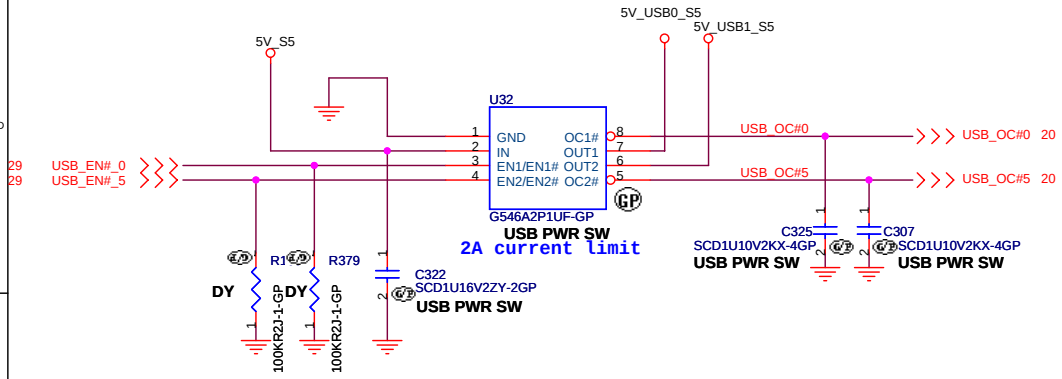
.N.E.W.C.A.R.D. C.O.N.N.

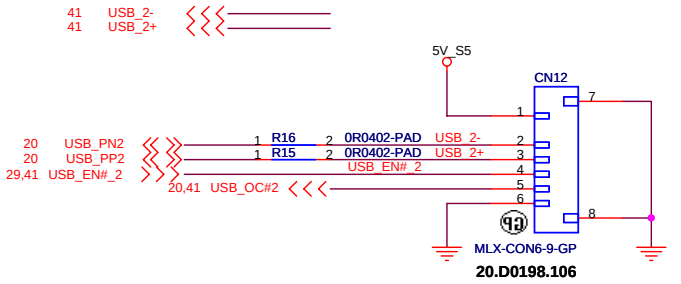


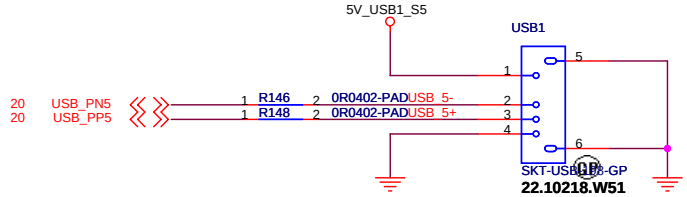
BOM1

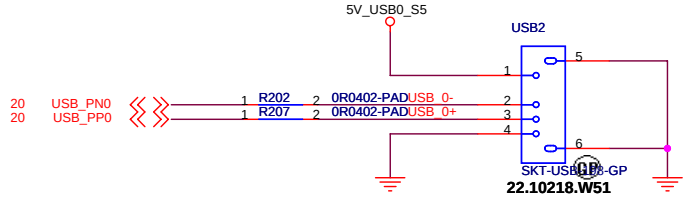
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD & NEWCARD	
Size A3	Document Number LZ2	Rev SB
Date: Wednesday, April 16, 2008	Sheet 31 of 41	

USB * 3 PORT

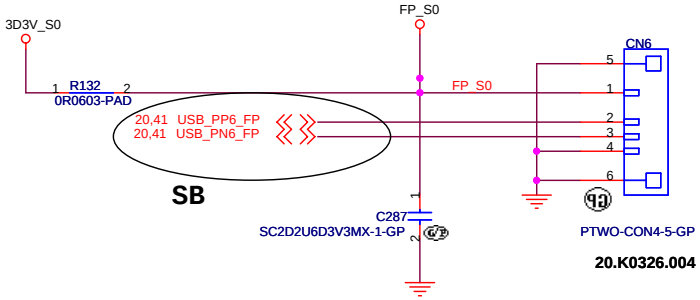


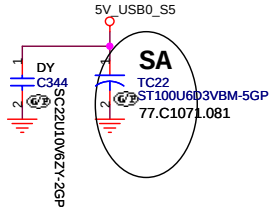


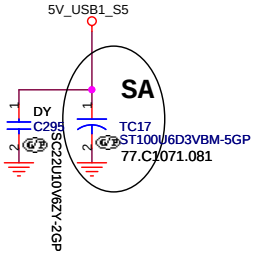


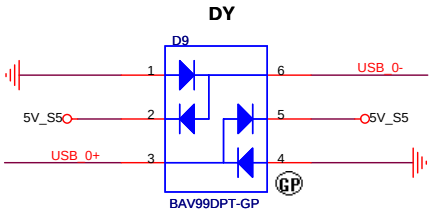


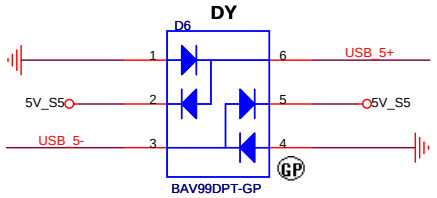
Finger Print











BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB CONN/FINGER PRINT**

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B	LZ2	SB

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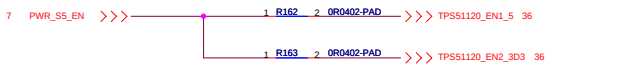
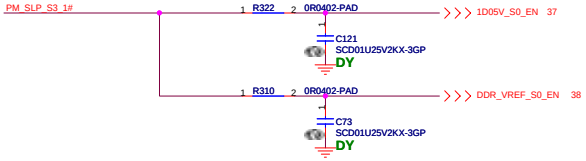
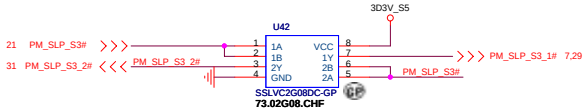
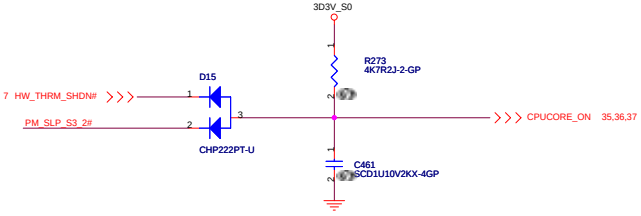
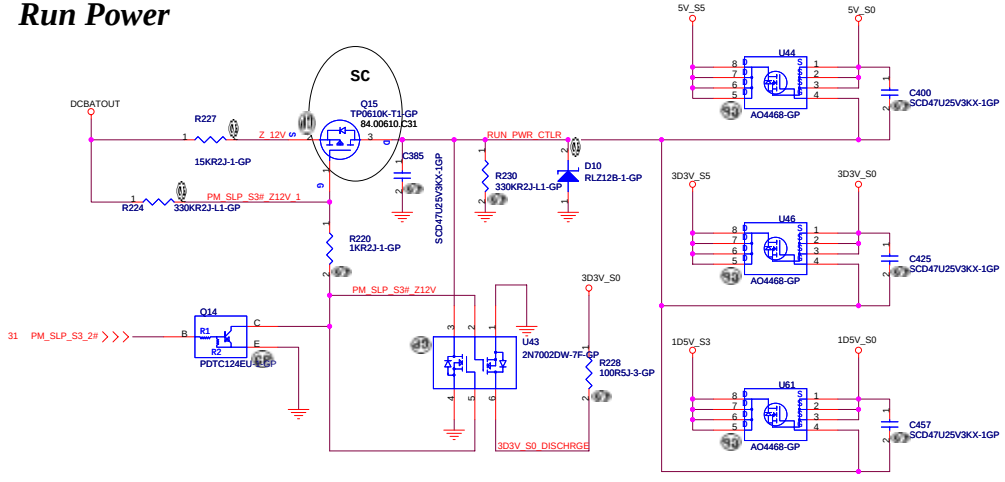


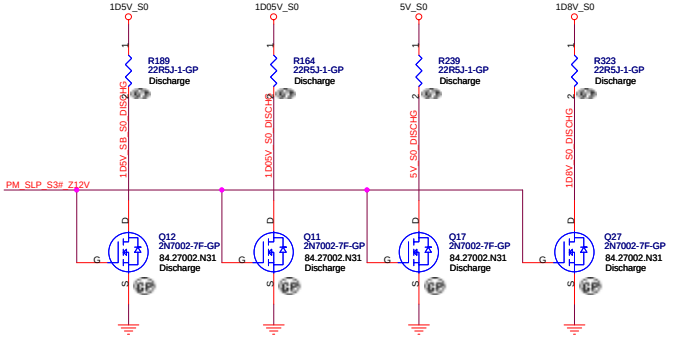


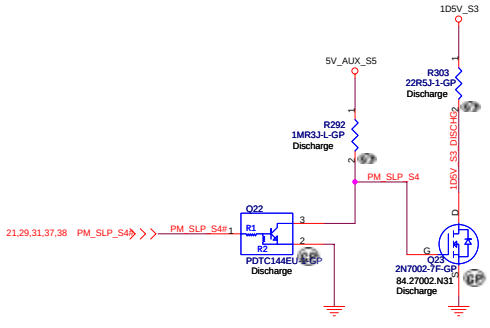




Run Power







BOM1

Wistron Corporation
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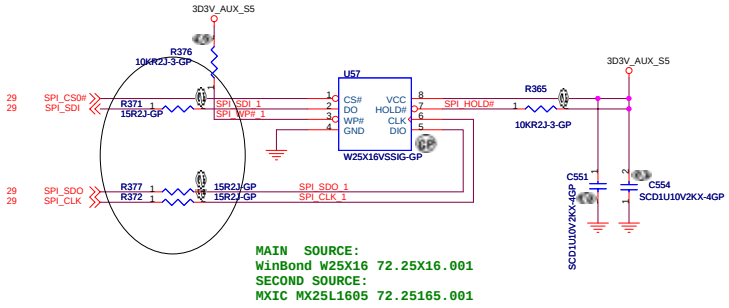
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESET LOGIC***

Size	Document Number	Rev
	LZ2	SB

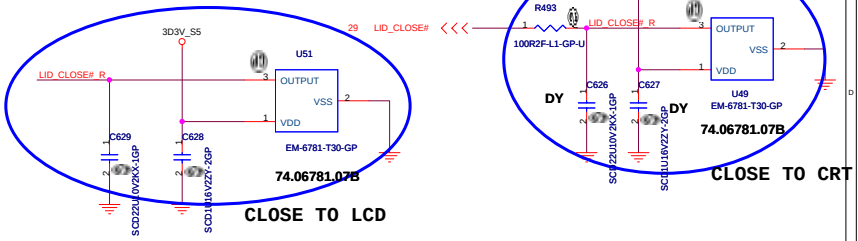
Date: Wednesday, April 16, 2008 Sheet 33 of 41

SPI Flash

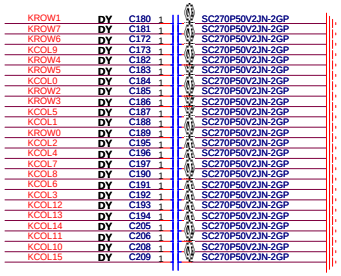


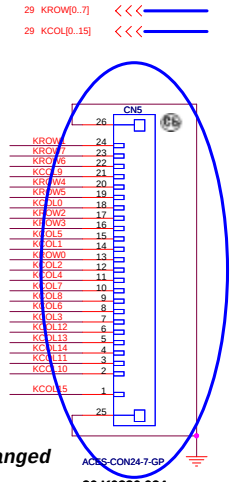
MAIN SOURCE:
WinBond W25X16 72.25X16.001
SECOND SOURCE:
MXIC MX25L1605 72.25165.001

Lid Switch



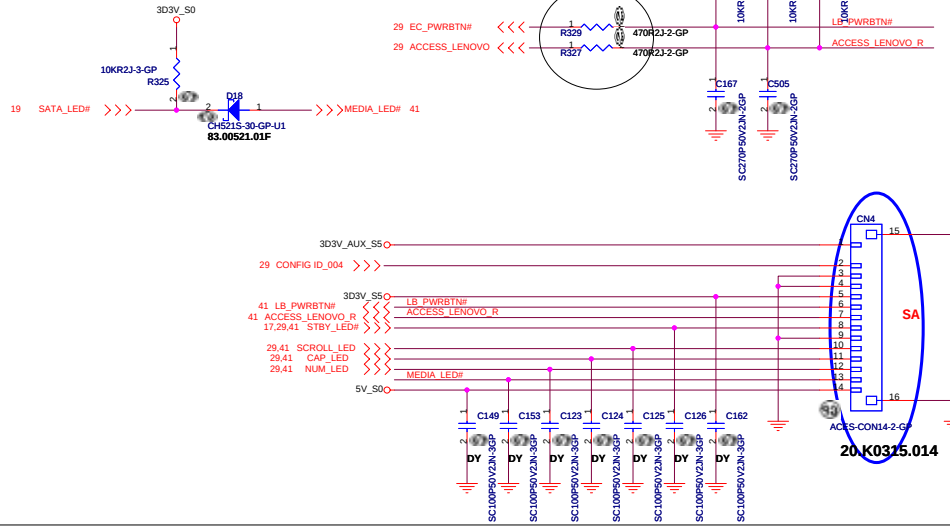
Keyboard Connector



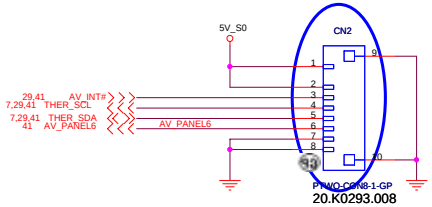


Changed

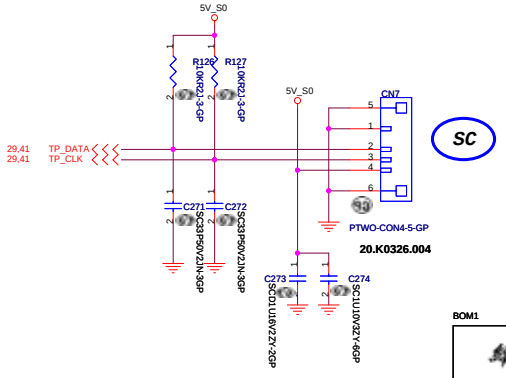
Launch Board



AV Panel



TouchPad Connector



BOM1

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP/SPI/AV/Charger

Size	Document Number	Rev
	LZ2	SB

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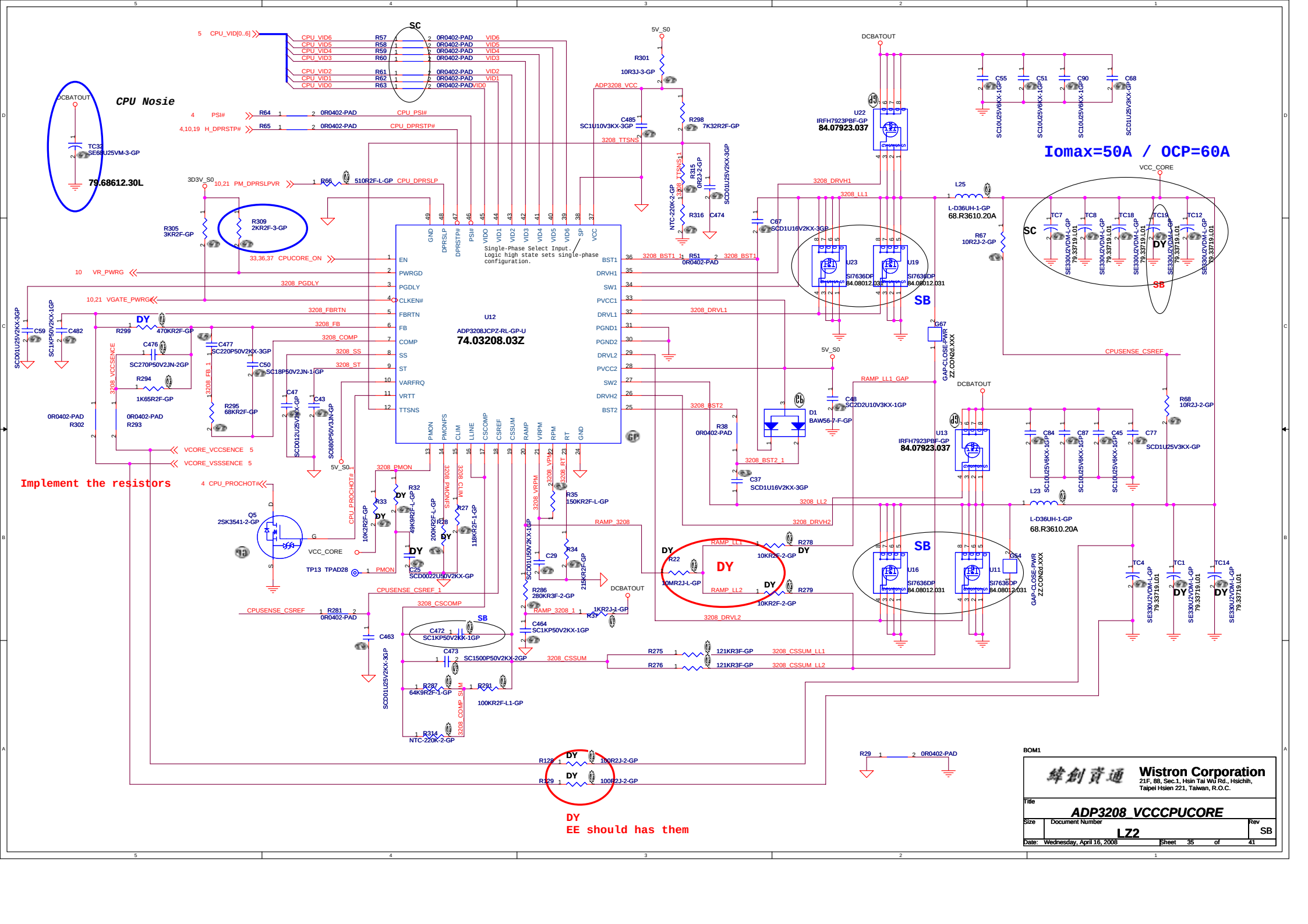
CPU Nosie
79.68612.30L
U12
ADP3208JCPZ-RL-GP-U
74.03208.03Z
Single-Phase Select Input.
Logic high state sets single-phase configuration.
Iomax=50A / OCP=60A
Implement the resistors
DY
EE should has them
SB
SC
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ADP3208_VCCCPUCORE
LZ2
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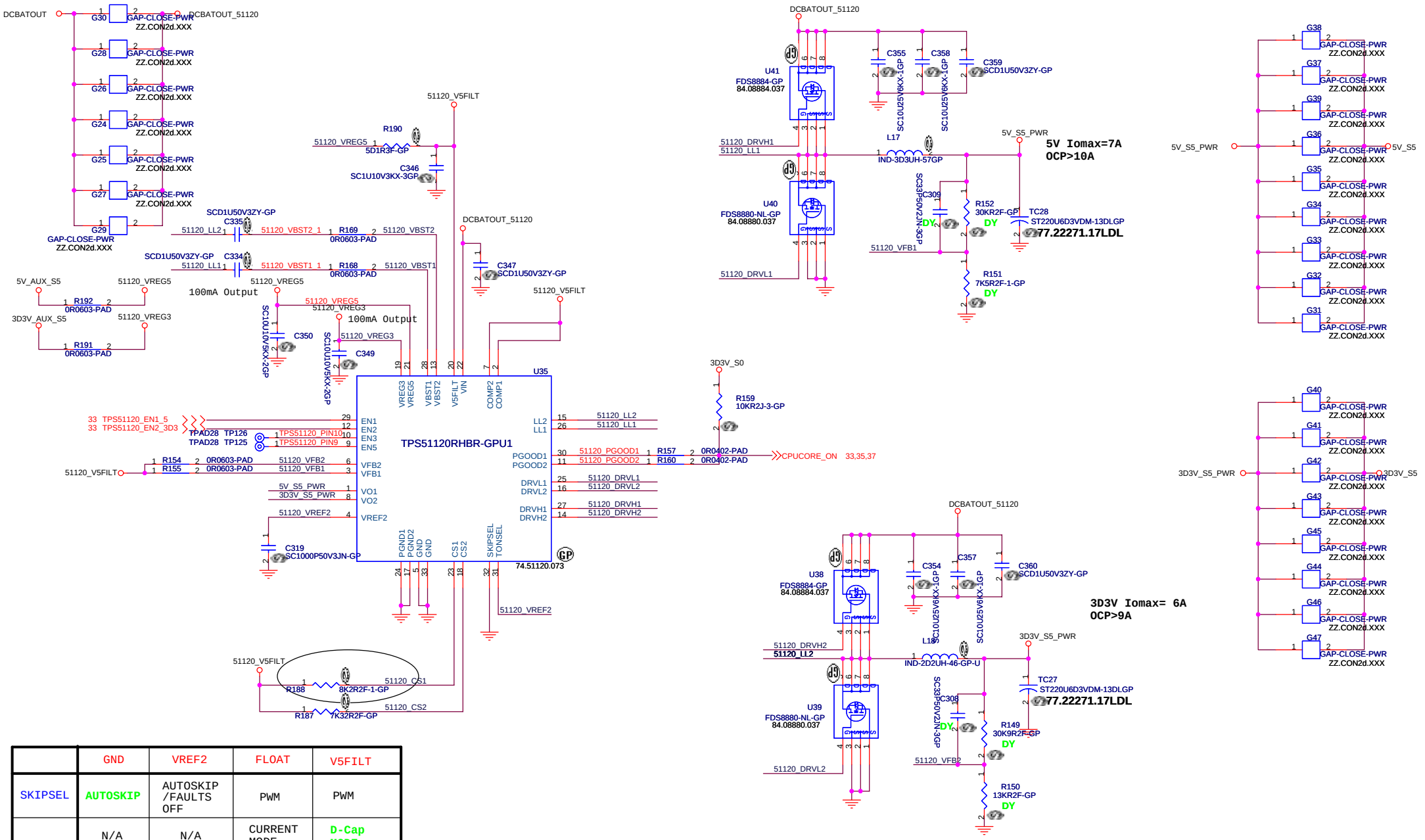

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	Switcher OFF	not use	Swithchr ON	Switcher ON
	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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Title: TPS51120 5V / 3D3V

Size	Document Number	Rev
A3	LZ2	SB

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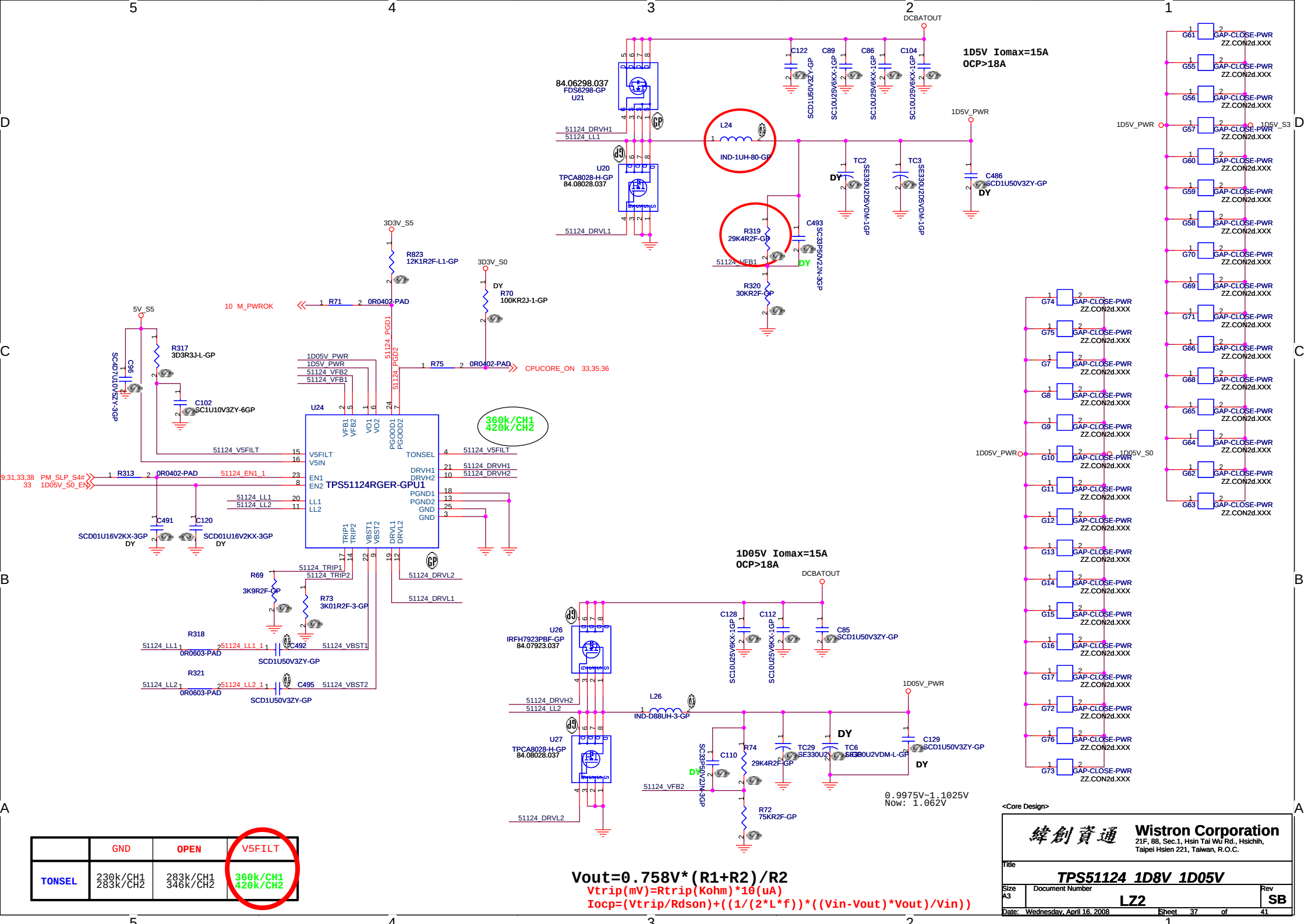

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360k/CH1 420k/CH2

<Core Design>

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Title: TPS51124 1D8V 1D05V

Size	Document Number	Rev
A3	LZ2	SB

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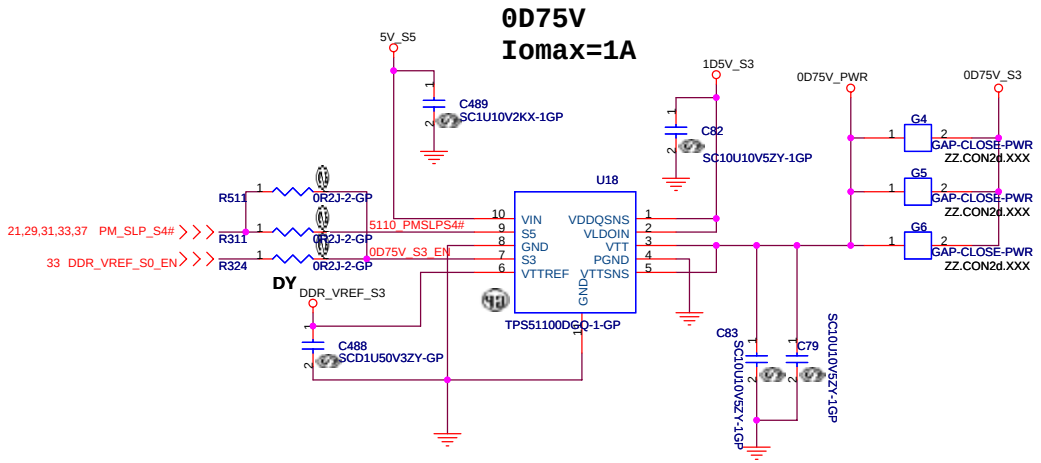

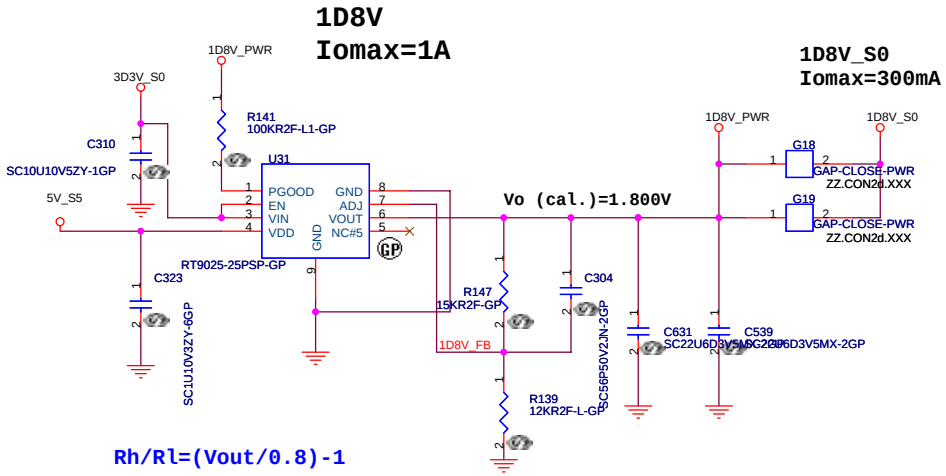

<Core Design>

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Title: LDO 0D9V / 1D5V_S0

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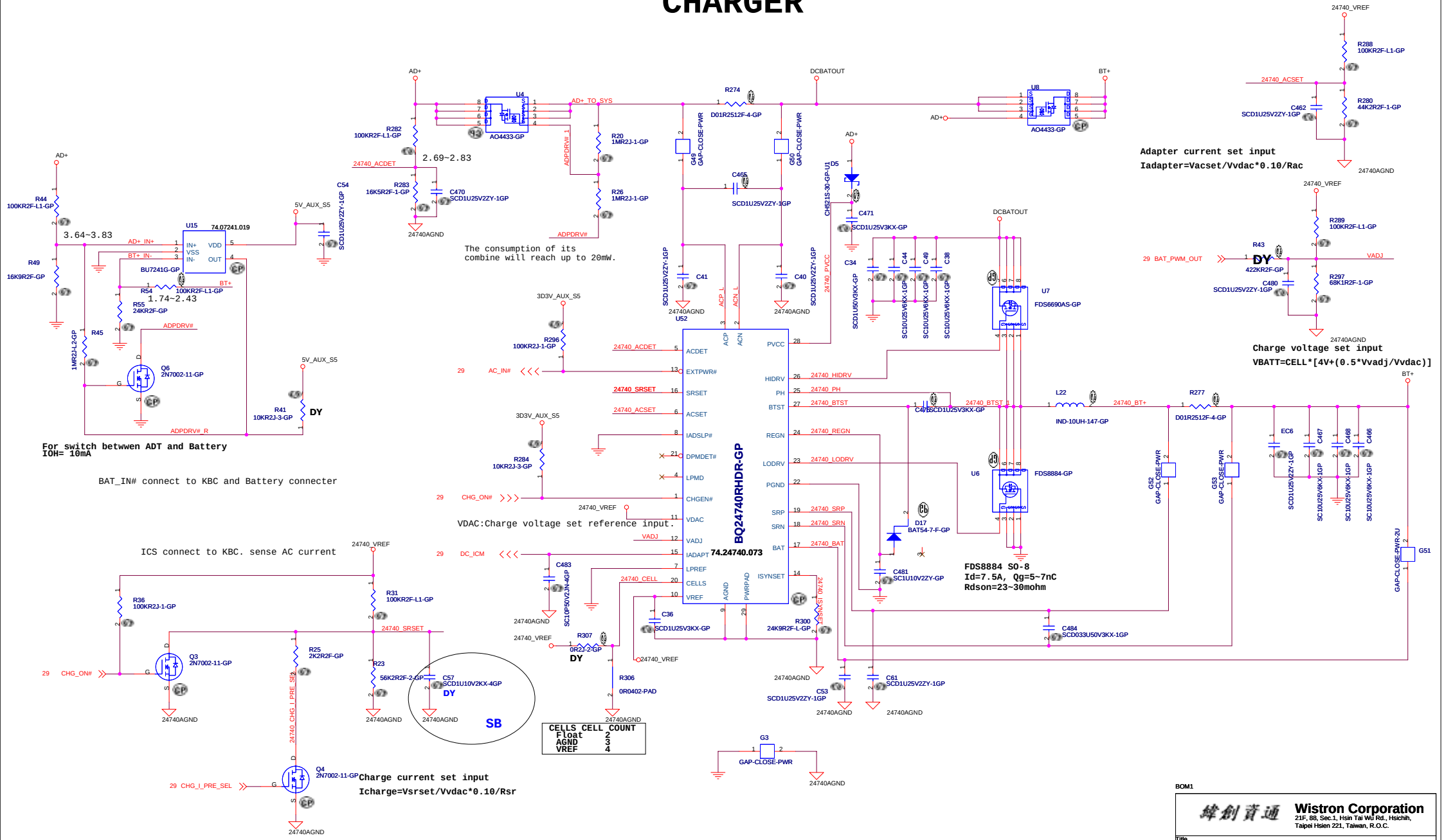
CHARGER



BOM1

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Title: Charger BQ24740

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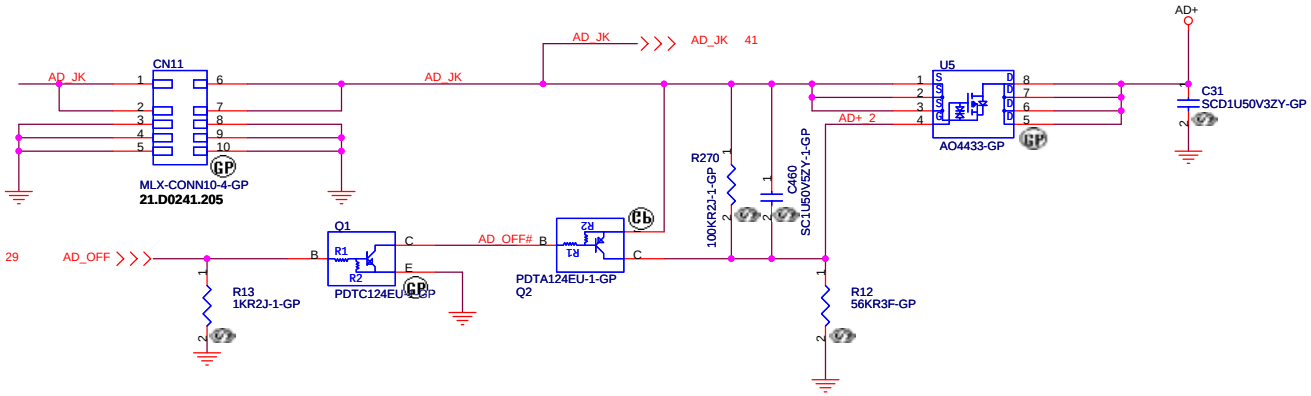
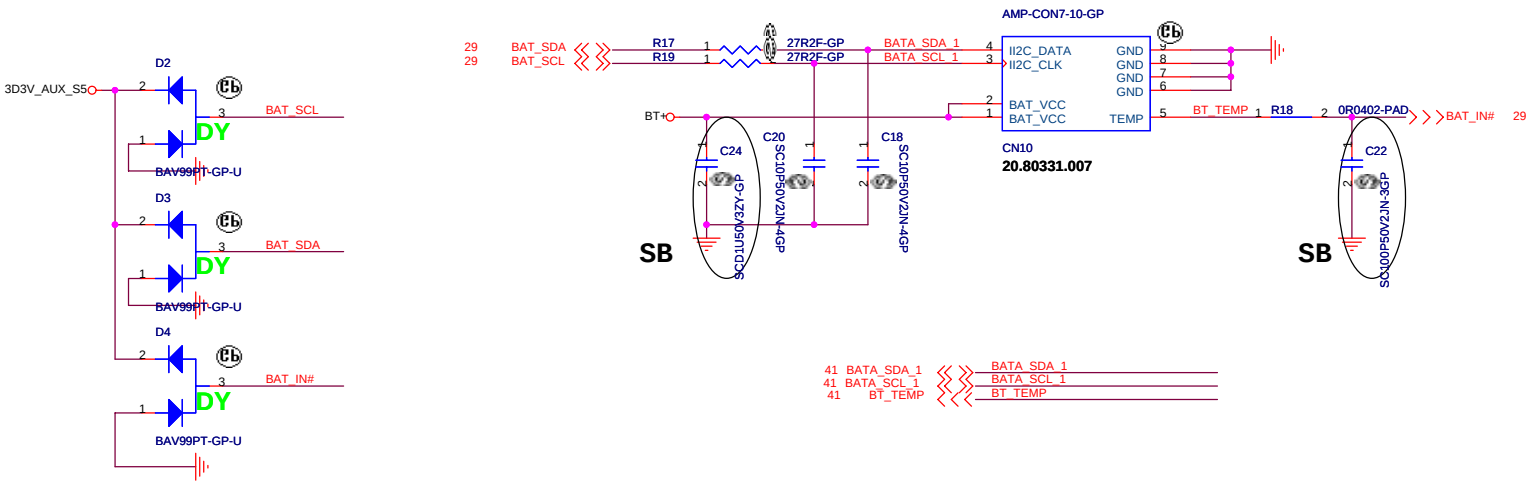
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Title: **PTH FOR SCREW HOLES**

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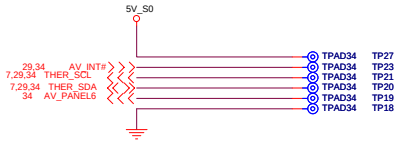
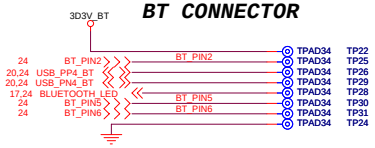
AV Panel



BT CONNECTOR

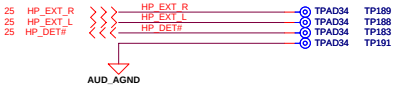


SATA CONN

TouchPad Connector

WIRELESS SWITCH

HEADPHONE CONN



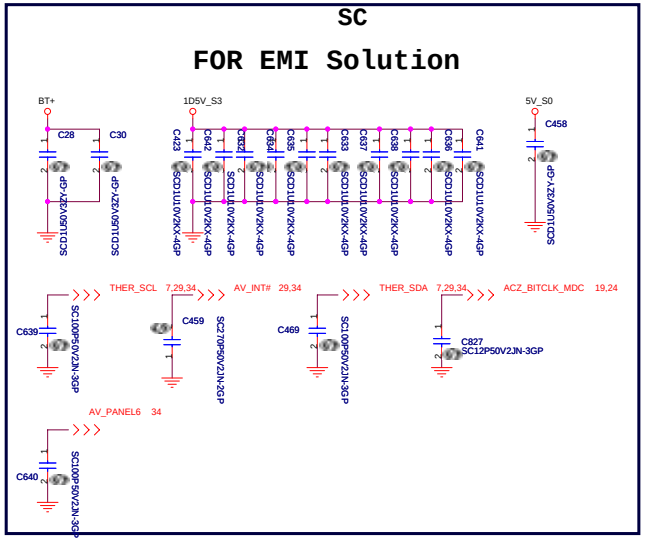
ODD CONN

MIC CONN

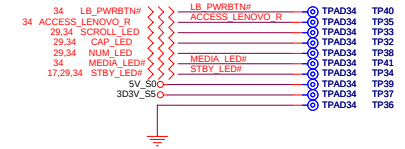
FAN CONN

SC

FOR EMI Solution

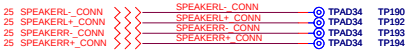


Launch Board

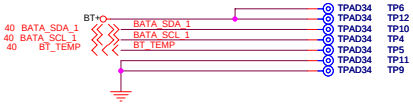


ADT BOARD CONN

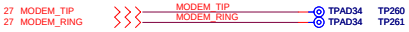
SPEAKER CONN



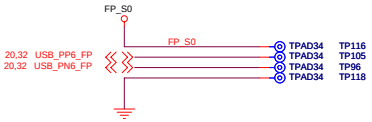
BATTERY CONN



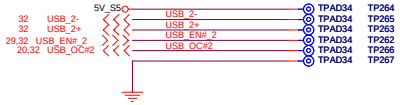
MODEM CABLE CONN



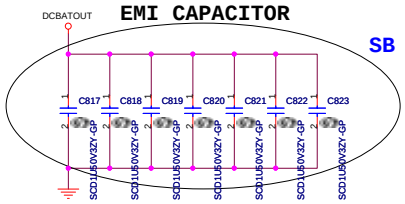
Finger Print CONN



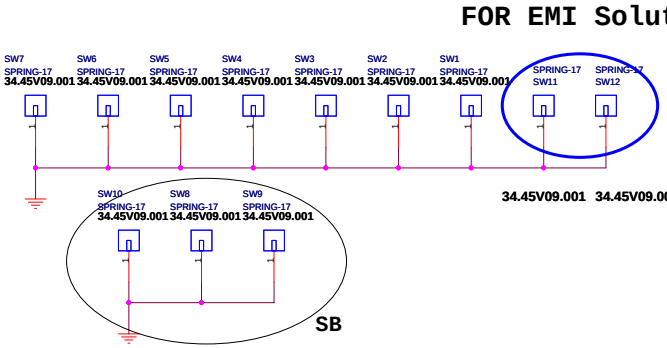
USB BOARD CONN

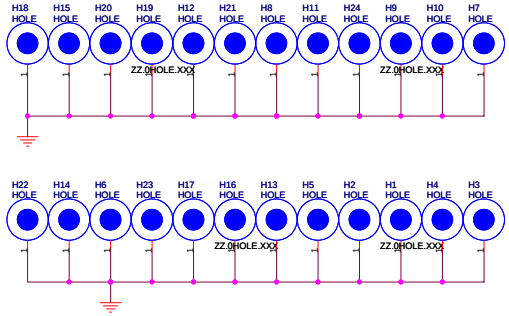


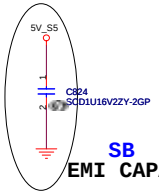
EMI CAPACITOR



FOR EMI Solution







BOM1

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Title: TTEST_PAD

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