Development and Testing of High-Voltage Devices Fabricated in Standard CMOS and SOI Technologies

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***Abstract*—This paper describes the work completed in the development of LDMOSFETs using only standard layers available in low voltage digital BULK and Silicon-on-Insulator (SOI) processes. Measurements indicate that breakdown voltages greater than 5X the rated process voltage can be achieved. The optimization method described involves the layout of a massive array. Transistor channel and drift region geometries are systematically varied in the layout. Optimization of the transistors must optimize the Drain-to-Source breakdown voltage while matching the threshold voltage and current drive to a given process. Current-voltage measurements must be evaluated and modeled for each process. A model for SOI, which accounts for back-gate MOSFET effects is presented. Testing setup is discussed, including. Breakdown measurements are presented and complications with LDSMOFET layouts and fabrication processes are discussed.**

I. Introduction

The demand for compact low power circuits continually steers the microelectronics industry deeper into submicron regions. Digital circuits have a distinct advantage at deep submicron lengths and extremely thin gate oxides. Deep submicron fabrication presents serious design constraints for analog and aerospace circuits. The reduced voltages associated with thin-oxide circuits require complex analog designs.

Typical system busses found in legacy and aerospace designs are 5V and 28V DC respectively. Compatibility between higher and lower voltage applications require low voltage interfacing of 3.3V, 2.5V, and 1.5V technologies with the higher voltage technologies. This voltage interfacing is difficult with standard deep submicron device configurations. One solution to high voltage tolerance for deep submicron is the development of Diffusion Metal Oxide Semiconductor Field Effect Transistors (DMOSFETs) in standard BULK and thin film Silicon-on-Insulator (SOI) processes.

Much effort has been dedicated to implementing Lateral DMOSFETs (LDMOSFETs) using standard fabrication layers found in both BULK and SOI. These transistors use a lightly doped drift region, either a pwell or nwell standard layer, between the drain and the gate region. This lightly doped drift region is native to the process mask steps and requires no additional processing mask.

This paper discusses the design of LDMOSFETs using a systematic approach. Variations of specific dimensions that lead to higher breakdown voltages in the LDMOSFET are mentioned. Results of breakdown voltages are presented and limitations of the LDMOSFET structure and processes are described.

The LDMOSFET have been developed in submicron and deep submicron processes for BULK CMOS and SOI. Included is work accomplished in radiation hardened SOI.

II. Layout

The LDMOSFET uses a lightly doped drift region to separate the standard drain region of a MOSFET from the gate channel region. This provides a voltage drop region between the drain connection and the gate channel. The reduced voltage decreases the E-field across the thin gate oxide; keeping the E-field below the oxide breakdown levels.

Cross sections of a BULK [1] and SOI [2] LDMOSFET are presented in Fig. 1 and Fig. 2. Optimization of the LDMOSFET in both BULK and SOI involve establishing an appropriate length for the transistor (L), the length of the drift region (Ld), and the overlap of the gate over the P-N- junction (Lg).

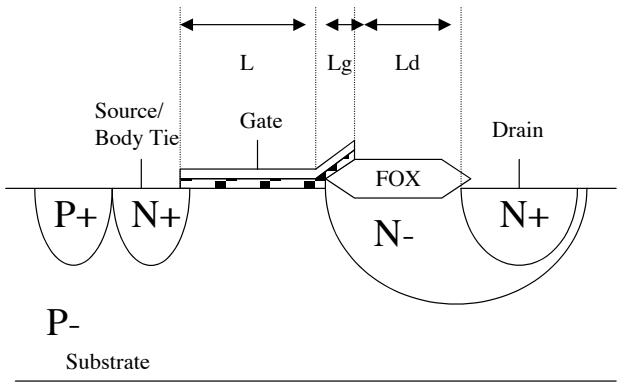

Figure 1 A cross section of a BULK LDMOSFET

New layouts for the LDMOSFETs must be generated in each process. This is in part due to the different doping levels of each process and feature size migration. Layouts must be adjusted to accommodate different mask rules imposed by the foundry. For

example, some SOI processes require a channel/well (Lcw) overlap be drawn under the gate oxide in the layout. The Lcw region is a drawn overlap of the gate-channel region and the drift region. Without a drawn Lcw overlap, a formation of intrinsic silicon or oxide may occur between the PN junction.

The development of the LDMOSFET in BULK CMOS investigated the development of self-enclosed non-Manhattan type devices [3]. Fig. 3 shows the topside view of a "race-track" structure. The self-enclosed structure isolates the high voltage drain from the surrounding low voltage circuits. This prevents the accidental latchup in surrounding circuits due to proximity effects. The race-track structure also prevents high E-field pinching observed in square-gated structures, for example as shown in Fig. 4.

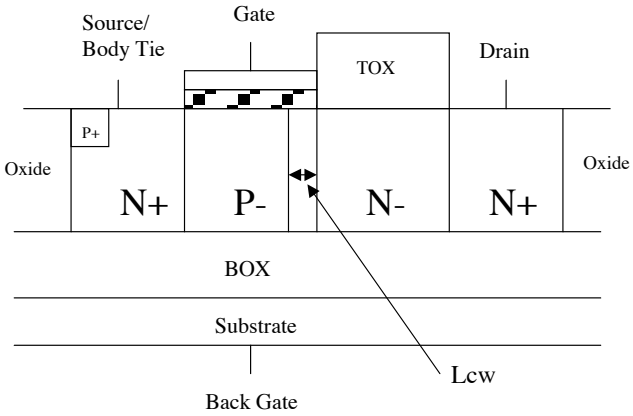

Figure 2 A cross section of an SOI LDMOSFET

Following the BULK CMOS layout approach, the initial devices developed in SOI were self-enclosed, primarily to prevent high E-field pinching. This caused severe layout problems for radiation hardened SOI processes. For example, in some cases the layout violations will result in metal flaking during fabrication, corrupting the entire fabrication run.

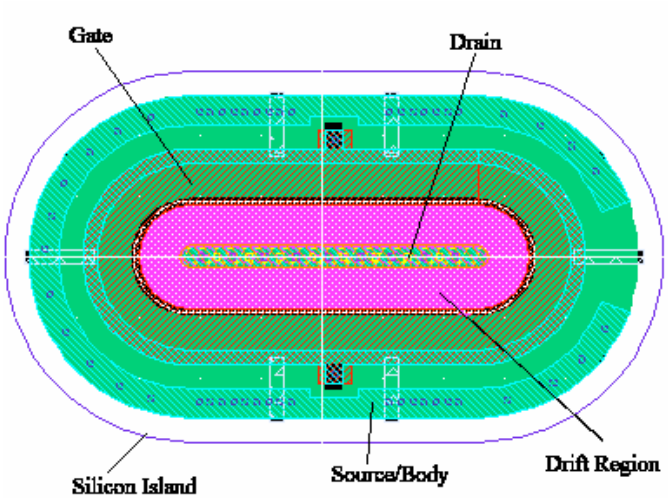

Figure 3 Self enclosed circular or racetrack LDMOSFET.

The single sided LDMOSFET, shown in Fig. 5 is not practical in BULK CMOS for compact layout. Latchup effects have been observed in BULK circuits where area intensive isolation techniques or self-enclosed devices were not used around the high voltage drain. An additional concern of the single sided LDMOSFET in BULK is the possibility of leakage currents from drain-to-source through or around the transistor sides. The single sided LDMOSFET developed for SOI uses the oxide separating silicon islands for latchup and leakage isolation.

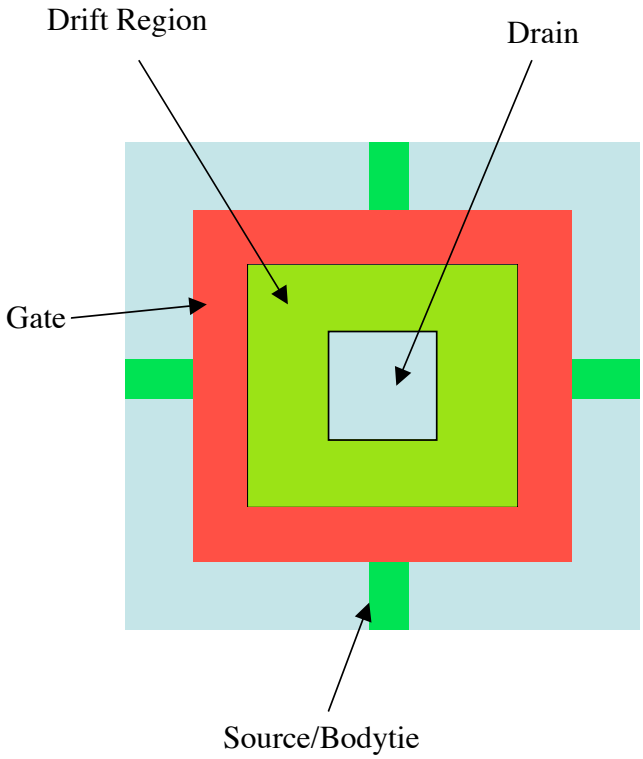

Figure 4 Self-enclosed LDMOSFET square device

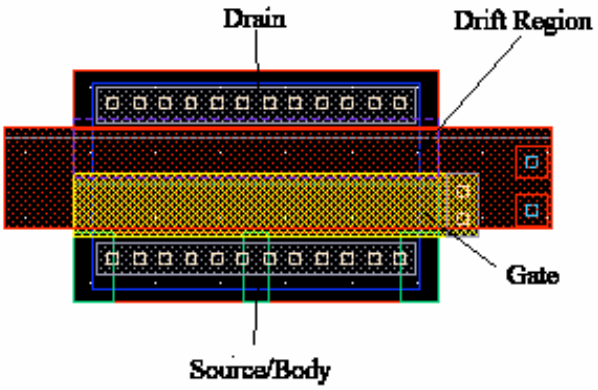

Figure 5 Single sided SOI LDMOSFET

III. Optimization

An optimized transistor must have a combination of a high VDS breakdown and approximately match the threshold voltage and drive current of a given process. A balance of these characteristics must be achieved for a successful transistor. It is

possible to have extremely high breakdown and have extremely low current capabilities.

Optimization of the LDMOSFET can be done in one of two ways. The first uses simulation techniques to optimize the LDMOSFET as in [4]. This requires extensive process information provided by the fabrication facility. Most semiconductor fabrication facilities do not disclose detailed doping profiles to protect the intellectual property of the fabrication processes. For this reason, a second method was used to create and optimize the LDMOSFETs. The second method involves the layout of a massive array, systematically varying L, Ld, Lg, and Lcw. Either method requires layout development for a specific process. The second method is measurement intensive, but in most cases delivers first pass results.

A full array characterization technique systematically varies features of an LDMOSFET. Full arrays where L is varied can be extremely area intensive when varying Lg, Ld, and Lcw by 0.1μm over lengths of 2μm. To reduce the area required for development, all transistors in this paper except for the 0.25mm LDMOSFETs use lengths of 4μm for NMOS and 2μm for PMOS. Long lengths avoid short channel effects and decrease the impact of process variations and poly placement variations.

The purpose for the characterization array is to determine which parameterized geometries provide the highest breakdown voltage, the lowest threshold voltage, and acceptable current drives. Typically, the goal is to match the threshold voltage and drive current of the LDMOSFET to the standard MOS transistors in a given process. An acceptable transistor balances all three characteristics. To find the optimized transistor in the array, some characterization data must be extracted from each transistor.

Each MOS structure contains two transistors in SOI, the first being the topside and the second being the back-gate transistor. Characterization data containing IDS-VDS, IDS-VGS information is measured, as shown in Fig. 6 and Fig 7 respectively.

Modeling of the most promising high voltage transistor must be created for the topside transistor and the back-gate transistor. This will provide an optimized model, taking into account back-gate effects that may vary the on-resistance and breakdown voltage [5].

IV. Testing

Testing a full development array can be very time consuming and repetitive. Designing the layout for testing must be considered when organizing the test arrays and structures. Simple techniques like sharing gates and sources can reduce the number of probe contacts, but not without penalty. Sharing gates and source connections across the entire array can lead to the failure of the entire array if one transistor conducts current, either by oxide failure or fabrication anomaly. If terminal sharing must be done, it is recommended at only the source terminal.

Automation of the test routine is recommended for large transistor arrays. This can be performed using a probe card structure compatible with the pad frame, a switch matrix, a semiconductor analyzer, and a GPIB/computer system for control and data storage.

V. Results

Both BULK and SOI submicron results are presented. Table 1 and Fig. 8 report breakdown voltages of the processes listed. The maximum breakdown voltage in BULK CMOS was recorded at 80V for an NMOS in a 5V process. The maximum SOI breakdown voltage in an NMOS was recorded at 75V and was fabricated in a 5V rad-hard process. The breakdown voltages in the PMOS devices are less than the NMOS in the given technologies.

The transistors in the deep submicron SOI were all single sided. The NMOS and PMOS voltages are more matched. Even in a 1.5V fully depleted SOI process the breakdown was reported at over 5X the rated voltage. Table I provides information on the process voltage and radiation hardness.

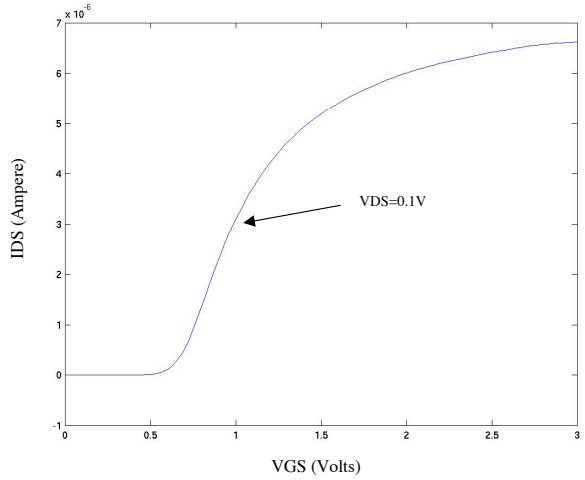

Figure 6 IDS-VGS curve for R6SOI

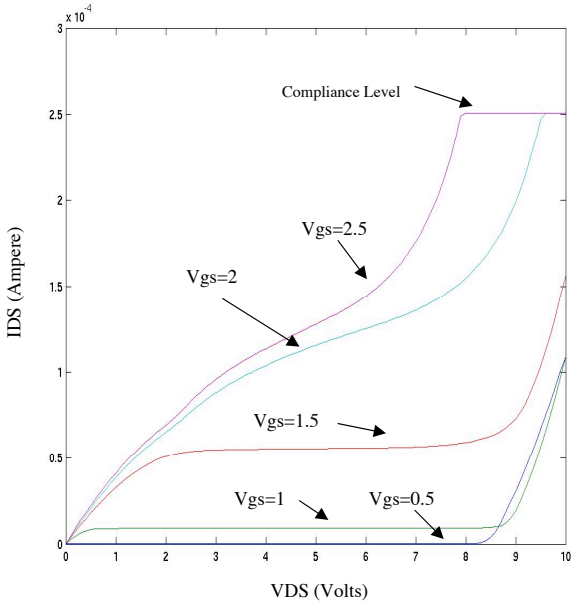

Figure 7 IDS-VDS curves for R6SOI

TABLE I

Process	NMOS (V)	PMOS (V)	TYPE	Rated Voltage	Radiation Hardened
HP CMOS26 0.8□m	80	32	BULK	5V	NO
Honeywell R4SOI 0.8□m	75	30	PDSOI	5V	YES
HPCMOS14TM 0.5□m	34	19	BULK	3.3V	NO
Honeywell R5SOI 0.35□m	18	N/A	PDSOI	3.3V	YES
Honeywell MOI5 0.35□m	27	25	PDSOI	3.3V	NO
Honeywell R6SOI 0.25□m	8	8	PDSOI	2.5V	YES
MIT Lincoln Labs 0.18□m	8	6	FDSOI	1.5V	NO

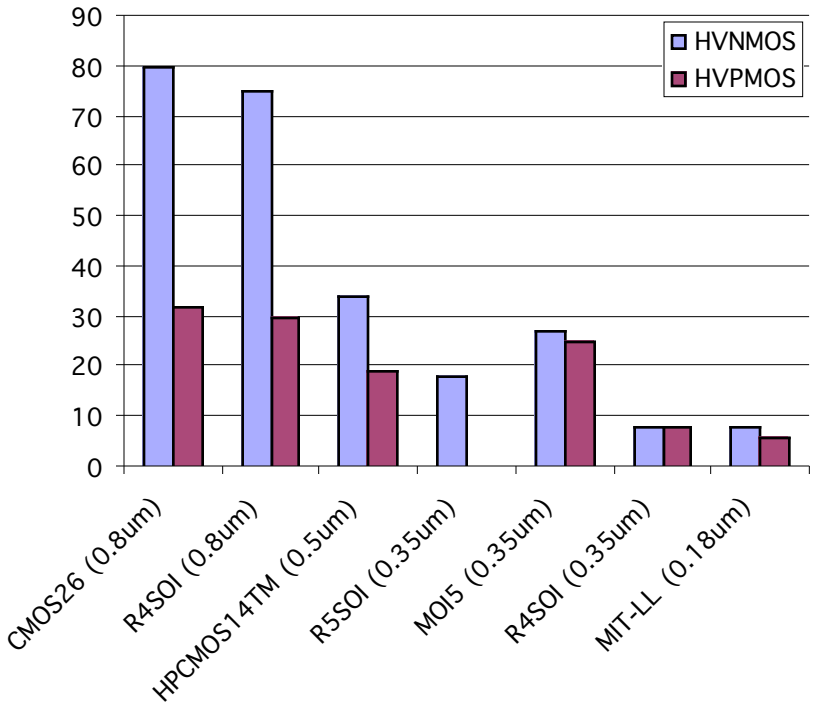

Figure 8 Breakdown voltages per process

Fig. 9 and Fig. 10 shows the back-gate IDS-VGS and IDS-VDS characteristics, respectively for an R4SOI NMOS SOI LDMOSFET. Note that the back-gate threshold of the NMOS shown is about 46V Back-gate to Source. Additionally, SOI MOSFETs and LDMOSFETs substrate can be biased to create the inversion, depletion, or accumulation region just above the buried oxide layer [5].

An equivalent SPICE circuit of the LDMOSFET must model the top-gate, back-gate and all associated resistances. Fig. 11 presents an equivalent circuit model for the LDMOSFET.

The Drain-to-Source leakage current is insignificant with a self-enclosed geometry. The leakage current of the single sided LDMOSFET in SOI was measured at 50pA with the top gate and back-gated transistors completely off.

VI. Discussion

The results in Tables I indicate that higher voltages per transistor can be achieved in the larger feature size processes. Data from Table I and Fig. 8 also indicates that the high voltage gap between NMOS and PMOS type LDMOSFETs decreases with feature size. It is desirable to have matching N and P-type LDMOSFET breakdown voltages when designing voltage tolerant structures. Otherwise the voltage of a circuit is limited to the smaller breakdown.

Table I also shows that high breakdown voltages can be achieved in radiation hardened and non-radiation hardened SOI. Native 5V process can achieve VDS breakdown voltages greater than 70V for NMOS and greater 25V for PMOS. Native 3.3V process achieve breakdowns between 28 and 18 volts VDS for NMOS and PMOS. Deep submicron

process with less than native 3V breakdowns can achieve greater than 6V breakdowns, even in fully depleted SOI.

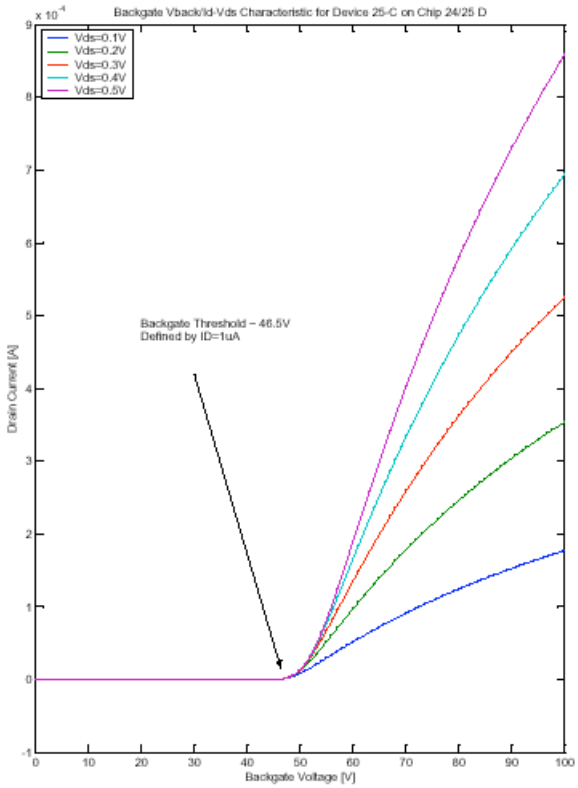

Figure 9 Back-gate Threshold Curves in R4SOI

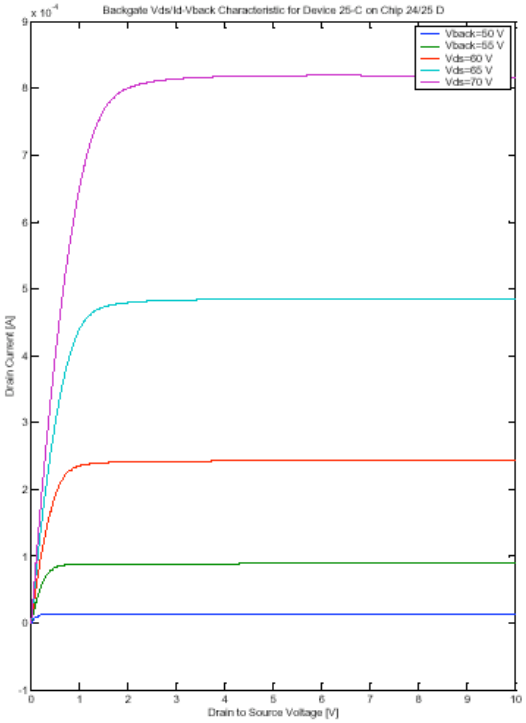

Figure 10 Transistor curves due to the back-gate in R4SOI.

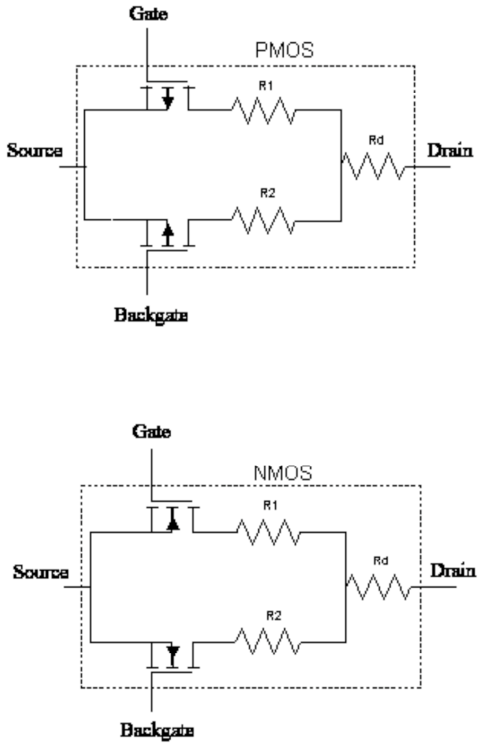

Figure 11 LDMOSFET circuit model for SOI due to back-gate effects.

SPICE models for the LDMOS are achieved by characterizing the top-gate for both BULK and SOI. Only SOI requires the characterization of a parasitic back-gated device. Complete SOI models must include this back-gate for high-performance models. Leakage paths can be created through the back-gated MOS, which will appear as a modulation of the channel resistance. The magnitude of the threshold voltages for the back-gate is much large than the top-gate transistor. For low performance models, the back-gate can be neglected.

The measurement procedure should be automated for large arrays to minimize the repetitive process of probing hundreds of transistors. Typical automation equipment include a probe-card structure, a switch matrix, a semiconductor analyzer, a computer, and a GPIB connected computer for automation control.

VII. Summary

This paper presented a method of optimizing LDMOSFET transistors that use a native lightly doped drift region to extend a high voltage tolerant drain from the gate-channel region. Optimization of an LDMOSFET for a given process involves the systematic layout of a large array of LDMOSFETs varying four parameters, Lg, Ld, and Lcw by 0.1 m over lengths of 2 m. Optimization procedures involved determining the highest breakdown voltage for a

transistor while matching the threshold voltage and drive current to a standard transistor in a given process. Measurements were presented for optimized LDMOSFETs in submicron and deep-submicron processes. These fabrication processes include BULK and SOI. Breakdown voltages in radiation hardened SOI are reported as well as a fully depleted version of the LDMOSFET. A proposed SPICE model is presented which includes the back-gate transistor inherent to SOI.

ACKNOWLEDGMENT

This work was supported by grants and contracts from the Boeing Corporation, Jet Propulsion Laboratory, and Honeywell Inc. Additional funding was provided by the NASA EPSCoR Grant NCC5-557.

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