

## L.C oscillator Tutorial

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### 1 ABSTRACT

This tutorial describes the operation of a basic L.C oscillator as used in RFIC circuits etc. The pertinent design parameters are given together with their relevant equations to allow basic 'hand' calculations before simulation is attempted. The initial design consists of a fixed frequency oscillator that is further developed into a voltage controlled oscillator (VCO), by the use of MOS devices configured as varactors. Finally a worked example is given to highlight the design steps required and CAD simulations are also described.

### 2 INTRODUCTION

L.C oscillators are probably the most common type of oscillator used in RFIC design. They can be designed for a fixed frequency and variable frequency operation (with the use of a varactor). The performance of the oscillator is determined by the Quality factor of the L-C resonator. Usually, a spiral inductor is used in the resonator and these have quite low Q's of around 3-5 at 2.5GHz. If a low-phase noise design is required the inductor can be made 'off-chip'. The inductor can be either resonated with the device drain capacitance or by adding a shunt capacitor (on chip or off).

### 3 OSCILLATOR DESIGN PHASE NOISE[1].

For a discussion on phase noise read the Phase Noise Tutorial.

But in summary Leeson's equation is given below:-

$$L(f_m) = \frac{FkT}{2P_{avs}} \left[ 1 + \frac{fc}{fm} + \left( \frac{f_o}{2f_m Q_L} \right)^2 \left( 1 + \frac{fc}{fm} \right) \right]$$

Phase perturbation

Resonator Q

Flicker effect

Usually the phase noise is specified in dBc/Hz ie :-

$$L(f_m) = 10 \log_{10} \left\{ \frac{FkT}{2P_{avs}} \left[ 1 + \frac{fc}{fm} + \left( \frac{f_o}{2f_m Q_L} \right)^2 \left( 1 + \frac{fc}{fm} \right) \right] \right\} \text{ dBc / Hz}$$

The Leeson equation identifies the most significant causes of phase noise in oscillators, in particular the key parameter is the loaded Q of the resonator. We know that typically in CMOS the loaded Q of a spiral inductor is in the range 3-5. Therefore, if a tighter phase noise specification is required then the inductor will need to be off-chip.

### 3.1 L-C OSCILLATOR OPERATION

The circuit of the L-C oscillator is shown in Figure 1.

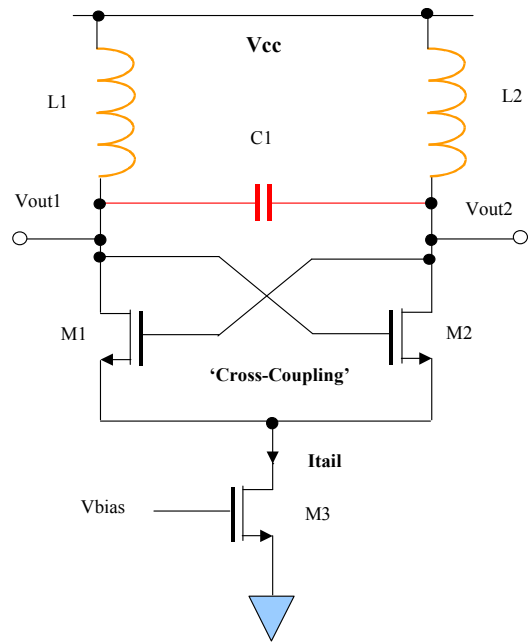


Figure 1 Schematic diagram of the 'cross-coupled' L-C MOS oscillator. M3 sets the currents through each arm of the differential oscillator, and M1 & M2 provide the negative impedance. The inductors L1 & L2 may be off-chip (depending on the phase noise requirement) and the resonating capacitors may be the drain capacitances of the devices themselves.

Each arm of the oscillator has a L-C tank circuit that determines the frequency of oscillation and form the drain loads. Frequency dependant signals at the drains are then 'cross-coupled' to the other devices' gate, which



creates a negative impedance of value  $-1/g_m$  at the drain terminals.

Generally then:

$$\text{Series } R \text{ of inductor} = \frac{2\pi \cdot f \cdot L}{Q_u}$$

For oscillation :

$$\frac{1}{g_m} \geq \frac{2\pi \cdot f \cdot L}{Q_u}$$

$$\text{Where } g_m = \frac{I_b}{(V_{gs} - V_t)}$$

Therefore,

$$\frac{(V_{gs} - V_t)}{I_b} \geq \frac{2\pi \cdot f \cdot L}{Q} \quad \text{Rearrange to get } I_b$$

$$I_b = \frac{Q(V_{gs} - V_t)}{2\pi \cdot f \cdot L}$$

To ensure reliable startup, L-C oscillators are designed to have a *startup safety factor* of at least 2 ie

$$\frac{2}{g_m} > R_p = \frac{2\pi \cdot f \cdot L}{Q_u}$$

## 3.2 VARIABLE FREQUENCY OSCILLATOR (VCO)

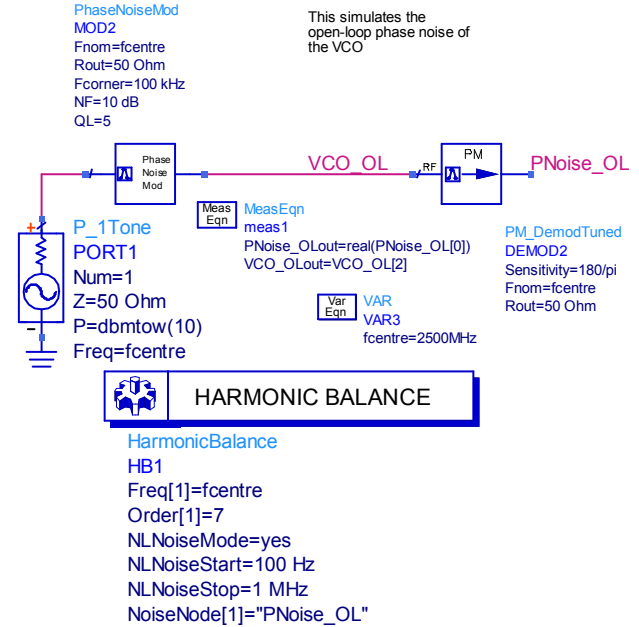
From the previous section we have seen how cross-connecting the two transistors gives a negative impedance of  $-1/g_m$ . We also know that this value has to exceed the losses of the resonator in order for the circuit to oscillate.

For this tutorial we shall design an example Vco with the following specification:

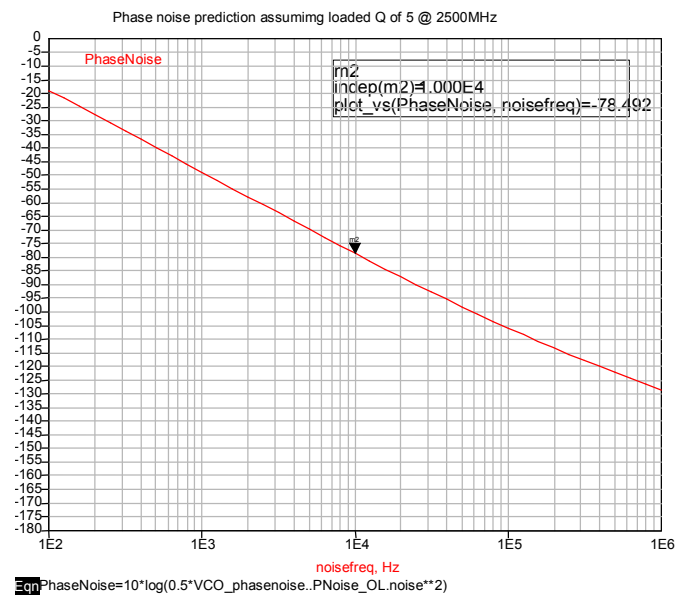
Parameter	Specification	Units
Centre Frequency	2.5	GHz
Tuning Bandwidth	500	MHz
Ko	>100	MHz/V
Phase noise (10KHz offset)	> 70	dBc/Hz
Supply	± 2.5	V
Power consumption	<100	mW

First of all we need to determine the minimum loaded Q of the resonator to achieve the required phase noise performance. The values of the circuit/resonator can be fed into Leeson's equation or the ADS simulation of **Figure 2** run. The resulting phase noise prediction of this simulation is shown in **Figure 3** and shows that if we use a

resonator with a minimum loaded Q of 5 then we should achieve our phase noise goal.



**Figure 2** ADS simulation to predict phase noise of an oscillator. Here we have entered the Q of the resonator of 5 (3-5 being the typical Q of a on-chip spiral inductor). We have made assumptions of the noise figure (10dB), output power (0dBm) and output impedance (50 ohms).



**Figure 3** Phase noise prediction of the L-C oscillator with a resonator Q of 5, resulting in a phase noise of  $-78\text{dBc/Hz}$  at an offset of 10KHz.

However, varactors with a high tuning constant ( $K_o$  (MHz/V)) will generate a lot of modulation noise and may well dominate the phase noise generated by the device and resonator.

The loaded Q of the resonator, will be determined by the loaded Q of the inductor and the loaded Q of the MOSFET varactor (variable capacitor). Each component can be represented by an ideal reactance with a parallel resistance representing the loss of the component.

Typical Q values for an 'on-chip' spiral inductor at 2.5GHz is 3 to 5. Therefore, if we wish to use an inductor with a higher Q, we have to consider off-chip inductors. Off-chip inductors are commonly formed using bond-wires and for completeness of this tutorial design notes on bond wire inductors will be given.

### 3.2.1 Bond wires as inductors [2]

Larger inductances can be realised with bond-wires that have Quality (Q) factors an order of magnitude higher than on-chip spiral inductors.

**Note** that low Q spiral inductors can still be used for low phase noise applications or for providing bias to the varactor(s).

The inductance of a bond wire is given by:

$$L = \frac{\mu_o \cdot l}{2\pi} \left( \ln\left(\frac{2l}{r}\right) - 0.75 \right)$$

Where  $r$  = radius of wire - typically 0.025mm (1mil)  
 $\mu_o = 4\pi \cdot 10^{-7}$  (permeability of free-space).

As we go higher in frequency the 'skin effect' becomes more important and increases the losses of the inductor:

$$R = \frac{l}{r \cdot 2\pi \cdot \delta \cdot \sigma} = \frac{1}{2r} \sqrt{\frac{f \cdot \mu_o}{\pi \cdot \sigma}}$$

Where  $\delta$  = skin depth in m,

$$\sigma = \text{Conductivity (S/m)} = 4.47 \times 10^7$$

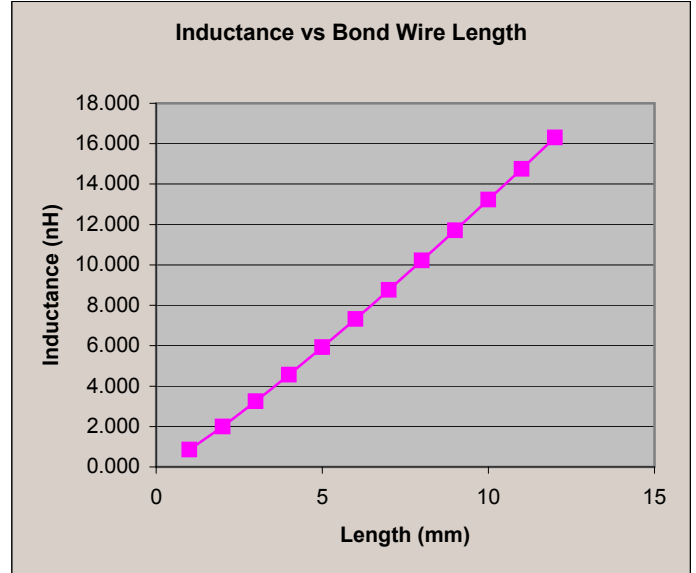
$$r = \text{radius of wire (m)}$$

$$l = \text{Length (m)}$$

We can now calculate the unloaded Q of the inductor thus:

$$Q = \frac{L \cdot \omega}{R} = 2r \left( \ln\left(\frac{2l}{r}\right) - 0.75 \right) \sqrt{\mu_o \cdot \rho \cdot \pi \cdot f}$$

The graph of **Figure 4** shows the inductance of a 1mil diameter gold bond wire for varying lengths.



**Figure 4 Bond wire inductance (nH) vs Bond wire length (mm) for a gold 1mil diameter bond wire.**

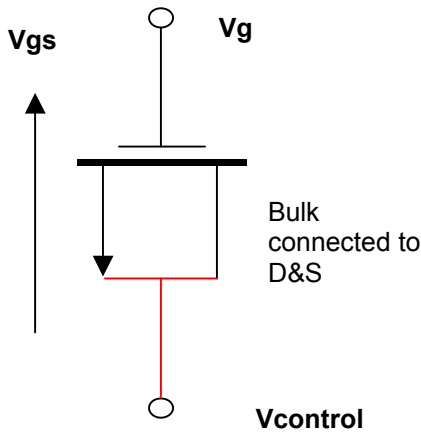
If for example we have a 2mm gold bond wire (of diameter 1mil) then we will have an inductance of **2nH**.

The associated Q of 2mm bond wire will be around **80** at a frequency of 2.5GHz a considerable improvement on an 'on-chip' inductor with a typical Q of between 3 & 5 at 2.5GHz. However, for our example we will assume an inductor Q of 5 can be realized 'on-chip'.

### 3.3 FREQUENCY CONTROL [3,4]

Using bond wires instead of on-chip inductors allows the design of low phase noise oscillators but makes the fabrication more difficult as it is difficult to precisely set the length of the bond wire. Also for use in Phase Locked Loop (PLL) applications it is necessary to have variable frequency. To make the fixed frequency oscillator into a variable frequency oscillator (VCO) we add/incorporate into the resonator an electronically controlled capacitor known as a varactor.

In MOS technology we can realise a varactor by connecting a FET as a diode and applying a reverse bias to it as shown in **Figure 5**.



**Figure 5 Implementation of a varactor by connecting together the source, drain and bulk of a MOS Fet (forming a diode) and applying a reverse bias across it.**

There are two common connections of the MOS fet as a diode:

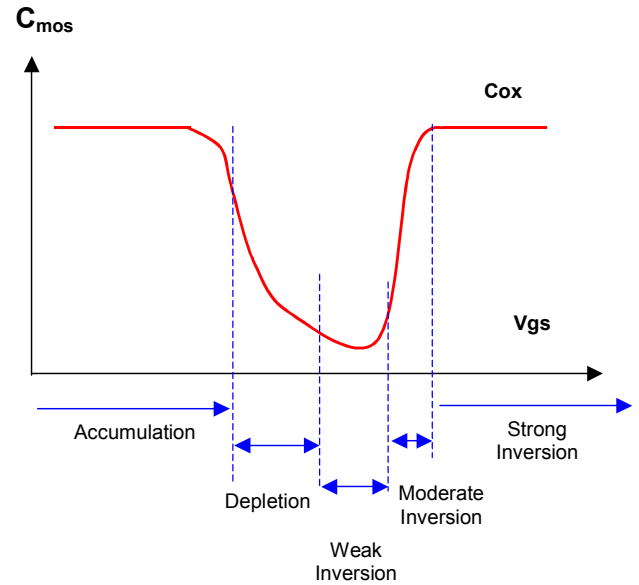
(1) B-S-D connected together, with voltage applied across the gate and B-S-D connection. If we plot capacitance vs ( $V_{\text{control}} - V_g = V_{gs}$ ) then we get the response shown in **Figure 6**. To simulate the varactor to determine the capacitance vs voltage characteristics, the ADS simulation of the varactor is shown in **Figure 12**.

The disadvantage of this varactor is that the control voltage needs to be kept below weak inversion in order to keep the capacitance reducing with increased control voltage.

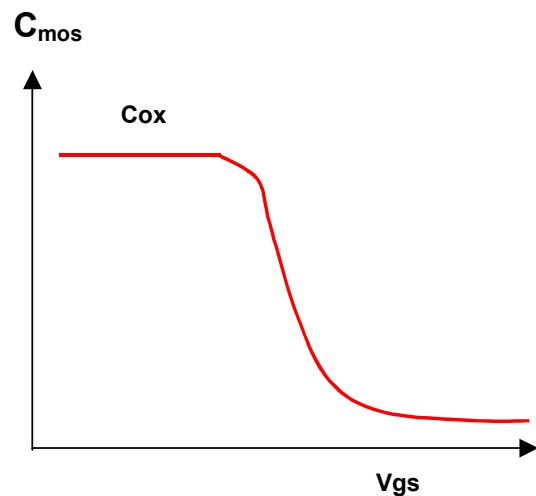
(2) In the second varactor, the voltage is applied across the gate and bulk only (S & D unconnected) – this is known as an **accumulation** varactor and produces the tuning characteristic shown in **Figure 7**.

The characteristic is more predictable in that the capacitance always falls with increasing control voltage.

**Note** however, a normal varactor's capacitance increases with increased reverse bias, therefore, it will be important to check the phasing of the PLL loop that the VCO is being used in, otherwise the Vco will go to an end stop and never lock up!!



**Figure 6 Capacitance variation of a P-mos capacitor with the bulk, source and drain connected together as per Figure 5. Voltage is applied across the gate and B-S-D connection.**



**Figure 7 Capacitance variation of a P-mos capacitor with voltage applied across the gate and Bulk connection (The source & drain are unconnected).**

### 3.4 VARACTOR DESIGN EQUATIONS [5]

For this design we will be using the ‘Accumulation’ mode varactor, where the source and drain terminals are unconnected and bias is applied across the gate and bulk only.

We first need to determine the maximum capacitance of the varactor shown as  $C_{ox}$  in **Figure 6** & **Figure 7**, followed by the minimum capacitance (that will allow the tuning bandwidth to be calculated) and the unloaded  $Q$ .

The value of  $C_{ox}$  or  $C_{MAX}$  is determined by the geometry of the varactor:

$$C_{ox} \text{ or } C_{MAX} = \frac{3.9 \cdot \epsilon_o \cdot W \cdot L}{T_{ox}} \cdot N$$

Where  $\epsilon_o = 8.84542 \times 10^{-12} \text{ F/m}$

$T_{ox} = 9.6 \times 10^{-9} \text{ m}$  (96 Å) (For HP CMOS 14TB process) &

$N$  = Number of gate fingers

The minimum value of the varactor is approximately given by:

$$C_{MIN} \cong C_{gdo} \cdot W$$

Where  $C_{gdo}$  = gate – drain capacitance

(=  $9 \times 10^{-11} \text{ F/m}$  For CMOS 14TB process)

To determine the maximum and minimum capacitance for a range of  $W/L$  ratio's it is easiest to use simulation. The ADS schematic of **Figure 12**, shows an S-parameter simulation, measuring  $Z_{in}$ . On the resulting simulation run the following equation has been used to determine the capacitance in pF.

$$C = 1E12 / (-2 \cdot \pi \cdot \text{Imag}(Z_{in}) \cdot \text{freq})$$

Using **Table 1** we can select a size of varactor that is going to resonate with the 2nH ‘on-chip’ spiral inductor at 2.5GHz with it's middle value capacitance using:

$$C = \frac{\left(\frac{1}{2 \cdot \pi \cdot f}\right)^2}{L} = \frac{\left(\frac{1}{2 \cdot \pi \cdot 2.5E9}\right)^2}{2E-9} = 2\text{pF}$$

Depending on the configuration two varactors are used end to end across a single inductor (see **Figure 13**) (And we need to use 2 times  $C$  resonating as capacitors in se-

ries!) or a varactor is connected to each of the two ‘load’ inductors (see **Figure 14**).

For this tutorial we will be simulating both design options.

W (um)	L (um)	Cmax (pF)	Cnom (pF)	Cmin (pF)
50	0.6	0.071	0.0775	0.013
100	0.6	0.141	0.0835	0.026
150	0.6	0.211	0.125	0.039
200	0.6	0.282	0.167	0.052
250	0.6	0.352	0.208	0.065
300	0.6	0.423	0.25	0.078
350	0.6	0.493	0.29	0.090
400	0.6	0.564	0.33	0.103
450	0.6	0.634	0.375	0.116
500	0.6	0.705	0.430	0.129
550	0.6	0.775	0.459	0.142
600	0.6	0.846	0.50	0.154
650	0.6	0.916	0.54	0.167
700	0.6	0.986	0.583	0.180
750	0.6	1.057	0.625	0.193
800	0.6	1.127	0.667	0.206
850	0.6	1.198	0.709	0.219
900	0.6	1.268	0.749	0.231
950	0.6	1.339	0.792	0.244
1000	0.6	1.409	0.833	0.257

**Table 1 Cmax & Cmin for an Accumulation varactor (Using the HP 14B process) with various W/L ratios. Note that we can increase the capacitance by increasing the number of gate fingers in parallel. So to give us a varactor with a nominal capacitance of 4pF (ie two capacitors in parallel to give 2pF) we could use a gate width of 500um with 10 fingers = 4.3pF.**

Note that the parasitic capacitances of the 1/gm devices will increase the minimum capacitance of the varactor reducing the tuning range. This can only be evaluated once the 1/gm device sizes are known.

The simulation of a P-type accumulation varactor (Where the voltage is applied across the gate and bulk only (S & D unconnected) with the dimensions of  $W=600$ ,  $L=0.6$  and  $N=5$ , is shown in **Figure 8** with the resulting capacitance (pF) vs control voltage characteristic shown in **Figure 9**.

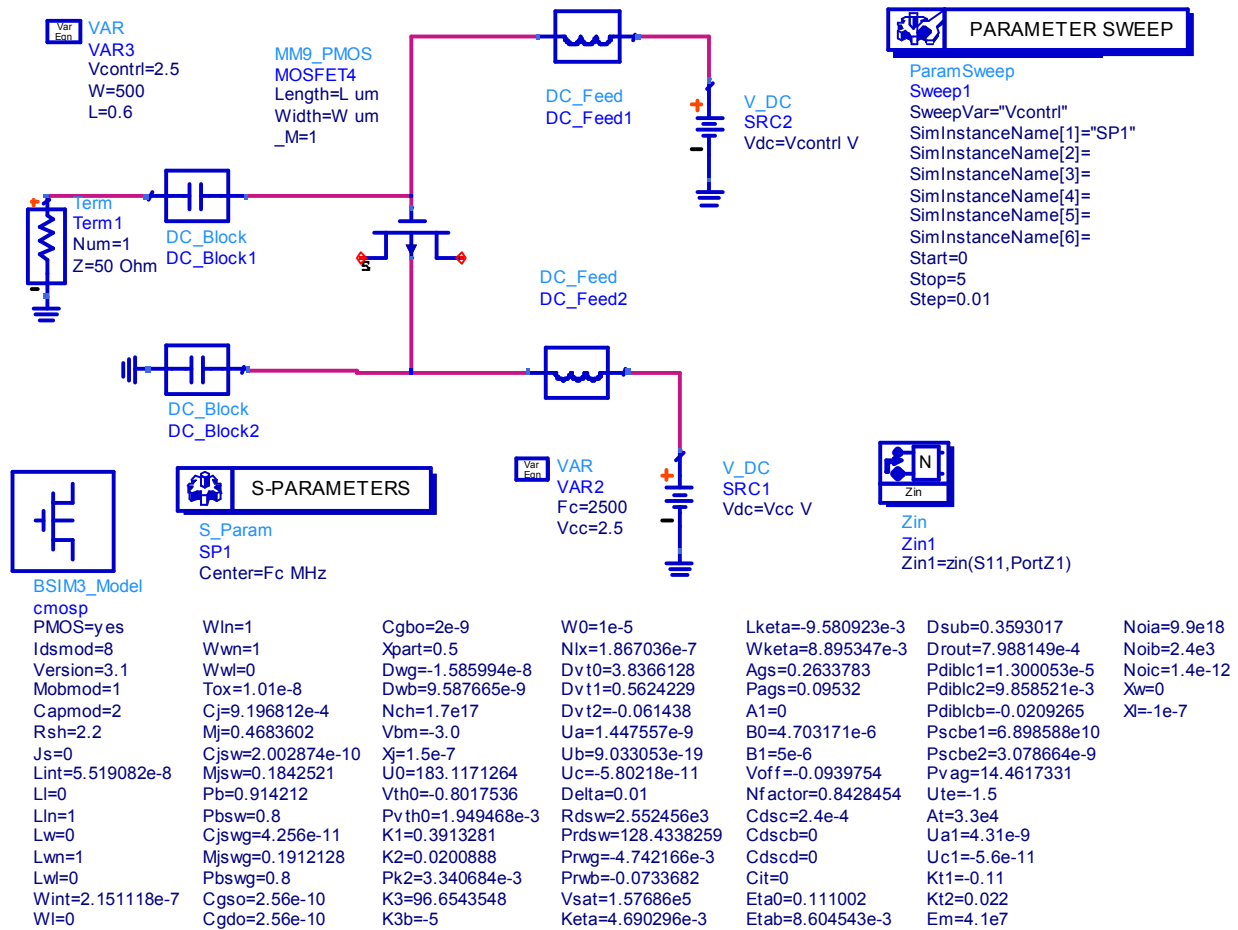


Figure 8 ADS simulation to determine the variation in capacitance of a P-type Accumulation varactor diode (Where the voltage is applied across the gate and bulk only (S & D unconnected) with the dimensions of W=600, L=0.6 and N=5. The input impedance is measured by adding the Zin parameter box, to allow calculation of the capacitance at 2.5GHz. The resulting plot of results is shown in Figure 10.

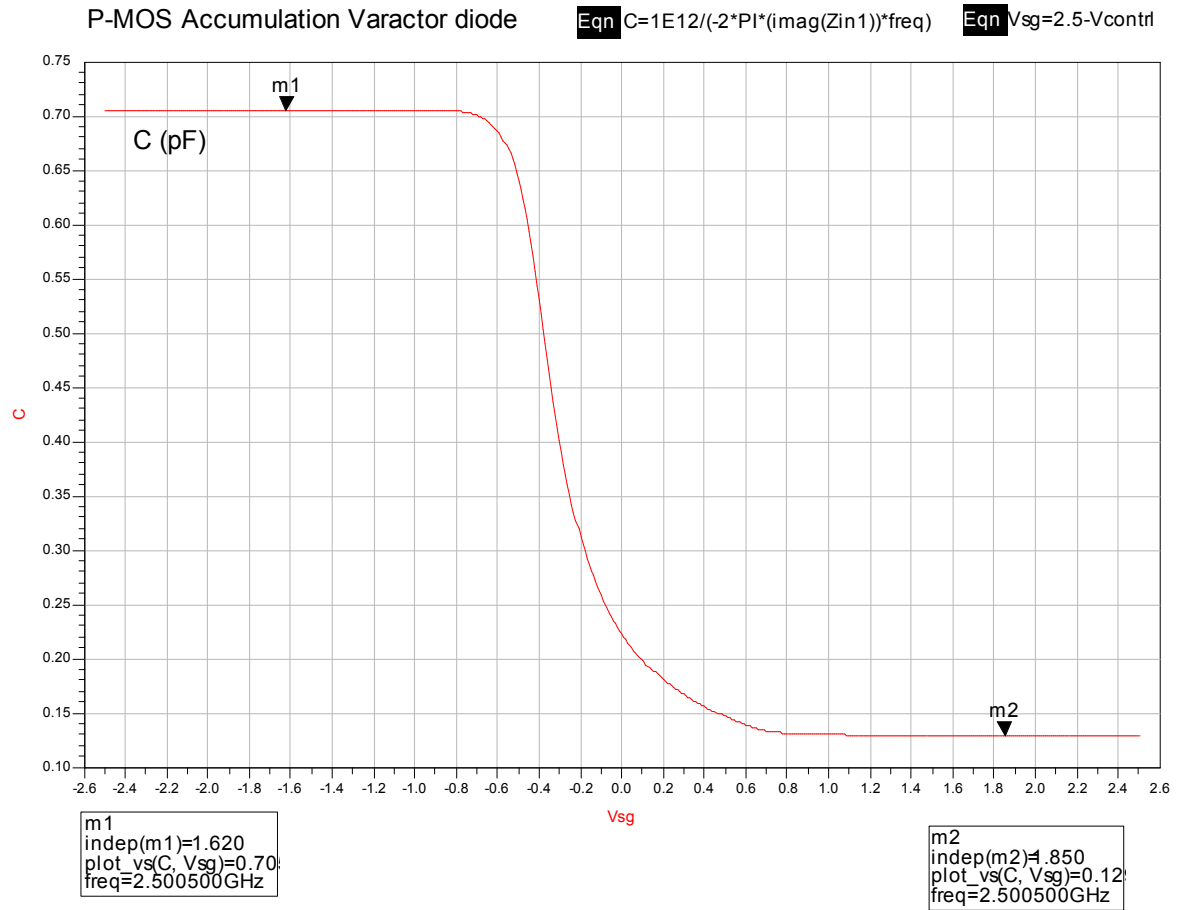


Figure 9 Resulting simulation plot of the ADS schematic (P-type Accumulation type varactor diode) shown in Figure 8. The equation C converts the imaginary input impedance ( $Z_{in}$ ) to capacitance pF





Finally, we need to calculate the unloaded Q of the varactor by using the following approximate expression:

$$Q_{\text{mos}} = \frac{12}{\omega \cdot C'_{\text{ox}} \cdot W \cdot L} \cdot K_p \cdot \frac{W}{L} (V_{\text{gs}} - |V_{\text{T}}|)$$

$$Q_{\text{mos}} = \frac{12 \cdot K_p \cdot (V_{\text{gs}} - |V_{\text{T}}|)}{\omega \cdot C'_{\text{ox}} \cdot L^2}$$

$K_p$  = gain factor given by :

$$K_p = \text{MUZ} \cdot C'_{\text{ox}}$$

$$\text{MUZ} = \text{Zero bulk mobility} = 1.36 \text{E}^2 \text{ cm}^2 / \text{Vs} \\ (\text{For CMOS14TB process})$$

$$\text{convert to m}^2 / \text{Vs} = 136 \cdot (1\text{E}^{-2} \cdot 1\text{E}^{-2}) = 13.6 \text{E}^{-3} \text{ m}^2 / \text{Vs}$$

$$C'_{\text{ox}} \text{ or } = \frac{3.9 \cdot \epsilon_0}{T_{\text{ox}}} =$$

$$C'_{\text{ox}} = \frac{3.9 \times 8.84542 \times 10^{-12}}{9.6 \text{E}^{-9}} = 3.59 \text{E}^{-3} \text{ F/m}^2$$

$$\text{Where } \epsilon_0 = 8.84542 \times 10^{-12} \text{ F/m}$$

$$T_{\text{ox}} = 9.6 \text{E}^{-9} \text{ m (96 \AA)} \text{ (For HP CMOS 14TB process)}$$

$$K_p = 13.6 \text{E}^{-3} \cdot 3.59 \text{E}^{-3} = 48 \text{uA/V}^2$$

$$\text{If we assume that } (V_{\text{gs}} - |V_{\text{T}}|) = \frac{V_{\text{dd}}}{2} = 1.25 \text{V}$$

then  $Q_{\text{mos}} =$

$$\frac{12 \cdot 48 \text{E}^{-6} \cdot (1.25)}{2\pi \cdot 2.5 \text{E}^9 \cdot 3.59 \text{E}^{-3} \cdot (0.6 \text{E}^{-6})^2} \approx 35$$

**Note: To maximize the Q of the varactor we need to keep L as short as possible!**

### 3.5 RESONATOR Q & BANDWIDTH

The overall unloaded Q of the resonator will depend on the loaded Q's of the inductor and varactor. However, if we minimize the varactor gate length and use on chip inductors the overall Q will be dominated by the Q of the inductor:

$$\frac{1}{Q_{\text{res}}} = \frac{1}{Q_{\text{IND}}} + \frac{1}{Q_{\text{varactor}}}$$

$$\frac{1}{Q_{\text{res}}} = \frac{1}{5} + \frac{1}{35} \approx 4.4$$

The ADS schematic of Figure 11 simulates the loaded Q of the resonator (ie P-type varactor diode and on-chip inductor). The resulting simulation plot with loaded Q calculation is shown in Figure 10, showing a similar loaded Q to the hand calculation.

For this initial design the varactor is connected directly across the inductor giving the largest tuning range. This however, may not always be required, as the  $k_o$  (MHz/V) will be very large.  $k_o$  is one of the variables in PLL loop calculations and will give a large open loop gain, which may be undesirable and prove difficult to stabilize the loop. In addition, with such a sensitive VCO comes the problem of noise on the varactor control line will modulating on the VCO RF output.

An additional design will be given in this tutorial that shows how the tuning bandwidth can be reduced, so lowering  $k_o$ .

### 3.6 AMPLIFIER GM CALCULATION

In order to determine the minimum cross-coupled amplifier negative GM we need to find the loss of the resonator. For this we take the inductance and calculate  $R_{\text{eq}}$ :

$$R_{\text{eq}} = Q \cdot 2\pi \cdot f_o \cdot L \text{ and for our example}$$

$$R_{\text{eq}} = 4.4 \cdot 2\pi \cdot 2.5 \text{E}^9 \cdot 2 \text{E}^{-9} = 138 \Omega$$

Therefore, the minimum Gm required for oscillation is:

$$GM > \frac{1}{R_{\text{eq}}} \Rightarrow GM > 7 \text{mS}$$

Where  $GM = GM_N + GM_P$  - for compliment ary VCO

To give us some margin make  $GM = 10 \text{mS}$ .

The start - up margin will now be 1.43 ie (10/7)

$$\text{Where } GM = \sqrt{2 \cdot K_{(n \text{ or } p)} \left( \frac{W}{L} \right) I_D}$$

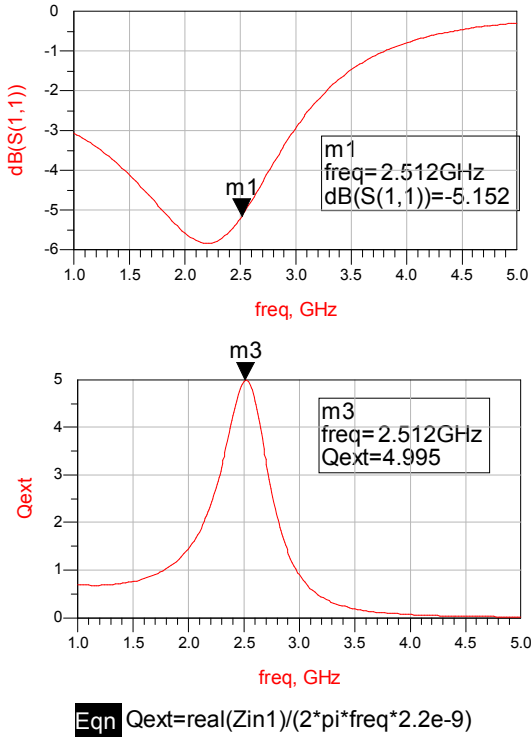
Thus we can re-arrange to give the minimum W/L ratio required to give oscillator:

$$\frac{W}{L} = \frac{gm^2}{2 \cdot K \cdot I_D}$$



We would obviously increase this ratio to give us margin allowing for lower Q in the resonator (reducing Req) and so ensure reliable startup and operation over temperature.

To calculate the gate widths we first have to decide on a drain current, for this example set  $I_D$  to 5mA.



**Figure 10** Frequency response of the resonator circuit shown in Figure 11. The equation has been added to determine the loaded Q of the circuit resulting in a loaded Q of 4.99 compared to the hand calculation value of 4.44.

### 3.6.1 N devices:

$$K_p = \mu_{Zn} \cdot C'_{ox}; \mu_{Zn} = 471 \text{ cm}^2/\text{V.s}$$

$$\text{convert to } \text{m}^2 = 471(10^{-2} \cdot 10^{-2}) = 471 \cdot 10^{-4} \text{ m}^2$$

$$C_{ox} = \frac{3.97 \cdot \epsilon_0}{T_{ox}} = \frac{3.97 \times 8.85 \cdot 10^{-12}}{9.6 \cdot 10^{-9}} = 3.645 \cdot 10^{-3} \text{ F/m}^2$$

$$K_p = \mu_{Zn} \cdot C_{ox} = 471 \cdot 10^{-4} \cdot 3.645 \cdot 10^{-3} = 171.7 \cdot 10^{-6} \text{ A/V.s}$$

$$\frac{W}{L} = \frac{(10 \cdot 10^{-3})^2}{2.171 \cdot 10^{-6} \cdot 5 \cdot 10^{-3}} = 58 \therefore W = 35$$

### 3.6.2 P devices:

$$K_p = \mu_{Zn} \cdot C'_{ox}; \mu_{Zn} = 136 \text{ cm}^2/\text{V.s}$$

$$C_{ox} = \frac{3.97 \cdot \epsilon_0}{T_{ox}} = \frac{3.97 \times 8.85 \cdot 10^{-12}}{9.6 \cdot 10^{-9}} = 3.645 \cdot 10^{-3} \text{ F/m}^2$$

$$K_p = \mu_{Zn} \cdot C_{ox} = 136 \cdot 10^{-4} \cdot 3.645 \cdot 10^{-3} = 49 \cdot 10^{-6} \text{ A/V.s}$$

$$\frac{W}{L} = \frac{(105 \cdot 10^{-3})^2}{2.49 \cdot 10^{-6} \cdot 5 \cdot 10^{-3}} = 200 \therefore W = 120$$

Estimation of phase noise performance

$$L(\Delta\omega) = \frac{k \cdot T \cdot R_{eff} \cdot [1 + A] \left( \frac{\omega_o}{\Delta\omega} \right)^2}{\frac{V_A^2}{2}}$$

Where

A = Startup safety factor

$$= \frac{\text{Equivalent parallel resistance of resonator}}{\text{Negative resistance of oscillator}}$$

$V_A$  = Peak voltage amplitude across resonator.

$R_{eff}$  = Effective equivalent series resistance of the resonator.

$\Delta\omega$  = Radial Frequency offset from carrier

From our example  $A \sim 138 / (1/10 \cdot 10^{-3}) = 1.38$ .

$$R_{eff} = \frac{2\pi \cdot f_o \cdot L}{Q_{res}} = \frac{2\pi \cdot 2.5 \cdot 10^9 \cdot 2 \cdot 10^{-9}}{4.4} = 7.15 \Omega$$

$$L(\Delta\omega) = \frac{k \cdot T \cdot R_{eff} \cdot [1 + A] \left( \frac{\omega_o}{\Delta\omega} \right)^2}{\frac{V_A^2}{2}}$$

$$\frac{(1.38 \cdot 10^{-23}) \cdot 293 \cdot (7.15) [1 + 1.38] \left( \frac{2.5 \cdot 10^9}{10 \cdot 10^3} \right)^2}{\frac{2.5}{2}} = 3.44 \cdot 10^{-9}$$

To get in dB =  $10 \log(3.44 \cdot 10^{-9})$

$$= -84.6 \text{ dBc/Hz}$$

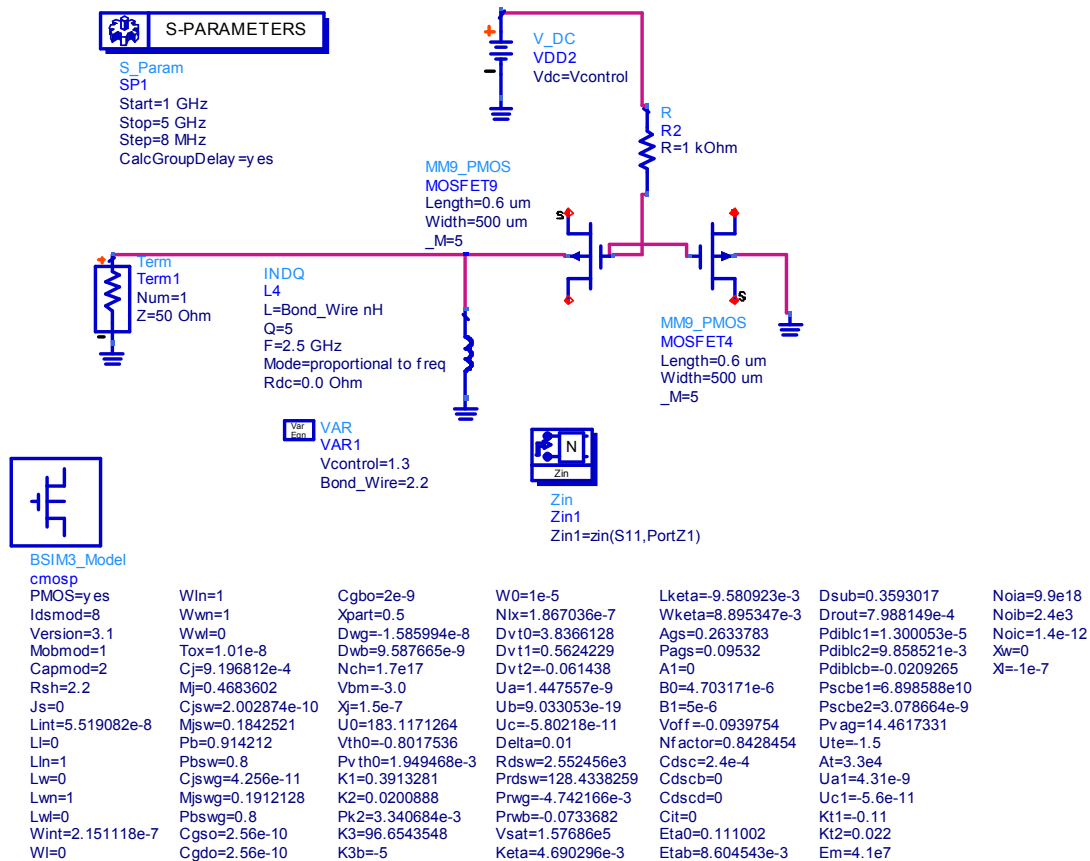
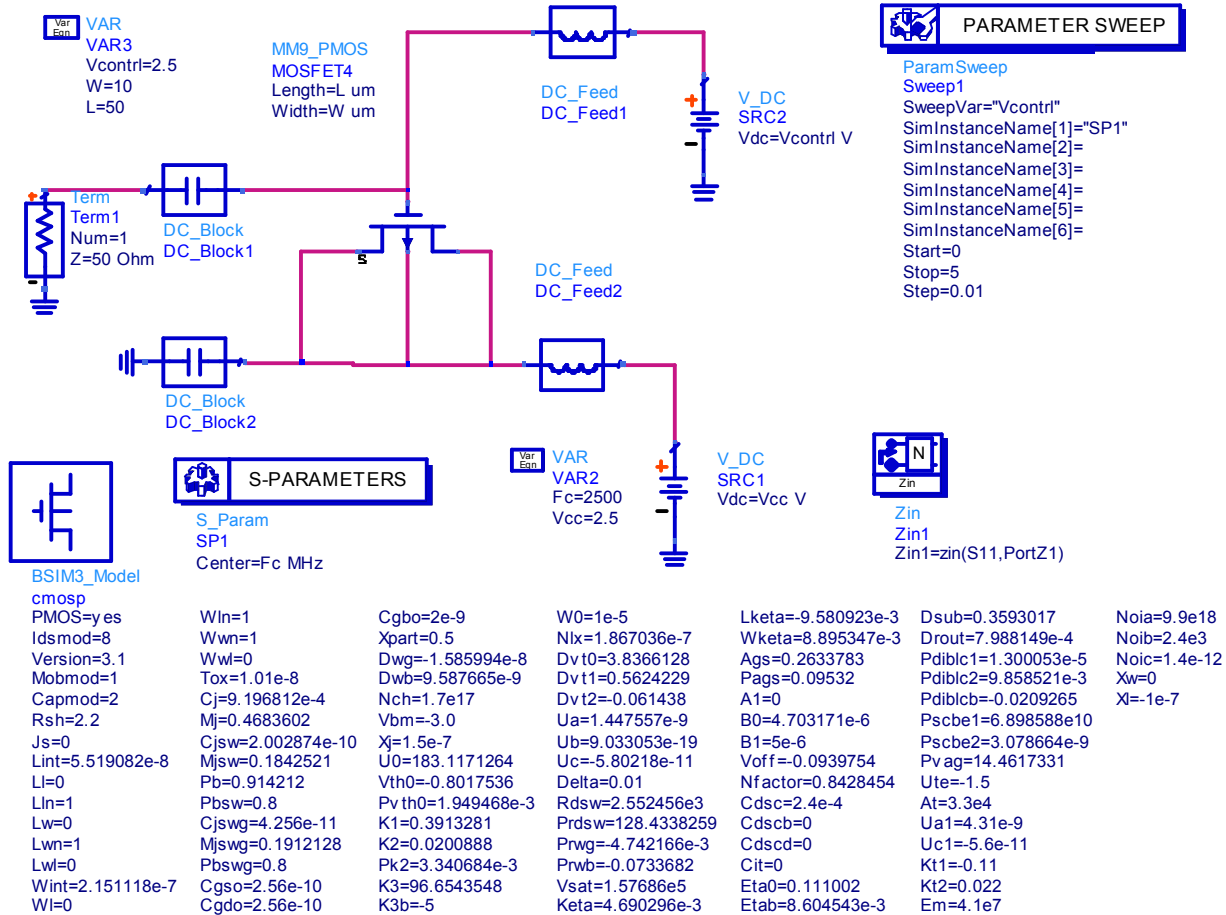
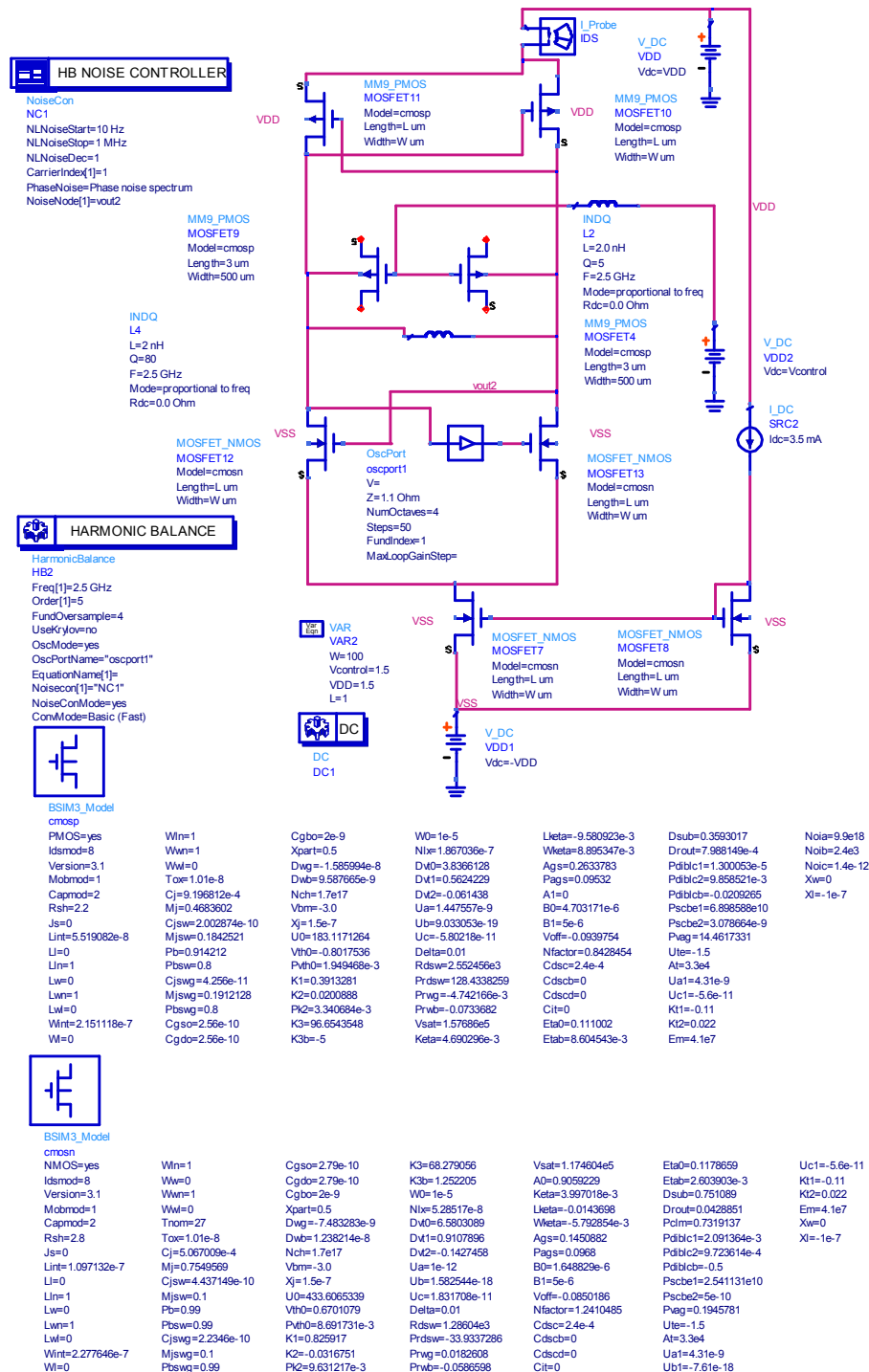


Figure 11 ADS simulation to determine the loaded Q of the resonator circuit. The input impedance is measured by adding the Zin parameter box. The resulting plot of results is shown in Figure 10.



**Figure 12** ADS simulation for determining the tuning characteristics of a P-type MOS varactor. In this simulation the bulk, source and drain are connected together to produce the response predicted in Figure 6. The S-parameter simulation contains a Zin block and we use the imaginary term of this to determine the capacitance of the varactor while sweeping the applied gate-source voltage (Vcontrl).



**Figure 13 ADS simulation of the basic L-C oscillator ‘option 1’ using harmonic balance. The ‘OscPort’ is used by the harmonic balance simulator, to inject a signal into the circuit to determine the frequency of operation etc. The fundamental oscillating frequency is entered into the harmonic balance simulator and ‘Oscmode’ is checked.**

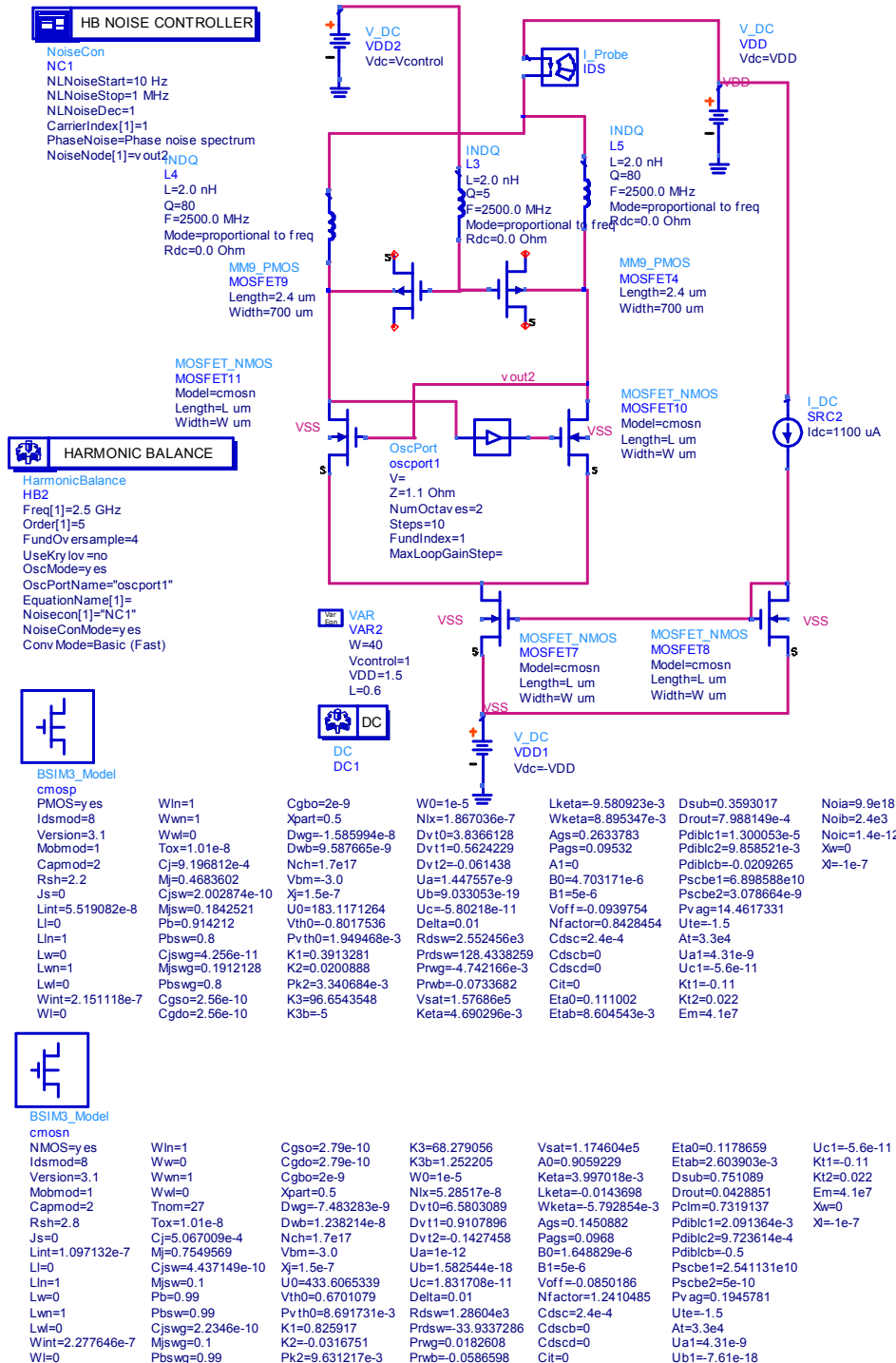


Figure 14 ADS simulation of the basic L-C oscillator ‘option 1’ using harmonic balance. The ‘OscPort’ is used by the harmonic balance simulator, to inject a signal into the circuit to determine the frequency of operation etc. The fundamental oscillating frequency is entered into the harmonic balance simulator and ‘Oscmode’ is checked.

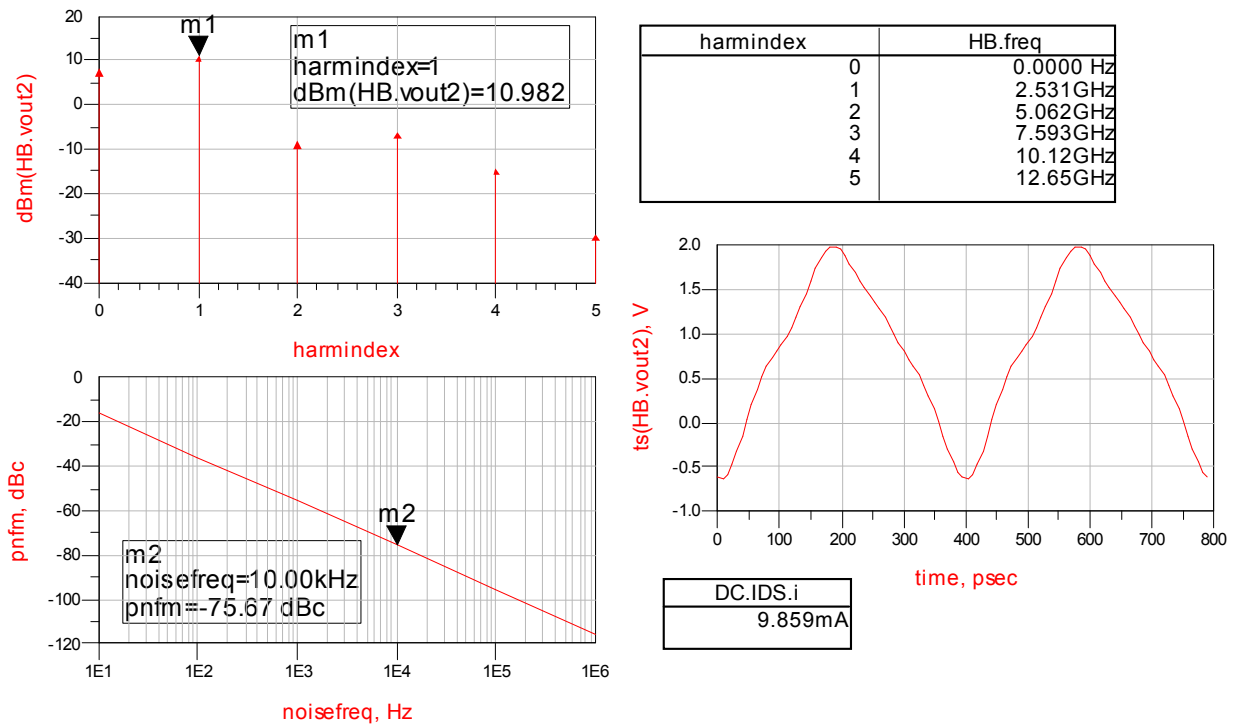


Figure 15 Resulting plots from the ADS simulation shown in Figure 13. Here the control voltage has been set to center the VCO on ~2.5GHz.

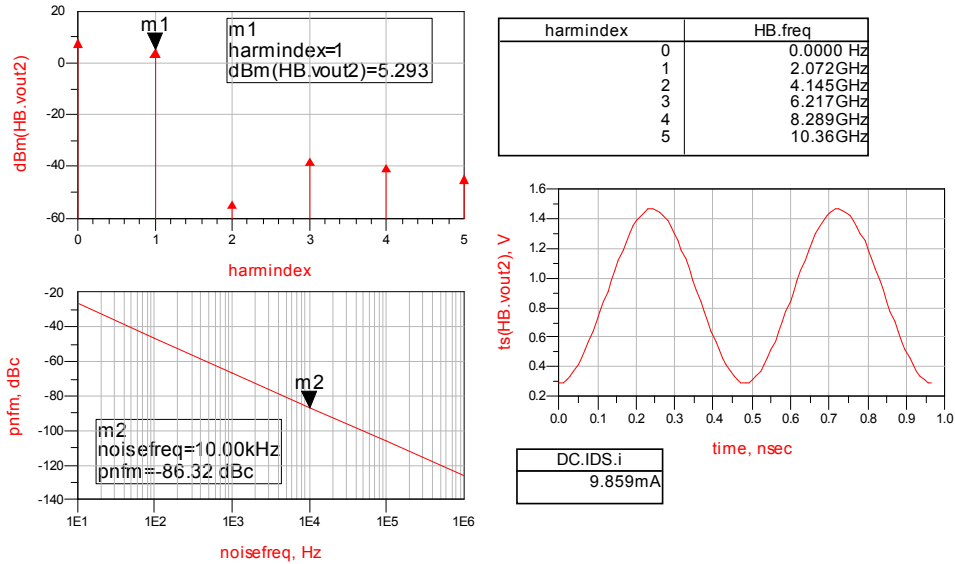


Figure 16 Resulting plots from the ADS simulation shown in Figure 13. Here the control voltage has been set to 2.5V giving a resulting oscillating frequency of ~2.07GHz.

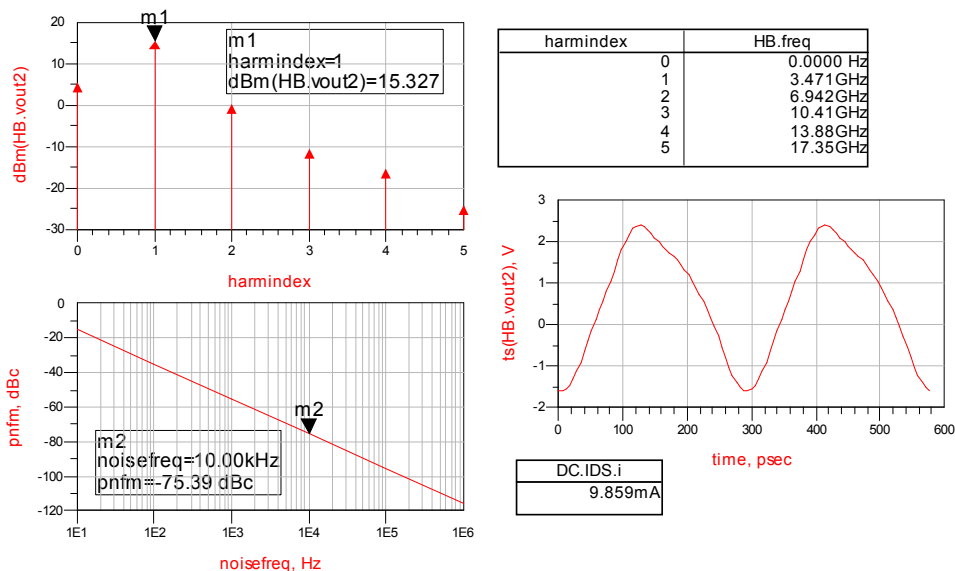


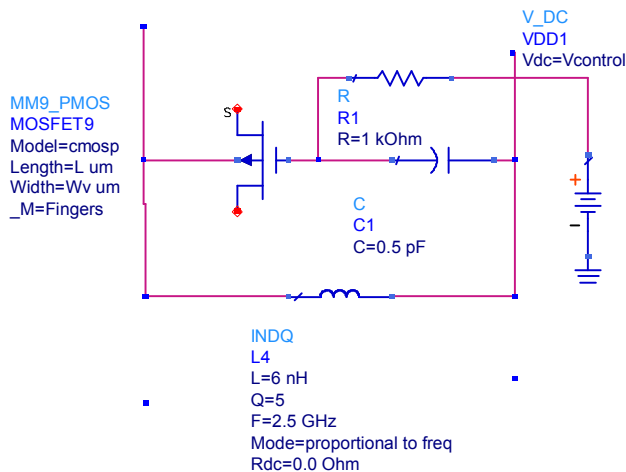
Figure 17 Resulting plots from the ADS simulation shown in Figure 13. Here the control voltage has been set to 0V giving a resulting oscillating frequency of ~3.47GHz.



### 3.7 REDUCING TUNING BANDWIDTH

The previous VCO was designed for maximum bandwidth, by directly connecting the varactor to the inductor. If we wish to have a VCO operating over a narrower bandwidth then we need to swap one of the varactors with a small value capacitor, such that the varactor capacitance swing is less dominant. The circuit arrangement for the resonator is shown in Figure 18. The easiest way to determine the value of the coupling capacitor is to generate a spreadsheet and enter values of Varactor coupling capacitor as shown in

Table 2 Prediction of VCO tuning bandwidth with the addition of a coupling capacitor  $C_c$  in series with a single MOS varactor. In order to achieve a % bandwidth of ~ 10% , the required value of  $C_c$  is 0.5pF (This will also give us some margin). Note the addition of the resonator coupling capacitor  $C_c$  will alter these values slightly and some adjustments may need to be made to the resonator to adjust the center frequency back to 2.5GHz.



**Figure 18** Circuit segment of the L-C Vco showing the modified resonator section. One of the varactors has been replaced with a small value capacitor to ‘dampen’ the varactor capacitance swing and thus reducing the VCO tuning bandwidth. Values for the varactor are  $_M=5$ ,  $W_v=500$  &  $L=0.6$  giving a predicted capacitance variation of 1.279pF to 4.613pF.

If we re-adjust  $L$  to be 5.5nH and  $C_c$  set to 0.6pF the new maximum and minimum VCO frequencies will be 2401MHz and 2657MHz. This will give a center frequency of 2529MHz and a % tuning bandwidth of 10.2%. This value may well need to be increased to allow for temperature effects etc.

Cc pF	Varactor Network		Min Freq (MHz)	Max Freq (MHz)	Tuning Range	
	Max C	Min C			(MHz/V)	(%)
0.1	0.09787821	0.092748	4644	4771	50.68	2.69
0.15	0.14527609	0.134255	3812	3965	61.35	3.94
0.2	0.19168918	0.172955	3318	3494	70.04	5.14
0.25	0.23714785	0.209124	2983	3177	77.45	6.29
0.3	0.28168125	0.243002	2737	2947	83.93	7.38
0.35	0.32531735	0.2748	2547	2772	89.70	8.43
0.4	0.36808298	0.304705	2395	2632	94.92	9.44
0.45	0.41000395	0.33288	2269	2518	99.67	10.41
<b>0.5</b>	<b>0.45110503</b>	<b>0.359472</b>	<b>2163</b>	<b>2423</b>	<b>104.03</b>	<b>11.34</b>
0.55	0.49141003	0.384609	2073	2343	108.06	12.24
0.6	0.53094188	0.408409	1994	2273	111.81	13.10
0.65	0.56972259	0.430975	1925	2213	115.30	13.93
0.7	0.60777339	0.4524	1864	2160	118.58	14.73
0.75	0.64511467	0.47277	1809	2113	121.66	15.51
0.8	0.68176612	0.49216	1760	2071	124.56	16.26
0.95	0.78776739	0.54511	1637	1968	132.36	18.36
0.9	0.75307455	0.52827	1674	1999	129.89	17.68
0.95	0.78776739	0.54511	1637	1968	132.36	18.36
1	0.82184215	0.561211	1603	1939	134.70	19.01

**Table 2** Prediction of VCO tuning bandwidth with the addition of a coupling capacitor  $C_c$  in series with a single MOS varactor. In order to achieve a % bandwidth of ~ 10% , the required value of  $C_c$  is 0.5pF

The plots of the narrow bandwidth Vco with Vcontrol set to 0V and 2.5V are shown in Figure 19 & Figure 20

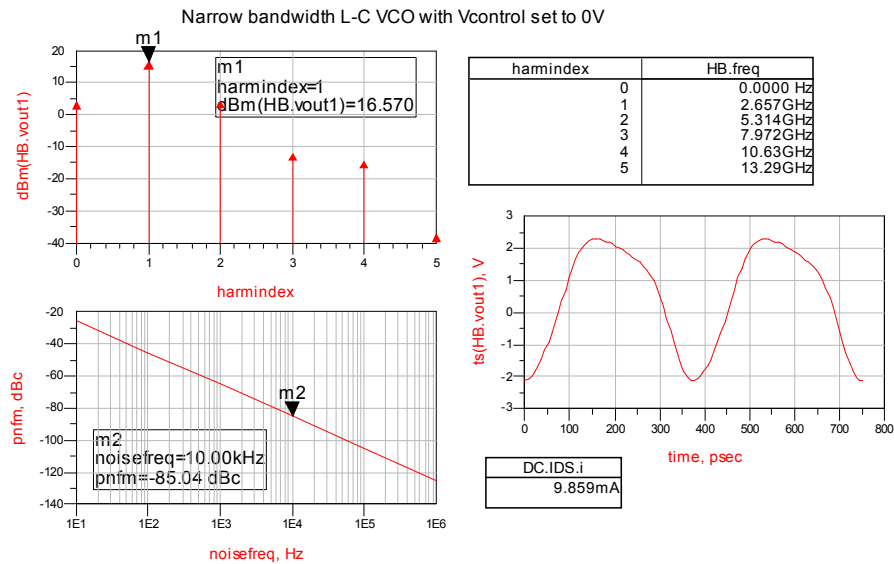


Figure 19 Prediction of the narrow band L-C VCO performance at a Vcontrol set to 0V.

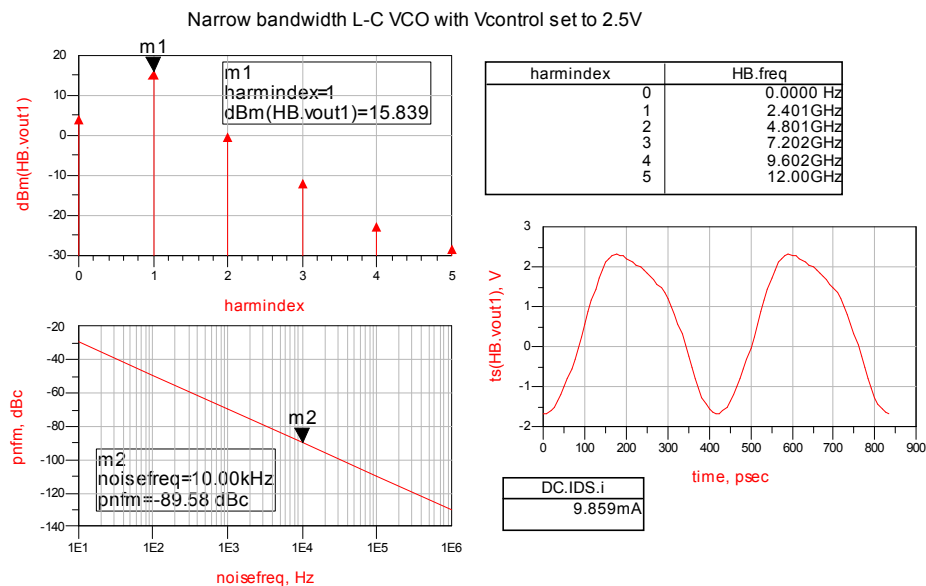


Figure 20 Prediction of the narrow band L-C VCO performance at a Vcontrol set to 2.5V.

#### 4 CONCLUSION

This tutorial described the small signal operation of a L-C oscillator. The relevant design theory was given together with several worked examples, both fixed frequency and voltage controlled versions.

Harmonic balance ADS simulations were given to simulate the circuits, using the hand calculations derived in the examples to predict, output frequency (and harmonics), output power and phase noise performance.

It was shown that in order to achieve good phase noise performance the use of low Q 'on-chip' inductors was to be avoided, opting instead for high Q bond-wire inductors – off-chip.

The first VCO was designed for maximum tuning range by connecting a pair of varactors directly across the inductor. The resulting tuning bandwidth was 55% (ie 2.07 to 3.47GHz), centred on 2.5GHz.

The step by step design of this Vco showed how to design the resonator and calculate it's loaded Q (and hence determine the VCO phase noise) and it's RF loss. With the knowledge of the loss of the resonator, the gm's of the reflection amplifier devices could be determined to ensure reliable oscillation (with some margin).

The predicted performance of the wide-band oscillator is shown in Table 3.

Parameter	Predicted Result	Units
Frequency band-width	2.07 – 3.47	GHz
Phase Noise	> 75	dBc/Hz @ 10KHz
Tuning Bandwidth	55	%
O/P Power	>5	dBm
Power Consumption	~ 100	mW
2 <sup>nd</sup> Harmonic	>10	dBc
Ko	~500	MHz/V

**Table 3 Predicted performance of the wide-band L-C VCO.**

The second VCO example was designed to have a greatly reduced bandwidth (~10%), thus lowering Ko to around 100MHz/V, giving a tuning range of 2.401GHz to 2.667GHz centred on 2.532GHz.

The predicted performance of the narrow-band oscillator is shown in Table 4. In both cases the harmonic content is quite high and so a buffer stage with a tuned output

will be required to improve this to a more acceptable 20dc or so.

Parameter	Predicted Result	Units
Frequency band-width	2.401 – 2.667	GHz
Phase Noise	> 83	dBc/Hz @ 10KHz
Tuning Bandwidth	10.5	%
O/P Power	>15	dBm
Power Consumption	~ 100	mW
2 <sup>nd</sup> Harmonic	>10	dBc
Ko	~100	MHz/V

**Table 4 Predicted performance of the narrow-band L-C VCO.**

#### 5 REFERENCES

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