 Analog Integrated Circuits and Signal Processing, 25, 309–318, 2000

Layout Dependent Matching Analysis of CMOS Circuits

KENICHI OKADA (NONMEMBER), HIDETOSHI ONODERA, AND KEIKICHI TAMARU (MEMBERS)

Department of Communications and Computer Engineering, Kyoto University, Kyoto-shi, 606–8501 Japan

Received June 30, 1998; Revised September 3, 1998

Abstract. Layout has strong influence on matching properties of a circuit. Current matching models, which characterize both local random non-uniformities and global systematic non-uniformities stochastically, are not adequate for the matching analysis taking the effect of layout realization into account. In order to consider topological information of layout into matching analysis, we propose a matching model which treats the random and systematic components separately. Also, we characterize the micro-loading effect, which modulates fabricated line-width according to the local density of layout patterns, into matching analysis. With these two techniques, we can perform matching analysis of CMOS circuits taking layout information into account.

Key Words: CMOS, matching, micro-loading-effect, fluctuation

1. Introduction

The minimum feature size of MOSFETs is continuously reducing due to the steady improvement of fabrication technologies. It has contributed to the remarkable growth of integration scale and the increase in operating speed. On the other hand, it casts many design challenges. One of serious challenges is the increased effect of process variation (non-uniformities) on circuit performances.

It is known that electrical properties of identically designed transistors have a certain amount of differences due to the non-uniformities of fabrication process and operating environment such as operating temperature [1]. With the decrease of transistor sizes, matching properties of a pair of devices become degrading [2]. In many analog signal processing circuits, the accuracy of their functions relies on the matching properties of certain devices. It is therefore important to design layout for better matching performances because layout has strong influence on matching [3]. Also, it is important to develop a method for matching analysis that can predict matching properties quantitatively based on the layout information of the devices under consideration. The purpose of this paper is to present such an method for matching analysis of MOSFET circuits.

For matching analysis, several mismatch models of MOSFETs have been proposed [1,3]. Among them, Pelgrom model is most widely accepted [2]. The model characterizes two sources of process non-uniformities: local random fluctuation and global systematic fluctuation. The global fluctuation is modeled as a stochastic process with a long correlation distance. This model works well for the matching analysis of a pair of transistors. It, however, is not adequate for the matching analysis of a circuit with dedicated layout that is designed for canceling out the deterministic fluctuation. We show a mismatch model which characterizes the local fluctuation as a random process according to the Pelgrom model but treats the deterministic fluctuation as such.

Another important source of mismatch is a deterministic deviation of fabricated (actual) line-width from designed width due to the micro-loading effect [4]. The amount of the deviation depends on the local density of layout patterns. The width of a tightly spaced line after fabrication is different from that of loosely spaced line with the same designed width. The channel length of a MOSFET has a dominant effect on its electrical property and hence the micro-loading effect should be taken into account in the mismatch analysis. In this paper we propose a

Copyright, 1999, IEICE, reprinted with permission from IEICE Transaction.

model of the micro-loading effect for poly-gate line-width. A method for model-parameter extraction is also presented.

With the micro-loading model and the mismatch model, we can perform mismatch analysis of a MOSFET circuit considering its layout realization. We show two methods for the application of our models. The first one is a Monte Carlo mismatch analysis which is applicable to a circuit in general with layout. The second one is a mismatch-model building for a circuit with specific layout such as the common-centroid [5]. Simulation examples with those two methods are explained.

This paper is organized as follows. Section 2 explains our mismatch model of MOSFETs and a model for the micro-loading effect on poly-silicon line-width. Section 3 discusses the parameter-extraction method for the micro-loading effect and experimental results. Section 4 shows two methods for the application of our models. Section 5 reports the simulation examples with those two methods. Finally, Section 6 concludes our discussion.

2. Characterization of Process Non-uniformities

MOSFET characteristics vary due to process non-uniformities. In this section we explain two models that are necessary for the mismatch analysis considering layout realization. They are a mismatch model of MOSFETs which can consider local random fluctuation and global systematic fluctuation of MOSFET's characteristics, and a model for deterministic variation of a line-width due to the micro-loading effect [4].

2.1. Characterization of MOS Transistors

Two identically designed MOSFETs have a certain level of differences in their electrical behaviors. Those differences are expressed as the mismatch in the parameters which represent their electrical behavior. The mismatch arises from two sources of process non-uniformity: random local variation and global systematic variation [5]. The first component is a white noise caused by a stochastic nature of fabrication processes. The second component represents a systematic parameter-value distribution over chip surface which is caused by, for example, non-uniform thermal distribution during fabrication processes. Another example of the second component is a non-uniform temperature distribution created by hot spots during circuit operation.

Pelgrom proposed a mismatch model for a pair of transistors [2]. The model characterizes both sources of mismatch as the random variation of the difference in the parameter values which model MOSFET behavior:

$$\sigma^2(\Delta P) = \frac{A_\Delta^2 P}{WL} + S_{\Delta P}^2 D_x^2 \tag{1}$$

Parameter ΔP represents the difference in parameter P, W and L are the gate-width and gate-length of the transistors spaced by distance D. Parameters $A_{\Delta P}^2$ and $S_{\Delta P}^2$ are process-dependent constant. The first term represents the local random variation, and the second term represents the systematic global variation which is modeled as an additional stochastic process with a long correlation distance.

This model is widely used for recent studies on the matching analysis [2,3,5–7] and works well for the analysis of a pair of transistors. However, if we want to perform matching analysis for a circuit with more than three transistors, we need to consider the correlation of mismatch behavior among transistors caused by the systematic variation. This means that the systematic component, in this case, should not be treated as a stochastic process. We therefore treat two components separately. The random local variation is expressed as the Pelgrom model. Each parameter varies around a mean value randomly with a normal distribution. The mean value, on the other hand, changes its value according to the position of the transistor deterministically.

We characterize the random variation of the threshold voltage V_{T0}, the gain factor $K_P(=\mu C_{ox})$, the deviation of the gate-width ΔW and the deviation of the gate-length ΔL of the ith transistor as follows:

$$\sigma_i^2(V_{T0}) = \frac{A_{V_{T0}}^2}{W_i L_i} \tag{2}$$

$$\sigma_i^2(K_P) = \frac{A_{KP}^2}{W_i L_i} \tag{3}$$

$$\sigma_i^2(\Delta W) = \frac{A_{\Delta W}^2}{W_i^2 L_i} \tag{4}$$

$$\sigma_i^2(\Delta L) = \frac{A_{\Delta L}^2}{W_i L_i^2} \tag{5}$$

Parameters $A_{V_{T0}}$, A_{K_P}, $A_{\Delta W}$, and $A_{\Delta L}$ are process-dependent constant. This model indicates that the decrease in a transistor size leads to the increase in the standard deviation which results in the degradation of matching characteristics. Fig. 1 explains this feature. The horizontal axis and the vertical axis represent the transistor area WL and the threshold voltage of the transistor respectively. The center line corresponds to the mean value which varies according to the systematic mismatch model described next.

In order to evaluate the effect of systematic variation precisely, we treat the systematic mismatch separately from the local random mismatch. The systematic mismatch is resulted from a global non-uniformity of process or operation condition. It causes the deterministic variation of the mean value of each parameter. The variation over a chip surface is expected to be small, so we assume linear relationship of the mean value with respect to the position of the transistor. The mean values of the threshold voltage, the gain factor, the gate-width variation and the gate-length variation ($\overline{V_{T0_i}}$, $\overline{K_{P_i}}$, $\overline{\Delta W_i}$, $\overline{\Delta L_i}$, respectively) of the ith transistor located at (x_i, y_i) are expressed as follows:

$$\overline{V_{T0_i}} = \overline{V_{T0}} + G^{(x)}_{V_{T0}} x_i + G^{(y)}_{V_{T0}} y_i \tag{6}$$

$$\overline{K_{P_i}} = \overline{K_P} + G^{(x)}_{K_P} x_i + G^{(y)}_{K_P} yi \tag{7}$$

$$\overline{\Delta W_i} = \Delta W^*_i + G^{(x)}_{\Delta w} x_i + G^{(y)}_{\Delta w} y_i \tag{8}$$

$$\overline{\Delta L_i} = \Delta L^*_i + G^{(x)}_{\Delta L} x_i + G^{(y)}_{\Delta L} y_i \tag{9}$$

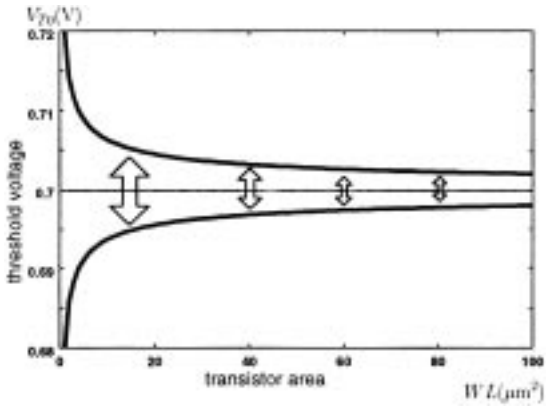

Fig. 1. The randon variation of the threshold voltage.

Parameters $\overline{V_{T0}}$ and $\overline{K_P}$ represent the mean values of the threshold voltage and the gain factor at the coordinate origin. The systematic mismatch is characterized by the model parameters ($G^{(x)}_{V_{T0}}$, $G^{(x)}_{K_P} i$, $G^{(x)}_{\Delta W} i$, $G^{(x)}_{\Delta L}$), ($G^{(y)}_{V_{T0}}$, $G^{(y)}_{K_P} i$, $G^{(y)}_{\Delta W} i$, $G^{(y)}_{\Delta L}$) as a linear gradient. ΔW^*_i and ΔL^*_i represent systematic deviation introduced by the micro-loading effect which is explained later.

With the above two models (the random mismatch model and the systematic mismatch model), we can evaluate the model parameters of the ith transistor. The random mismatch model provides a variance of each parameter from the size of the transistor. The systematic mismatch model provides a mean value of each parameter from the location of the transistor. They are summed up to reproduce the overall parameters as follows.

$$V_{T0_i} = \overline{V_{T0_i}} + \sigma_i(V_{TO}) \times (rand_1) \tag{10}$$

$$K_{P_i} = \overline{K_{P_i}} + \sigma_i(K_P) \times (rand_2) \tag{11}$$

$$\Delta W = \overline{\Delta W_i} + \sigma_i(\Delta W) \times (rand_3) \tag{12}$$

$$\Delta L = \overline{\Delta L_i} + \sigma_i(\Delta L) \times (rand_4) \tag{13}$$

Parameter $rand_j$ is a random number with a normal distribution whose mean value and dispersion are 0 and 1, respectively.

As explained before, our model treats random mismatch and systematic mismatch separately so that it can consider the correlation of mismatch behavior caused by the systematic mismatch among more than two transistors. For mismatch analysis of a single pair of transistors, we can show that our model can be reduced to the Pelgrom model under proper assumption. Let us consider the matching properties, parameters P_a and P_b, of a pair of transistors. These parameters are expressed as follows in our model:

$$P_a = \overline{P_a} + \sigma_a(P) \times (rand_a) \tag{14}$$

$$P_b = \overline{P_b} + \sigma_b(P) \times (rand_b) \tag{15}$$

We assume that the transistors have an equal gate-length and gate-width and are spaced by distance D, where only the dependency in the spaced-direction is assumed for simplicity. Parameters $(rand_a)$ and $(rand_b)$ are independent random variables and $\sigma_a(P)$ and $\sigma_b(P)$ have the same value of $\sigma(P)$.

Then, the difference of the parameters, ΔP, is expressed as

$$\Delta P = P_a - P_b \tag{16}$$

$$= \overline{P_a} - \overline{P_b} + \sqrt{2}\sigma(P)(rand_p) \tag{17}$$

$$\overline{P_a} - \overline{P_b} = G_p D \tag{18}$$

where G_p is the assumed gradient of parameter P in the spaced-direction and $(rand_p)$ is a random number with a normal distribution whose mean value and dispersion are 0 and 1, respectively.

In our model, G_p has a deterministic value inside a chip. However, if we want to model matching behavior of a pair of transistors statistically over a large number of chips, it is reasonable to assume that G_p fluctuates with a normal distribution whose mean value and dispersion are 0 and $S^2_{\Delta P}$ as shown below:

$$G_P = S_{\Delta P}(rand_s) \tag{19}$$

where $(rand_s)$ is a random number similar to $(rand_p)$.

With this assumption, the difference of the parameters, ΔP, is expressed as follows:

$$\Delta P = S_{\Delta P} D(rand_s) + \sqrt{2}\sigma(P)(rand_p) \tag{20}$$

We can therefore derive the dispersion of the difference of the parameters, $\sigma^2(\Delta P)$:

$$\sigma^2(\Delta P) = \overline{(\Delta P - \overline{\Delta P})^2} \tag{21}$$

$$= \overline{2\sigma^2(P)(rand_p)^2} + \overline{2\sqrt{2}\sigma(P) S_{\Delta P} D(rand_p)(rand_s)} + \overline{S^2_{\Delta P}(rand_s)^2 D^2} \tag{22}$$

$$= 2\sigma^2(P) + S^2_{\Delta P} D^2 \tag{23}$$

$$= \frac{2A_P^2}{WL} + S^2_{\Delta P} D^2 \tag{24}$$

$$= \frac{A^2_{\Delta P}}{WL} + S^2_{\Delta P} D^2 \tag{25}$$

Equation (24) is essentially the same as equation (1) of the Pelgrom model. The factor of 2 at the first term comes from the fact that equation (1) is defined as the variance of the difference of the parameters of two transistors whereas equations (2) and (3) are those of the absolute parameters of a single transistor.

2.2. *Characterization of the Micro-Loading Effect*

The gate-length of a transistor has a direct effect on the MOSFET electrical behavior. The fluctuation of the gate-length becomes serious in submicron processes, and therefore it is crucial to precisely characterize the fluctuation of the MOSFET gate-length. It is known that a line-width after fabrication differs from a design line-width depending on the value of its line-width (size effect) and the distance to its adjacent pattern (proximity effect) [4]. It is called the micro-loading effect [11]. The effect is caused by the optical interference in the photolithographic process and the non-uniformity in the etching process modulated by the local pattern density. The micro-loading effect produces a systematic deviation of the gate-length of a transistor, and hence it should be considered in the matching analysis with layout information.[1]

Lieneweg proposed a model of the micro-loading effect for a paired metal line [11]. The model predicts the fabricated width W_{ij} as

$$W_{ij} = W_i + \Delta W + sgn(W_c)\frac{W_c^2}{W_i} + sgn(S_c)\frac{S_c^2}{S_{ij}} \tag{26}$$

W_i = design line-width,
S_{ij} = design spacing from single adjacent line,
ΔW = constant line-width aberration,
W_c = characteristic width of size effect,
S_c = characteristic spacing of proximity effect,

and

$$sgn(X) = X/|X|.$$

This model characterizes the effect of a single adjacent line.

For the matching analysis of MOSFET circuits, we need to extend the model suitable for the calculation of the effective width of a poly-silicon line surrounded by multiple transistors. We thus propose the following model that accommodates the effect of multiple adjacent poly-silicon (gate) lines and the width of the adjacent line.

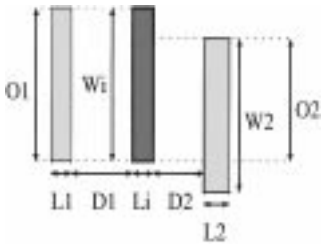

Fig. 2. Parameters of micro-loading effect model.

$$\tilde{L}_i = L_i + \Delta L_0 + \frac{K_L}{L_i} + \sum_{n=1}^{m} \left(\frac{K_D}{D_n} - \frac{K_D}{D_n + L_n} \right) \frac{O_n}{W_i} \tag{27}$$

where

L_i = fabricated gate-length,
L_i = design gate-length,
W_i = design gate-width,
ΔL_0 = constant gate-length aberration,
m = number of transistors around it,
D_n = design spacing from adjacent transistors,
L_n = design length of their gate,
O_n = overlap length,
K_L = characteristic length of size effect,
K_D = characteristic spacing of proximity effect.

Fig. 2 explains each parameter graphically. Parameters ΔL_0, K_L, K_D are process-dependent constants to be extracted experimentally. Next section discusses an extraction method for the parameters.

Parameters ΔW_i^* and ΔL_i^* in equations (8) and (9) are calculated as follows:

$$\Delta W_i^* = \tilde{W}_i - W_i \tag{28}$$

$$\Delta L_i^* = \tilde{L}_i - L_i \tag{29}$$

3. Measurement Methodology

This section explains an extracting method for the parameters in our micro-loading model. Experimental results in a 1.2 μm process are also shown.

We designed a TEG (Test Element Group) similar to the Cross-Quad-Bridge Resistor [11] which is able to measure the fluctuation of line-width electrically. Fig. 3 conceptually explains the structure of the TEG. The TEG has a line of poly-silicon with/without dummy lines around. The width of the center line is partially changed by the dummy lines. The parameters of the model are calculated from the change. We apply a DC voltage between the both ends (VDD, GND) of the TEG. The current flows through the center line is I. The bridge voltages V_{ij} is measured between adjacent points (1, 2, 3, 4, 5, 6). The resistance (R_{ij}) between the measured points is calculated as

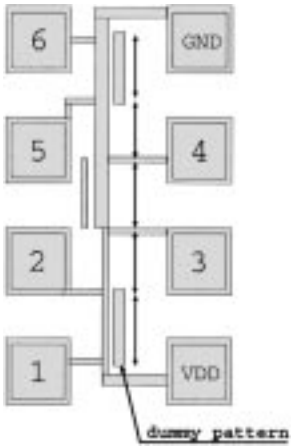

Fig. 3. The conceptual structure of the micro-loading effect TEG.

$$R_{ij} = V_{ij}/I \tag{30}$$

The width of the fabricated line $(\tilde{L}_i)$ is calculated by dividing the resistance R_{ij} by the sheet resistance R_{sheet} as

$$\tilde{L}_i(\mu\text{m}) = \frac{W_i(\mu\text{m})}{R_i(\Omega)} \times R_{sheet}(\Omega/\square) \tag{31}$$

According to the result of measurement, the sheet resistance depends on the width of a fabricated line. We thus model the relationship between the sheet resistance and the line-width by

$$R_{sheet} = R_{base} - \frac{K_R}{\tilde{L}_i} \tag{32}$$

We have designed two circuits having the structure of Fig. 3, each with 10 bridge segments, for a 1.2 μm process and sent them for fabrication.

The micro-loading effect produces a systematic (deterministic) deviation of fabricated line-width depending on the local density of layout patterns. Thus the fluctuation of measured line-width from this TEG has systematic components modeled by equation (27) and random components modeled by equation (5). We may extract the model parameters of equations (5) and (27). However, a wide variety of line-widths and line-lengths are required for statistically meaningful extraction of the model parameter of equation (5) [7], whereas only two line-widths (1.2 and 3.0 μm) with the same length are available in this TEG. We therefore extract only the parameters of equation (27) from the mean values of measured widths from 20 fabricated chips. Parameter extraction of equation (5) (random component) may require dedicated TEGs such as proposed in [7] and our future work includes the characterization of the random component.

Fig. 4 explains the proximity effect. The measured line-width and the calculated line-width by the model for a line with 1.2 μm design width are presented. The horizontal axis represents the distance to adjacent lines. The vertical axis represents the fabricated line-width. In this case, the maximum deviation of the fabricated width is about 4% when the adjacent line comes to the closest position.

The size effect is characterized by the width measurement of lines with different design widths. They are not surrounded by dummy patterns. Fig. 5 shows the measured values and the calculated line by the model. The horizontal axis represents the design line-width, and the vertical axis represents the fabricated line-width. In this process, the size effect is not remarkable than the proximity effect.

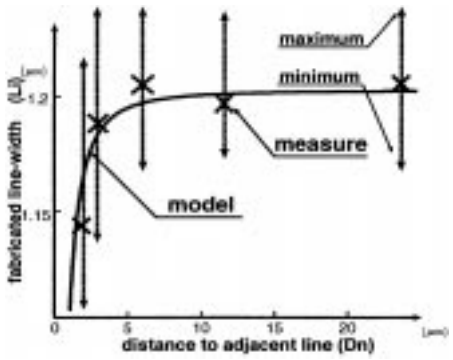

Fig. 4. Proximity effect.

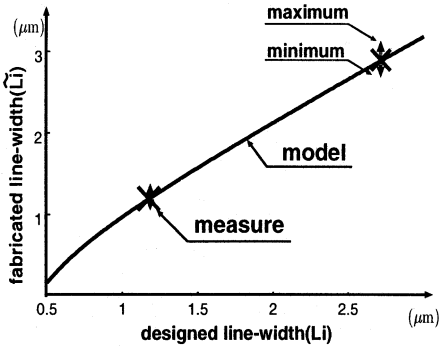

Fig. 5. Size effect.

4. Simulation Methodology

This section explains the methodology of matching analysis using the models in the previous section. We show two methods for the matching analysis that considers layout realization. The first one is a Monte Carlo matching simulation. Given a layout of the circuit under study, a number of parameter sets, whose statistical characteristics are determined by the mismatch models, is generated and the circuit performance is simulated with the parameter sets. The second one is a mismatch model building for a circuit with a predetermined layout structure. The resulting model can be used for the prediction of matching characteristics during a circuit design phase.

4.1. Monte Carlo Matching Simulation

This method is a Monte Carlo simulation. After layout design, we can find the location of each transistor. From this information we can predict the amount of the micro-loading effect and the systematic mismatch which determines the mean value of transistor parameters. The deviation of each parameter is determined by the local mismatch model and a number of parameter sets is generated. The matching properties are examined by simulation with the parameter sets.

The procedure is summarized as follows:

1. Extract the netlist and the position of transistors from a layout pattern.

2. Estimate the deviation $(\Delta W_i^*, \Delta L_i^*)$ between the fabricated width and the designed width of gates by the micro-loading effect. These values based on the systematic mismatch model.
3. Calculate each mean value of transistor parameters ($\overline{V_{T0}}, \overline{K_P}$, etc.) from the position of the transistors based on the systematic mismatch model (6)–(9).
4. Estimate the standard deviation of the transistor parameters based on the random mismatch model (2)–(5).
5. Calculate the transistor parameters (V_{T0_i}, K_{P_i}, etc.) with equations (10)–(13).
6. Simulate the circuit properties with the generated parameters.
7. Extract the statistical distribution of the circuit properties from a number of simulation runs.

4.2. *Mismatch Model Building for a Circuit with a Predetermined Layout Structure*

After the designing of a layout pattern, we can perform a Monte Carlo matching simulation. It however requires a lot of computation costs and cannot be done without complete layout. Before getting a layout pattern, even in the circuit design phase, we need to assess the matching properties of the circuit under design. It can be done by building a mismatch model beforehand for a circuit element, such as a current mirror and differential pair, with a predetermined layout structure. For the building of mismatch models, we first obtain an analytical equation for the circuit performance of interests. We then derive a mismatch model of the performance from the analytical equation. The process of matching analysis using the mismatch model is summarized as follows:

1. Derive an analytic equation that expresses the circuit performance of interests.
2. Estimate the deviation of transistor dimension due to the micro-loading effect.
3. Derive the mean values of the performance using the systematic mismatch model.
4. Derive the dispersion of the performance using the random mismatch model.
5. Calculate the fluctuation of the performance from the mean and the dispersion.

For an example of this process, we show a mismatch analysis of current mirrors. From the analytic expression of output currents, the deviation of output current is expressed as,

$$\frac{\Delta I_{DS}}{\overline{I_{DS}}} = \frac{\Delta K_P}{\overline{K_P}} - \frac{2\Delta V_{T0}}{V_{GS} - \overline{V_{T0}}} + \frac{\Delta W}{\overline{W}} - \frac{\Delta L}{\overline{L}} \tag{33}$$

The dispersion of the output current is thus expressed by

$$\left(\frac{\sigma(\Delta I_{DS})}{\overline{I_{DS}}}\right)^2 = \left(\frac{\sigma(\Delta K_P)}{\overline{K_P}}\right)^2 + \frac{4\sigma^2(\Delta V_{T0})}{(V_{GS} - \overline{V_{T0}})^2} + \left(\frac{\sigma(\Delta W)}{\overline{W}}\right)^2 + \left(\frac{\sigma(\Delta L)}{\overline{L}}\right)^2 \tag{34}$$

$$= \left(\frac{A_{K_P}^2}{\overline{K_P}^2} + \frac{4A_{V_{T0}}^2}{(V_{GS} - V_{T0})^2}\right)\frac{1}{WL} + \frac{A_{\Delta w}^2}{\overline{W}^2 L} + \frac{A_{\Delta L}^2}{WL^2} \tag{35}$$

If there is no source of systematic mismatch, the output current mismatch is a normal distribution with mean value equal to zero and dispersion being calculated by equation (35). Otherwise, we need to consider the effect of systematic mismatch which produces the deviation of the mean value. First we estimate the micro-loading effect. In this case, two transistors in a current mirror are equally influenced by the micro-loading effect, and hence the parameters ΔW_i^*, ΔL_i^* are both zero. The deviation of the mean value is thus expressed as

$$\frac{\overline{\Delta I_{DS}}}{\overline{I_{DS}}} = \frac{\overline{\Delta K_P}}{\overline{K_P}} - \frac{2\overline{\Delta V_{T0}}}{V_{GS} - \overline{V_{T0}}} + \frac{\overline{\Delta W}}{\overline{W}} - \frac{\overline{\Delta L}}{\overline{L}} \tag{36}$$

$$= \left(G_{K_P}^{(x)} - \frac{G_{V_{T0}}^{(x)}}{V_{GS} - V_{T0}} + \frac{G_{\Delta W}^{(x)}}{\overline{W}} + \frac{G_{\Delta L}^{(x)}}{\overline{L}}\right) D_x \tag{37}$$

where only the dependency in the x-direction is included for simplicity.

The layout structures of current mirrors are classified into two groups. The first group is a simple pair of transistors placed in parallel. The layout is symmetric with respect to the center line. On the other hand, the second group has a symmetric layout with respect to the center point. Examples of this group are the common-centroid (QUAD) layout [5,8] and the waffle layout [8]. The structure of the QUAD layout is diagonally arranged 2 pairs of

transistors. The structure of the waffle layout is a lot of divided transistors arranged in a mesh.

The output current mismatch for the first group is the sum of the systematic mismatch and the random mismatch as

$$\Delta I_{DS} = \overline{\Delta I_{DS}} + \sigma(\Delta I_{DS}) \times rand \tag{38}$$

On the other hand, the systematic error is canceled out in the second group, and hence the systematic mismatch term does not appear in the output current mismatch as

$$\Delta I_{DS} = \sigma(\Delta I_{DS}) \times rand \tag{39}$$

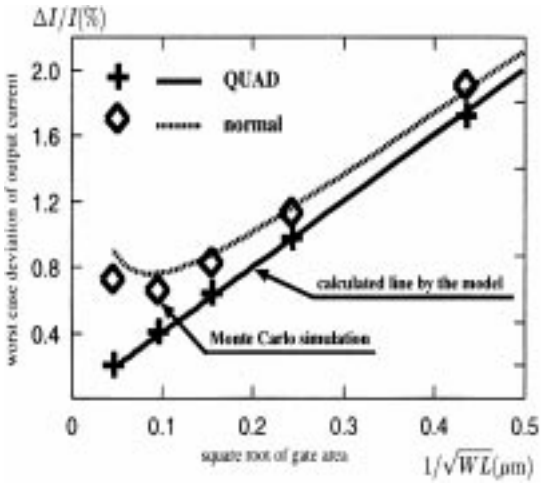

Fig. 6. Result of matching simulation for current mirror.

5. Example of Simulation

This section reports the result of matching simulation for current mirrors with our technique. The matching property is analyzed for circuits with common-centroid layout structures and normal paired-transistor structures. Both of Monte Carlo matching simulation and mismatch model analysis are performed. The gradients of threshold voltage and the gain factor, $G_{V_{T0}}$ and G_{K_P} respectively, are fixed to 0.1%/μm. The input current I_{ds} is 20 μA. The horizontal axis represents the square root of gate area. The vertical axis represents the worst case (3σ) deviation of the output current. We execute the Monte Carlo Matching simulation under five different sizes of transistors as $(L, W) = (1.2,\ 4.8)$, $(2,\ 8)$,$(3,\ 12)$, $(5,\ 20)$ and $(10,\ 40)$. W/L is fixed to 4 so that the operating condition of each pair of transistors becomes the same under the same input current. Fig. 6 shows the results.

The larger the size of transistors increases on each layout, the better the matching property caused by the random error improves. The increase of transistor size, however, makes the pair transistors being placed apart, which increases the amount of systematic error. The effect of the systematic error do not appear in a circuit with common-centroid structure, whereas it does affect a circuit with normal paired-transistor structure. Indeed, matching properties become worse by increasing the size of the transistor beyond a certain value. On the other hand, a circuit with the common-centroid structure can further improve matching properties by the increase of the size. The layout of common centroid improves the matching property by 0.41% $(= 0.72\text{–}0.31\%)$ over the normal layout at the size of 400 μm^2. We can see that our technique can analyze the matching property quantitatively considering the effect of layout structure.

6. Conclusions

We have presented a method for matching analysis of MOSFET circuits taking layout information into account. In order to analyze the matching properties of transistors, we consider local random fluctuations, global systematic fluctuations and the micro-loading effect.

In order to evaluate the effect of systematic variation precisely, we treat the systematic mismatch separately from the random mismatch. The random mismatch model provides a variance of each parameter from the size of the transistor. The systematic mismatch model provides a mean value of each parameter from the location of the transistor. Those models are summed up to reproduce overall parameters.

The channel length of a MOSFET has a dominant effect on its electrical properties and hence the micro-loading effect for the poly-silicon gate has been taken into account. The micro-loading effect is characterized by the local density of layout patterns. We have explained an extracting method for the parameters in our micro-loading model. Our measured results in a 1.2 μm CMOS process indicate that there exists the

maximum deviation of 4% in line-width for a poly-silicon line with a 1.2 μm design width.

We have shown two methods for the application of our models. The first one is a Monte Carlo mismatch analysis, which is done after the completion of layout design. It is applicable to a circuit in general with layout, but it requires huge amount of computation costs. The second one is a mismatch-model building for a circuit with a predetermined layout structure. Those two methods are used to simulate the matching properties after/before getting of layout design appropriately. As an example of the application, we have simulated the matching properties of current mirrors with a conventional structure and a common-centroid structure, and confirmed the amount of improvement provided by the latter structure quantitatively.

Note

1. In some advanced fabrication process, this effect is intentionally compensated by modifying layout pattern in the opposite direction in the reticle preparation process. We assume that this is not the case in the fabrication process under discussion.

References

1. K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, ''Characterisation and modeling of mismatch in MOS transistors for precision analog design.'' *IEEE J. Solid-State Circuits*, pp. 1057–1066, December 1986.
2. M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, ''Matching properties of MOS transistors.'' *IEEE J. Solid-State Circuits*, pp. 1433–1439, October 1989.
3. E. Felt, A. Narayan, and A. S. Vincentelli, ''Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's.'' *IEEE Proc. ICCAD '94*, pp. 272–277, 1994.
4. J.-S. Choi and I.-S. Chung, ''A test structure for monitoring micro-loading effect of MOSFET gate length.'' *IEEE International Conference on Microelectronic Test Structure*, pp. 3–7, March 1996.
5. H. Elzinga, ''On the impact of spatial parametric variations on MOS transistor mismatch.'' *IEEE International Conference on Microelectronic Test Structures*, Vol. 9, pp. 173–177, March 1996.
6. S.-C. Wong, J.-K. Ting, and S.-L. Hsu, ''Characterization and modeling of MOS mismatch in analog CMOS technology.'' *IEEE International Conference on Microelectronic Test Structures*, Vol. 8, pp. 171–176, March 1995.
7. J. Bastos, M. Steyaert, R. Roovers, P. Kinget, W. Sansen, B. Graindourze, A. Pergoot, and E. Janssens, ''Mismatch characterization of small size MOS transistors.'' *IEEE International Conference on Microelectronic Test Structures*, Vol. 8, pp. 271–276, March 1995.
8. J. Bastos, M. Steyert, B. Graindourze, and W. Sansen, ''Matching of MOS transistors with different layout styles.'' *IEEE International Conference on Microelectronic Test Structures*, Vol. 9, pp. 17–18, March 1996.
9. J. Bastos, M. Steyert, B. Graindourze, and W. Sansen, ''Influence of die attachment on MOS transistor matching.'' *IEEE International Conference on Microelectronic Test Structures*, Vol. 9, pp. 27–31, March 1996.
10. P. Kinget, *Analog VLSI Integration of Massive Parallel Processing Systems*. Kluwer, 1996.
11. U. Lieneweg and N. Zamani, ''Measurement and modeling of size and proximity effects in conducting linewidths.'' *IEEE International Conference on Microelectronic Test Structures*, Vol. 7, pp. 57–61, 1994.

Kenichi Okada received a B.E. degree in electronic engineering from Kyoto University, Kyoto, Japan, in 1998. Currently, he is studying toward the M.E. degree in the Department of Communications and Computer Engineering, Kyoto University.

Hidetoshi Onodera received B.E. and M.E., and D.E. degrees in electronic engineering from Kyoto University, Kyoto, Japan, in 1978, 1980, 1984, respectively. Since 1983 he has been an Instructor (1983–1991) and an Associate Professor (1992–) in the Department of Electronics and Communication, Graduate School of Engineering, Kyoto University. His research interests include computer-aided-design for integrated circuits, analog and mixed analog-digital circuits design, and neural networks. He is a member of the Information Processing Society of Japan, and IEEE.

Keikichi Tamaru was born in Sendai, Japan in 1936. He received the B.E., M.E. and D.E. degrees in electronic engineering from Kyoto University, Kyoto Japan, in 1958, 1960 and 1970, respectively. From 1960 to 1979 he was engaged in the development of high-speed logic circuits and micro computers at Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan. Since 1979, he has been a Professor in the Department of Electronics and Communication, Graduate School of Engineering, Kyoto University. His research interests include computer-aided design for digital and analog integrated circuits and the architecture of special-purpose VLSI processors. Dr. Tamaru is a member of IPSJ, IEEE, and ACM.