

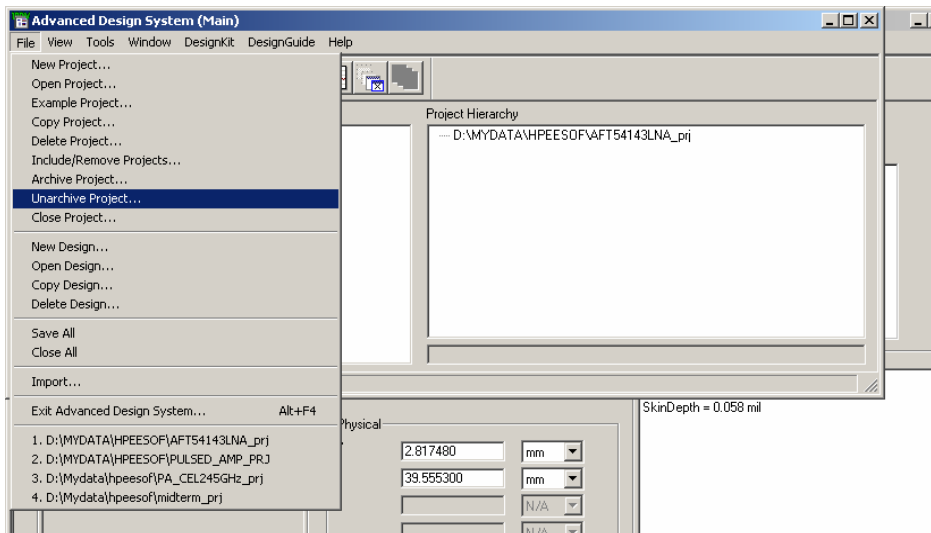
## Lab 1 Linear LNA design

## Objective:

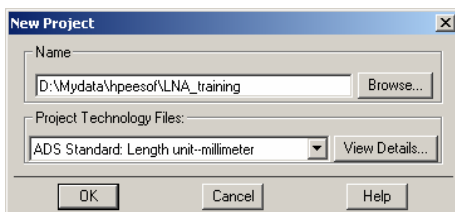
1. Obtaining the FET Model from the manufacturer website
2. Operating point using DC trace
3. Bias circuit design
4. Noise Circle and Input matching
5. Output matching for maximum gain
6. Final matching network design

## FET Model

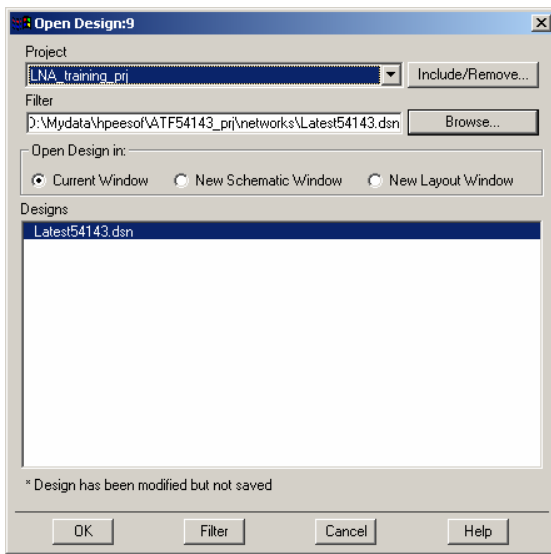
We will use a PHEMT FET from Agilent technology. The part number is ATF54143. We can download the model zap file (the proprietary zip file for ADS project) from the Agilent website (<http://www.home.agilent.com/USeeng/nav/-536893727.536886206/pd.html>). Download the model file (ATF54143.zip). Unarchive the zap file as shown.



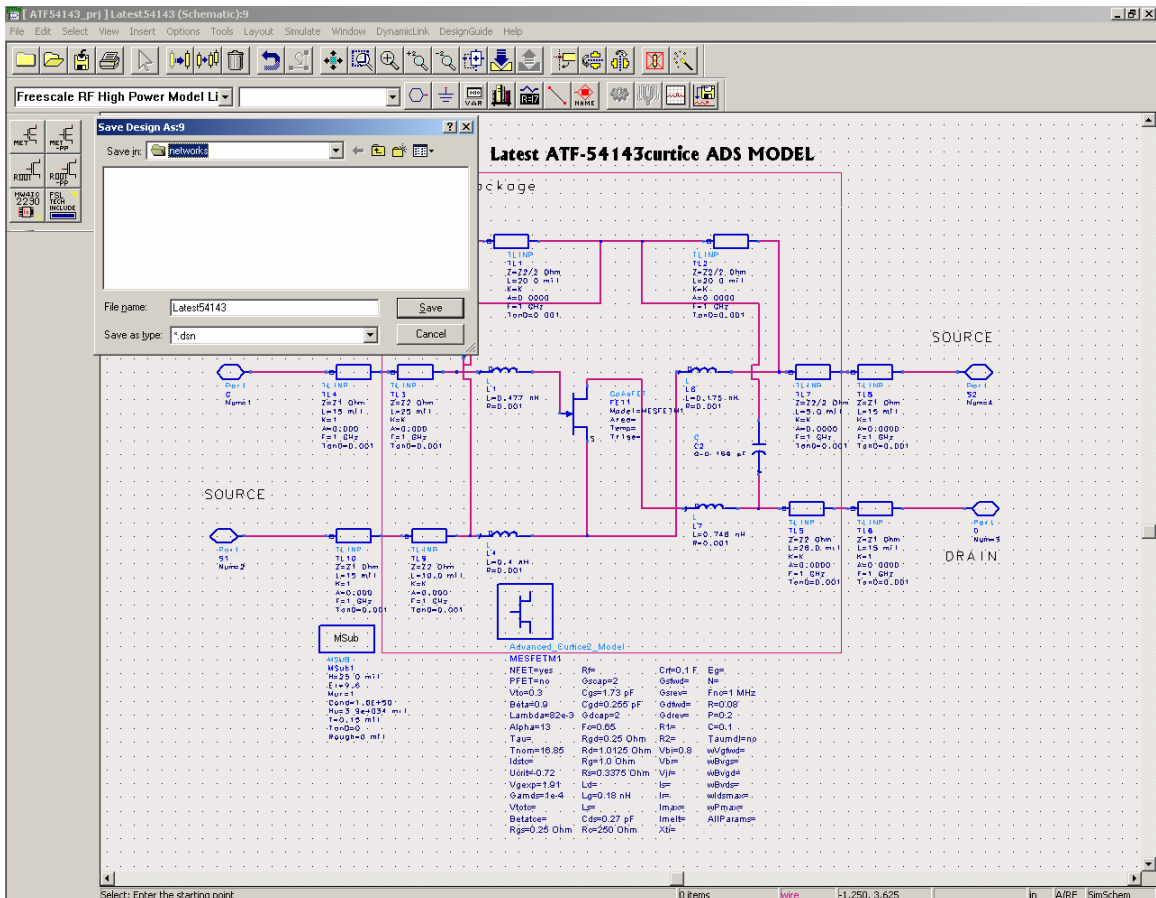
Create a new project and name it LNA\_training. Click OK.



Open Latest54143.dsn design from the ATF54143\_prj directory.

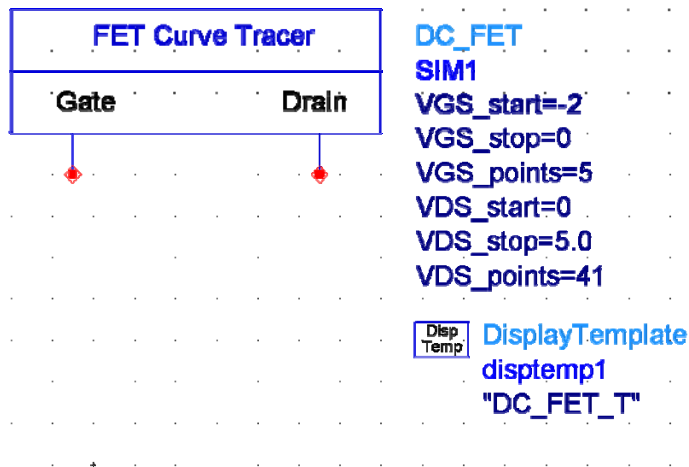
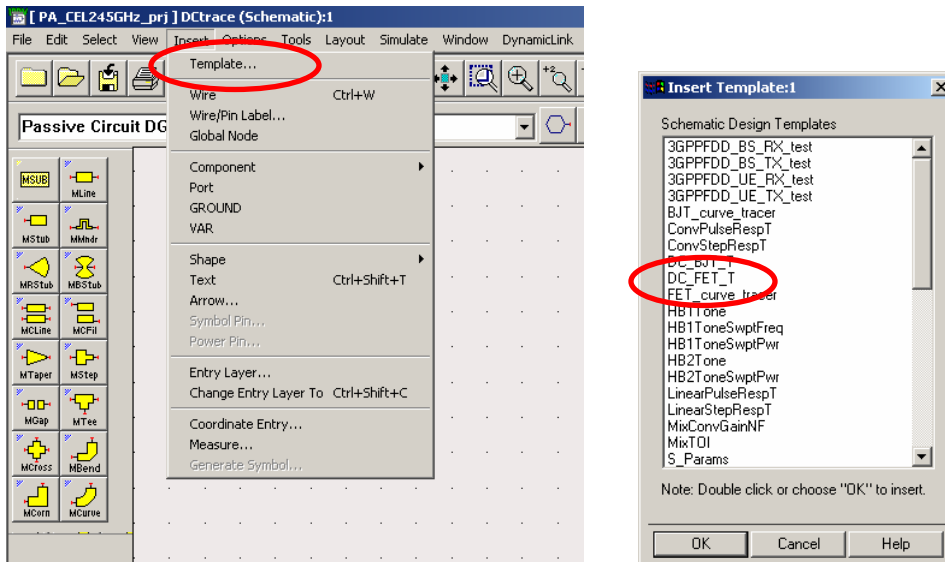


We need to save this design into our project directory so that we can use it as ATF54143 model in our simulation. Choose Save As from File menu and Click save.

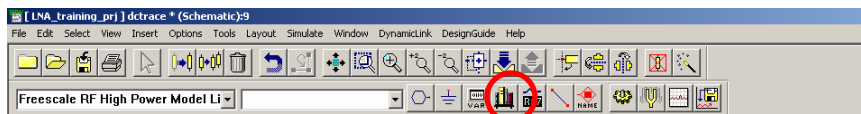


## DC Tracing

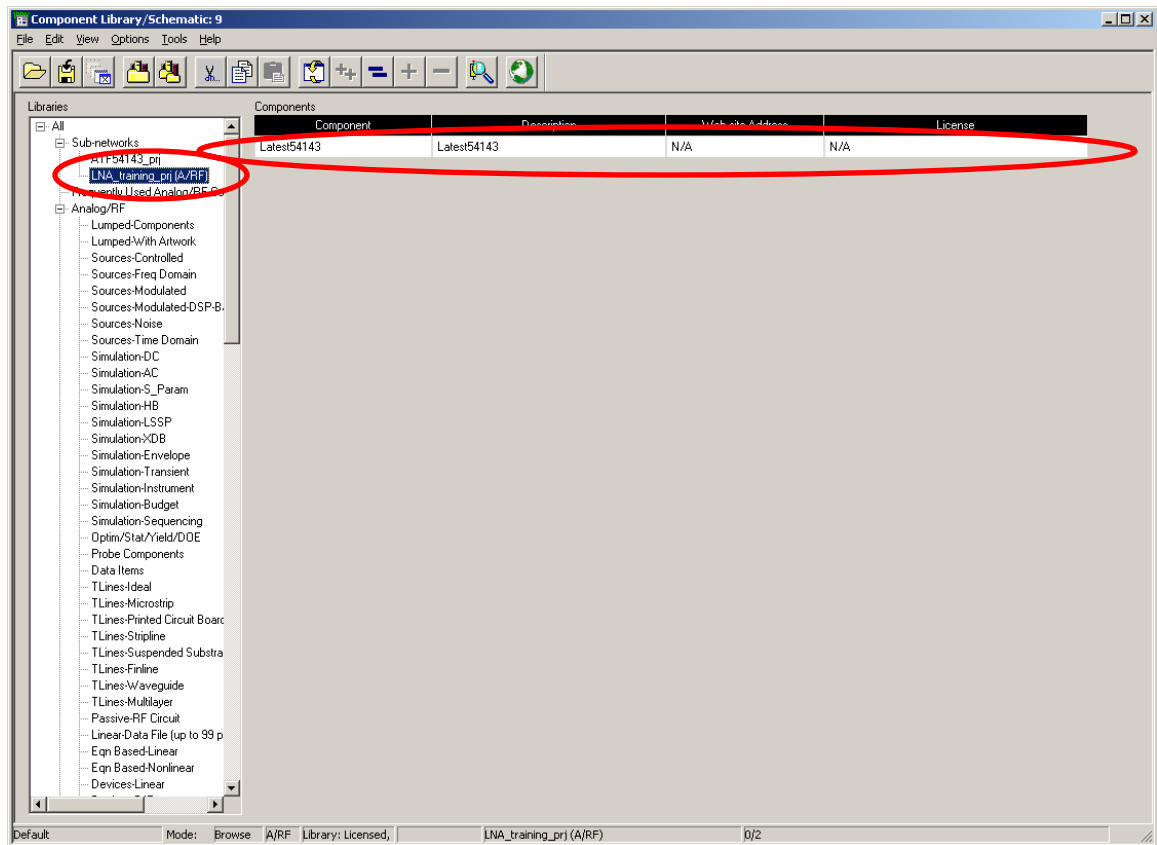
1. Create a new schematic
2. Choose FET biasing template



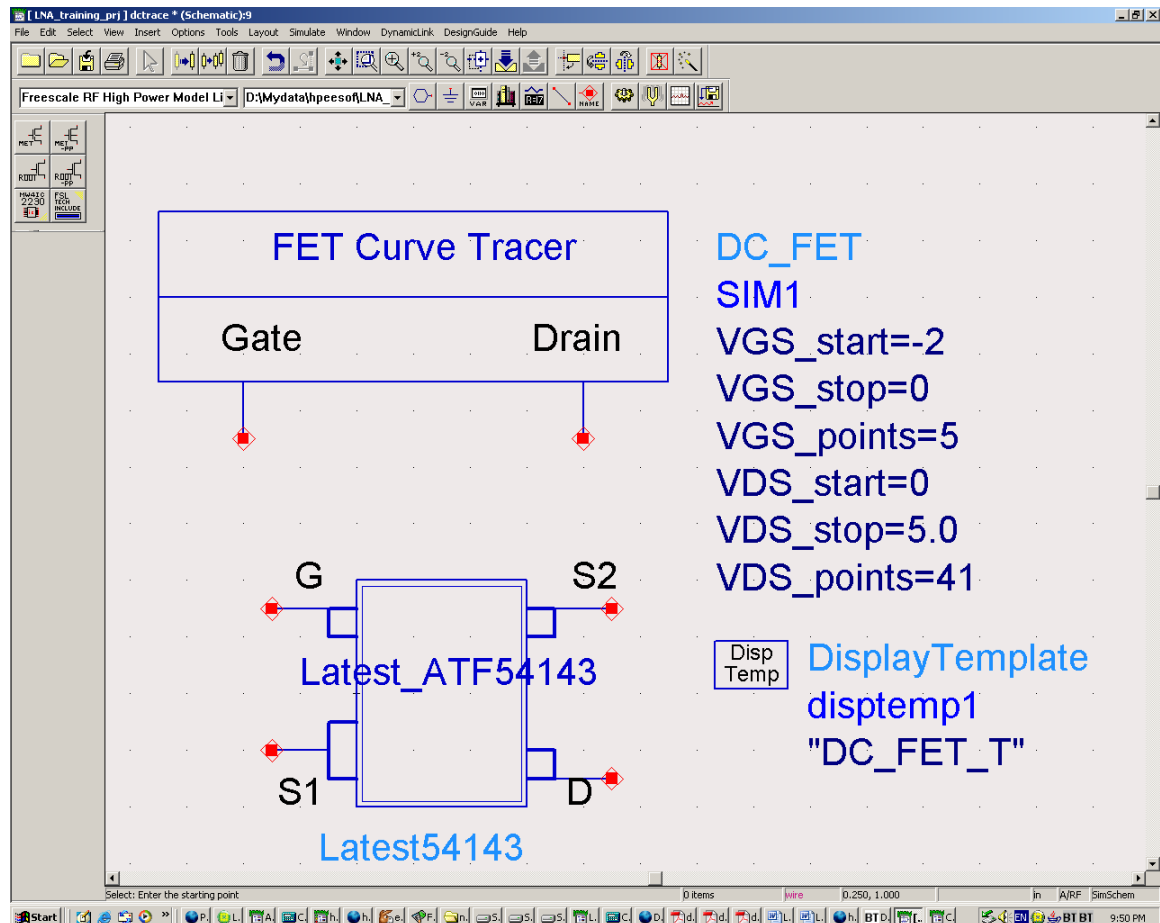
3. Insert the FET model from the library list.



Click on Library as shown. The library window will show up



Click on Latest54143 Sub-networks. Back to the schematic window, place ATF54143 into the DC Tracing template



The VI-curve from ATF54143 datasheet shows that  $V_{gs}$  is about 0.3 to 0.7 V. (ATF54143 is a PHEMT FET. It requires positive  $V_{gs}$ )

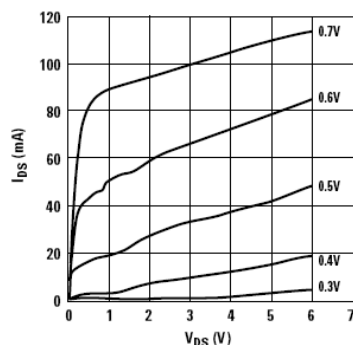
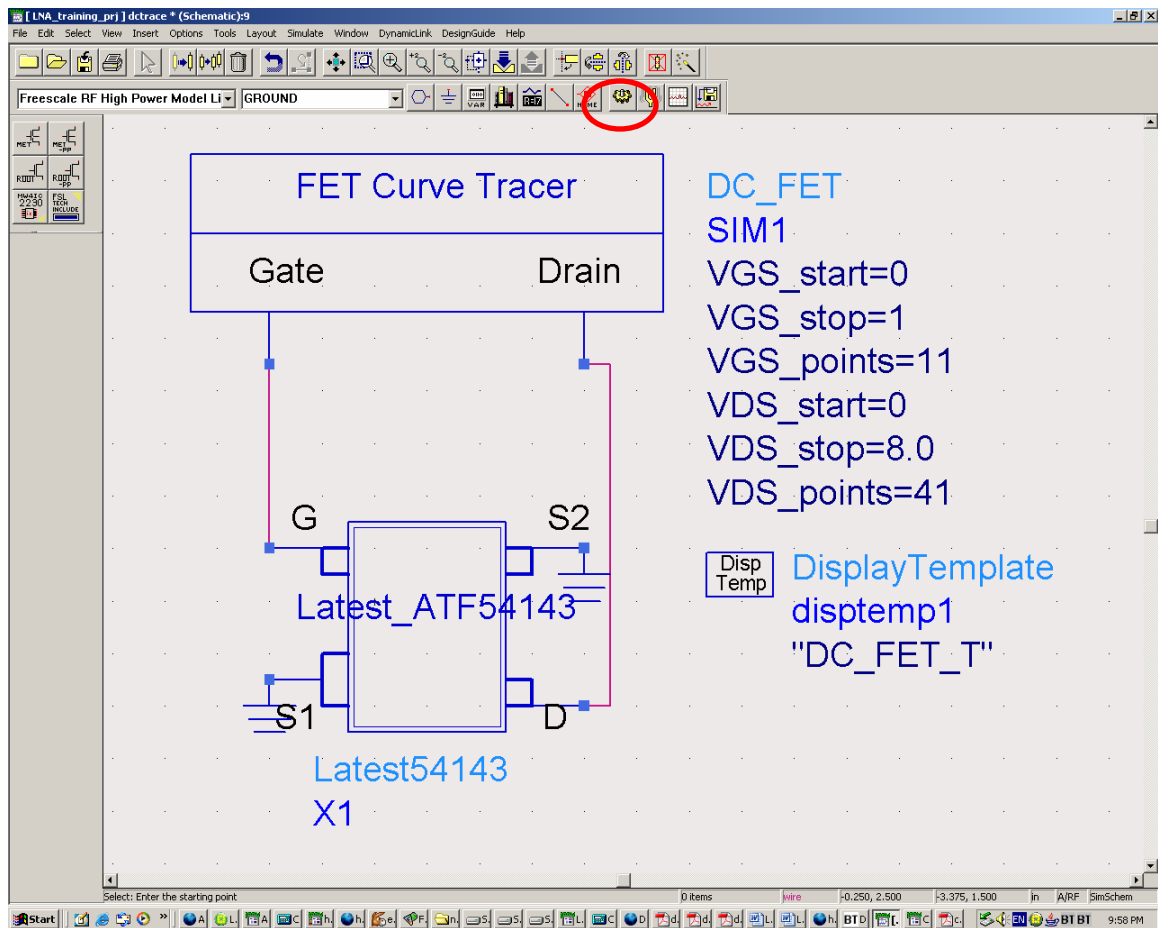

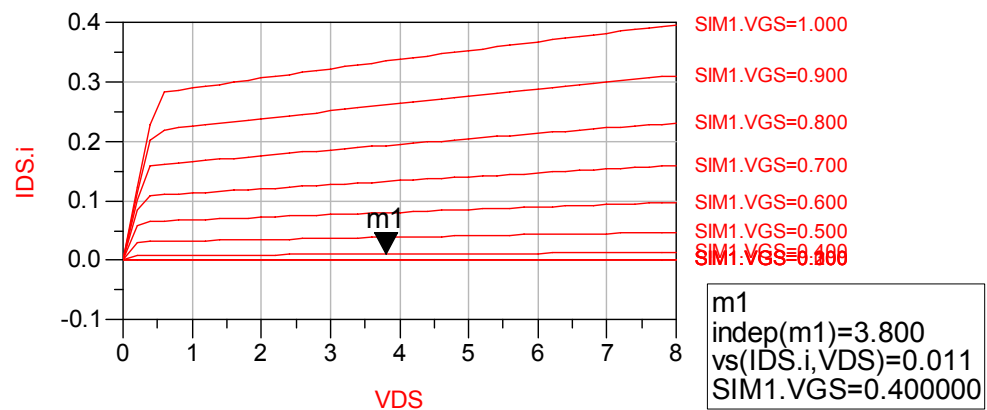


Figure 1. Typical I-V Curves.  
( $V_{GS} = 0.1V$  per step)

Hence, we set the DC tracing parameters as shown and connect D to Drain, G to Gate, S1 to GND and S2 to GND.



Simulate the circuit by clicking .



We can now look at ATF54143 datasheet to determine operating point.

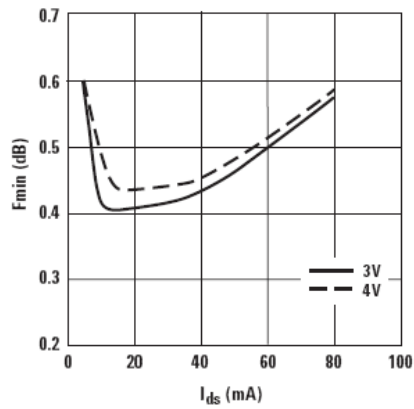


Figure 6.  $F_{min}$  vs.  $I_{ds}$  and  $V_{ds}$  Tuned for Max OIP3 and  $F_{min}$  at 2 GHz.

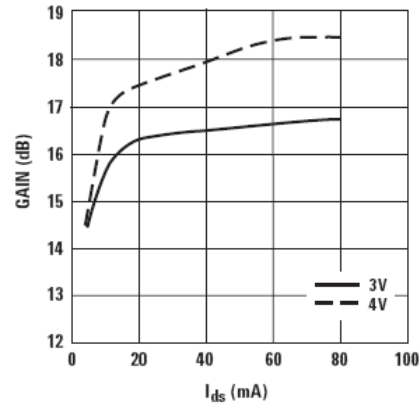
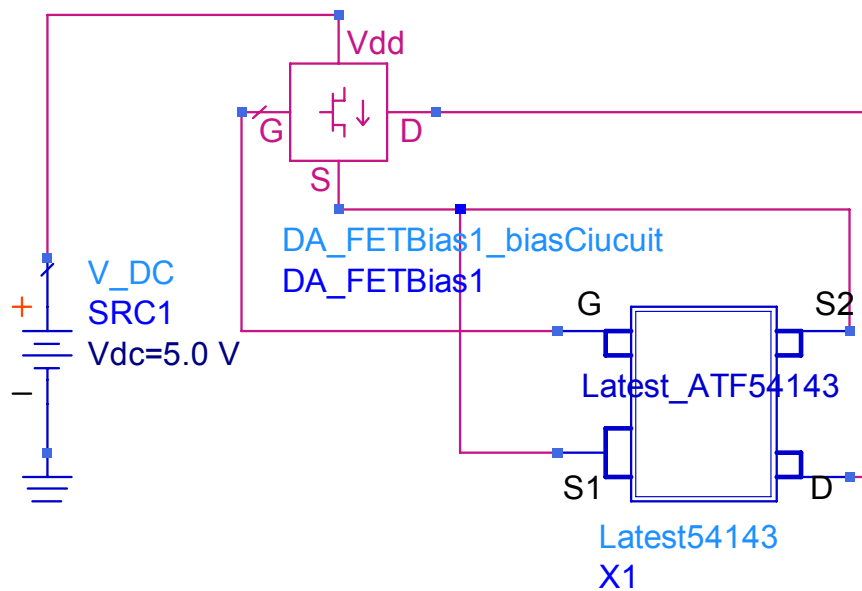
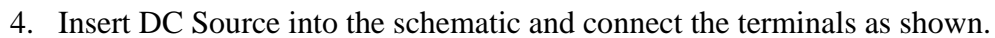


Figure 8. Gain vs.  $I_{ds}$  and  $V_{ds}$  Tuned for Max OIP3 and  $F_{min}$  at 2 GHz.

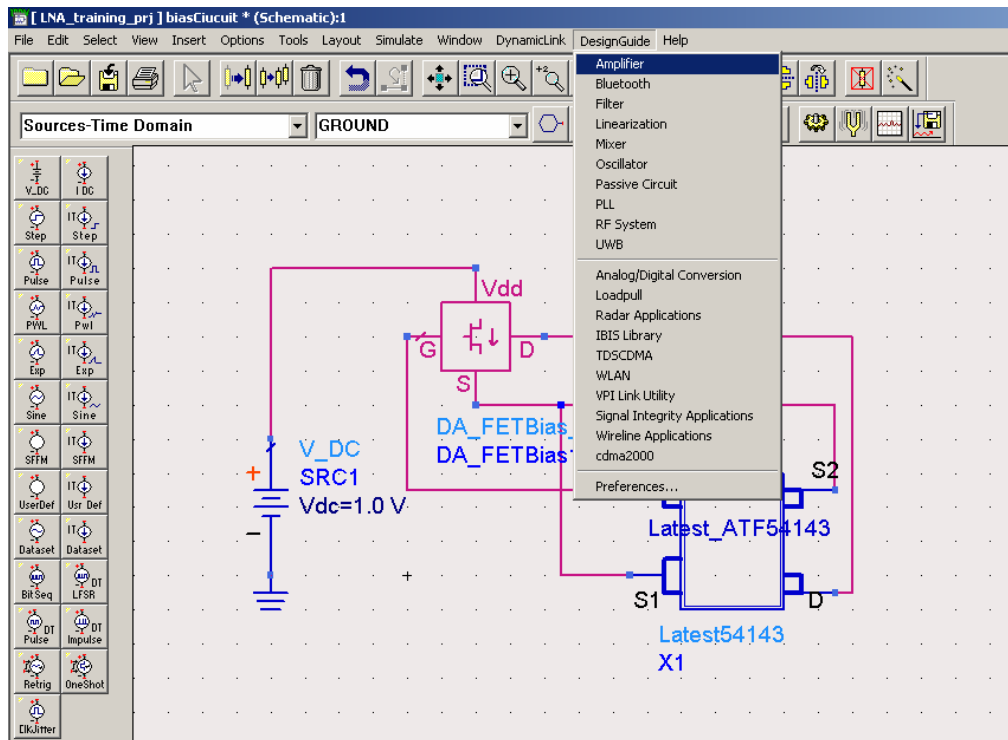
The NFmin is about 0.44 dB at  $V_{ds} = 4 V$  and  $I_{ds} = 20 mA$  but gain is about 17.5 dB at  $I_{ds} = 20 mA$  and  $V_{ds} = 4 V$ .



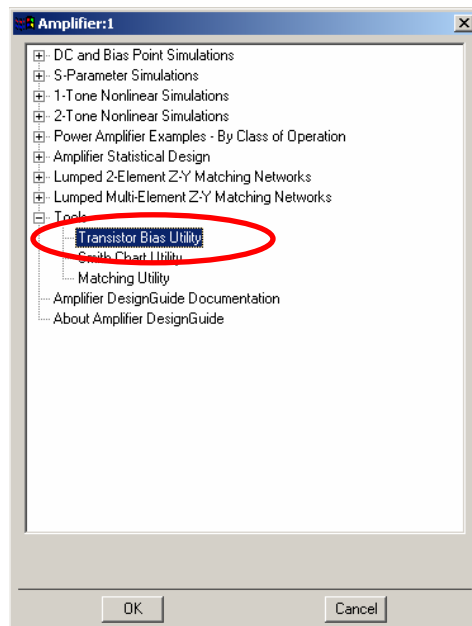
1. Create a new schematic.
2. Place ATF54143 PHEMT as shown in the previous section.
3. Insert DA\_FETbias to the schematic



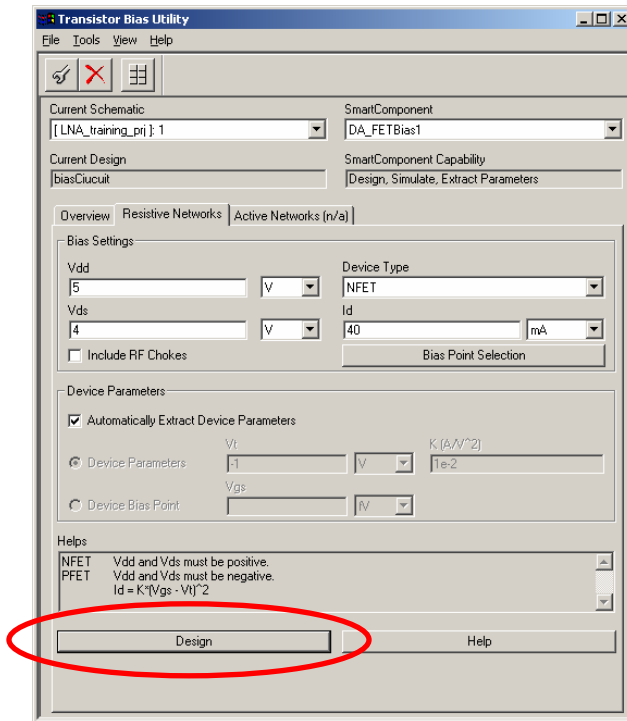
## 5. In Design Guide choose Amplifier



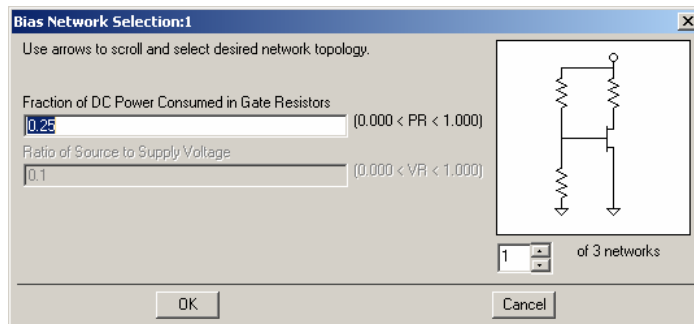
## Choose Transistor Bias Utility



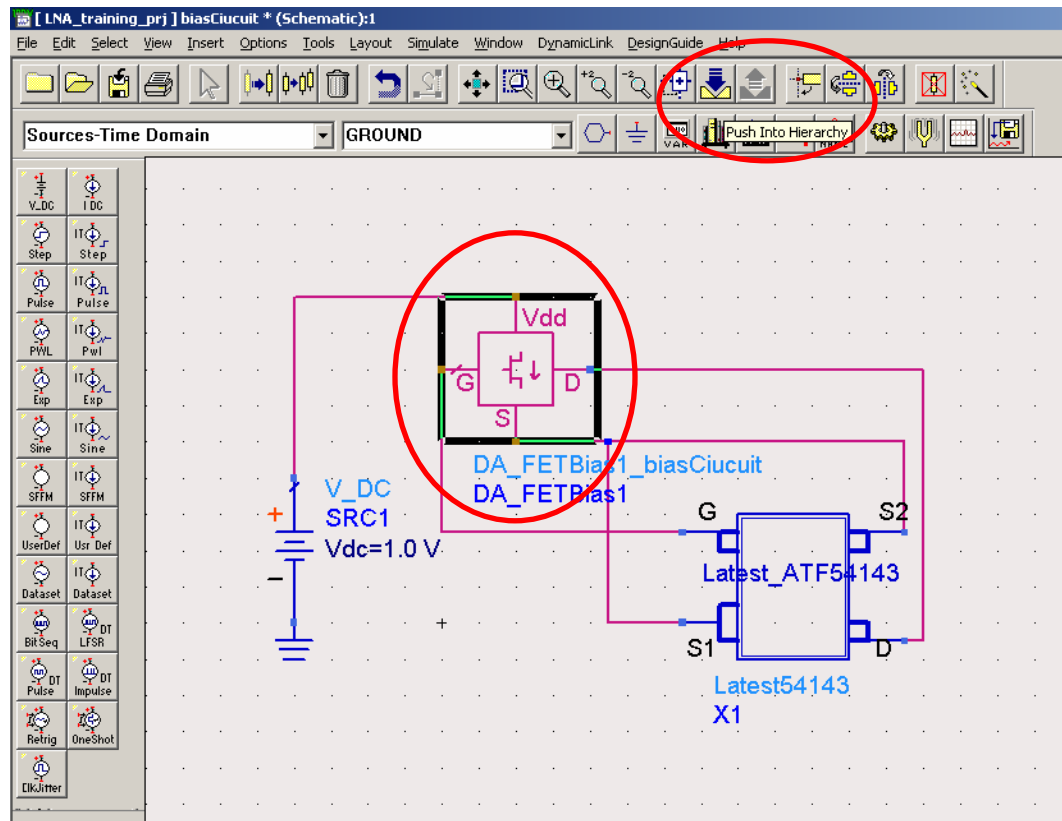
Change Vdd, Vds and Id to 5 V, 4 V and 40 mA respectively. Click Design



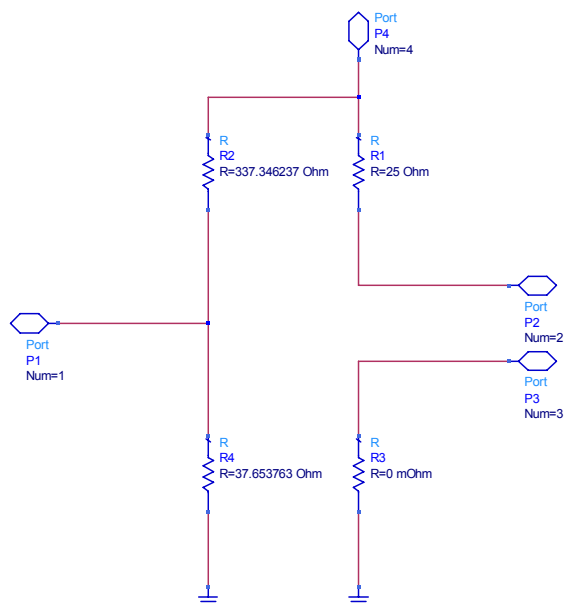
We will the first passive bias network for this circuit. Click OK.



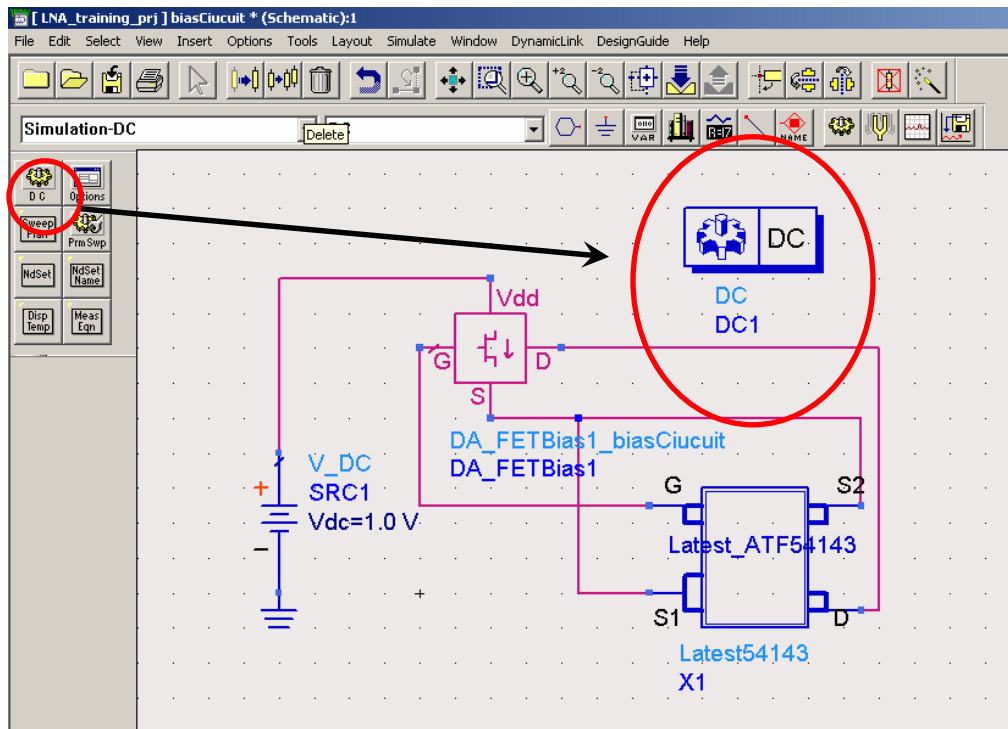
Select DA\_FETBias1 and click Push Into Hierarchy to display the bias circuit.



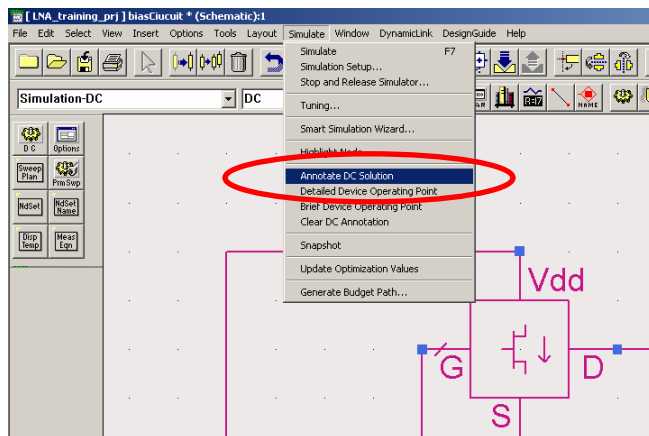
We might need to change the resistor values to the commercial values.



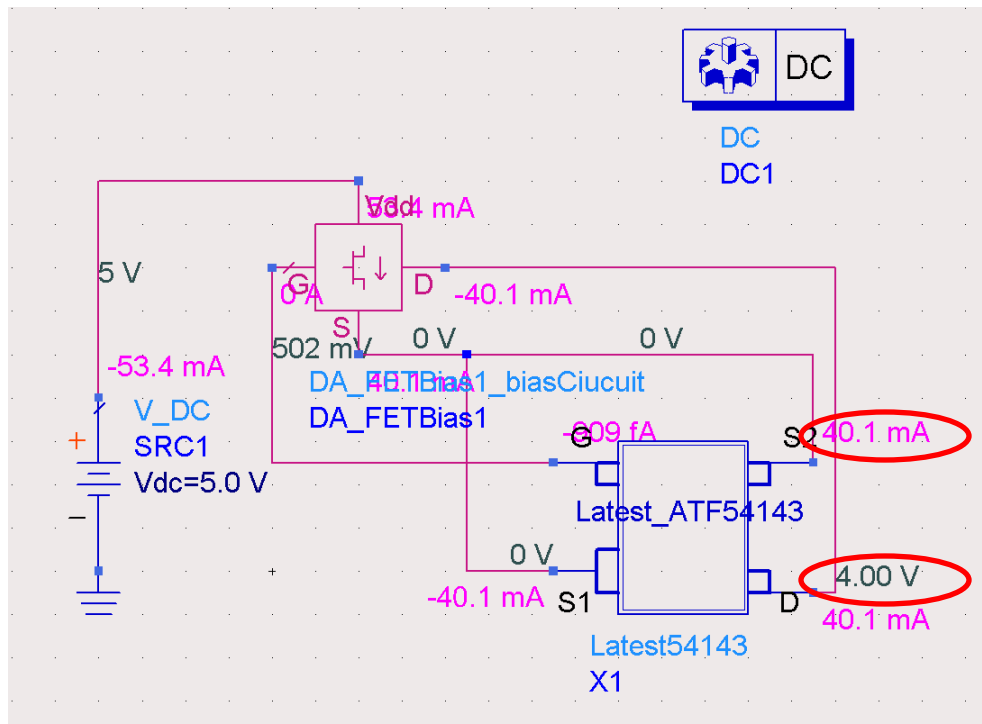
Back to schematic. We now verify the biasing point by using DC simulation by inserting DC simulation controller and lick simulate.



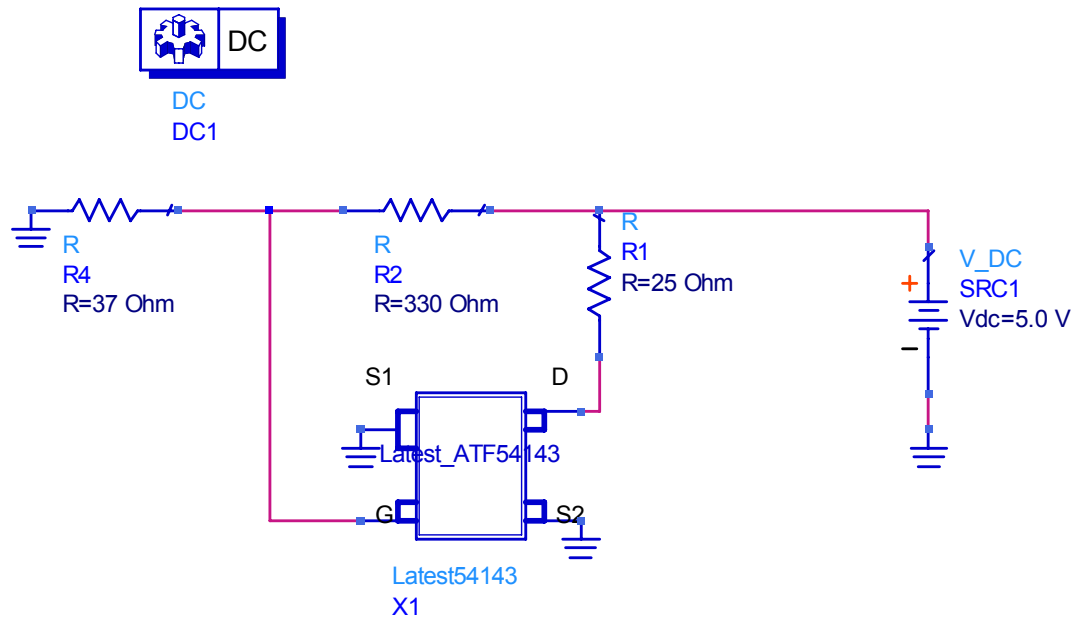
In simulate menu, click Annotate DC solution to show voltage and current at each node.



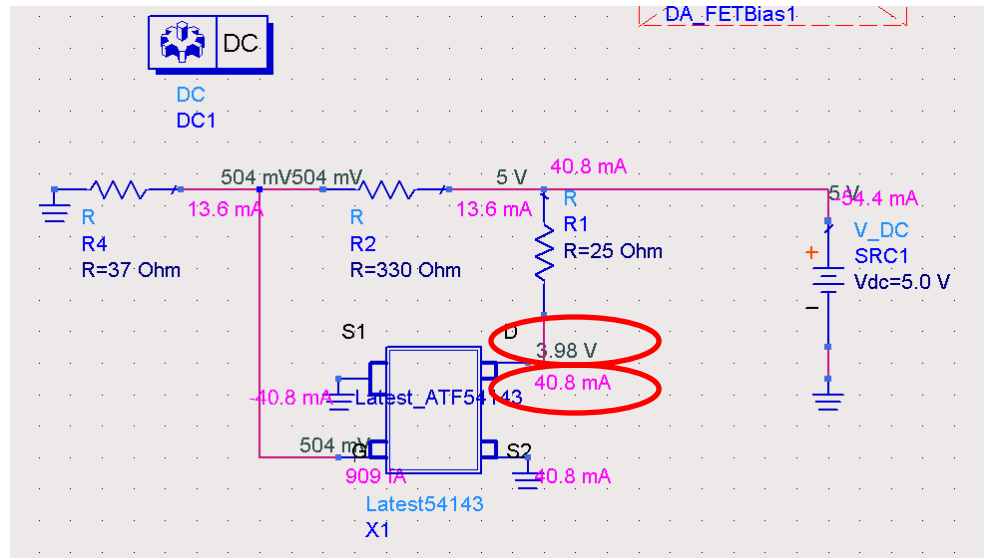
It can be seen that  $V_{ds}$  and  $I_{ds}$  are 4 volts and 40 mA as desired.



The resistors need to be change to commercially available resistors. Let modify the schematic as shown.

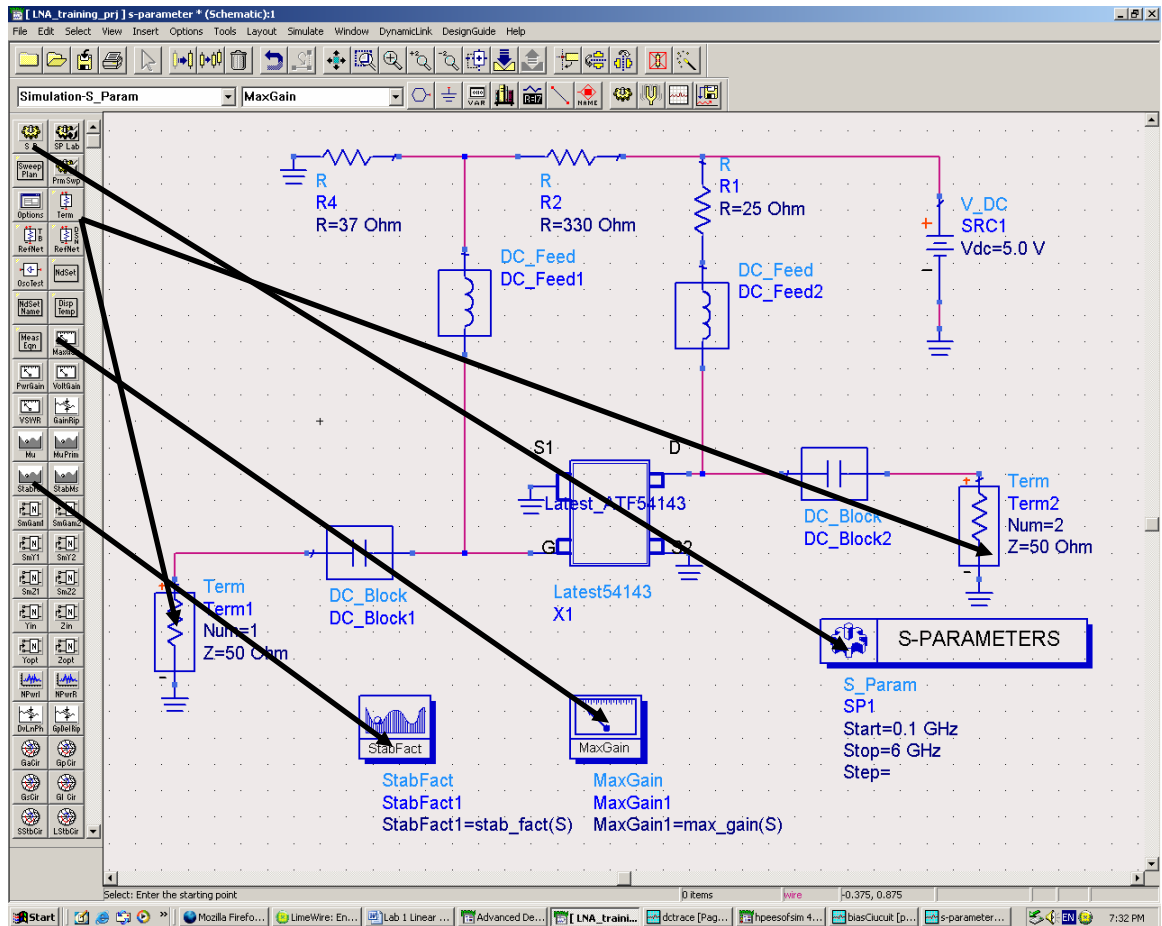


Simulate. It can be seen that the bias point is slightly off from desired point.

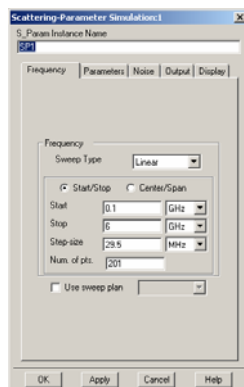


# S-parameters, NF and stability

1. Create a schematic as shown. You might copy most of the schematic from the previous one.

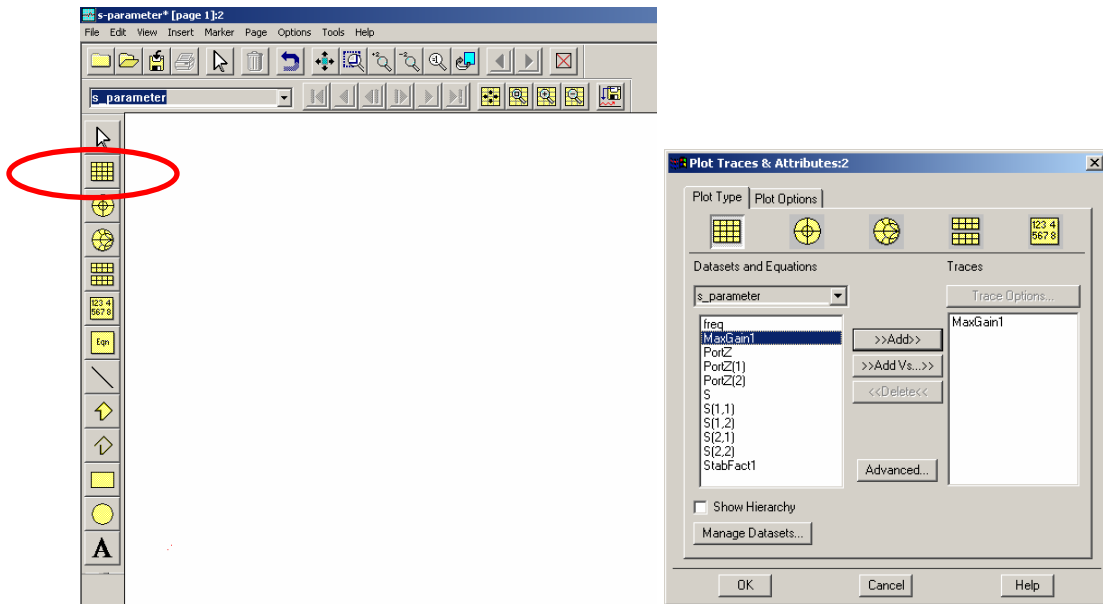


Double click on S-parameters simulation controller. Change the start, stop and Num of pts as shown. Click OK.

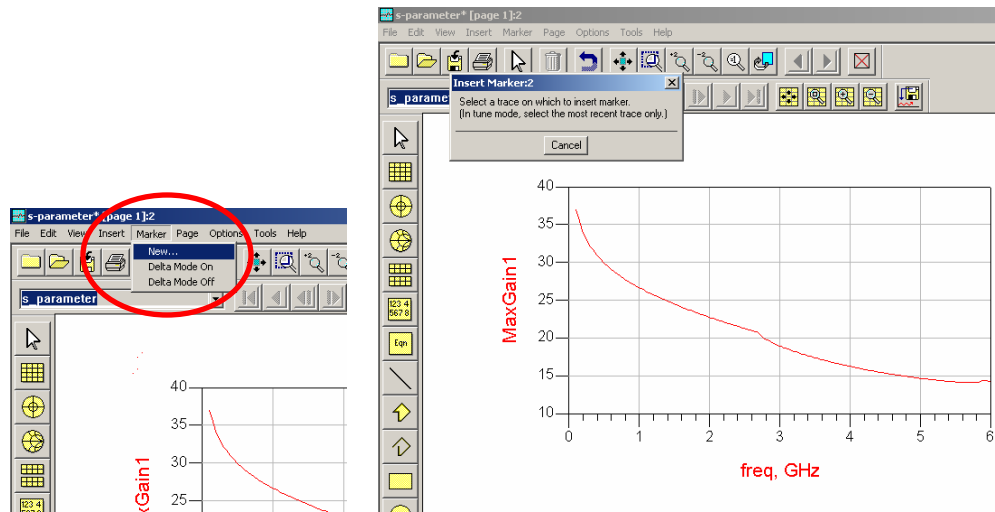




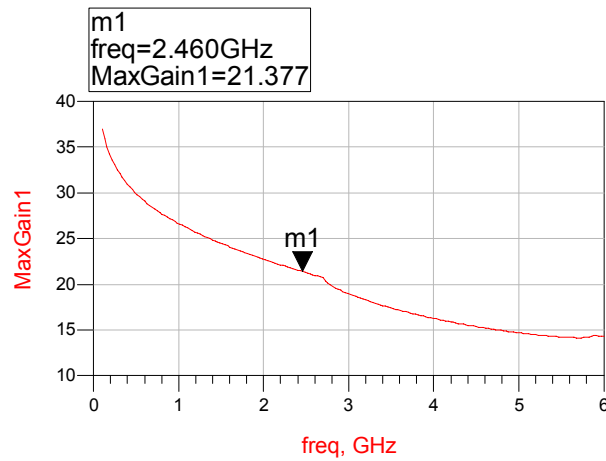
2. Simulate. In data display window, we plot, maximum gain and stability factor. Click at rectangular plot. In Plot Traces & Attributes, add MaxGain1 to Traces. Click OK.



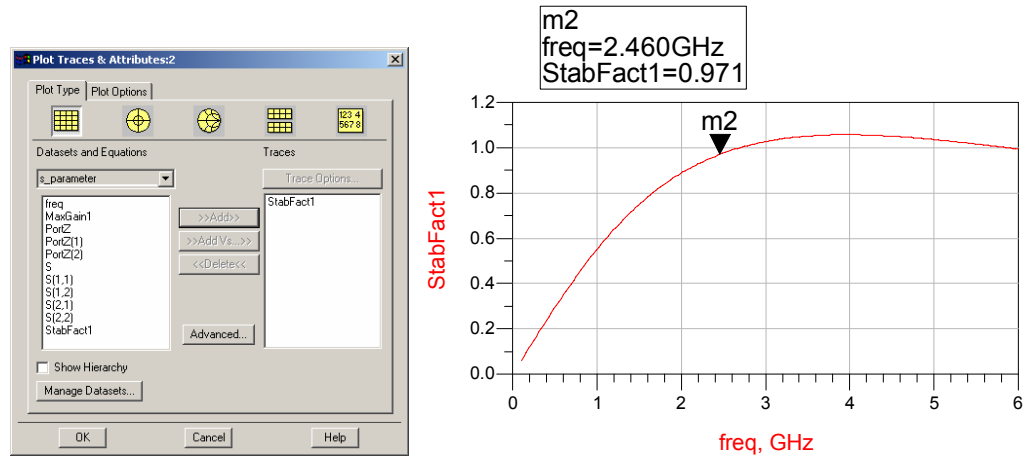
Place a marker to the Trace by clicking at Marker menu and choose New. Click at the trace.



It can be seen that the maximum gain is 21.377 at 2.46 GHz.

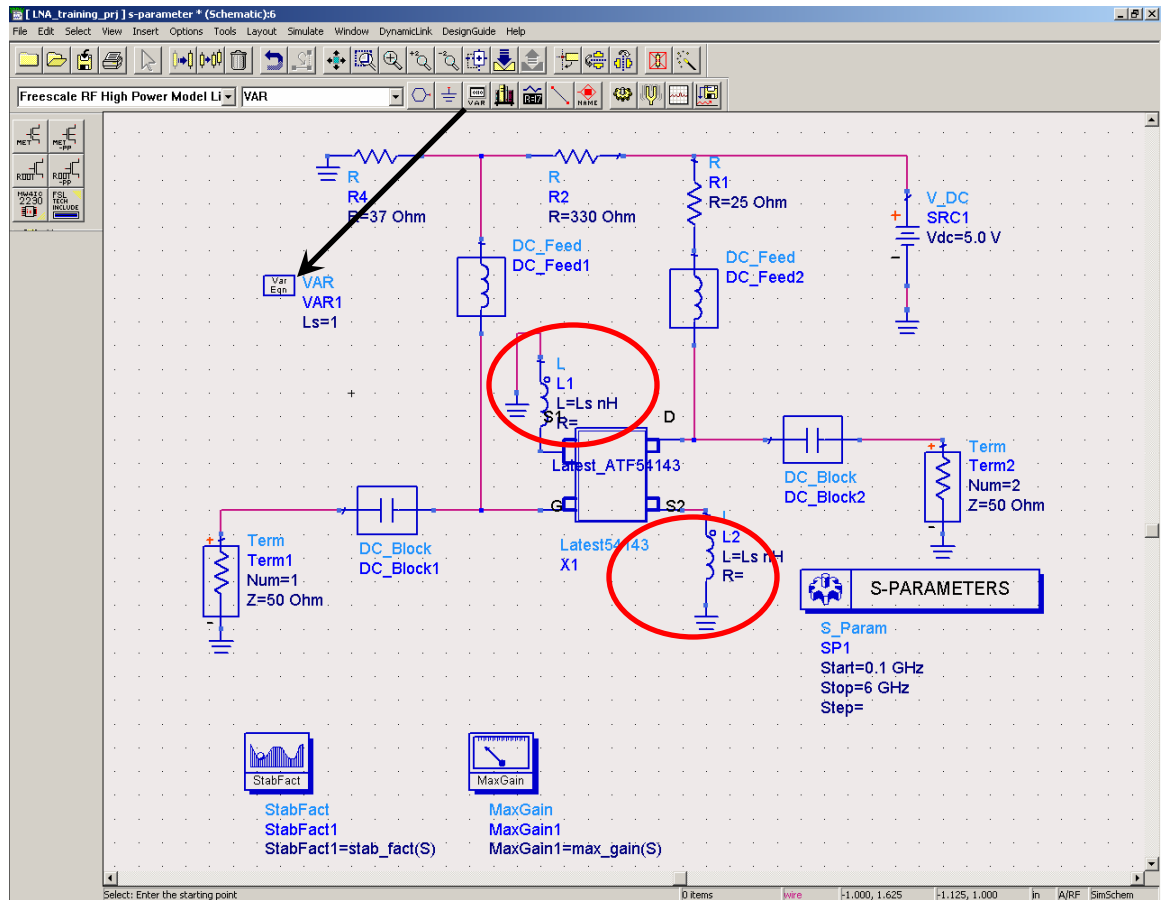


We now plot stability factor to see whether the LNA is stable at desired frequency. In data display window, choose rectangular plot . Add StabFact1 to Traces. Click OK. Add a marker to display stability factor at desired frequency.

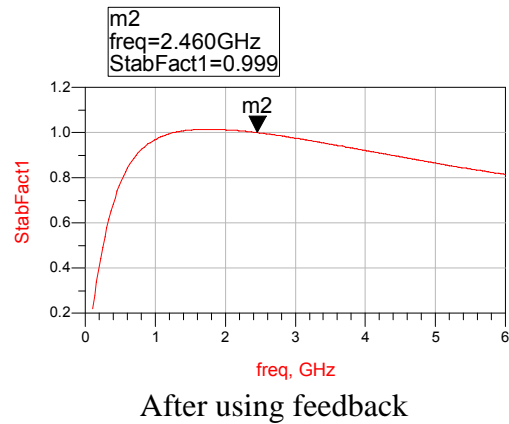
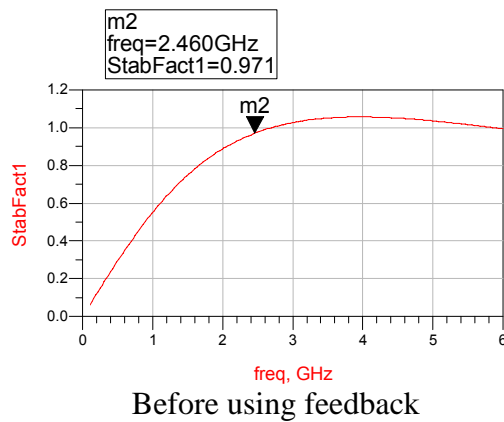


We observe that the stability factor is less than one at 2.46 GHz. The LNA might be unstable so we need to stabilize the LNA.

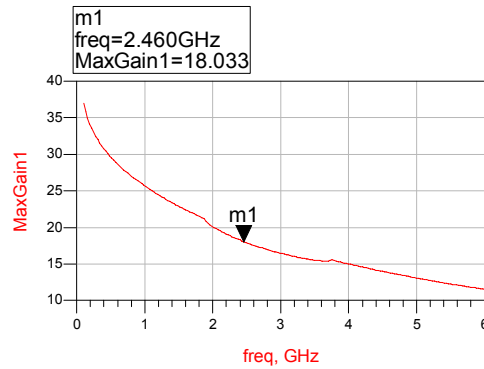
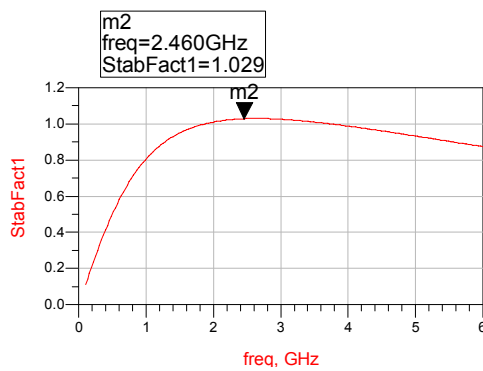
The most common method to stabilize a system is to use a negative feedback. Two small inductors are added at both sources of the PHEMT to create the feedback path. Add two inductors and Var to the Schematic as shown



We start with  $L_s = 1$  nH. Simulate and observe the stability factor improvement. The stability factor is still less than one.

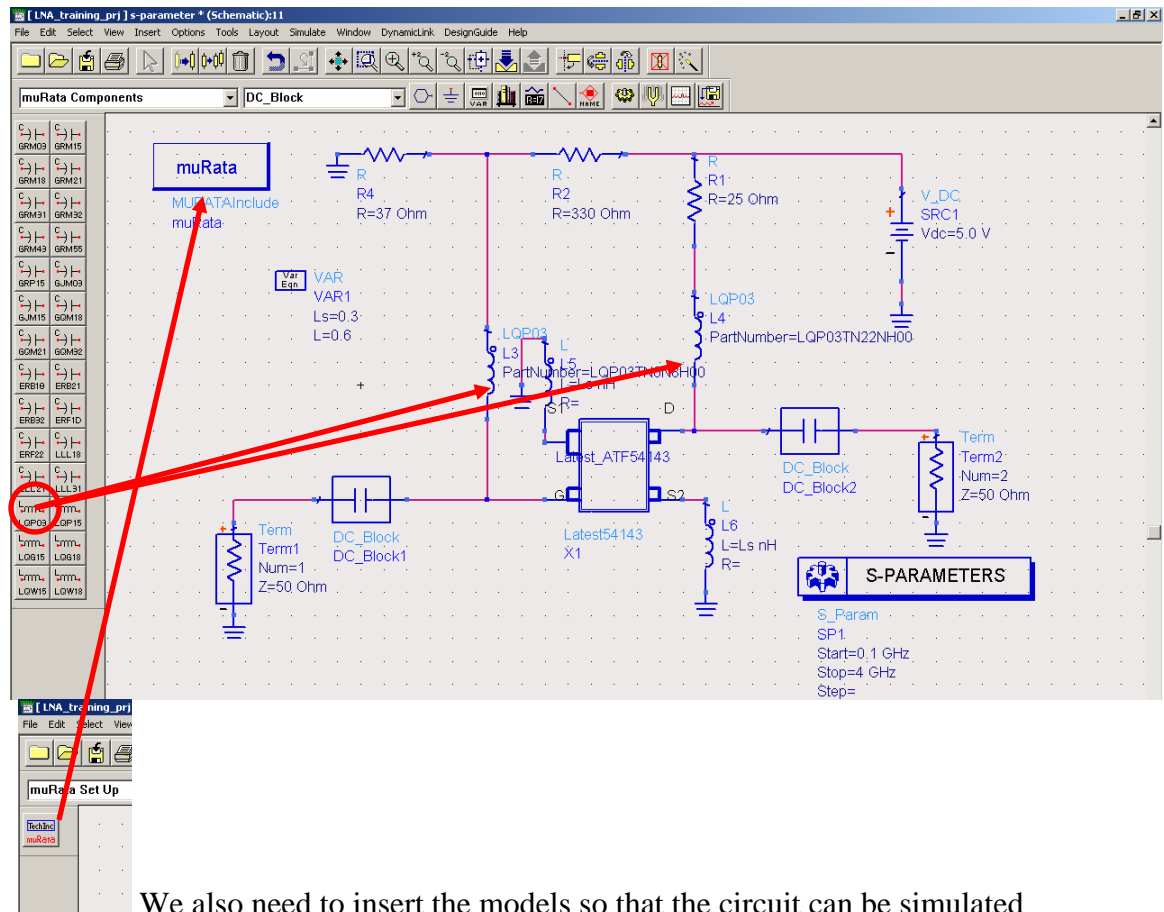


We tweak the feedback inductor further and found the optimum value is about  $L_s = 0.3$  nH.

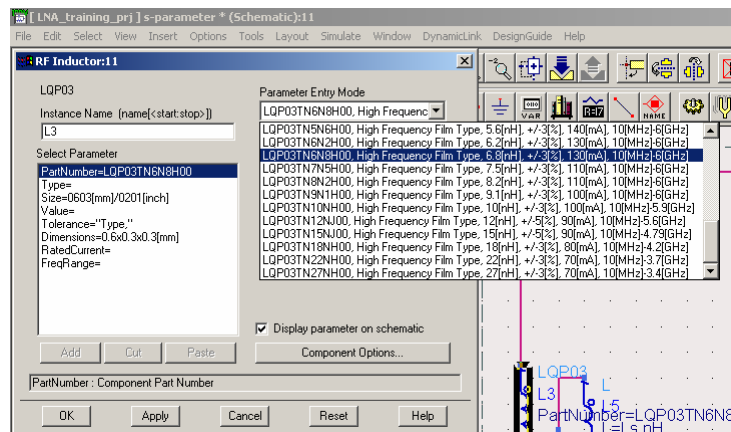


The maximum gain reduces from 21 dB to 18 dB due to negative feedback. Stability problem at low frequency still exists, however.

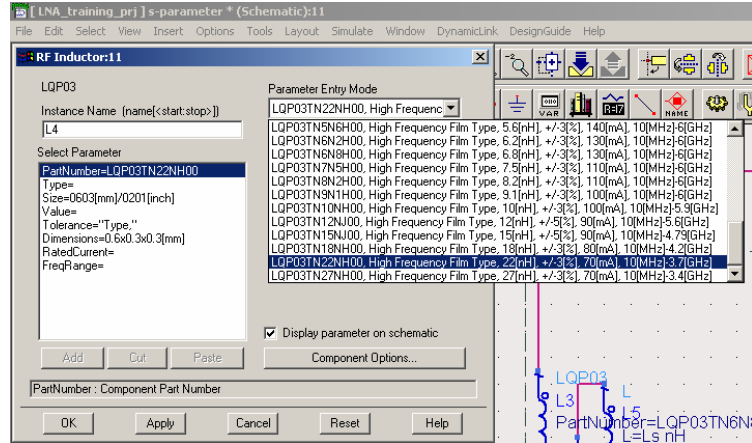
The stability problem at low frequency can be remedied by using small value terminating resistors. We replace the DCFeed ideal components with real inductors. Place Murata Inductors as shown.



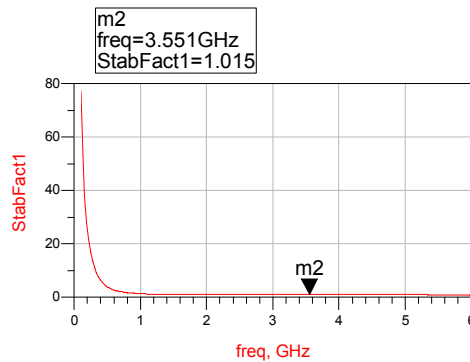
We also need to insert the models so that the circuit can be simulated properly. Double click on the gate inductor and choose 6.8 nH from the drop down list.



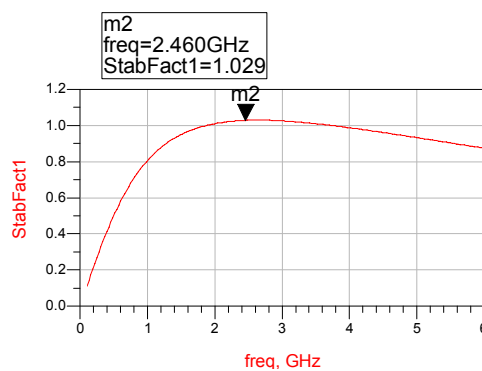
Double click on the drain inductor and choose 22 nH from the drop down list.



Simulate.

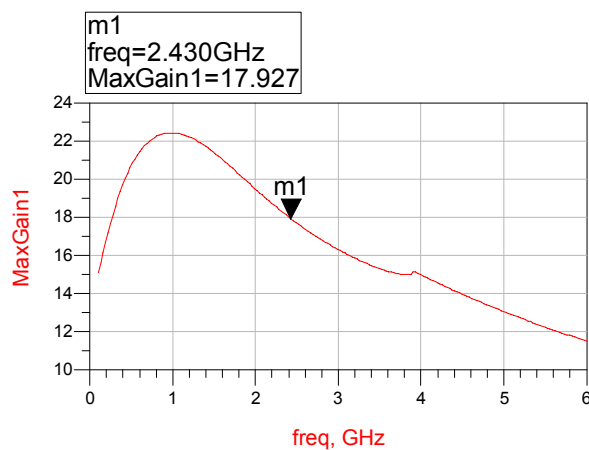


After inserting muRata inductors.



Before inserting muRata inductors.

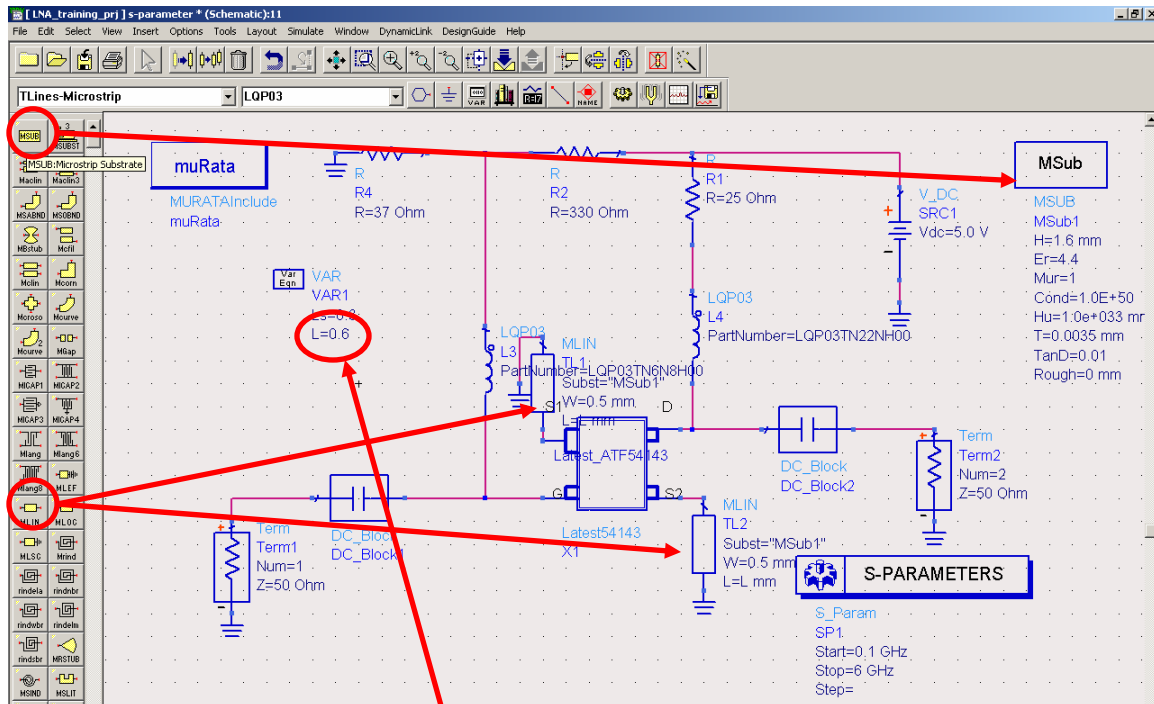
The stability factor improvement at low frequency is obviously seen. The gain reduction can be seen.



We need to replace the ideal inductors at source terminals with real inductors. The inductor value, however, is very small for a lumped component. A small value inductor can be implemented by a high impedance transmission line. There is a formula to approximate the transmission line length for a given inductor value.

$$l = \frac{11.81L}{Z_0\sqrt{\epsilon_r}}$$

Where  $l$  = length in inches and  $L$  = inductance in nH. We, however, can place a transmission line and let the simulator determine the proper length. Insert two transmission lines with the length of  $L$  at the source terminals.

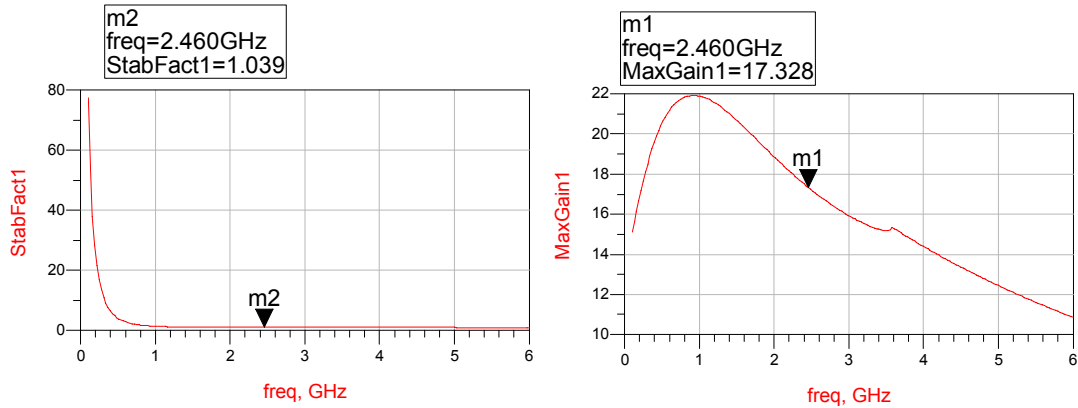


Insert a substrate into the schematic and edit all parameters as shown. These values are for standard FR4 material. Add  $L=0.6$  into Var.

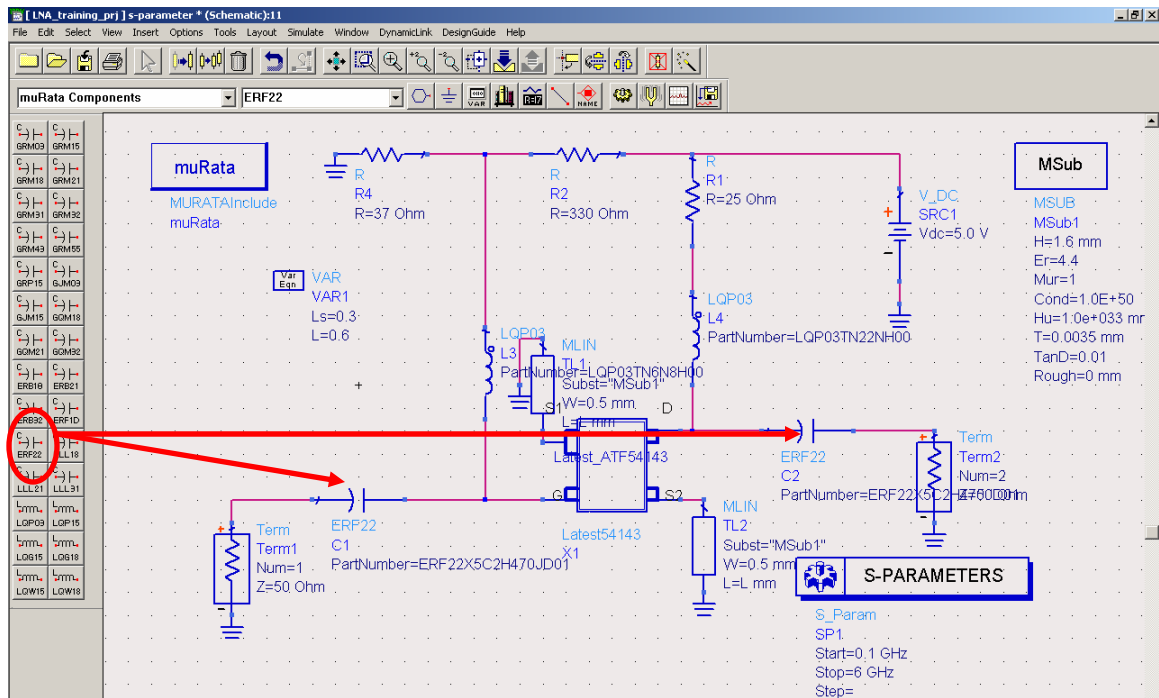
MSUB

MSUB  
MSUB1  
H=1.6 mm  
Er=4.4  
Mur=1  
Cond=1.0E+50  
Hu=1.0e+033 mm  
T=0.0035 mm  
TanD=0.01  
Rough=0 mm

Simulate.

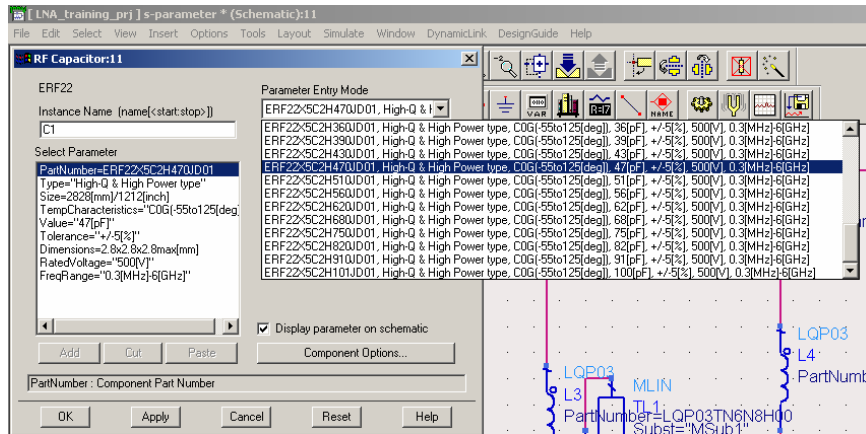


Stability factor and gain are ok. We can now replace ideal DC\_block with real capacitors. Replace DC\_blocks with muRata series ERF22 capacitor.

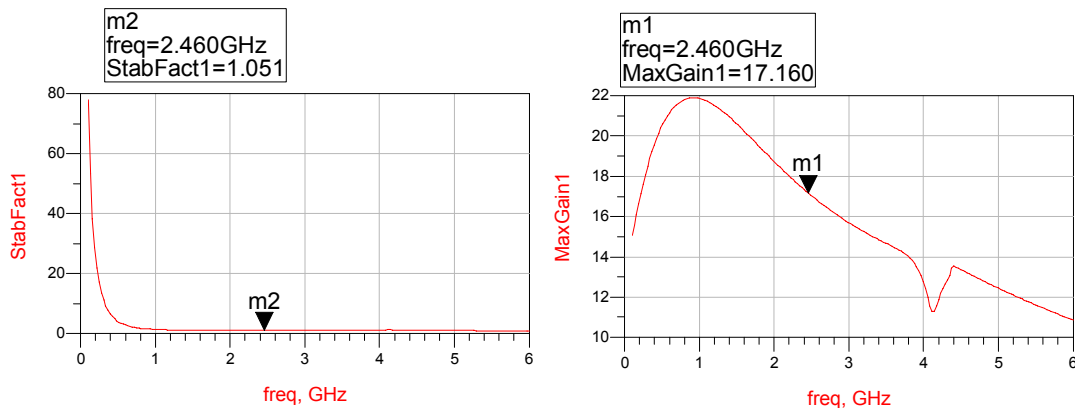




Double click on the capacitor. Choose the capacitor value of 47pF for both coupling capacitors.



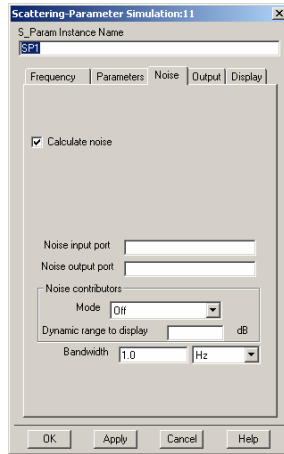
Simulate.



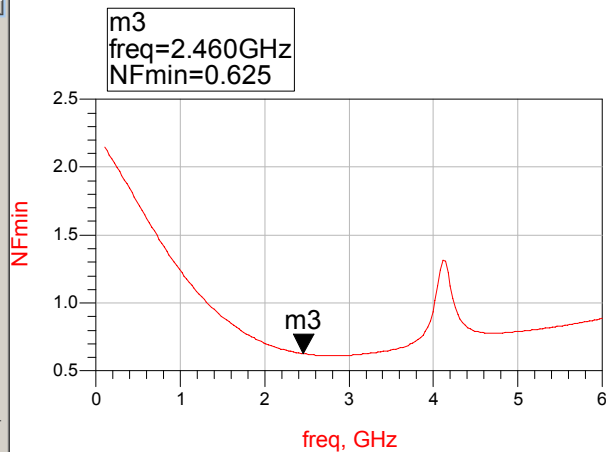
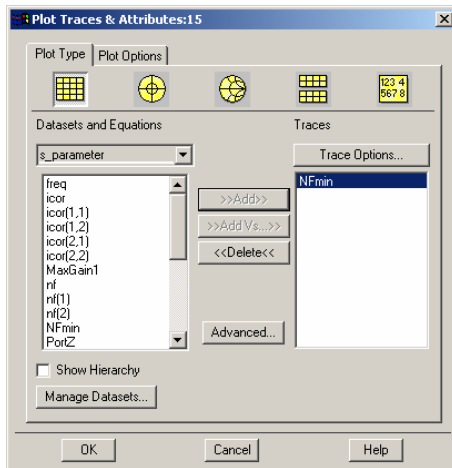
Stability factor and gain is ok after all real components have been added.

## Noise Circle and input matching

1. To simulate noise, we need to enable noise in S-parameter simulator controller. Double click on S-parameter controller. Choose noise tab and enable noise simulation.

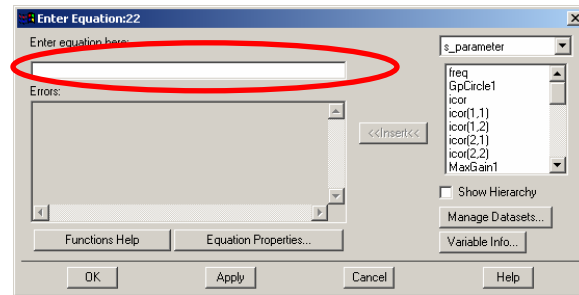
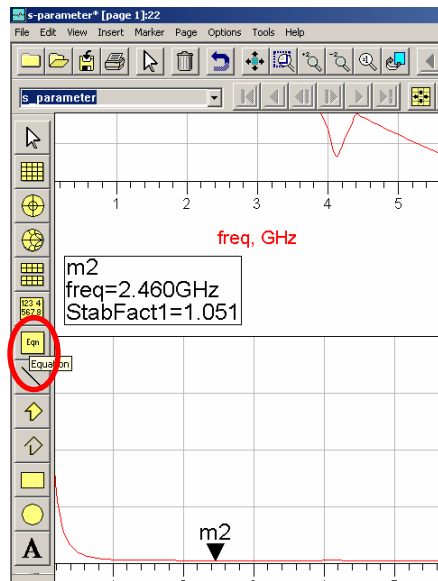


Simulate and plot NFmin using a rectangular plot.



It can be seen that the minimum NF is about 0.625 dB at 2.46 GHz. Next we need to determine a proper input matching network to achieve the minimum NF.

2. Add the following equation in the data display by Clicking on Eqn and Enter the expression into the box.

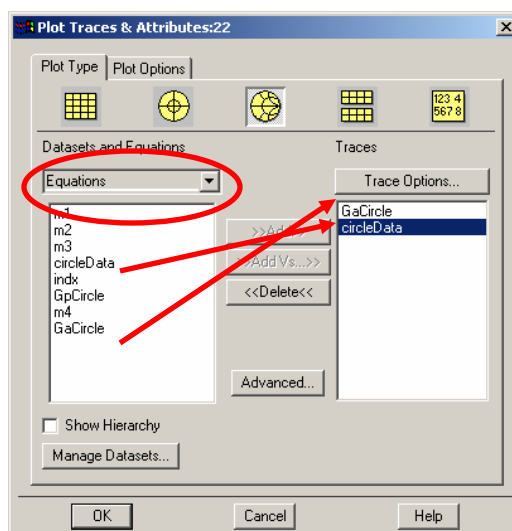
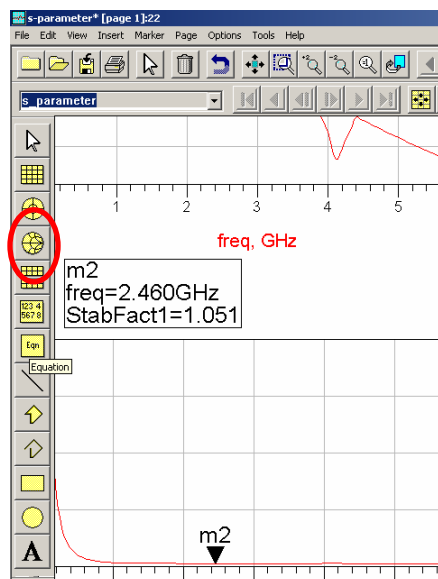


**Eqn**  $\text{indx} = \text{find\_index}(\text{SP.freq}, \text{indep}(\text{m1}))$

**Eqn**  $\text{circleData} = \text{ns\_circle}(\text{NFmin}[\text{indx}] + \{0, 0.1, 0.2\}, \text{NFmin}[\text{indx}], \text{Sopt}[\text{indx}], \text{Rn}[\text{indx}]/50, 51)$

**Eqn**  $\text{GaCircle} = \text{ga\_circle}(\text{S}[\text{indx}], \text{MaxGain1}[\text{indx}] - \{0, 0.5, 1, 2, 3\}, 51)$

The expression “ $\text{indx} = \text{find\_index}(\text{SP.freq}, \text{indep}(\text{m1}))$ ” returns the index of Freq (frequency) when we move the marker m1. You can use any maker as an index controller. Move the maker m1 to 2.46 GHz point and plot NF Circle and Ga Circle. Click on Smith Chart plot and add GaCircle and circleData from Equation dataset.



```

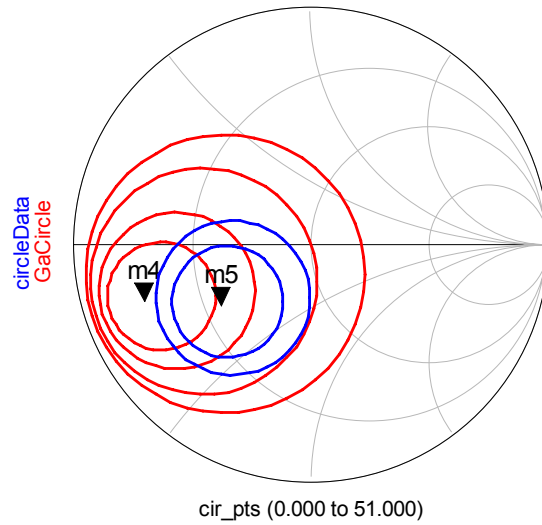
m5
indep(m5)=51
circleData=0.460 / -145.305
ns figure=0.624581
impedance = Z0 * (0.400 - j0.266)

```

```

m4
indep(m4)=51
GaCircle=0.745 / -160.771
gain=17.159538
impedance = Z0 * (0.151 - j0.166)

```



It can be seen that the optimum point for gain (m4) and NF (m5) are located at different location. We need to sacrifice gain for the optimum NF. Let us consider the next constant gain circle.

```

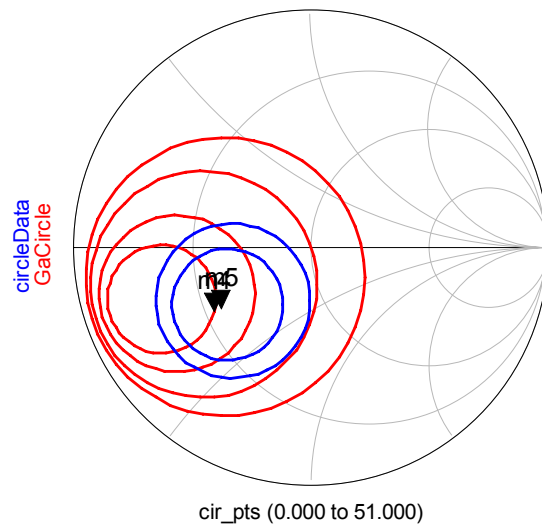
m5
indep(m5)=51
circleData=0.460 / -145.305
ns figure=0.624581
impedance = 20.007 - j13.310

```

```

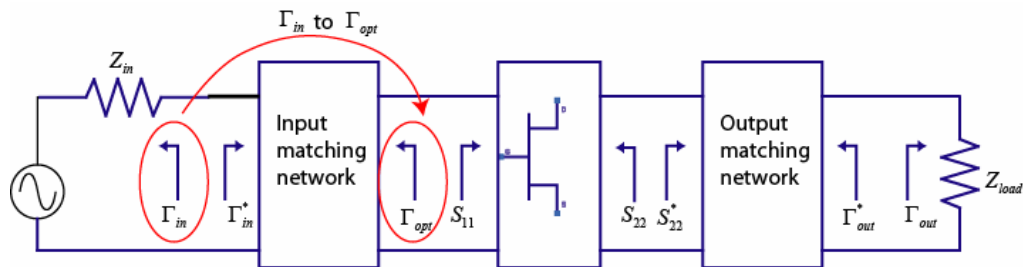
m4
indep(m4)=49
GaCircle=0.493 / -146.017
gain=16.659538
impedance = 18.372 - j13.371

```



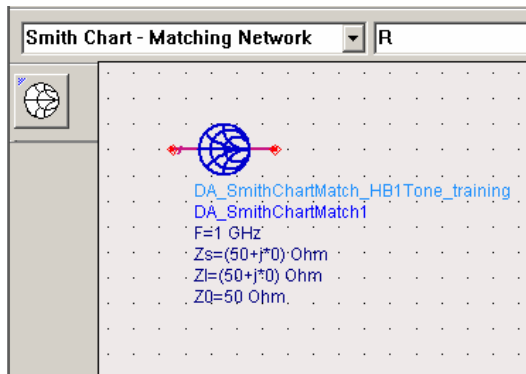
At 16.65 dB constant gain circle, the optimum NF can be obtained. Hence, the optimum source impedance is 20.007-j13.310 ohms.

To obtain the optimum NF,  $\Gamma_{opt}$  needs to present at the input of the PHEMT. This can be achieved by transforming the input impedance (50 ohms) to  $\Gamma_{opt}$  (20.007-j13.310 ohms).




We will use a utility called DA\_SmithChartMatch in the ADS.

3. Place smith chart design assistance from Smith Chart-Matching network.



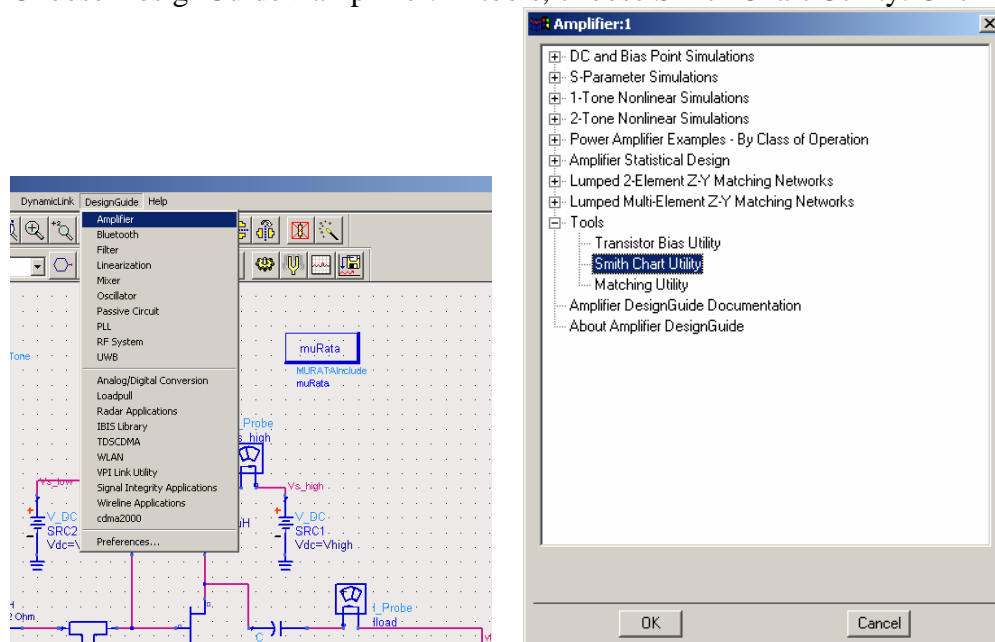
Desired impedance side



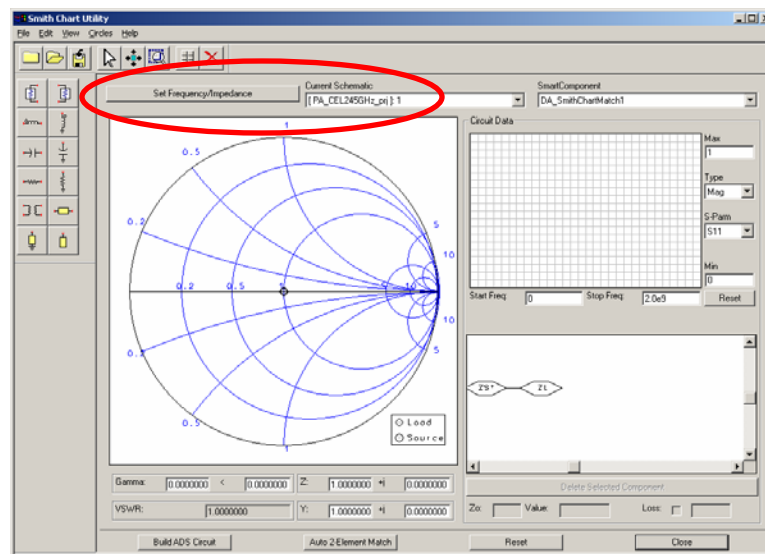
DA\_SmithChartMatcl  
DA\_SmithChartMatcl  
F=1 GHz  
Zs=(50+j\*0) Ohm  
Zl=(50+j\*0) Ohm  
Z0=50 Ohm

Load/source impedance side

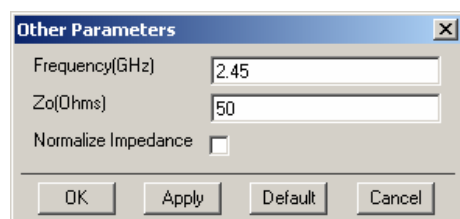
Choose DesignGuide->amplifier. In tools, choose Smith Chart Utility. Click OK.



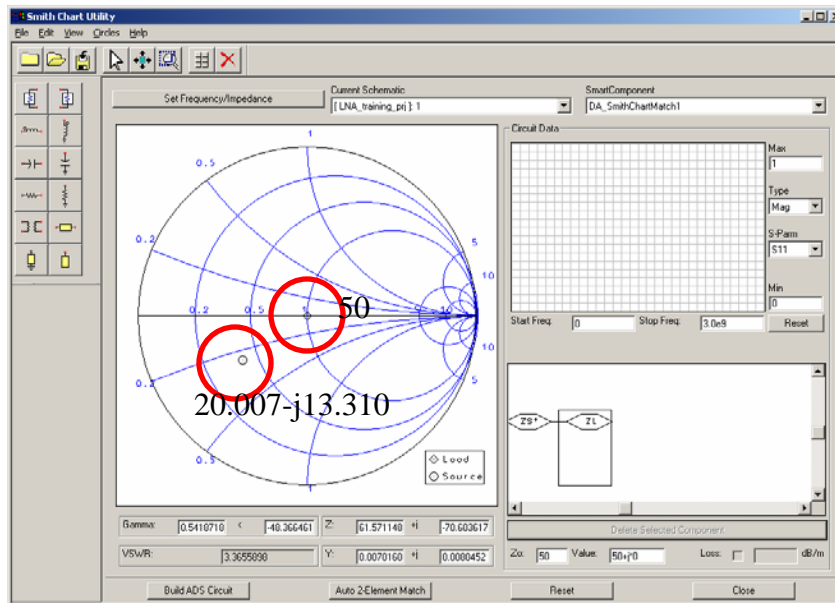
A smith chart utility window will be shown.




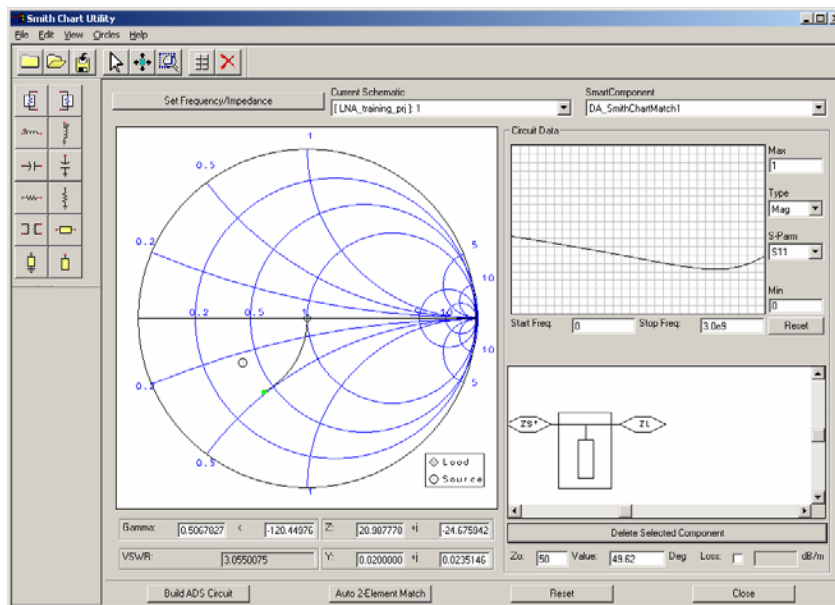
Set Frequency to 2.45 MHz,  $Z_o = 50$  Ohms and uncheck Normalize impedance. Click OK.



Set source and load impedance to  $20.007-j13.310$  ohms and  $50$  ohms respectively.

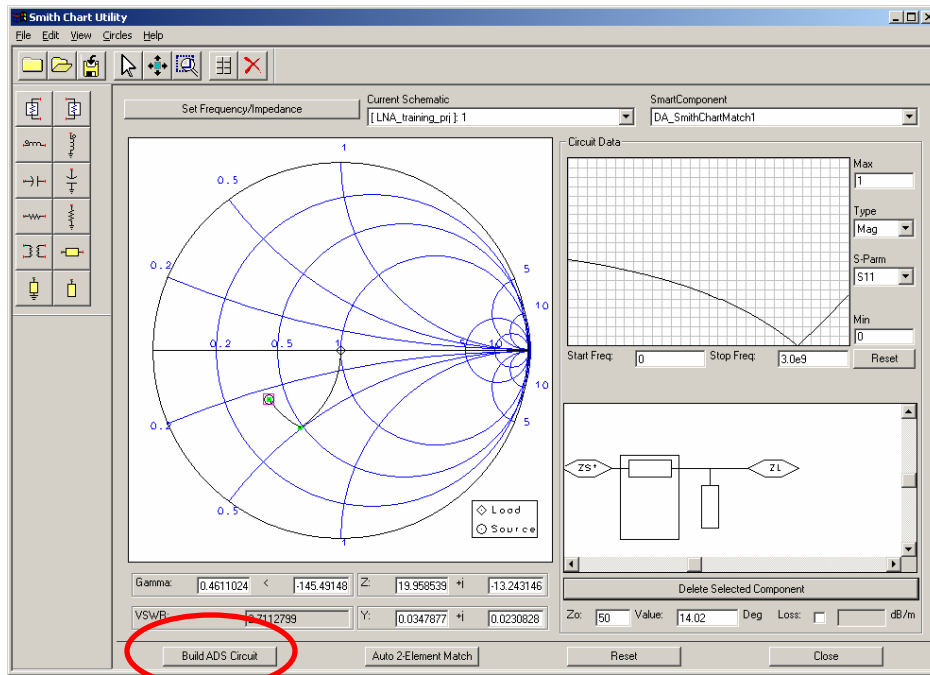


Place matching components. Start with shunt open-transmission line . Drag the end point to a point closed to source impedance.





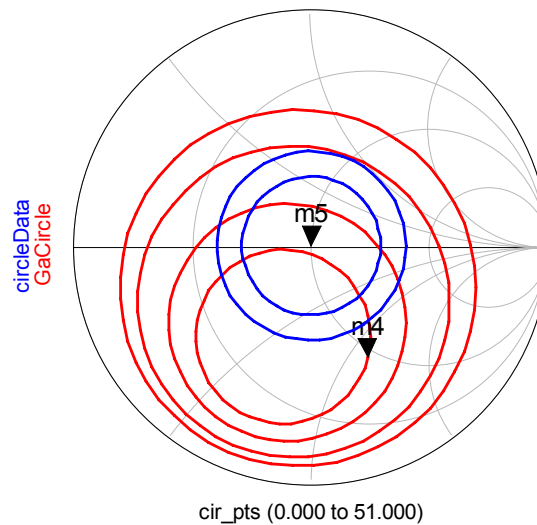
Next add a transmission line and drag the end point to the source impedance. Click Build ADS circuit.



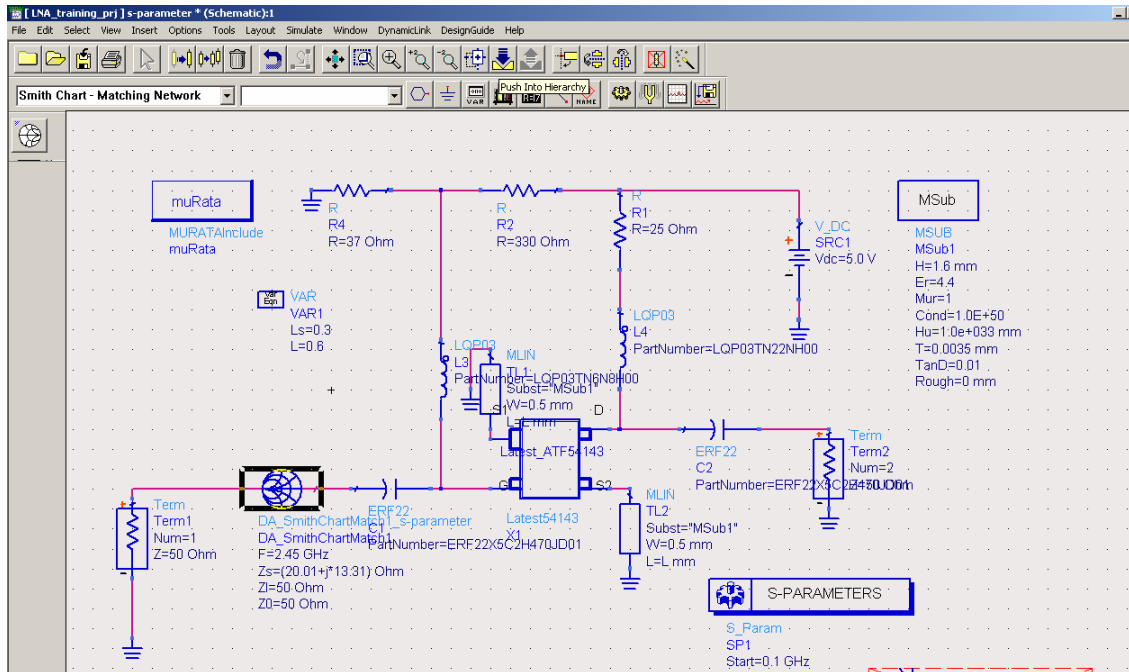
Simulate. Now, the 50 ohms point is an optimum point for NF.

```
m5
indep(m5)=51
circleData=0.006 / 66.797
ns figure=0.624581
impedance = 50.235 + j0.558

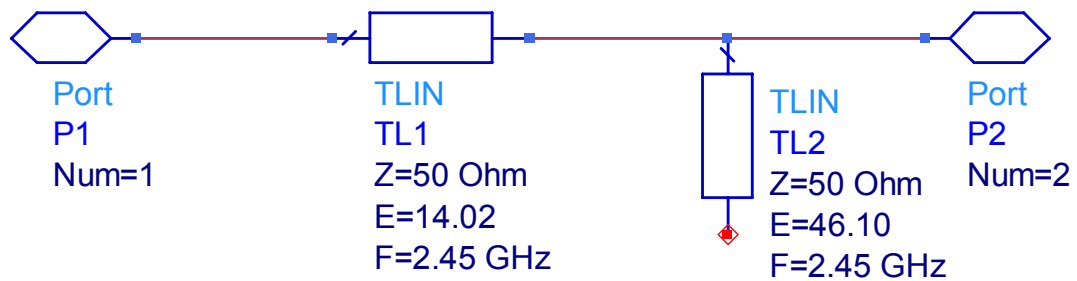
m4
indep(m4)=49
GaCircle=0.527 / -62.809
gain=16.659538
impedance = 45.351 - j58.901
```



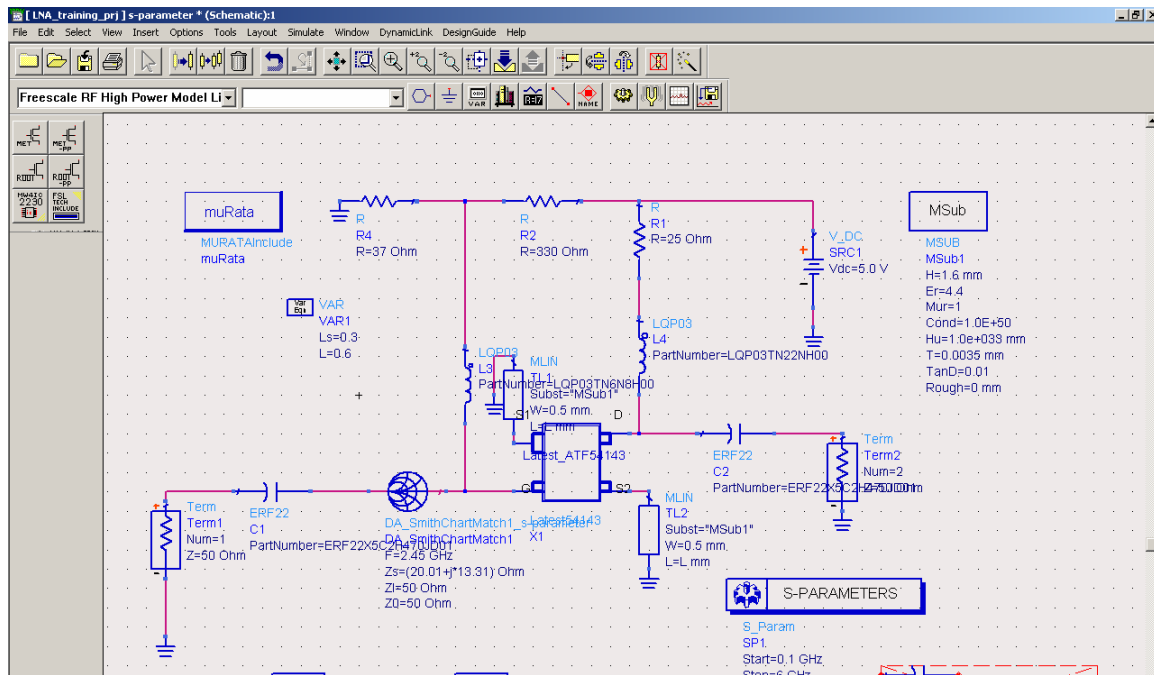
We can use “Push Into Hierarchy” to see the implementation of the matching network.



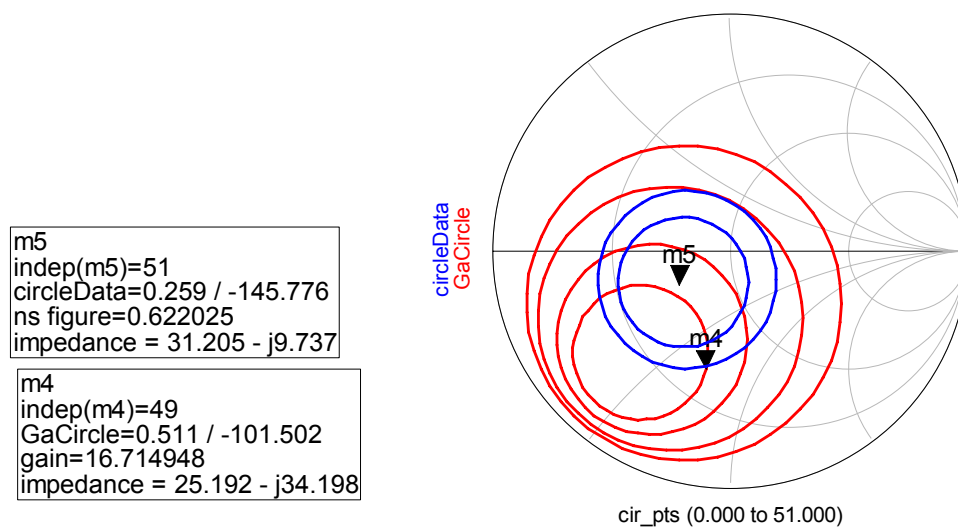
The figure below shows the matching elements.



The coupling capacitor at the input will cause a complication in circuit construction. We need to move the coupling capacitor to the source. Swap the coupling capacitor and the matching network as shown and simulate.

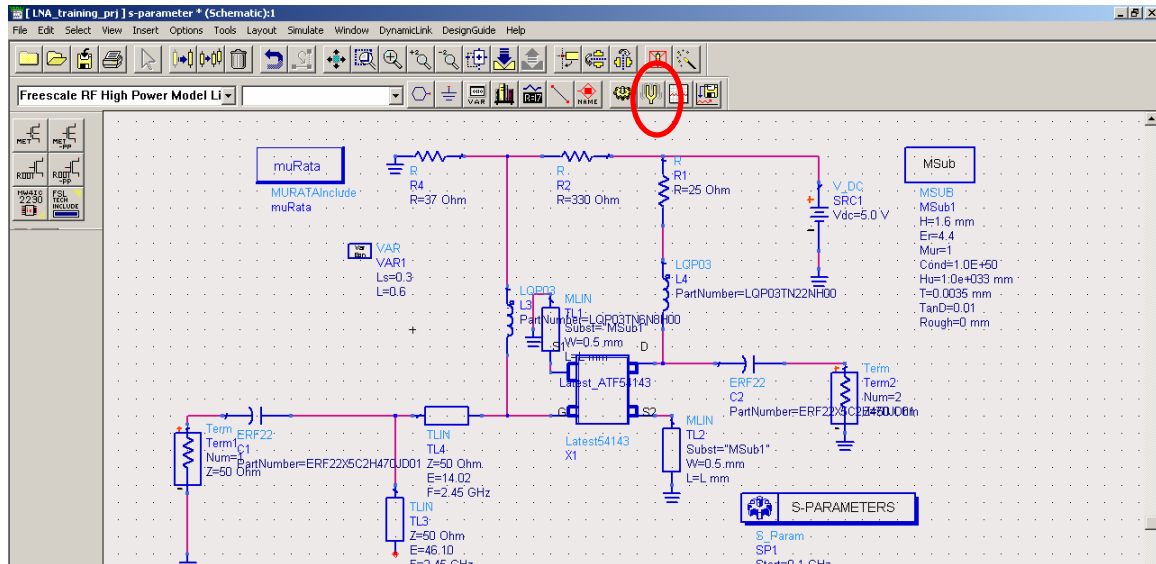


After the capacitor is swap, the optimum point has been off from the 50 Ohm.

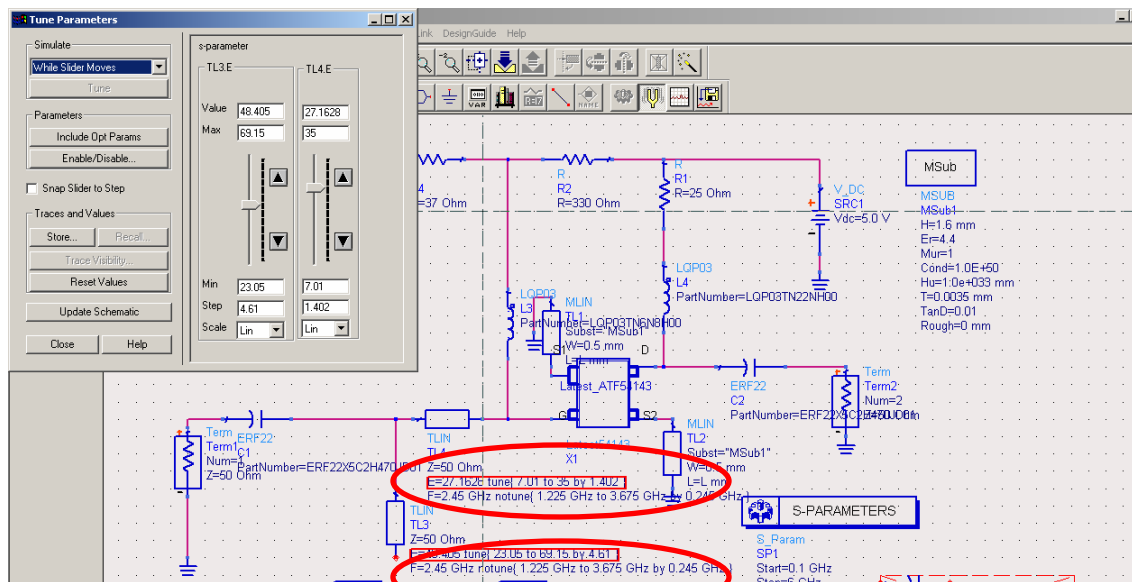


We need to change to length of the transmission line to compensate this change.

For convenient, we copy the section of transmission lines from the DA to the schematic as shown.

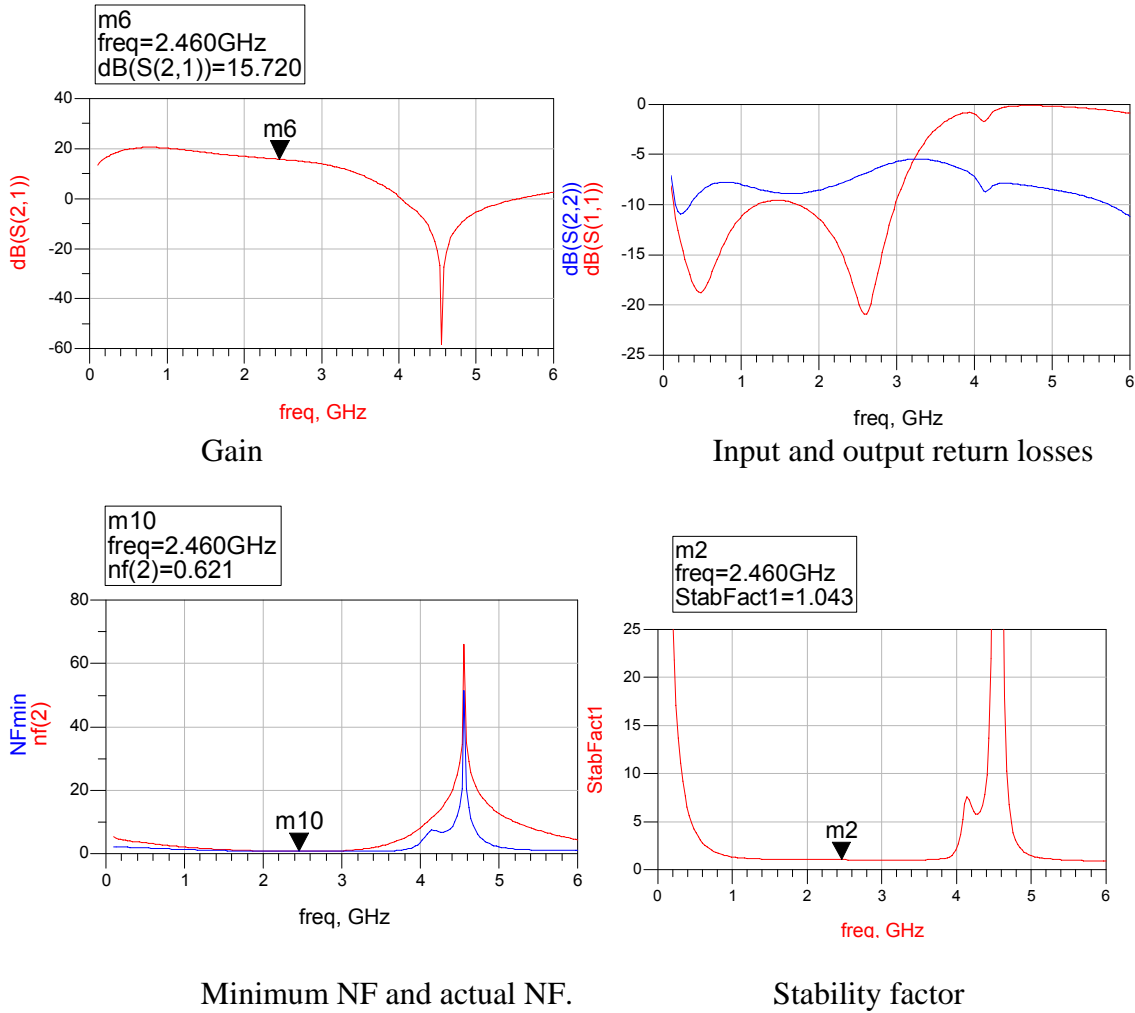


We now use a tuning tool to adjust the length of transmission lines. Click on  and click on both electrical length of the transmission lines.



At tune Parameters window, the transmission line length can be changed and we can see the result interactively.

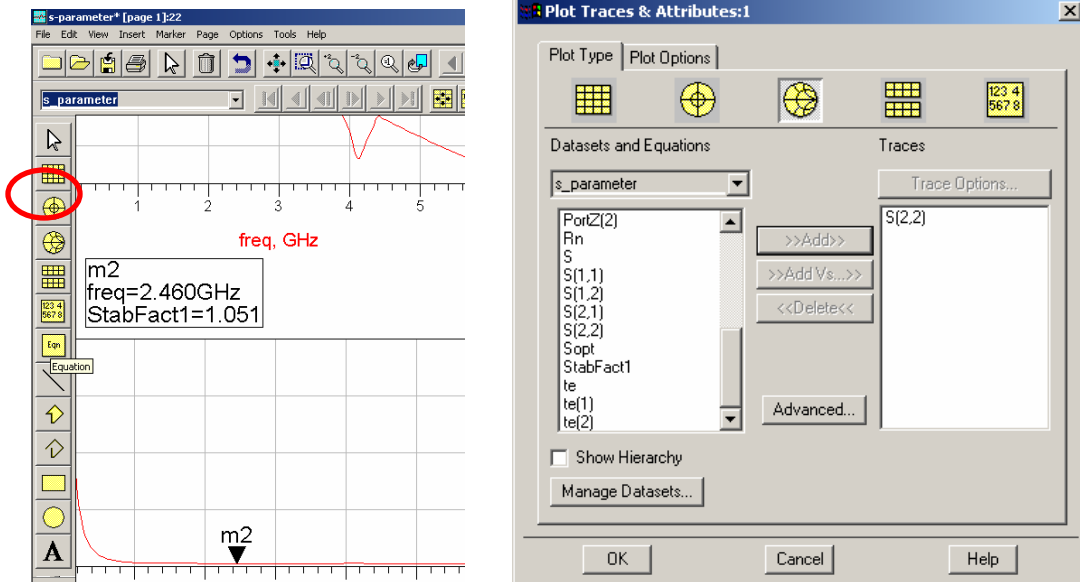
The optimum length for TL4 and TL3 are 27.1628 and 48.405 degrees respectively. The results of Gain, output return loss, output return loss NF and stability factor are shown in the figure below.



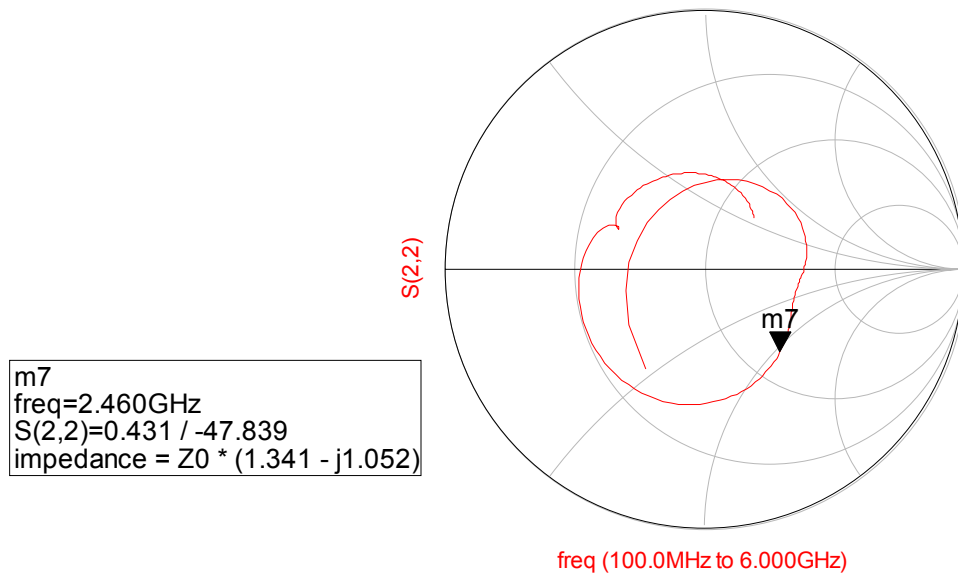
Gain can be improved by the output matching networks. In a LNA, the output matching network will not interfere with the NF. Only input impedance influence the NF.

## Output Matching for Gain

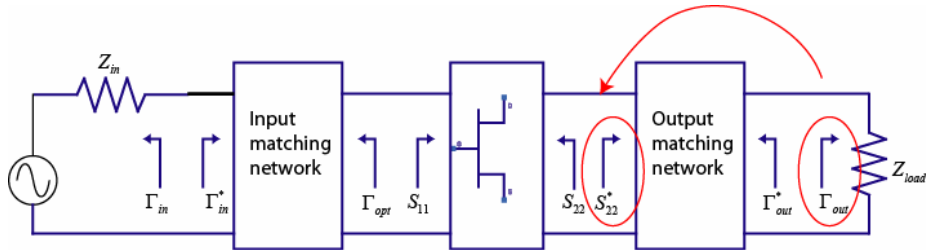
1. Plot S22 on a smith chart. Click on smith chart plot. In Plot Traces & Attributes Window, add S(2,2) to trace, click OK.



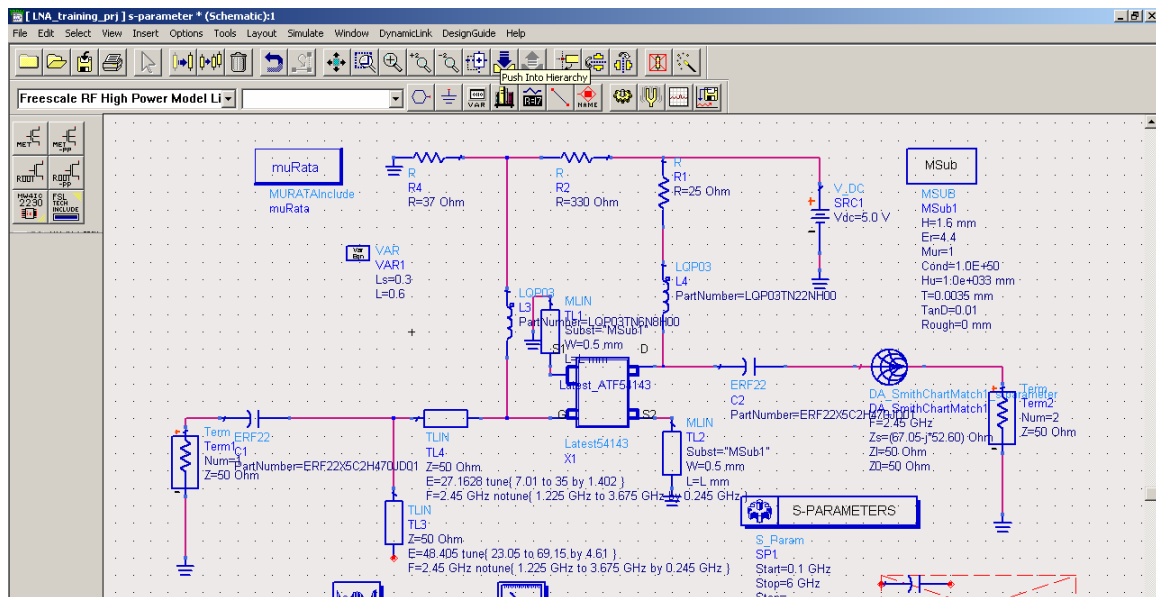
Add a Marker to S22 plot.



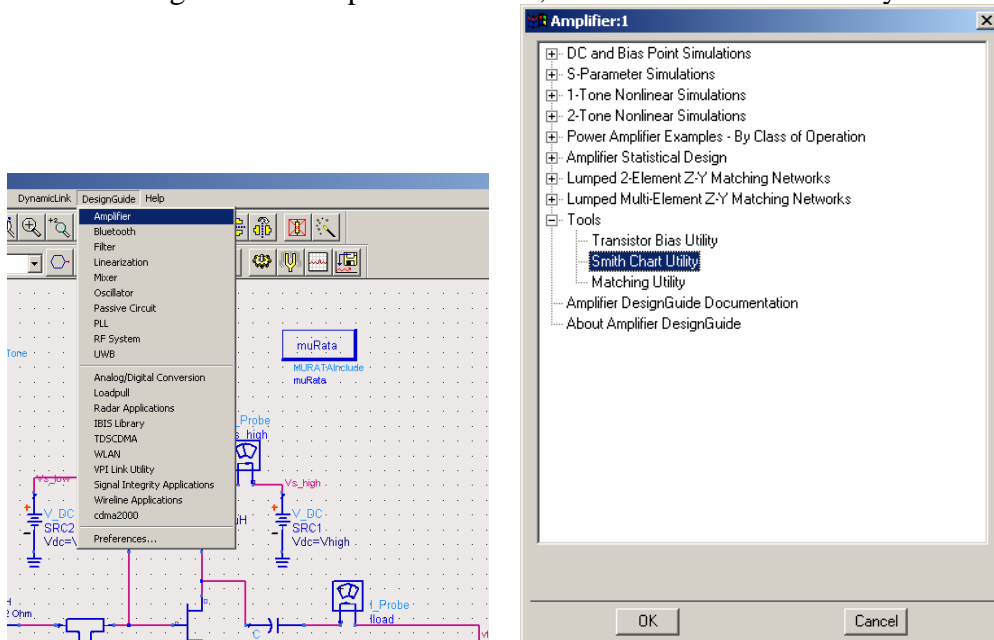
To achieve the maximum gain, we need to match 50 ohms to conjugate  $S_{22}$ .



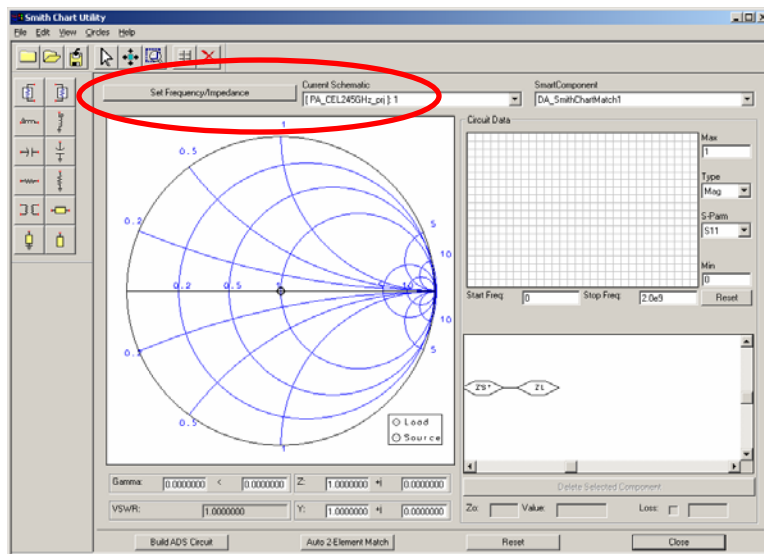
We shall re-use DA\_smithChartMatch in input matching part. Place the DA\_smithChartMatch as shown. Be careful about the direction of the DA\_smithChartMatch.



Choose DesignGuide->amplifier. In tools, choose Smith Chart Utility. Click OK.

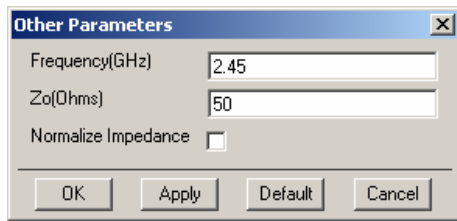


A smith chart utility window will be shown.

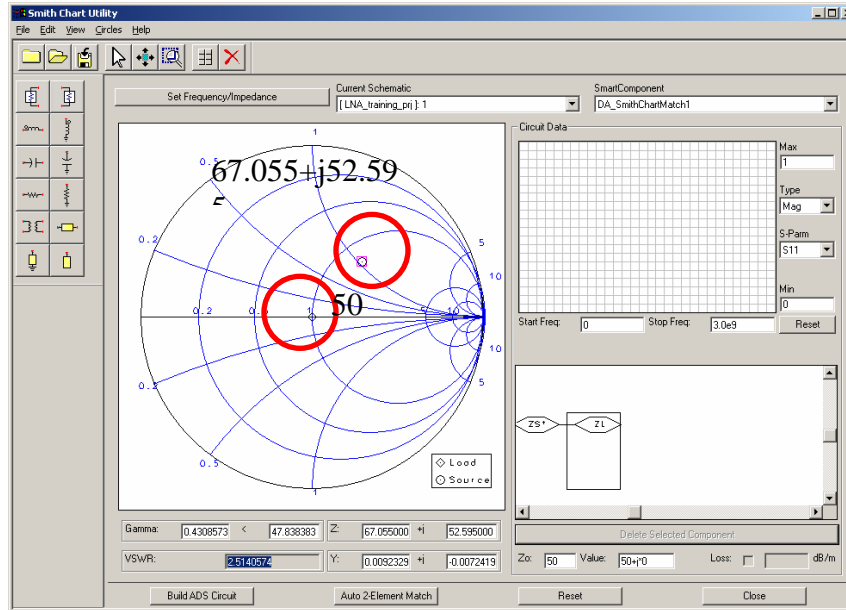



Set Frequency to 2.45 MHz,  $Z_o = 50$  Ohms and uncheck Normalize impedance. Click OK.

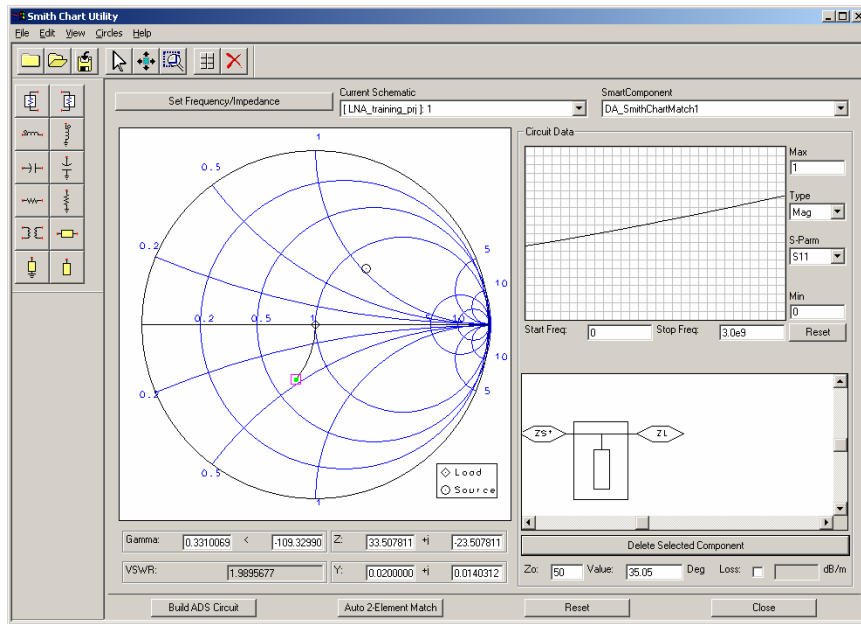




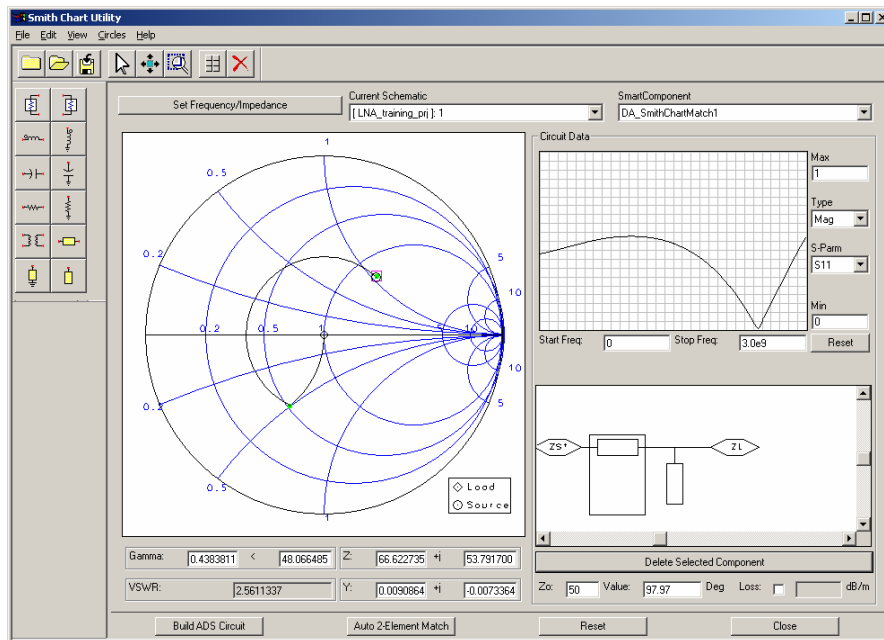
Set source and load impedance to  $67.055 + j52.595$  ( $S_{22}^*$ ) ohms and 50 ohms respectively.



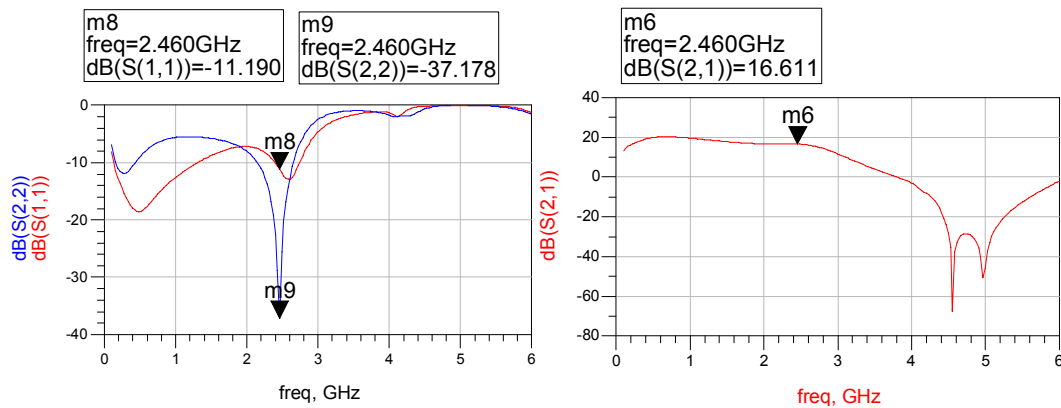
Place matching components. Start with shunt open-transmission line . Drag the end point as shown.



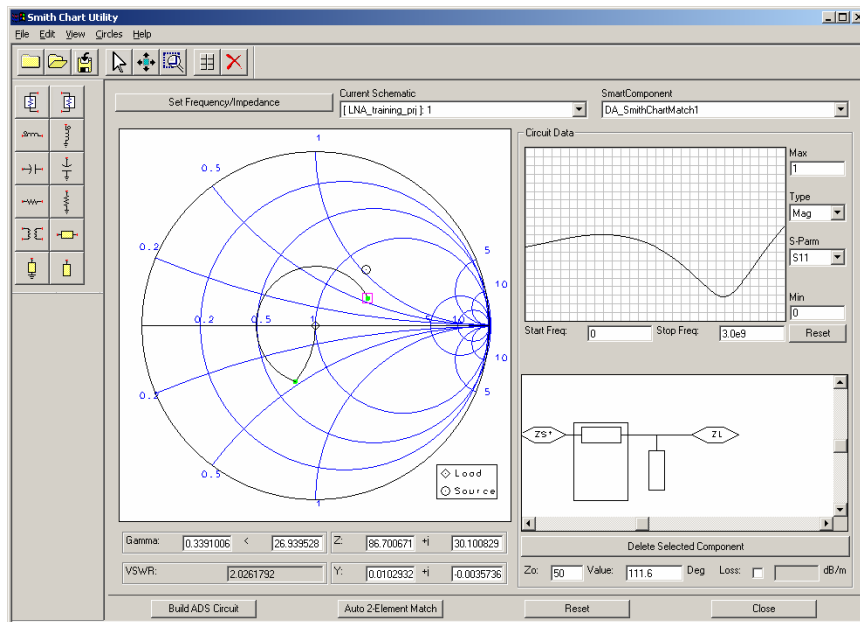
Add a section of transmission line and drag both points until the end point is at the source impedance. Click Build ADS Circuit.



Simulate.

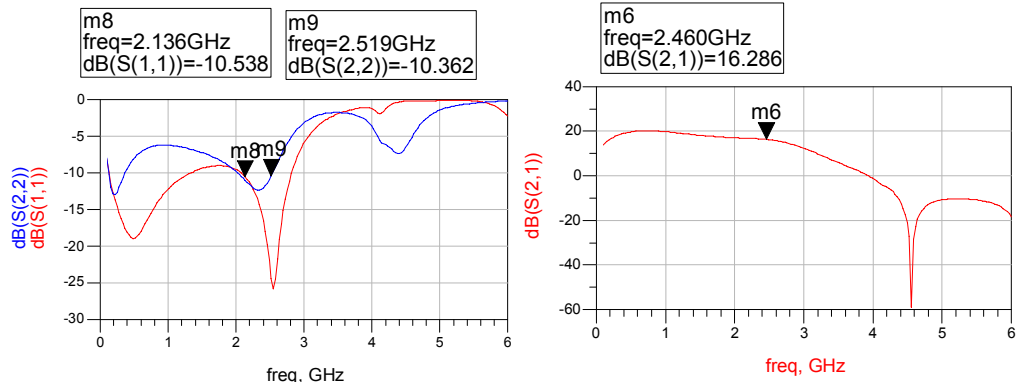


It can be seen that the output return loss is very good but the input return loss get worse. The input return loss can be improved by mis-match the output a little. Back to Smith Chart Utility window and try to mis-match the output.



After the output matching network is changed as shown, we re-simulate to see the improvement

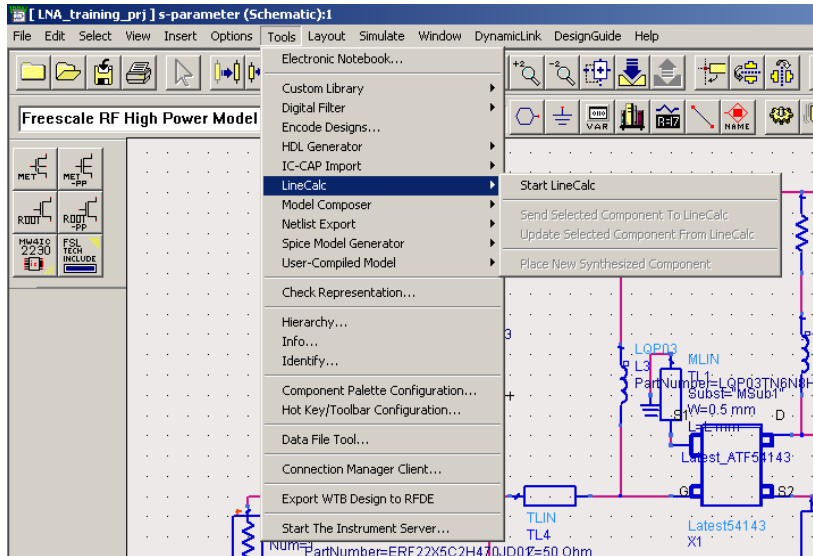




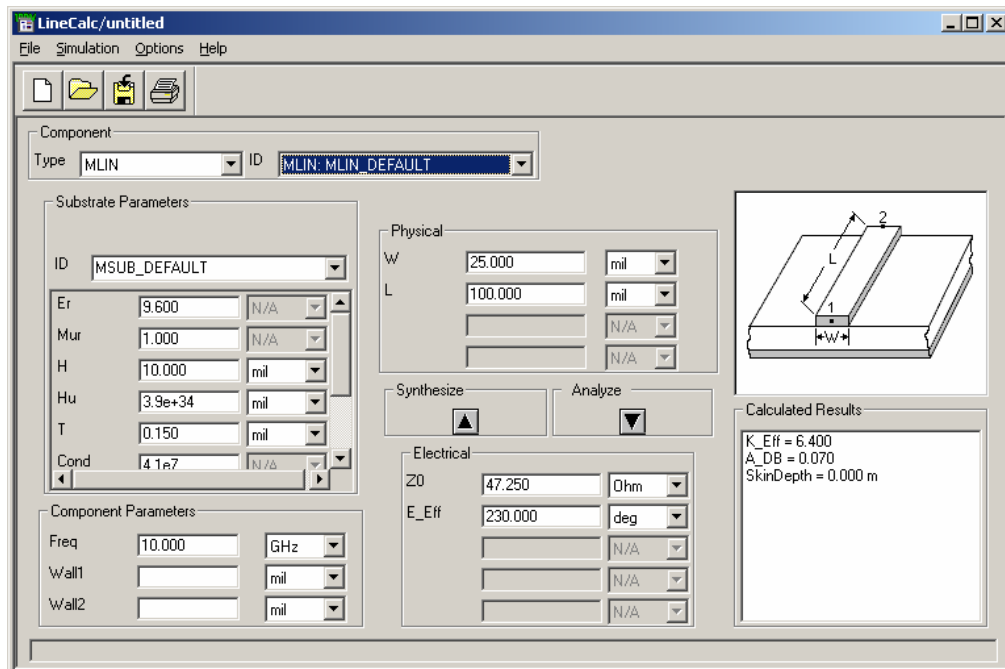
Both input and output return losses are less than -10dB at 2.46 GHz and gain is about 16 dB. Hence, there is no need to tune the output matching network.

## Matching network implementation

The ideal matching networks are implemented using microstrip transmission lines. In ADS, there is a very useful tool called lineCalc. Various types of transmission line can be designed by using this tool. To use the LineCalc, go to tools-> lineCalc-> Start LineCalc.



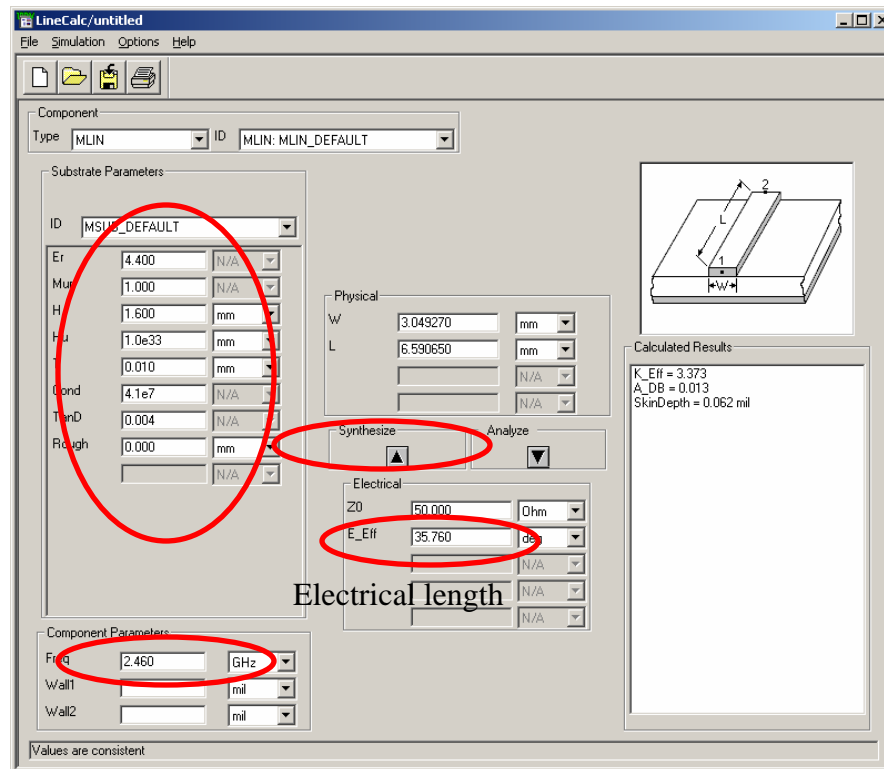
The LineCalc Tool is shown in figure below.



All microstrip lines and their electrical length are listed below. The physical length will be determined using the LineCalc.

	Electrical length (degrees)	Physical length (mm)
TR3	48.405	
TR4	27.163	
TR5	35.79	
TR6	111.6	

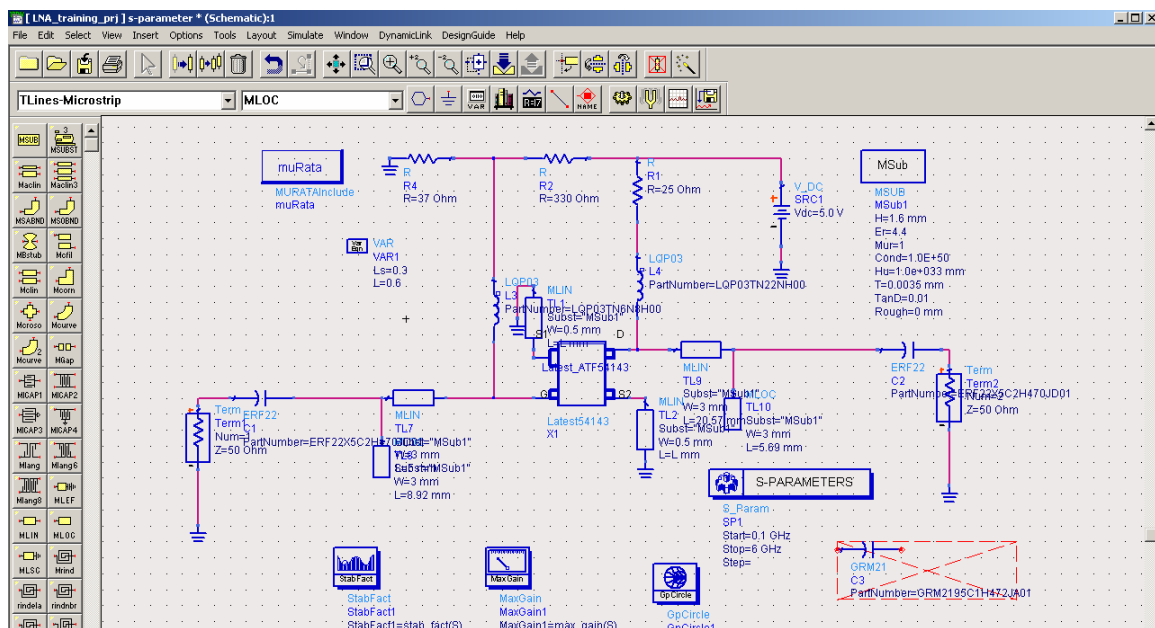
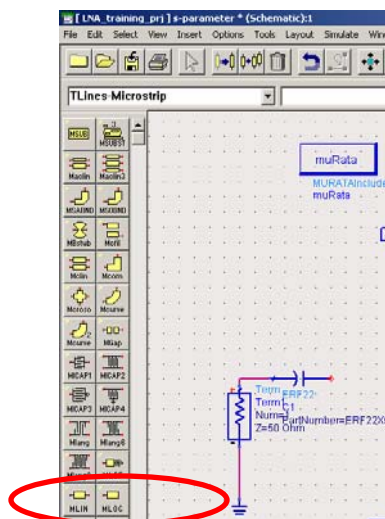
Change parameters in the LineCalc tool as shown



We set the substrate parameter to match the FR4 material and change to frequency to 2.46 GHz. Change the electrical length (E\_Eff) to the value in table above and click Synthesize to obtain the physical length. For example, 35.760 degrees of electrical length is 6.59 mm. Repeat this step for all ideal microstrip lines. The physical length of all microstrip lines are shown below.

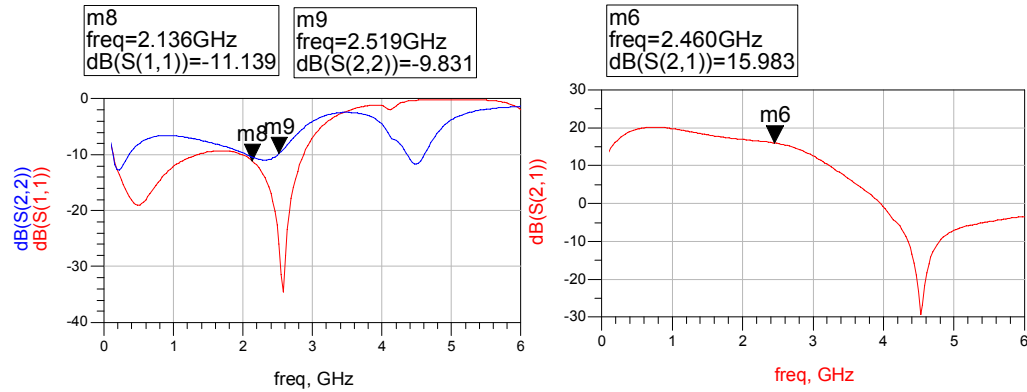
	Electrical length (degrees)	Physical length (mm)
TR3	48.405	8.92
TR4	27.163	5.00
TR5	35.79	5.69
TR6	111.6	20.57

Back to schematic window, replace all ideal transmission lines with the microstrip lines on FR4 as shown.

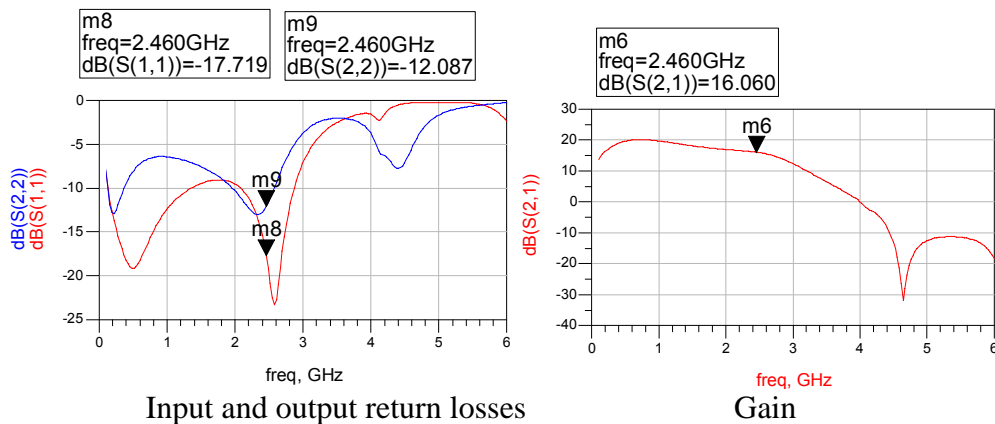




Simulate,

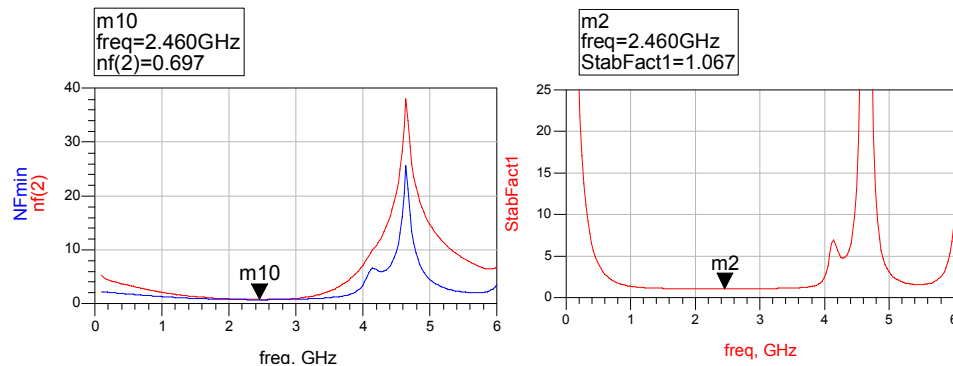


Input return loss is worse than the ideal matching components. The matching networks can further tweak for the optimum values. After the tuning, all parameters are shown below.



Input and output return losses

Gain



Minimum NF and actual NF.

Stability factor

The final parameters at 2.46 GHz are, gain > 15 dB, NF < 1 dB, input and output VSWR < 1:2 and unconditionally stable.