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Characteristics of an Extended Drain N-Type MOS Device for Electrostatic Discharge Protection of a LCD Driver Chip Operating at High Voltage

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We have evaluated the effects of the background doping concentration (BDC) on electrostatic discharge (ESD) protection by using an extended drain N-type metal oxide semiconductor (EDNMOS) field effect transistor device operating at high voltage. The EDNMOS device with low BDC suffers from strong snapback in the high current region, which results in poor ESD protection and high latchup risk. However, the strong snapback can be avoided in the EDNMOS device with high BDC. This implies that both good ESD protection and latchup immunity can be realized in terms of the EDNMOS by properly controlling its BDC. As a result of transmission line pulse (TLP) test, an ESD current immunity level of 5.08 mA/um and a good linear scaling behavior were achieved for a multi-finger-type device.

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I. INTRODUCTION

Electrostatic discharge (ESD) protection is a major concern in microchips operating at high voltage [1, 2]. Stable ESD protection is hardly achieved in terms of N-type metal oxide semiconductor field effect transistor (MOSFET) devices operating at high voltage. Their drawback to the ESD stress is attributed to the extremely strong snapback, which results in current crowding and melting damage, non-uniform multi-finger triggering, and high latchup risk [3–5]. Extensive work has been devoted to achieving stable ESD protection, but ended with only limited success [6–9].

The conduction mechanisms in the high-current region must be understood in order to realize stable ESD protection in these devices. Recently, double diffused drain n-type MOSFET (DDDNMOS) devices operating at high voltage were exhibit double snapback, where the 2nd on-state was characterized by a very low snapback holding voltage [10]. A related mechanism is known to be high-electron-injection-induced base push-out [11,12]. Since base push-out happens when the injected electron density overwhelms the background carrier densities, the background doping concentration (BDC) may be a critical factor in the occurrence of the double snapback phenomenon. Thus, the effects of the BDC on the current-voltage (I-V) characteristics of N-type MOSFETs operating at high voltage need to be evaluated. This paper, focusing on an optimization methodology for ESD protection, presents the effects of the BDC in an extended drain N-type MOSFET (EDNMOS) device, which is one specific type of DDDNMOS device.

II. DEVICE STRUCTURE AND SIMULATION

The EDNMOS device operating at high voltage is characterized by a double diffused drain structure and non-adjacency of the gate to the drain N+ diffusion, as shown in Fig. 1. The background of the EDNMOS device consists of a high voltage P-type well (HP-well) region and an N-drift region. When the EDNMOS device is used for ESD protection, the drain N+ diffusion is connected to the Vdd power pad (or to each I/O pad) while the gate, the source, and the well-pickup are all tied together and connected to the Vss ground pad.

The high-current characteristics of the EDNMOS devices are investigated using thermal-incorporated 2-dimensional simulations. The devices were fabricated

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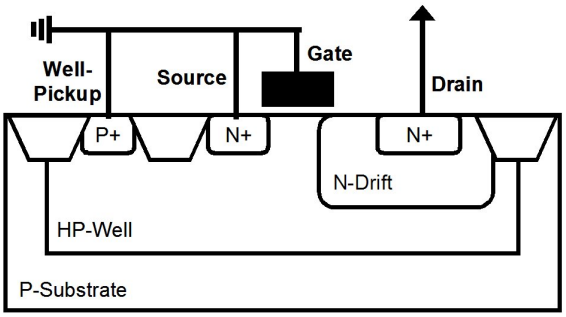

Fig. 1. Schematic diagram of an extended drain N-type MOSFET (EDNMOS) device.

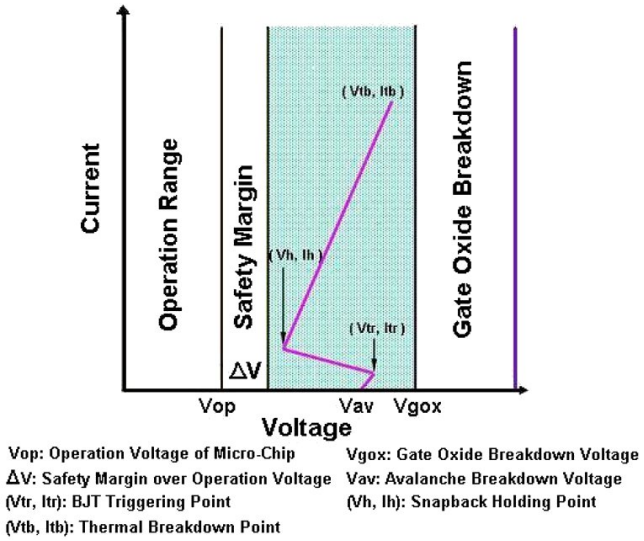

Fig. 2. Design window for the ESD protection device.

Table 1. Requirements for ESD protection.

Requirements for ESD protection
Vop < Vav, Vtr
Vtr, Vtb < Vgox
Vop + △V < Vh
Itb: Large
Vtr ≤ Vtb

using the TSUPREM4 (Synopsys Co.) process simulator following high-voltage operating technology (@0.18 um, 30 V), and their characteristics were analyzed using a DESSIS (ISE Inc.) device simulator. In order to simulate human body model (HBM) ESD stress, we performed mixed mode transient (MMT) simulations, adopting ladder-type current pulses with a rise time of 10 ns and a duration of 100 ns. A transmission line pulse (TLP) test system was used to monitor the high-current response of the EDNMOS devices experimentally [13]. During the measurement, the pulse rise time and the duration were kept at 10 ns and 100 ns, respectively.

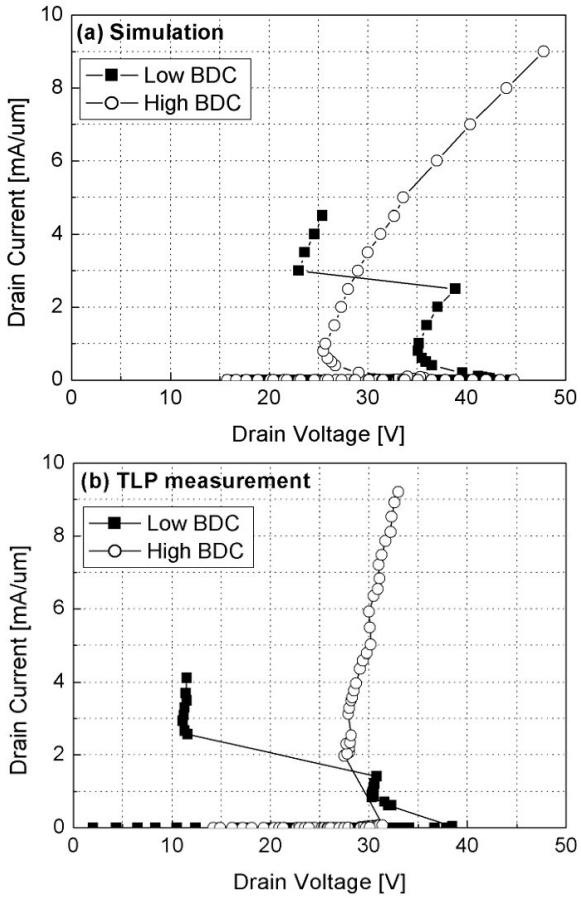

Fig. 3. (a) Simulation results for the I-V relations of 1-finger EDNMOS devices with different background doping concentrations as listed in Table 2 and (b) TLP measurement data of two BDCs.

Table 2. Implant conditions of the background region.

Background	HP-well implant dose	N-drift implant dose
Low BDC	7.5×10^{12} cm^{-2}	1.1×10^{13} cm^{-2}
High BDC	1.7×10^{13} cm^{-2}	4.0×10^{13} cm^{-2}

Fig. 2 shows the design window for the ESD protection device exhibiting triggering, snapback holding, and thermal breakdown points in the I-V characteristics. The key parameter requirements for ESD protection are shown in Table 1.

III. RESULTS AND DISCUSSION

Figs. 3 (a) and (b) show the I-V characteristics of 1-finger structure EDNMOS devices with the two different BDC conditions shown in Table 2. The BDC is shown to be a critical factor in the high-current behavior of the EDNMOS device. The characteristic double snapback phenomenon is seen in the EDNMOS with low BDC

(low BDC: HP-well implant dose = 7.5×10^{12} cm^{-2} and N-drift implant dose = 1.1×10^{13} cm^{-2}). The 2nd on-state is characterized in terms of a low snapback holding voltage, low thermal breakdown current, and a low thermal breakdown voltage much smaller than the triggering voltage. Once the EDNMOS device enters the 2nd on-state with such characteristics, current localization and subsequent melting damage may easily occur, resulting in high vulnerability to the ESD stress. Non-uniform multi-finger triggering and high latchup risk are other problems [3,4].

If the BDC is increased above a certain critical limit (high BDC: HP-well implant dose = 1.7×10^{13} cm^{-2} and N-drift implant dose = 4.0×10^{13} cm^{-2}), the EDNMOS device does not show the double snapback phenomenon. Instead, it just remains within the 1st on-state with a moderate snapback holding voltage, a high thermal breakdown current, and a consequential high thermal breakdown voltage. Thus, both stable ESD protection and latchup immunity are realized in the EDNMOS device with a high BDC.

The high thermal breakdown voltage, comparable to or larger than the triggering voltage, implies uniform multi-finger triggering, which subsequently results in the linearity of the ESD current immunity level with respect to the number of fingers in the EDNMOS device. Both the high thermal breakdown current level and the linearity of the current immunity level in the finger number guarantee stable ESD protection. Moreover, the moderate snapback holding voltage compared to its triggering voltage implies low latchup risk for the given operation voltage applicable to the EDNMOS device with a high BDC.

Both the simulation data (Fig. 3(a)) and the corresponding TLP measurement data (Fig. 3(b)) show qualitatively consistent results, even though there are quantitative mismatches due to poor calibration. It should be noted that the practical usage of this methodology, controlling of BDC for ESD protection, is very limited because the junction breakdown voltage and the consequential operating voltage strongly depend on the BDC. That is to say, a high BDC above a certain critical limit may guarantee stable ESD protection in an EDNMOS device. However, an EDNMOS device with enhanced BDC can be adopted only in a limited range of operation voltages because of its lower junction breakdown voltage.

Related mechanisms for the effects of the BDC can be clearly understood in terms the contour data for the current density, the electric field, and the maximum temperature, as shown in Fig. 4. Upon triggering of parasitic bipolar junction transistor (BJT) operation, a vertical directional U-shaped current path is formed between the drain N+ diffusion and the source N+ diffusion regions. This is the situation in the 1st on-state before the characteristic double snapback occurs [10].

When a higher current is applied to the EDNMOS with a low BDC, high-electron-injection-induced base push-out occurs, and a lateral directional deep electron channel is formed right under the gate, resulting in a low resistivity and short current path between the source and the drain. The high-electric-field region, which designates the boundary of the base region, is shifted from the original HP-well/N-drift boundary to the N-drift/N+ diffusion boundary. As a result, a highly localized maximum temperature region appears at the surface of N-drift/N+ diffusion boundary.

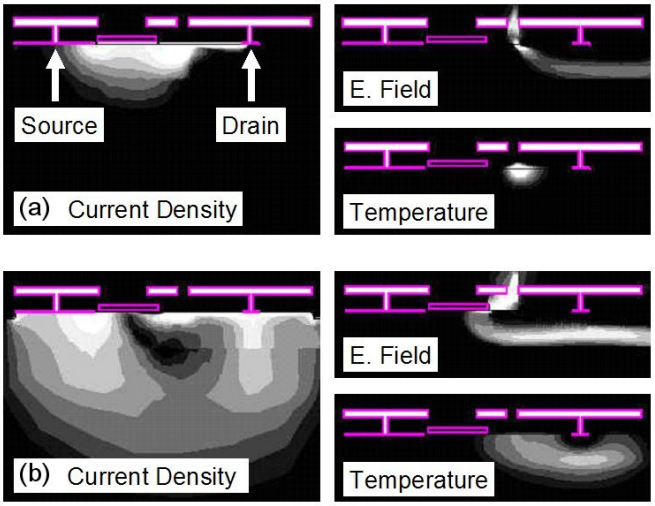

Fig. 4. Contours of the current density, the electric field, and the local temperature (a) for an EDNMOS device with low BDC. The contour data are obtained at a drain current level of 4 mA/um, (b) for EDNMOS device with high BDC at a drain current level 8 mA/um.

An exact matching between the site of the high electric field and that of the maximum temperature is clearly seen. The low resistivity and the short current path following the deep electron channel can explain the occurrence of the 2nd on-state with such a low on-resistance. The high-electron-injection-induced base push-out and the consequential double snapback have been addressed in several publications [10–12].

The EDNMOS with a high BDC never exhibits base push-out, not even in the high- current region. Thus, the initially formed U-shaped current conduction path is maintained until thermal breakdown occurs. The high electric-field region is stuck to the HP-well/N-drift boundary. The non-localized maximum temperature region is formed along the bottom directional HP-well/N-drift boundary. The non-localized property of the maximum temperature region guarantees a higher current immunity level under ESD stress.

The TLP measurement data in Fig. 5 shows the I-V relations of the high BDC EDNMOS devices for various finger numbers. The non-uniformity of multi-finger triggering has been a critical problem and hinders the EDNMOS device from being adopted as an ESD protection device. It is generally accepted that uniform multi-finger triggering is guaranteed when the thermal break-

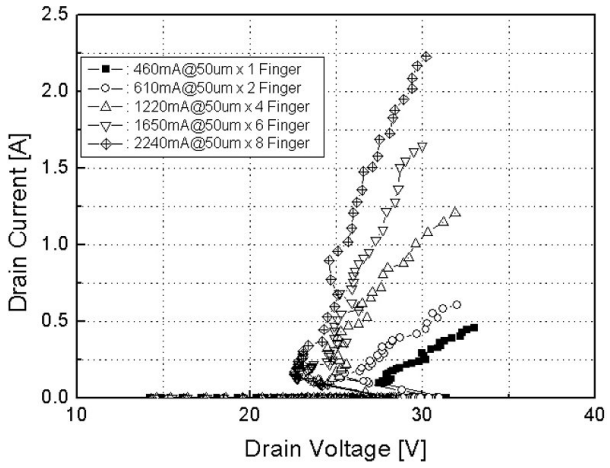

Fig. 5. TLP measurement data for the I-V relations of the high-BDC EDNMOS devices with various finger numbers.

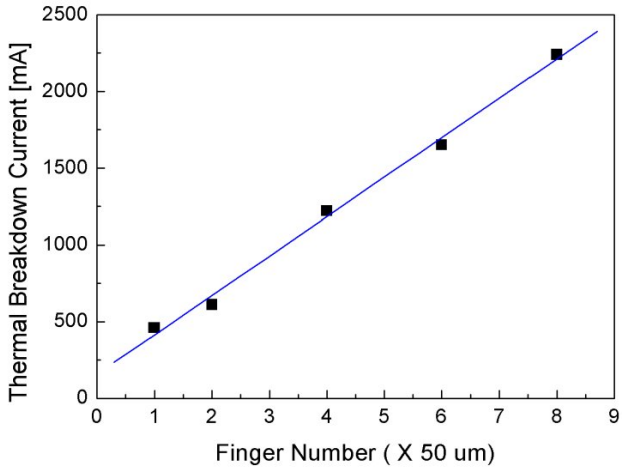

Fig. 6. ESD current immunity level as a function of the active width and the number of finger.

down voltage is larger than the BJT triggering voltage. The data in Fig. 3 show that this uniformity condition is largely violated in the EDNMOS with a low BDC. However, the EDNMOS with a high BDC appears to satisfy the required uniformity condition. Thus, uniform multi-finger triggering is expected in the EDNMOS with a high BDC. This suggests that the poor scaling behavior of EDNMOS devices can be cured by properly controlling their BDCs.

Fig. 6 shows that the thermal breakdown current (It_2), which is defined as the ESD current immunity level, of the EDNMOS device with a high BDC generally increases when its finger number increases. The linearity of the thermal breakdown current upon increasing the finger number from 1 to 2 is relatively poor because the drain site of the EDNMOS is commonly used upon increasing the finger number from 1 to 2. However, an almost linear dependence of the current immunity level on the finger number is clearly seen upon increasing the

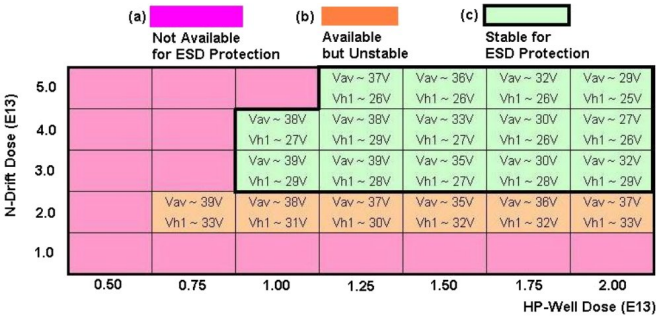

Fig. 7. Two-dimenstional matrix data for the avalanche breakdown voltage (Vav) and the first snapback holding voltage ($Vh1$) for various HP-well and N-drift implant doses.

finger number from 2 to 4, 6, or 8. Note that the 8-finger trigger efficiency compared to the 2-finger trigger efficiency is 91 %. Also, the slope of the line is shown to be about 5.08 mA/um, which correspond to the ESD current immunity level per unit active width of the unit finger in the multiple-finger EDNMOS device.

Fig. 7 shows the 2-dimenstional matrix of the avalanche breakdown voltage (Vav) and first snapback holding voltage ($Vh1$) for various HP-wells and N-drift implant doses. It presents (a) not available for ESD protection, (b) available but unstable, and (c) stable for ESD protection. In summary, we performed simulation analyses for various HP-well doses of $0.5 \times 10^{13} \sim 2.0 \times 10^{13}$ cm^{-2} and N-drift doses of $1.0 \times 10^{13} \sim 5.0 \times 10^{13}$ cm^{-2}. We also did TLP verification by varying either the HP-well dose or the N-drift dose in the corresponding range. This BDC corresponds to an operating voltage range of $18 \sim 40$ V. Collecting 2-dimensional matrix data, we can conclude that a high BDC results in stable snapback with the 1st on-state while a low BDC results in double snapback. Thus, we can utilize Fig. 7 as a look-up-table for optimizing an EDNMOS ESD protection device. On the other hand, the graphs in Fig. 3 show only representative data among many the 2-dimensional matrix data shown in Fig. 7.

IV. CONCLUSION

The inveterate problems of the EDNMOS can be cured by properly controlling its background doping concentration (BDC). An EDNMOS with a high BDC does not show double snapback and remains within the 1st on-state. This implies that both stable ESD protection and latchup immunity can be realized in terms of the EDNMOS device by keeping its BDC sufficiently high. It should be noted that controlling its BDC for ESD protection is practically of limited usage because the junction breakdown voltage depends on the BDC. Further progress in overcoming this limit is expected in future works.

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