```
module johnson(clk,rst,init,rjmode,q);
input clk,rst,rjmode,init;
parameter n=5;
output [n-1:0]q;
reg [n-1:0]q_i;
reg temp;
integer I;
always @(posedge clk or negedge rst)
begin
if(!rst)
for(I=0; I<=n-1; I=I+1)
q_i <= 1'b0;
else
begin
if (!rjmode)
temp = ~q_i[n-1];
else
temp = (q_i[n-1]) &&(init);
for(I=n-1;I>=1; I=I-1)
begin
q_i[I] = q_i[I-1];
end
q_i[0] = temp;
end
end
assign q = q_i;
endmodule
```