JFET Characteristics

Objective

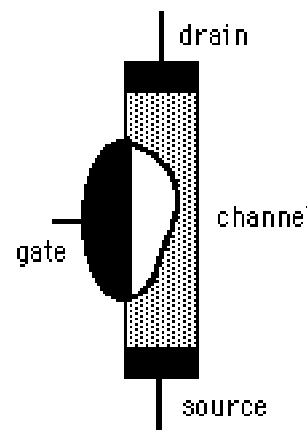
Although arguably the first transistor invented the field-effect transistor did not become established as an important semiconductor device until experience with the BJT had established a broadened understanding of semiconductor phenomena and technology. In this note distinctions between the Junction Field-Effect Transistor (JFET) and the Bipolar Junction Transistor are examined. Static terminal characteristics of two representative JFETs are examined using a PSpice computer analysis of a sophisticated device model.

Although the JFET is a different device from the BJT nevertheless various aspects of device use are similar in general concept if not in precise detail. The following paragraph is a modest paraphrase of that introducing a note on BJT Biasing.

In general all electronic devices are nonlinear, and operating characteristics can change significantly over the range of parameters under which the device operates. The junction field-effect transistor, for example, has a 'normal' amplifier operating drain voltage range bounded by the VCR range for low voltages and drain-gate junction breakdown for high voltages. It also is bounded by excessive drain current on the one hand and cutoff on the other hand. In order to function properly the transistor must be biased properly, i.e., the steady-state operating voltages and currents must suit the purpose involved. Our primary concern here however is not to determine what an appropriate operating point is; that determination depends on a particular context of use and even more so involves a degree of judgment. Rather we consider how to go about establishing and maintaining a given operating point. Where a specific context is needed for an illustration we assume usually that the transistor is to provide linear voltage amplification for a symmetrical signal, i.e., a signal with equal positive and negative excursions about a steady-state value.

Junction Field Effect Transistor

The Junction Field-Effect Transistor (JFET) is a device providing a controlled transport of majority carriers through a semiconductor. The figure illustrates the essential nature of the JFET topology, actual geometry varies depending on the intended application and fabrication techniques. The JFET is at its heart a nonlinear resistor fabricated from a doped semi-conductor material. To be specific we refer to an 'N-channel' device, meaning the conducting material is an N-type semiconductor. Operation of the complementary P-channel device operation is similar and can be inferred directly from the N-channel discussion. In the figure the lightly shaded region is the conducting channel. The darker regions at the ends of the channel are relatively heavily doped terminations for the channel to assure good connections to externally accessible terminals.



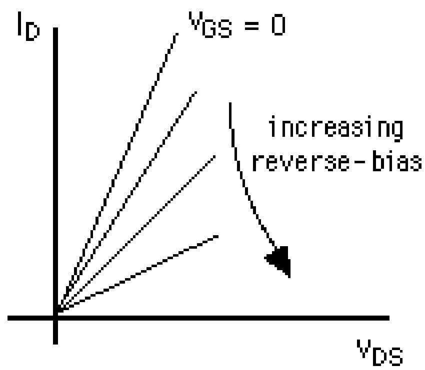
By convention the terminal designations are defined so that carriers (electrons for the N-channel device) flow from the source and to the drain. For the N-channel device, therefore, a voltage is assumed to be applied so that the drain is positive relative to the source.

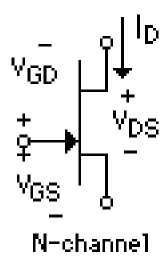
The resistance of the channel is a function of its geometry and the electron transport parameters of the doped semiconductor. The device as described thus far is more or less a (temperature-sensitive) resistor. Suppose now that the channel geometry is changed, e.g., by gouging out the white area shown on the left side of the channel. This is a change of channel geometry, in particular a smaller channel crosssection, which increases the channel resistance, and therefore for a given drain-source voltage less current will flow after the gouging. Even less current flows with further gouging. We have then a variable resistance, although a mechanically 'gouged' the resistor would have a short service life.

On the other hand the channel cross-section can be effectively varied without physically removing material. That is, charge carriers can be effectively removed from part of the cross-section electrically , effectively reducing the channel cross-section and so reducing its conductivity, without actual removal of bulk material.

To effectively remove carriers from a region we simply need to 'shove' them out of that region, and the way to shove a charged carrier is with an electric force. The JFET makes use of the fact that a very strong electric field exists across a PN junction, and that field effectively removes carriers from the junction region. The 'gate' electrode shown in the figure is formed as a PN junction, with the channel forming one side of the junction. The gate side of the junction is relatively heavily doped so that the junction depletion region extends largely into the channel.

The width of the depletion region increases with increasing reverse-bias, extending further into the channel and further increasing the channel resistance. For <u>small</u> values of drain-source voltage the JFET characteristic is linear, as illustrated by the sketch. Increasing the magnitude of the (reverse-biased) gate-source voltage increases the depletion width and increases the channel resistance. The drain characteristics correspond to a variable resistor, with a voltage-controlled resistance.

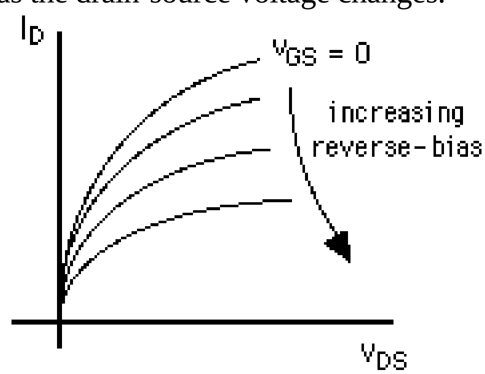




The conventional JFET icon for an N-channel device also is shown in the figure, and is identified as to type by the gate terminal PN junction arrow. Note that following common convention the drain current is positive (in the direction of the current polarity arrow shown) for an electron carrier flow from source to drain.

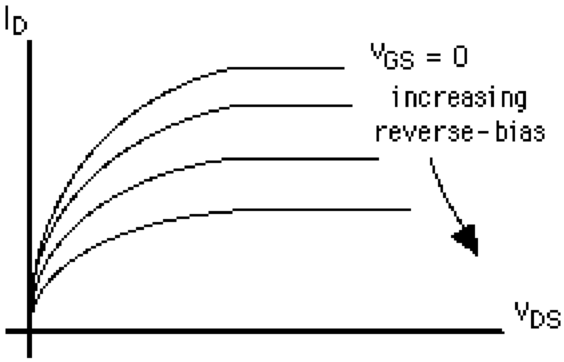
The P-channel device icon would have the gate arrow reversed, and the voltage polarities also would be reversed so that normally the hole carriers flow from source to drain, and the gate junction is reverse-biased.

The reason for the emphasis on <u>small</u> values of drain-source voltage in the discussion above arises from the fact that the gate junction extends a significant distance <u>along</u> the channel length as well as across the channel width. Since the channel is a continuous resistor there is a voltage drop along the length of the channel, and so the gate reverse-bias actually varies along the gate perimeter. The general shape of the depleted region in the earlier illustration is not accidental. It is intended to reflect the increasing junction reverse-bias voltage, and the consequent increasing depletion region width, moving from the source towards the drain. In addition of course the reverse-bias changes as the drain-source voltage changes, and so there is an influence of the drain-source voltage on the resistance of the channel. In this respect make careful note of the fact that the junction voltage is <u>not</u> the same as the gate-source voltage; it is the channel and not the source terminal that forms one side of the junction. As already noted because of the voltage variation along the channel the width of the depletion region varies along the channel, being larger at the drain end of the channel. And moreover the depletion region width changes as the drain-source voltage changes.



Indeed, as the drain-source voltage increases (for an N-channel device) the reverse bias across the junction increases and the channel carries <u>less</u> current for a given voltage than it would otherwise. The drain characteristics viewed over a larger range of drain-source voltage than before appear (roughly) as shown to the right.

As the drain-source voltage increases further a condition known colloquially as 'pinch-off' occurs; this is the condition wherein (theoretically) the depletion region extends entirely across the channel. This occurs initially at the drain end of the channel since that is where the depletion width always is widest. When pinch-off occurs there is a junction depletion region between the drain and the source end of the channel. Further increases in drain-source voltage are taken up primarily by depletion-width changes in this junction region, with only second-order effects on overall channel conduction thereafter. This second order 'channel length modulation' effect is considered further later. The channel current is (to first-order) fixed by the conditions when pinch-off occurs; all carriers forming the source-end current are swept across pinch-off junction region by the strong electric field. This is (roughly) similar to the carrier injection through the base of a BJT, although the mechanism of carrier injection is different.



A still more extended range of variation of the drain characteristics is sketched to the right. The voltage-controlled (VCR) region, i.e., operation before pinch-off, is conventionally called (mostly) just that, i.e., VCR region. The 'constant' current (pinch-off) region to the right is 'saturation' (probably all the remarks respecting a conflict with BJT terminology already have been said, repeatedly).

To summarize: the JFET carrier-transport channel conductivity is modified by the electric field associated with the depletion region of a reverse-biased junction which extends into the channel. The nature of the control process is such that the ability of the channel to carry current is greatest when the control junction has zero bias (or slightly positive, but well below the diode 'knee') and decreases with increasing reverse bias. A JFET thus inherently is a device that is 'full on' with no control exerted, and is turned off with increasing reverse bias. This is 'depletion-mode' operation, so-called after the nature of the physical process through which control is exerted.

The details of the physics underlying the terminal behavior are complex. However it is the terminal behavior and not a quantitative physical explanation for that behavior that is the principal concern here. An exact form of a theoretical expression for a drain characteristic depends on details of both geometry and doping. However various theoretical expressions, despite major differences in mathematical appearance, actually produce very similar numerical characteristics. Thus we describe a commonly used 'working' expression, a quadratic approximation for a drain characteristic in the VCR region of operation, which has the advantage of relative simplicity and adequacy for initial design purposes. This working expression is the quadratic equation:

$$I_D = 2I_{DSS}\left\{ \left(1-\frac{V_{GS}}{V_P}\right)\frac{V_{DS}}{-V_P} - \frac{1}{2}\left(\frac{V_{DS}}{V_P}\right)^2 \right\}$$

V_P is the 'pinch-off' voltage, i.e., the gate-to-drain voltage at which the channel first becomes pinched. 'Pinch-off' is defined as the point where maximum drain current (for a given gate voltage) occurs; the current is assumed to remain substantially unaffected by the drain voltage thereafter. Differentiate the expression to determine that the drain-source voltage at which pinch-off occurs is $V_{DS} = -V_P + V_{GS}$; note (for a N-channel device) that $-V_P$ is positive, that V_{GS} is negative, that $0 \geq V_{GS} \geq V_P$, and because of all this that $V_{DS} \geq 0$ at pinch-off!

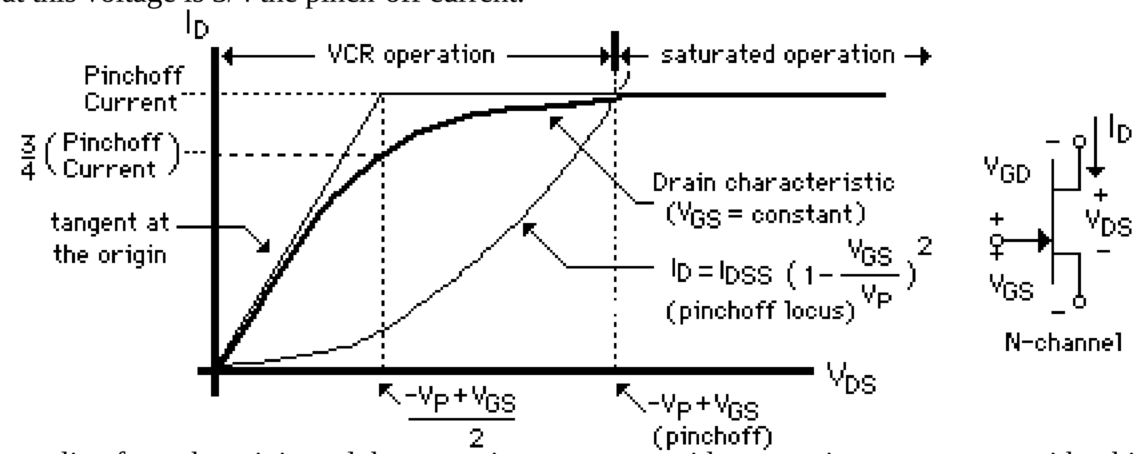
As the expression indicates the drain current I_D is zero for $V_{DS} = 0$ whatever the gate bias. This is notably different from the BJT, where there is a small (millivolts) collector-emitter voltage for zero collector current, and zero offset can be an advantage in applications where the JFET is used as an analog switch.

The maximum current for a given gate bias occurs at $V_{DS} = V_{GS} - V_P$, i.e., at pinch-off, and is given by the first-order expression

$$I_{D(max)} = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

This latter quadratic expression is the locus of the pinch-off points on the common source (I_D vs. V_{DS}, with V_{GS} as a parameter) characteristics. The theoretical equations are described graphically in the figure following. The drain current follows the quadratic expression up to its apex (i.e., over the VCR range), at which point pinch-off occurs and the drain current then remains roughly constant into the saturation range. (Not shown is the drain-gate reverse-bias breakdown at higher drain voltages; 2N3819 device characteristics presented later show this phenomena.) The quadratic pinch-off characteristic, i.e., the locus of the drain current at pinch-off for different gate-source voltages also is drawn on the figure.

Straightforward calculation shows that the extension of the tangent at the origin to the pinch-off current level intersects that current where V_{DS} equals half the pinch-off voltage, i.e., $(-V_P+V_{GS})/2$. The actual current at this voltage is 3/4 the pinch-off current.



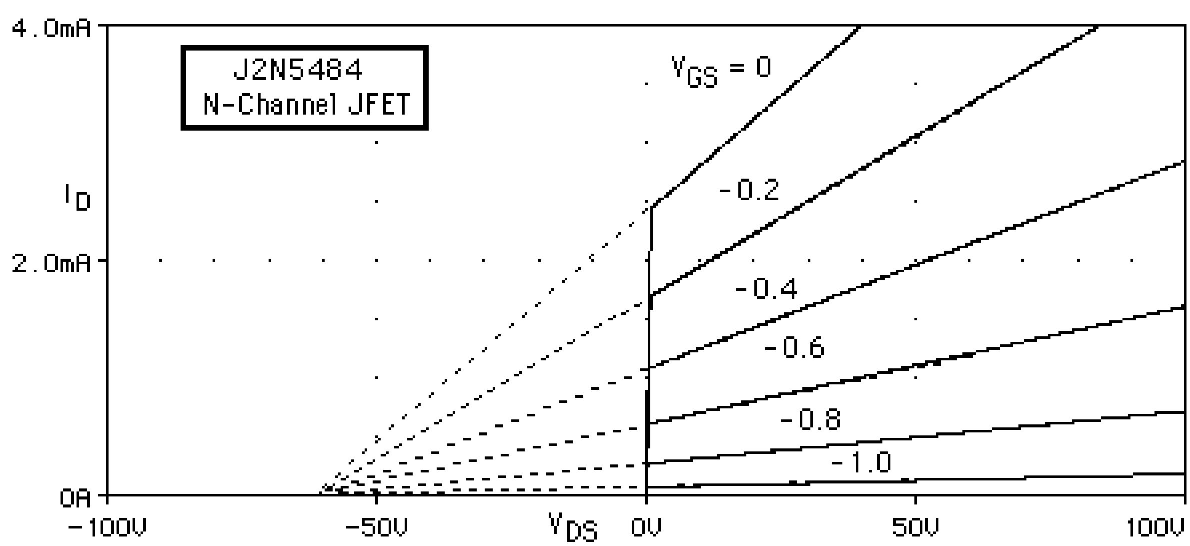
The tangent line from the origin and the saturation current provide convenient asymptotes with which to sketch a characteristic fairly accurately; note again that the actual current is 3/4 that at the intersection of the asymptotes.

Drain Characteristics for 2N5484 N-Channel JFET

Common-Source drain characteristics computed for the 2N5484 N-channel JFET PSpice model are plotted below over a large voltage range; the voltage range is chosen to provide emphasis for certain aspects of the characteristics. Note however that operation with $V_{DS} < 0$ is quite inappropriate. In effect the roles of the source and drain are interchanged, the gate junction becomes forward-biased , and the resulting large gate current is virtually certain to lead to destruction of the device.

```
*JFET 2N5484 Characteristics
VDS       2    0          DC   12
VGS       1    0                0
J2N5484   2    1    0     J2N5484
.LIB  EVAL.LIB
.OP
.PROBE
.DC VDS 0 1.5 .01  VGS  -1.2 0 0.2
.END
```

The left half-plane is included only to display an effect similar to the Early Effect for the BJT, i.e., a second-order dependence of the drain current on the drain-source voltage. (The scale is chosen, as stated before, to overemphasize this dependence; the slope of the curves actually is only of the order of a few kilohms.) The 'channel-length modulation effect causes the characteristics to converge at a common intersection, about -60 volts for the 2N5484.



To account for this effect analytically the saturation characteristics may be multiplied by a factor $1+\lambda V_{DS}$, essentially the leading terms of a series expansion:

$$I_{D(max)} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1+\lambda V_{DS})$$

The channel-length modulation parameter λ is the inverse of the common drain-source voltage at which the several curves meet.

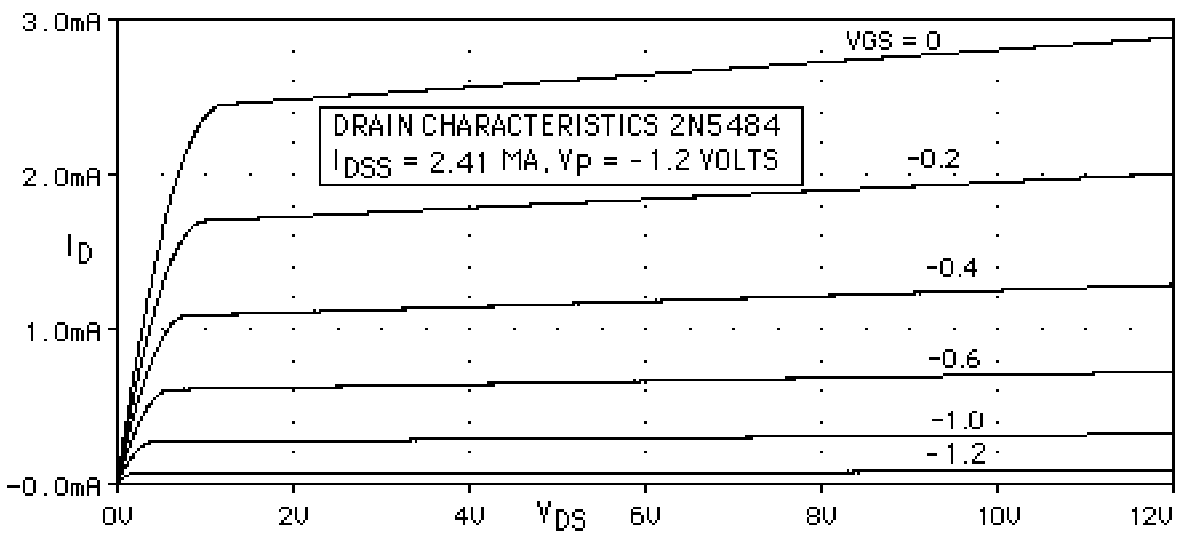
The VCR expression is multiplied by the same factor so as to make the two expressions predict the same current at pinch-off as well as $V_{DS} = 0$.

$$I_D = 2I_{DSS}\left\{\left(1 - \frac{V_{GS}}{V_P}\right)\frac{V_{DS}}{-V_P} - \frac{1}{2}\left(\frac{V_{DS}}{V_P}\right)^2\right\}(1+\lambda V_{DS})$$

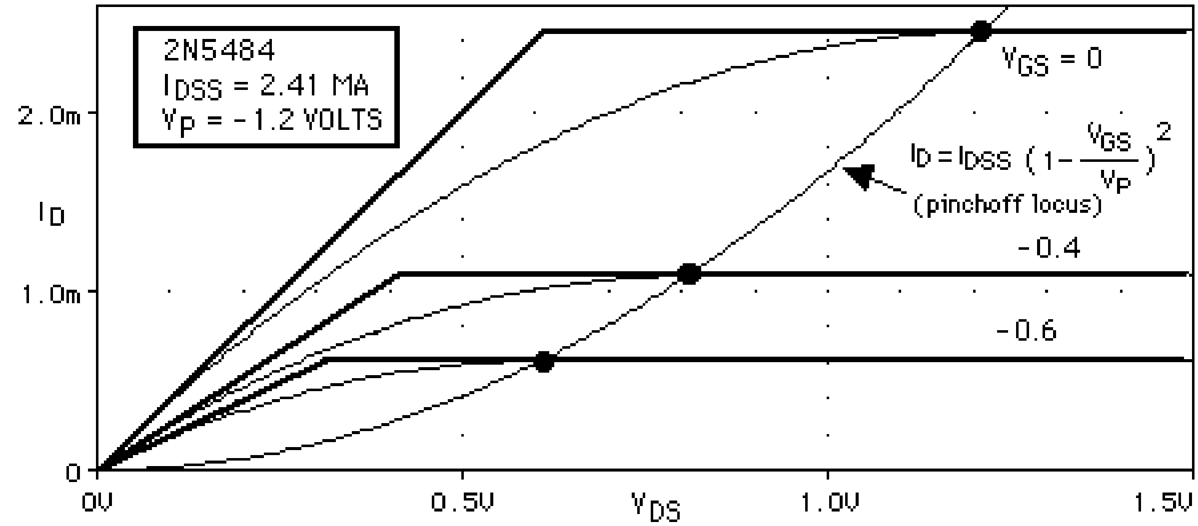
(Note that the value of λ corresponding to the -60 volt common intersection for the 2N5484 is 0.017.) In general the second-order correction is small and generally simply can be neglected for preliminary design calculations. Computer models use these equations with the parameters IDSS, V_P, and λ chosen to match measured device characteristics.

The common-source characteristics are redrawn below, this time to emphasize a more appropriate range of operation. Note that for $V_{DS} > -V_P$, i.e., when the device operates in saturation, the characteristics closely resemble in appearance those of the BJT. One notable distinction is that the control parameter is gate-source voltage, and not a (base) current as for the BJT. Indeed the gate current of a JFET corresponds to a reverse-biased junction, and therefore is very small.

Note also that the VCR operating range ($0 \le V_{DS} \le -V_P$ is typically wider than the saturation range of a BJT, so that a greater voltage margin is necessary to avoid distortion at low drain voltages.



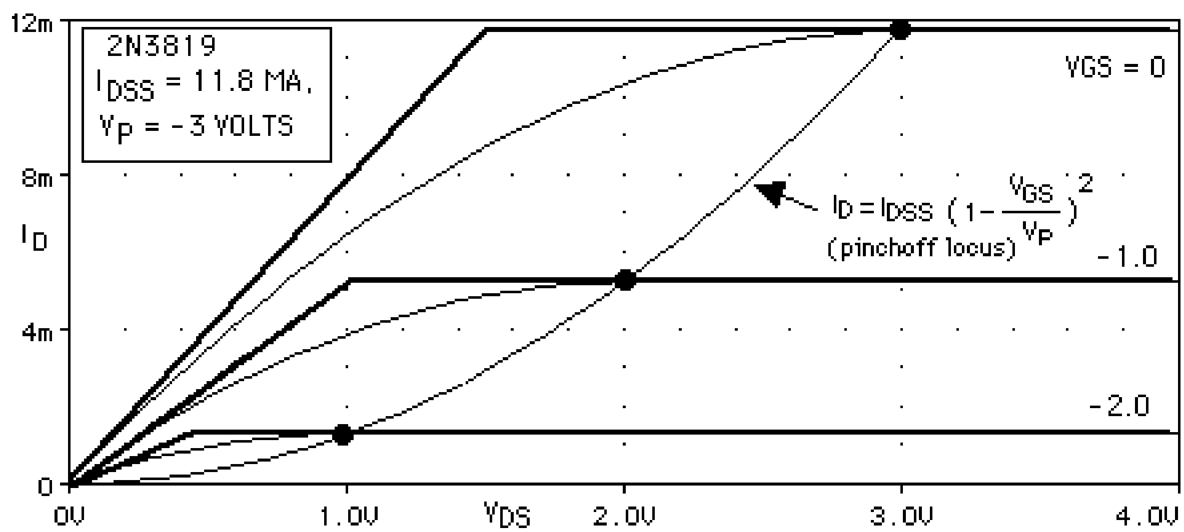
The 2N5484 drain characteristics are re-plotted once again, this time to emphasize the 'voltage-controlled resistance' range. The solid circles • in the figure below mark the intersection of the pinch-off locus with each characteristic (i.e., where $V_{DS} = -V_P + V_{GS}$). The asymptotes for the $V_{GS} = 0$ characteristic, for example, intersect at ≈ 0.6 volts, i.e., $-V_P/2$, as expected theoretically. The actual current at this voltage is ≈ 1.8ma, i.e., 0.75 I_{DSS}, also as expected theoretically.



To obtain an estimate of the channel resistance in the VCR region (for small values of V_{DS}) we can use the ratio of coordinates of the asymptote intercept point, i.e., the slope of the tangent at the origin.. For the VGS = 0 characteristic this estimate is $(-V_P/2)/I_{DSS}$ = (1.21/2)/0.00241= 251 Ω; the channel resistance increases for more negative gate voltages.

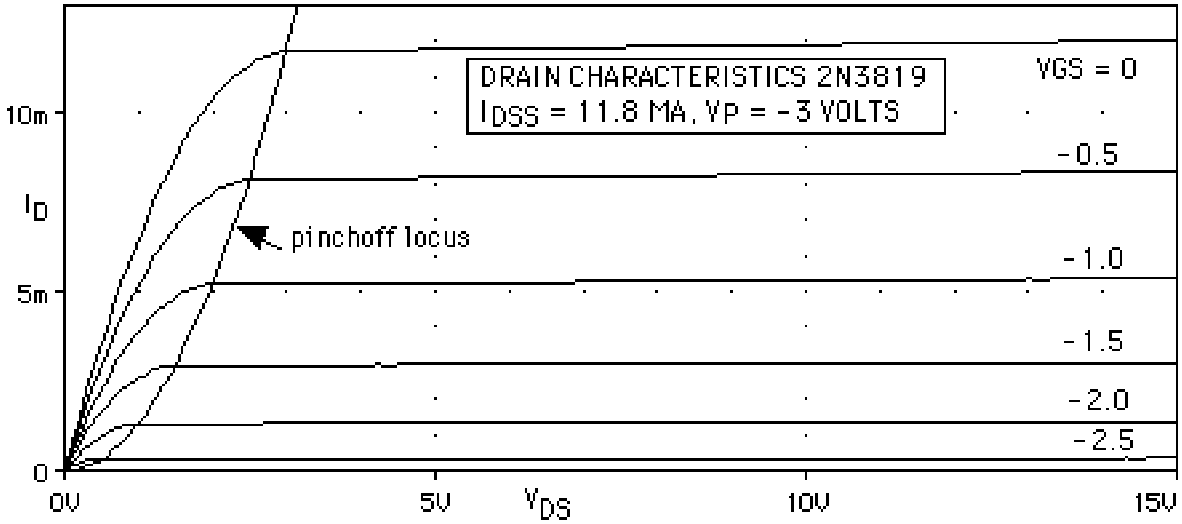
2N3819 N-Channel JFET Characteristics (Another illustration)

Drain characteristics emphasizing the 'voltage- controlled resistance' operating range of the 2N3918 JFET are plotted below. The circles identify the intersection of the pinch-off locus with each characteristic (i.e., where $V_{DS} = -V_P + V_{GS}$). Estimate the channel resistance in the VCR region for V_{GS}=0 as (3/2)/0.00118 = 1.27 KΩ.

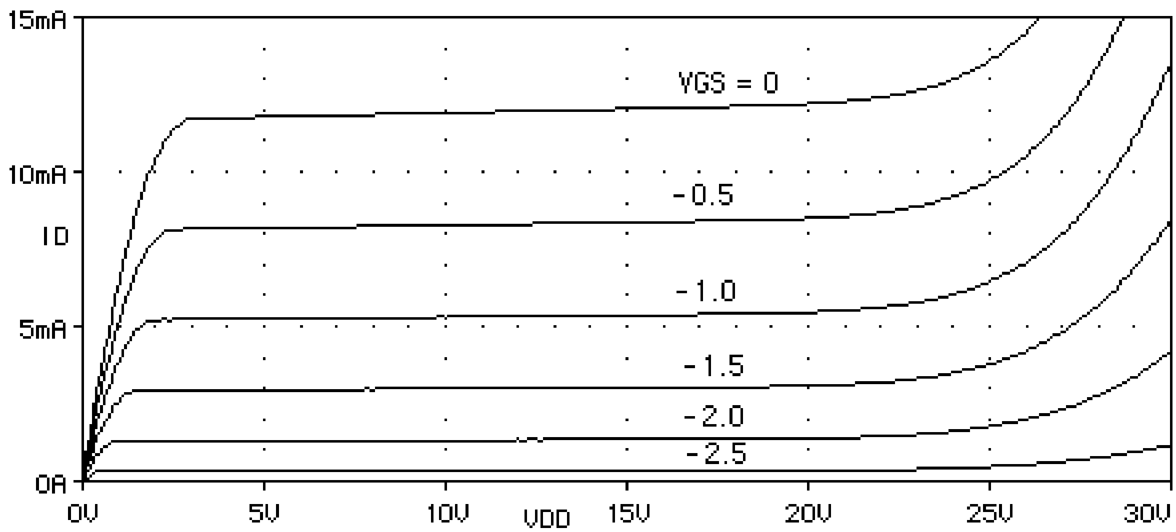


Computed drain characteristics covering both the VCR range and saturation are drawn below.

```
*JFET 2N3819Characteristics
VDD     2       0               DC      12
VGS     1       0                       0
J2N3819         2       1       0       J2N3819
.LIB    EVAL.LIB
.OP
.PROBE
.DC VDD 0 15 .1  VGS 0 -3 .5
.END
```

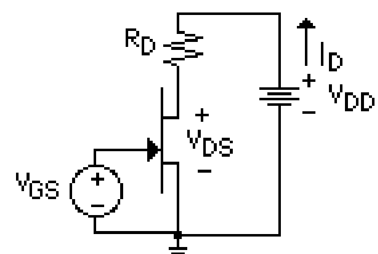


The drain characteristics are re-plotted below over a still larger range of drain-source voltage to show the inception of reverse-bias breakdown of the part of the gate junction near the drain for relatively large drain-source voltages.



JFET Amplifier

We start with an examination of a more or less specific circuit to provide a broad background for a consideration of biasing. Some distinctions from the BJT case are underlined here to call special attention to them.

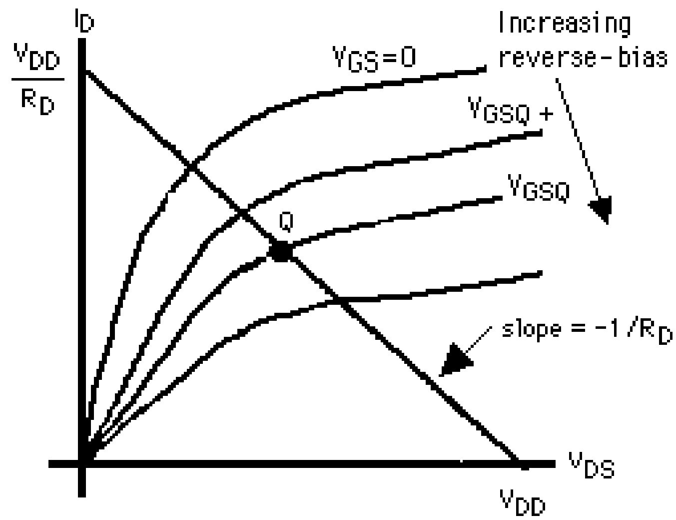


Consider the simplified N-channel JFET amplifier circuit drawn to the right. A voltage source in the base loop reverse-biases the gate junction, setting the gate-source voltage to a fixed value $V_{GS} \le 0$. Provided the drain source voltage is large enough, and the voltage drop across the drain resistor is not too large, the JFET is in its normal saturated operating mode.

The drain current is in general a function of the gate voltage. If then a small change is made in V_{GS} there is a corresponding change in drain current, and a consequent change in the voltage drop across the drain resistor. The battery (DC) voltage V_{DD} provides a source of energy in the collector circuit. The battery provides each coulomb of charge carried by the drain current around the loop with the ability to do V_{DD} joules of work. Part of this work-doing ability, $I_D R_D$ joules per coulomb, is expended in the collector resistor. The remainder, $V_{DD} - I_D R_D$ joules per coulomb, is dissipated in the transistor. The rate of doing work, i.e., power, is determined by the drain current, i.e., the rate of charge transport. Hence by controlling the current the power provided by the battery and divided between the resistor and the transistor is controlled. (The power expended in the resistor should be interpreted as a general consumption of energy, for example by a loudspeaker or a small motor.)

The transistor provides the current-control capability by acting as a current valve; a change in gate voltage causes a corresponding drain current change. The change in power expended in the drain resistor can be considerably greater than the power needed to cause the change. Because the gate junction is (supposed to be) reverse-biased there is only a very small gate current. Moreover only a small gate-source voltage change is needed to change drain current significantly. The power that must be provided at the transistor gate to effect a power change in the collector loop is therefore the product of a quite small gate current and a small gate voltage change. On the other hand not only is the drain current much larger than the gate current but also the battery voltage ordinarily is much larger than the base voltage and can support larger voltage changes.

To solve for the loop current one could write in the usual manner a KVL loop equation $V_{DS} = V_{DD} - I_D R_D$, and substitute for V_{DS} from the volt-ampere relation of the transistor. It is convenient to illustrate the solution graphically, particularly so because the transistor volt-ampere relation is nonlinear. Thus the transistor collector characteristics are drawn (sans numerical values for simplicity), and superimposed on the plot is a graph of the KVL loop equation. This latter equation plots as a line; a convenient way of doing this is by locating the axis intercepts as shown. Since the initial gate voltage is V_{GSQ} the operating point (solution) must lie somewhere along the emphasized collector characteristic curve; in other words the transistor volt-ampere relationship must be satisfied. Concurrently the KVL expression must be satisfied; the operating point also must lie on the 'load' line. Therefore the operating point must be the intersection of the two curves, i.e., the point Q (for 'quiescent').



Suppose now the gate voltage is changed, say increased (i.e., made less negative) to V_{GS+}. There is a consequent increase in drain current, an increase in the voltage drop across the drain resistor, and a decrease in the drain-source voltage. Locating the new operating point graphically is a matter of moving 'up' the load line to the transistor characteristic identified by the gate voltage V_{GS+}.

Biasing the JFET Amplifier

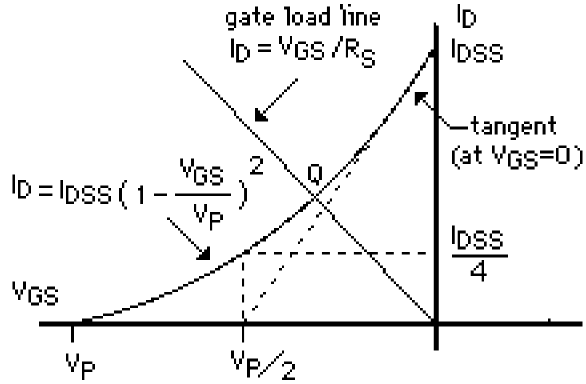
The converse of analyzing a specified amplifier circuit to determine the quiescent point is 'biasing' the transistor, i.e., arranging for a specified quiescent point. There are two aspects to this synthesis: first deciding where the quiescent point is to be located, and then locating it there.

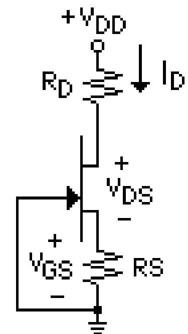
There is no unequivocal choice as to the proper quiescent point; it depends on what performance the amplifier is to provide. For example suppose the amplifier is to provide a symmetrical voltage swing about the Q point. For a maximum symmetrical swing the Q point should be located at roughly $(V_{DD} - V_P)/2$; the (negative) pinch-off voltage provides an offset for the nonlinear VCR range. For a lesser amplitude swing the Q point might be located lower down on the load line; this would involve lower drain currents and therefore lowered requirements on the power supply.

For the present purpose we need not be overly concerned with a specific location of the Q point. Rather we concern ourselves here with just the means for establishing a given operating point, and not what the Q point values are. More than just this. Transistor parameters have significant uncertainties; parameters are quite temperature sensitive, and in addition have large manufacturing tolerances. Not only must a specified Q point be implemented with uncertain circuit element parameters but also it must be maintained during environmental changes and despite device manufacturing tolerances.

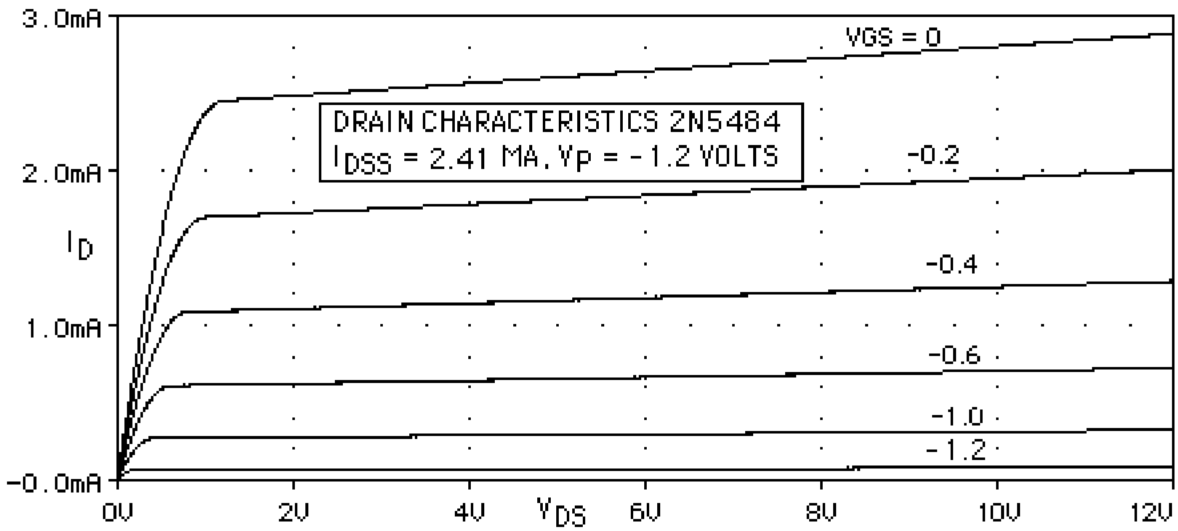
The theoretical relationship between the JFET drain current <u>in saturation</u>, neglecting the second-order slope of the characteristics, is a quadratic, shown below plotted on the I_D-V_{GS} plane. It is not difficult to verify that the tangent at $V_{GS} = 0$ intercepts the abscissa at $V_P/2$; the current for this gate voltage is $I_{DSS}/4$. The asymptote and the V_P intercept are helpful in sketching the quadratic.

The source resistor R accomplishes the biasing (within limitations to be discussed)$_S$. Because of the negligible gate current the source and drain currents are essentially equal, and the voltage drop across the source resistor provides the reverse-bias for the gate. This gate 'load line' also is shown in the figure. The operating point is at the intercept Q. Note: Because the gate often serves as an input, for example for an incremental signal, the short-circuit connection really is inappropriate. However the gate leakage current is quite small (about 1 nanoampere for the 2N5484) so that a rather large resistor can replace the short-circuit connection to provide an input resistance across which there is a negligible voltage drop due to the gate current.





A (rough) illustrative design using the 2N5484 JFET in the circuit described above follows; the common source characteristics (PSpice model) for the 2N5484 are reproduced below.



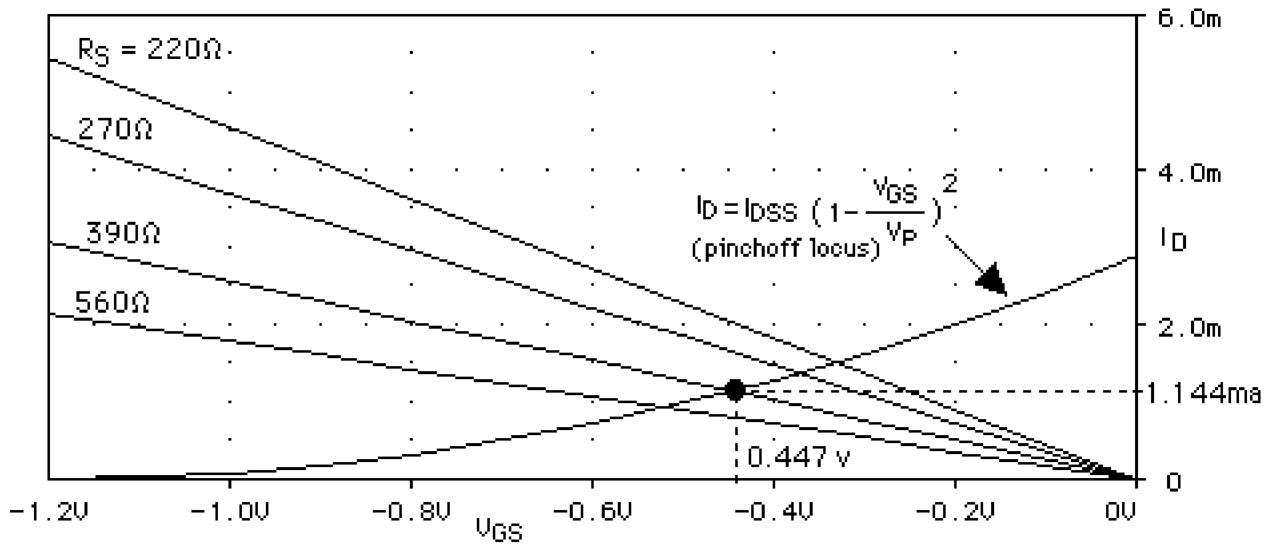
Suppose V_{DD} is 12 volts. The pinch-off voltage for the JFET is V_P = -1.2 volts , and to avoid low current nonlinearities near cutoff allow (say) a drain voltage maximum of 11 volts. Then for a symmetrical voltage swing over the remaining 9.8 volt range bias the JFET at about 1.2+(9.8/2) = 6.1 volts. From the characteristics we might chose a nominal middle' current of 1 ma, with the gate-source voltage needed being about -0.38 volts. This means we need a source resistance of 0.38/1 or 380Ω; 390Ω is the closest 10% standard value. Finally to drop 4.9 volts with a drain current of 1ma requires 4.9K; use R_D = 4.7K

Recalculated values for the specified circuit parameters (substitute into and solve the quadratic expression using the <u>smaller</u> root (why?) are: I_D = 1.048 ma, VGS = - 0.408 volt, and VD = 7.074 volts. A PSpice computation (see netlist following) sets the operating point for the specified circuit parameters at I_D = 1.1 ma, V_{GS} = -0.43 volts, and V_D = 6.83 volts.

The PSpice netlist for the computation is:

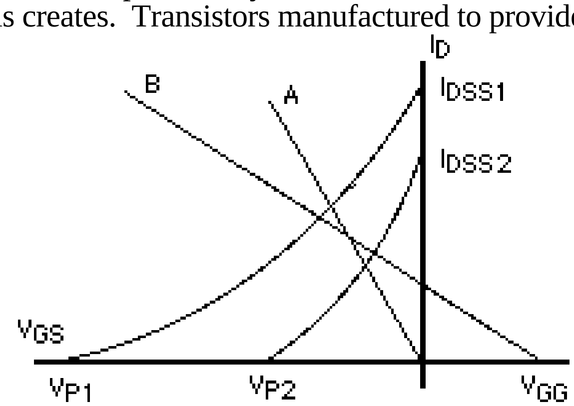
```
*JFET  Bias Illustration
VDD3        3     0     DC    12
RS          1     0           390
J2N5484     2     0     1     J2N5484
RD          3     2           4.7K
.LIB  EVAL.LIB
.OP
.PROBE
.END
```

The biasing analysis may be computed by calculating the drain current (saturation) as a function of the gate-source voltage; the plot below is for V_{DS} = 12 volts. Note that IDSS differs somewhat from the nominal value of 2.41 ma because of the channel length modulation.

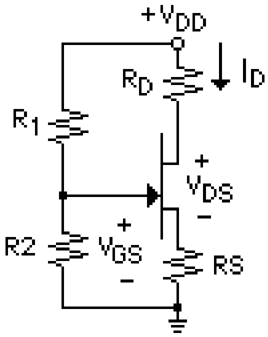


Biasing the JFET Better

The preceding illustration may imply an impressive computational accuracy but it is not a overly practical calculation. In practice the transistor characteristics will be uncertain, particularly because of manufacturing tolerances. The figure to the right illustrates the problem this creates. Transistors manufactured to provide certain nominal characteristics actually will show a spread of gate characteristics from device to device roughly bounded as indicated. (Actually the characteristic with the most negative V_P does not necessarily correspond to the characteristic with the largest I_{DSS}. However it is conservative to presume this; the actual device characteristic then falls somewhere between the bounds. The difficulty, of course, is that except for the bounds the actual characteristic is not predictable.)



The bias load line labeled ‘A’ corresponds to providing the bias with just a source resistor; the load line in this case passes through the origin. Note that there is a difference in the drain current, depending on whether the device involved lies to one side or the other within the bounding gate characteristics. Note also that a load line such as ‘B’ has a smaller range of uncertainty; the gate-source bias then is $V_{GG} - I_D R_S$, where V_{GG} is the intercept on the abscissa. The larger V_{GG} the less the slope of the load line, and therefore the smaller the spread between the current intercepts on the bounding curves.

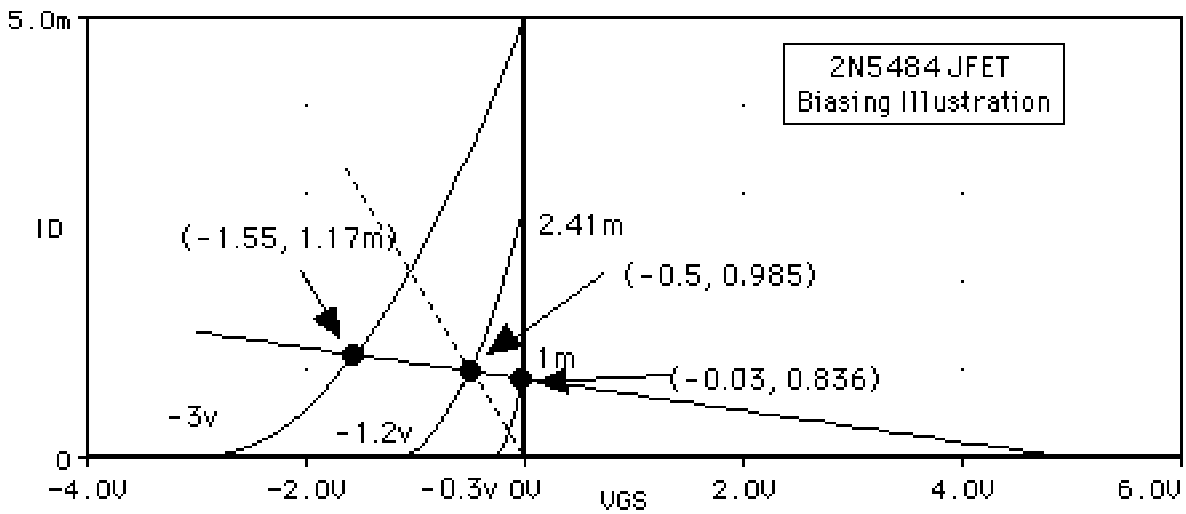


A bias configuration to provide the V_{GG} offset is shown to the left. The R1, R2 resistors form a voltage divider (the gate current is negligible if the resistors carry, say, a microampere or more of current) to bias the gate by $V_{DD}(R_2/(R_1+R_2))$; this corresponds to VGG. Note the trade-off. V_{GG} should be high to reduce the current intercept spread. But operation in saturation requires the drain voltage to exceed the gate voltage by at least the pinch-off voltage magnitude, and the gate bias should not force an excessive V_{DD} for a given drain voltage swing.

Better-Biasing Illustration

The manufacturer's data for the 2N5484 JFET indicates that the pinch-off voltage varies between -3 volts and -0.3 volts, and that IDSS varies between about 1ma and 5 ma. As noted before these data are interpreted conservatively by assuming that the extremes are correlated. Quadratic expressions using the respective pairs of parameters are plotted in the figure following as bounds on the actual gate characteristic. The nominal characteristic, computed from the PSpice model using V_P = -1.2 volts and I_{DSS} = 2.41ma, also is plotted.

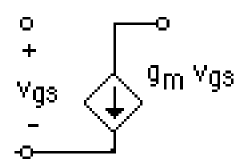
More or less arbitrarily, in lieu of an explicit specification, a nominal operating point is assumed at V_{GS} = -0.5 volt (roughly centered). A load line with a 5 volt offset (again a more or less arbitrary choice) is drawn. The intercepts with the bounding curves as noted were determined (using the cursor capability of Probe). Note the comparatively modest range of current variation (0.836 ma to 1.17ma) for devices within the manufacturing tolerance limits. For comparison the load line for simple source biasing also is drawn (dotted); note the much larger range of current variation predicted.



JFET Incremental Parameter Equivalent Circuit

The formal development of an incremental parameter circuit for the JFET is essentially the same for the BJT. In both cases device characteristics in a small region about a DC operating point are approximated by tangent lines, and the topology of linear equivalent circuit representations is the same. There are, of course, significant differences in circuit element values for different devices.

A simplified incremental parameter circuit commonly used for JFET design calculations is as drawn to the right. For a JFET the input resistance is that of a reverse-biased junction diode, and is ordinarily so large compared to other circuit resistances in series with or shunting the gate-source terminals that it simply may be neglected.



In the saturation range of operation, and neglecting second order channel-length modulation

$$I_{D(max)} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Approximate this quadratic at a particular DC bias point by a tangent whose slope (the relation between an incremental change in gate-source voltage v_{gs} and an associated incremental change in drain current i_d is obtained by differentiating the quadratic:

$$i_d = 2\,\frac{\sqrt{IDSS\;ID}}{-Vp}\,v_{gs} \triangleq g_m v_{gs}$$

The coefficient g_m is the incremental transconductance of the JFET. Unlike the BJT the JFET is by its nature a (gate-source) voltage-controlled device. As noted above the incremental input resistance of the JFET corresponds to a reverse-biased diode, and except for very special cases the input current is negligible.

If the channel-length modulation is to be accounted for then a gate-drain resistor (not shown above) is added, i.e., the drain current includes a small dependence on the drain-source voltage. To account for this include the factor 1+ λ VDS factor in the expression for drain current, i.e.,

$$I_{D(max)} = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 (1+\lambda\,VDS)$$

Calculate the incremental drain resistance

$$\frac{v_{ds}}{i_d} = \frac{1}{\lambda\, I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2} \leq \frac{1}{\lambda I_{DSS}}$$

For the 2N5484 JFET for example IDSS = 2.41ma and $\lambda \approx 1/60$; the minimum r_{ds} is ≈ 25KΩ.) This is rarely important for preliminary design calculations for reasons similar to those applied to the BJT Early Effect. In general a JFET would be designed to transfer drain current into some sort of load and a comparatively low resistance load would be used. In any event initial design calculations would be adjusted by computer calculations using models which include various second order effects.

A more complete model accounts for small gate-drain and gate-source capacitances. However as for the BJT introduction of inherent reactive effects is postponed.