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**Lecture No.:** 13

**Lecture Title:** Analog Circuits - JFET Biasing

### Script

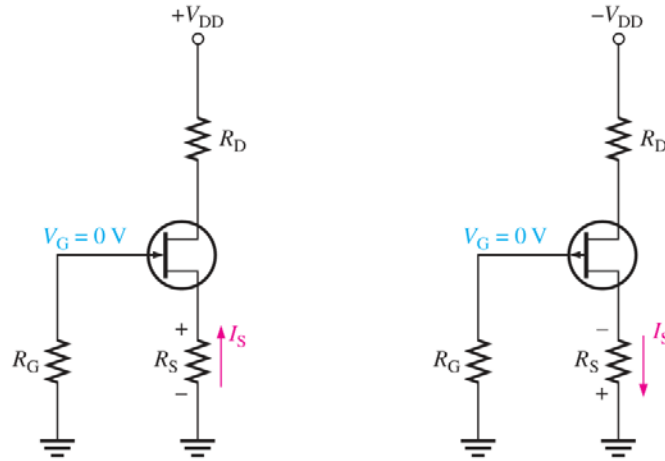
Hello friends in the previous lecture we discussed about the Field-effect transistors being uni-polar device having three terminals namely source, drain, and gate. The JFET operates with a reverse-biased pn junction with high input resistance due to the reverse-biased gate-source junction. FET is called a square-law device because of the relationship of  $I_D$  to the square of a term containing  $V_{GS}$ . In today's lecture we shall discuss and analyze JFET biasing, describe self-bias and the Q-point of a self-biased JFET, graphically analyze a self-biased and voltage-divider biased JFET, discuss Q-point stability of JFET, and finally talk about Ohmic regions.

## JFET BIASING

Using some of the JFET parameters discussed previously, you will now see how to dc-bias JFETs. Just as with the BJT, the purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. Three types of bias are self-bias, voltage-divider bias, and current-source bias.

### Self-Bias

Self-bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative  $V_{GS}$  for an n-channel JFET and a positive  $V_{GS}$  for a p-channel JFET. This can be achieved using the self-bias arrangements shown in figure here.



The gate resistor,  $R_G$ , does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V.  $R_G$  is necessary only to force the gate to be at 0 V and to isolate an ac signal from ground in amplifier applications.

For the n-channel JFET as shown in the figure,  $I_S$  produces a voltage drop across  $R_S$  and makes the source positive with respect to ground. Since  $I_S = I_D$  and  $V_G = 0$ , then  $V_S = I_D R_S$ . The gate-to-source voltage is then given by

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Thus,

$$V_{GS} = -I_D R_S$$

For the p-channel JFET, shown in part (b) of the figure the current through  $R_S$  produces a negative voltage at the source, making the gate positive with respect to the source. Therefore, since  $I_S = I_D$ ,

$$V_{GS} = +I_D R_S$$

Keep in mind that analysis of the p-channel JFET is the same except for opposite-polarity voltages. The drain voltage with respect to ground is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

Since  $V_S = I_D R_S$ , the drain-to-source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D (R_D + R_S)$$

### Setting the Q-Point of a Self-Biased JFET

The basic approach to establishing a JFET bias point is to determine  $I_D$  for a desired value of  $V_{GS}$  or vice versa. Then calculate the required value of  $R_S$  using the following relationship. The vertical lines indicate an absolute value.

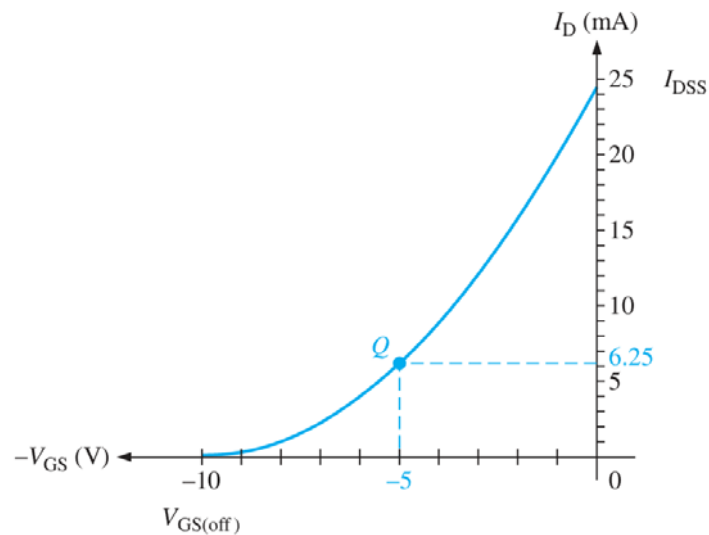
$$R_S = \left| \frac{V_{GS}}{I_D} \right|$$

For a desired value of  $V_{GS}$ ,  $I_D$  can be determined in either of two ways: from the transfer characteristic curve for the particular JFET or, more practically, from this equation

$$I_D \cong I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

$I_{DSS}$  And  $V_{GS(off)}$  values are taken from the JFET datasheet. The next two examples illustrate these procedures.

Determine the value of  $R_S$  required to self-bias an n-channel JFET that has the transfer characteristic curve shown in figure at  $V_{GS} = -5V$



From the graph,  $I_D = 6.25\text{mA}$  when  $V_{GS} = -5V$ .

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{5V}{6.25\text{mA}} = 800\Omega$$

In the second example we are to determine the value of  $R_S$  required to self-bias a p-channel JFET with datasheet values of  $I_{DSS} = 25\text{mA}$  and  $V_{GS(\text{off})} = 15\text{V}$ .  $V_{GS}$  is to be  $5\text{V}$ .

In order to calculate  $I_D$  we use this equation

$$I_D \cong I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

Substituting the given values in equation, we get

$$\cong 25\text{mA} \left( 1 - \frac{5\text{V}}{15\text{V}} \right)^2$$

$$\cong 25\text{mA} (1 - 0.333)^2$$

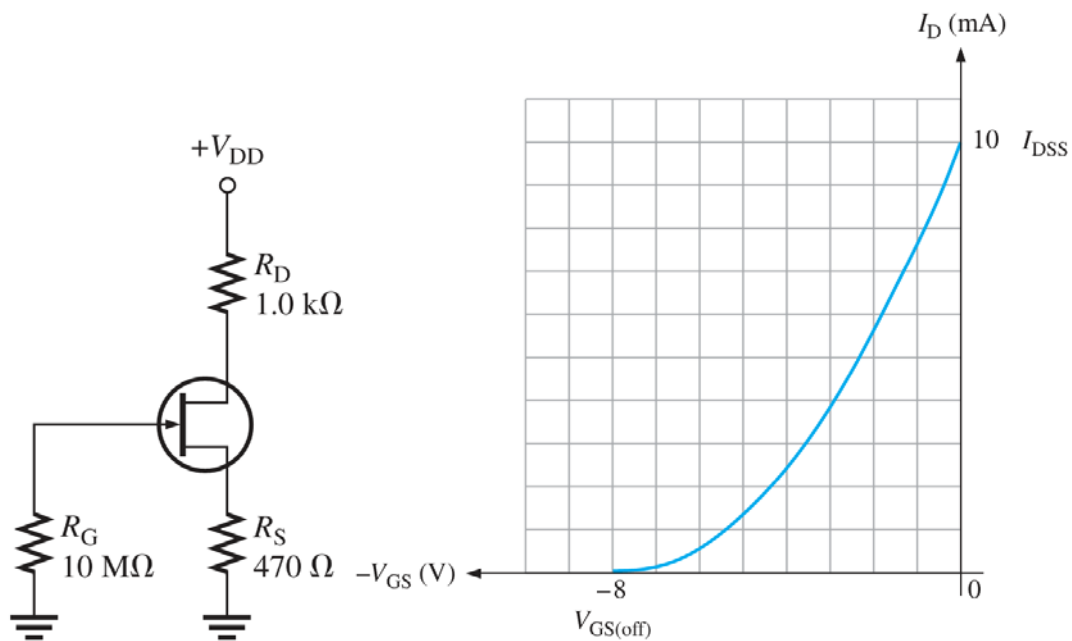
$$I_D = 11.1\text{mA}$$

Now we determine  $R_S$  using the equation as given here,

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{5\text{V}}{11.1\text{mA}} = 450\Omega$$

### Graphical Analysis of a Self-Biased JFET

You can use the transfer characteristic curve of a JFET and certain parameters to determine the Q-point of a self-biased circuit. A circuit and its transfer characteristic curve are shown here in figure.



To determine the Q-point of the circuit, a self-bias dc load line is established on the graph as follows. First, calculate  $V_{GS}$  when  $I_D = 0$ .

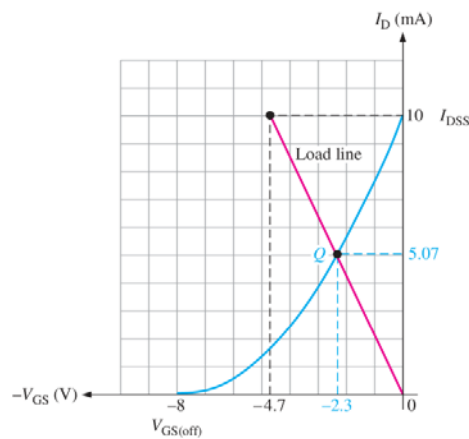
$$V_{GS} = -I_D R_S = (0)(470) = 0V$$

This establishes a point at the origin on the graph. Next, calculate  $V_{GS}$  when  $I_D = I_{DSS}$ . From the curve we can see that  $I_{DSS} = 10mA$ .

So,

$$V_{GS} = -I_D R_S = -(10mA)(470) = -4.7V$$

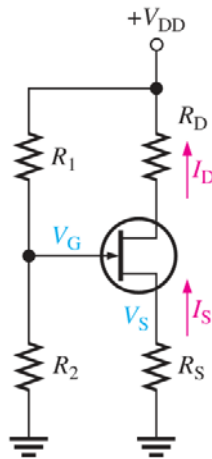
This establishes a second point on the graph. Now, with two points, the load line can be drawn on the transfer characteristic curve as shown in this figure.



The point where the load line intersects the transfer characteristic curve is the Q-point of the circuit as shown, where  $I_D = 5.07mA$  and  $V_{GS} = -2.3V$ . For increased Q-point stability, the value of  $R_S$  in the self-bias circuit is increased and connected to a negative supply voltage. This is sometimes called dual-supply bias.

### Voltage-Divider Bias

An n-channel JFET with voltage-divider bias is shown in figure.



The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage-divider formula where

$$V_G = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$$

The gate-to-source voltage is

$$V_{GS} = V_G - V_S$$

And the source voltage is

$$V_S = V_G - V_{GS}$$

The drain current can be expressed as

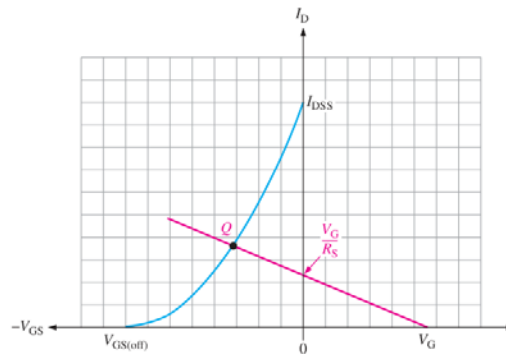
$$I_D = \frac{V_S}{R_S}$$

Substituting for  $V_S$ ,

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

## Graphical Analysis of a JFET with Voltage-Divider Bias

An approach similar to the one used for self-bias can be used with voltage-divider bias to graphically determine the Q-point of a circuit on the transfer characteristic curve.



In a JFET with voltage-divider bias when  $I_D = 0$ ,  $V_{GS}$  is not zero, as in the self-biased case, because the voltage divider produces a voltage at the gate independent of the drain current. The voltage-divider dc load line is determined as follows.

For  $I_D = 0$ ,

$$V_S = I_D R_S = (0)R_S = 0V$$

$$V_{GS} = V_G - V_S = V_G - 0V = V_G$$

Therefore, one point on the line is at  $I_D = 0$  and  $V_{GS} = V_G$ .

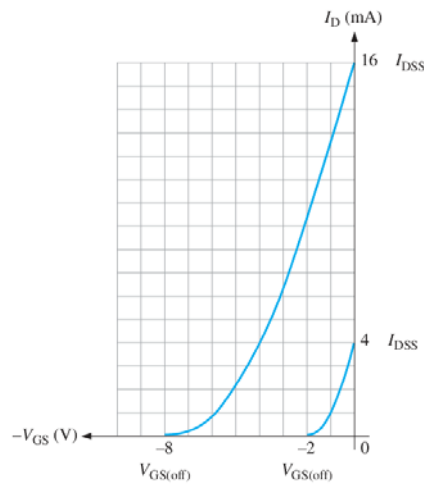
For  $V_{GS} = 0$ ,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

A second point on the line is at  $I_D = V_G/R_S$  and  $V_{GS} = 0$ . The point at which the load line intersects the transfer characteristic curve is the Q-point.

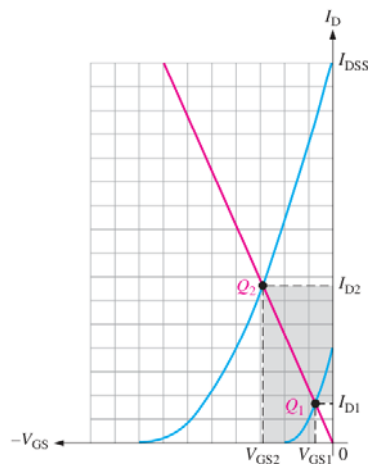
## Q-Point Stability

Unfortunately, the transfer characteristic of a JFET can differ considerably from one device to another of the same type. If, for example, a 2N5459 JFET is replaced in a given bias circuit with another 2N5459, the transfer characteristic curve can vary greatly, as illustrated in figure.



In this case, the maximum  $I_{DSS}$  is 16mA and the minimum  $I_{DSS}$  is 4mA. Likewise, the maximum  $V_{GS(off)}$  is -8V and the minimum  $V_{GS(off)}$  is -2V. This means that if you have a selection of 2N5459s and you randomly pick one out, it can have values anywhere within these ranges.

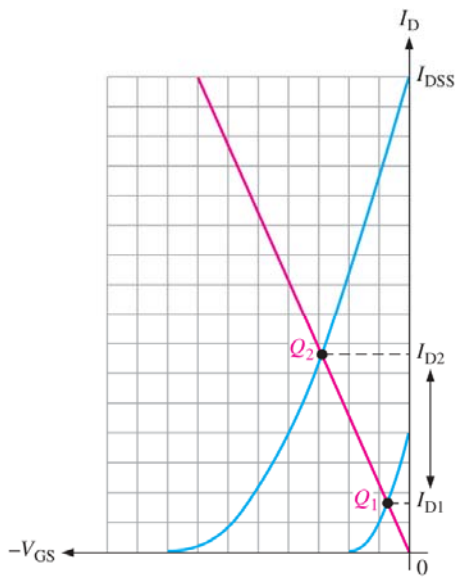
If a self-bias dc load line is drawn as illustrated in figure here,



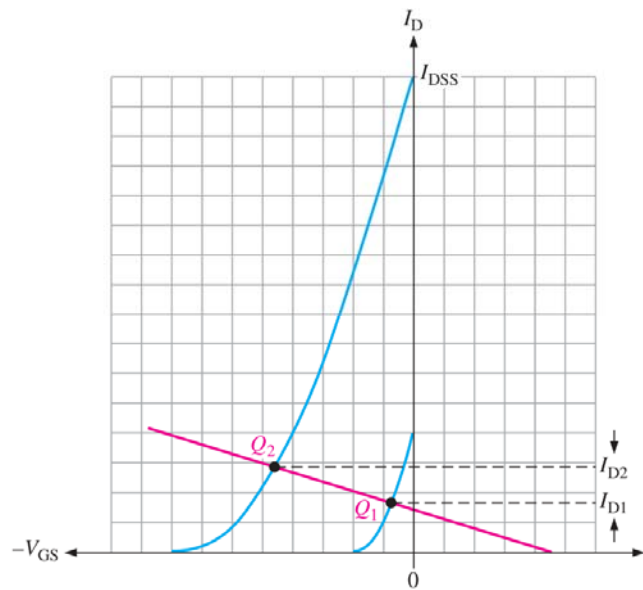
The same circuit using a 2N5459 can have a Q-point anywhere along the line from Q1, the minimum bias point, to Q2, the maximum bias point. Accordingly, the drain current can be any value between  $I_{D1}$  and  $I_{D2}$ , as shown by the shaded area. This means that the dc voltage at the drain can have a range of values depending on  $I_D$ . Also, the gate-to-source voltage can be any value between  $V_{GS1}$  and  $V_{GS2}$ , as indicated.

Figure here illustrates Q-point stability for a self-biased JFET and for a JFET with voltage-divider bias.





(a) Self-bias

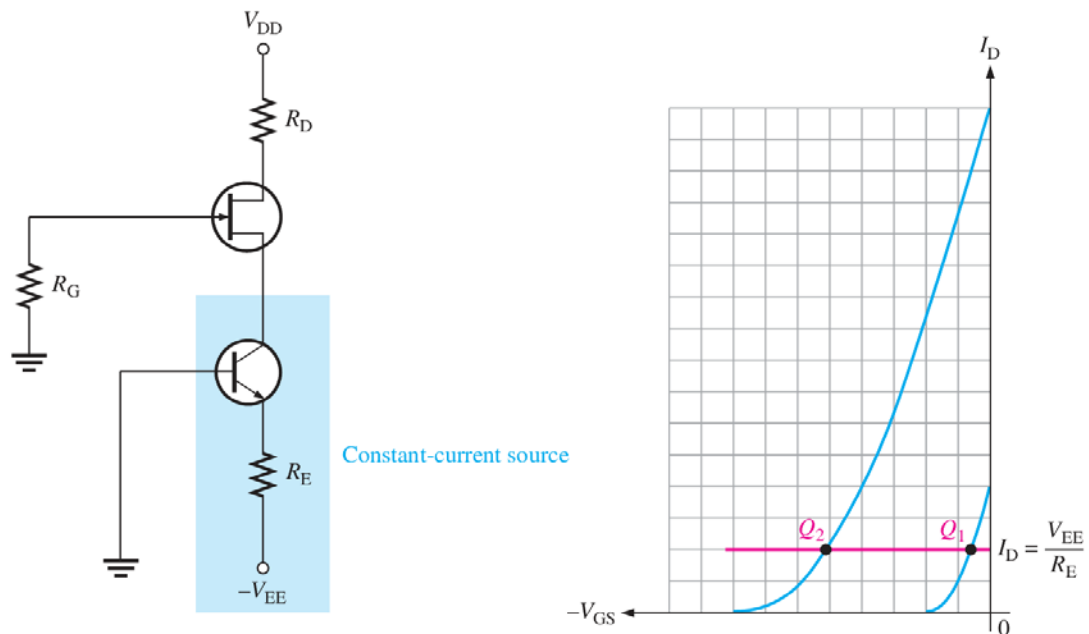


(b) Voltage-divider bias

With voltage-divider bias, the dependency of  $I_D$  on the range of Q-points is reduced because the slope of the load line is less than for self-bias for a given JFET. Although  $V_{GS}$  varies quite a bit for both self-bias and voltage-divider bias,  $I_D$  is much more stable with voltage-divider bias.

### Current-Source Bias

Current-source bias is a method for increasing the Q-point stability of a self-biased JFET by making the drain current essentially independent of  $V_{GS}$ . This is accomplished by using a constant-current source in series with the JFET source, as shown in figure.



In this circuit, a BJT acts as the constant-current source because its emitter current is essentially constant if  $V_{EE} \gg V_{BE}$ . A FET can also be used as a constant-current source. As you can see in part (b) figure,  $I_D$  remains constant for any transfer characteristic curve, as indicated by the horizontal load line.

### THE OHMIC REGION

The ohmic region is the portion of the FET characteristic curves in which Ohm's law can be applied. When properly biased in the ohmic region, a JFET exhibits the properties of a variable resistance, where the value of resistance is controlled by  $V_{GS}$ . After completing this section, you should be able to

Discuss the ohmic region on a JFET characteristic curve

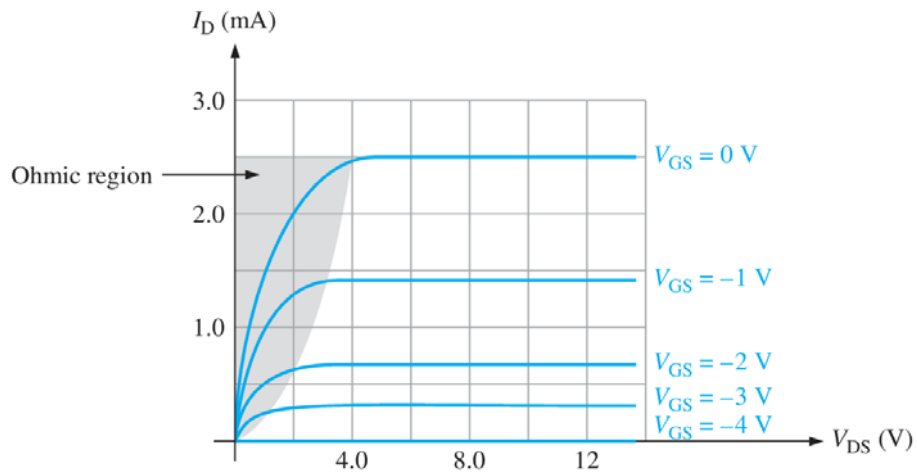
Calculate slope and drain-to-source resistance

Explain how a JFET can be used as a variable resistance

Discuss JFET operation with the Q-point at the origin, and

Calculate trans-conductance

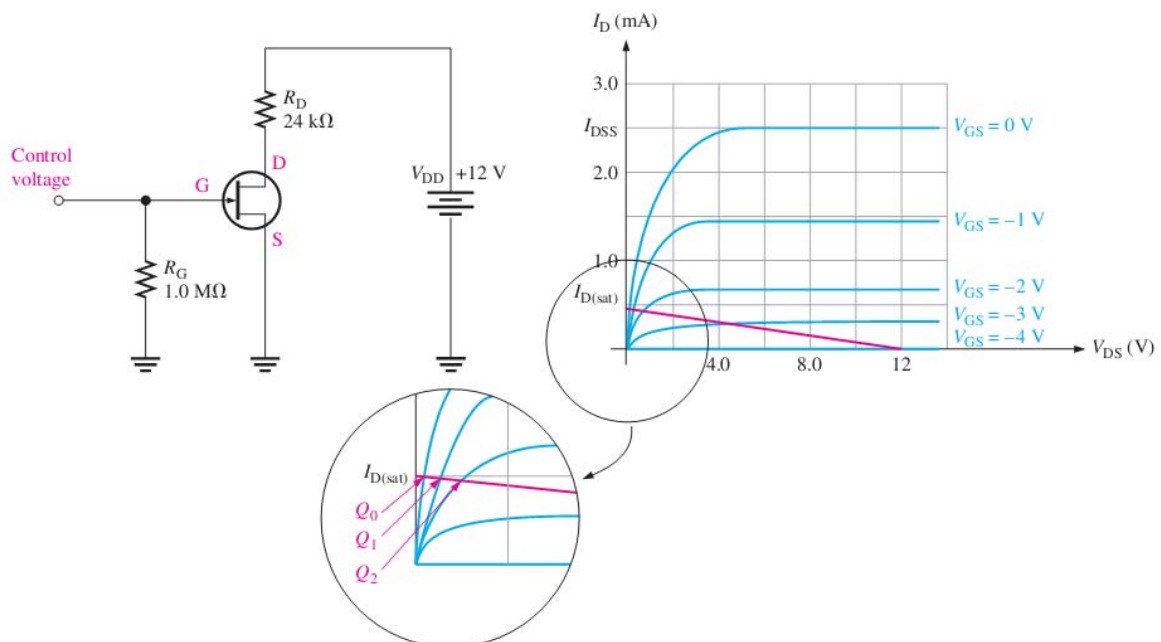
As shown on a typical set of curves in figure, the ohmic region extends from the origin of the characteristic curves to the break point of the  $V_{GS} = 0$  curve in a roughly parabolic shape.



The characteristic curves in this region have a relatively constant slope for small values of  $I_D$ . The slope of the characteristic curve in the ohmic region is the dc drain-to-source conductance  $G_{DS}$  of the JFET.

### The JFET as a Variable Resistance

A JFET can be biased in either the active region or the ohmic region. JFETs are often biased in the ohmic region for use as a voltage-controlled variable resistor. The control voltage is  $V_{GS}$ , and it determines the resistance by varying the Q-point. To bias a JFET in the ohmic region, the dc load line must intersect the characteristic curve in the ohmic region, as illustrated in this figure.



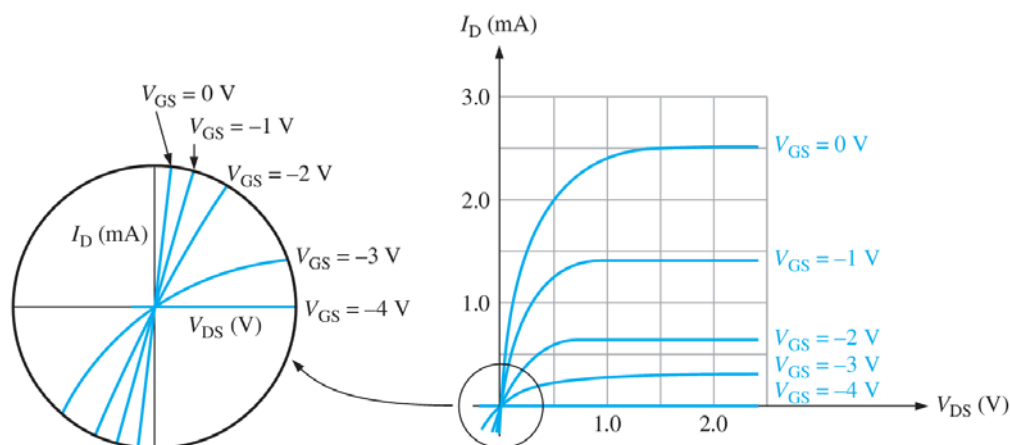
To do this in a way that allows  $V_{GS}$  controlling  $R_{DS}$ , the dc saturation current is set for a value much less than  $I_{DSS}$  so that the load line intersects most of the characteristic curves in the ohmic region, as illustrated. In this case,

$$I_{D(sat)} = \frac{V_{DD}}{R_D} = \frac{12V}{24\Omega} = 0.5mA$$

Part (b) shows the operating region expanded with three Q-points shown (Q0, Q1, and Q2), depending on  $V_{GS}$ . As you move along the load line in the ohmic region, the value of  $R_{DS}$  varies as the Q-point falls successively on curves with different slopes. The Q-point is moved along the load line by varying  $V_{GS} = 0$  to  $V_{GS} = -2$ , in this case. As this happens, the slope of each successive curve is less than the previous one. A decrease in slope corresponds to less  $I_D$  and more  $V_{DS}$ , which implies an increase in  $R_{DS}$ . This change in resistance can be exploited in a number of applications where voltage control of a resistance is useful.

### Q-point at the Origin

In certain amplifiers, you may want to change the resistance seen by the ac signal without affecting the dc bias in order to control the gain. Sometimes you will see a JFET used as a variable resistance in a circuit where both  $I_D$  and  $V_{DS}$  are set at 0, which means that the Q-point is at the origin. A Q-point at the origin is achieved by using a capacitor in the drain circuit of the JFET. This makes the dc quantities  $V_{DS} = 0V$  and  $I_D = 0mA$ , so the only variables are  $V_{GS}$  and  $I_d$ , the ac drain current. At the origin you have the ac drain current controlled by  $V_{GS}$ . As you learned earlier, trans-conductance is defined as a change in drain current for a given change in gate-to-source voltage. So, the key factor when you bias at the origin is the trans-conductance. This figure shows the characteristic curves expanded at the origin. Notice that the ohmic region extends into the third quadrant.



So friends here we come to the end of our discussion in this lecture and therefore we sum up:

We learnt that

The Q-point in a JFET with voltage-divider bias is more stable than in a self-biased JFET.

Current-source bias increases the stability of a self-biased JFET.

A JFET used as a variable resistor is biased in the ohmic region.

To bias in the ohmic region,  $I_D$  must be much smaller than  $I_{DSS}$ .

The gate voltage controls  $R_{DS}$  in the ohmic region and finally we learnt that

When a JFET is biased at the origin, the ac channel resistance is controlled by the gate voltage.

So that is it in today's lecture in the next lecture we shall talk about the MOSFET characteristics, parameters and its biasing. So that is it for today thank you very much.