JEDEC STANDARD

Stub Series Terminated Logic for 1.8 V (SSTL_18)

JESD8-15A

Addendum 15 to JESD8 Series
(Revision of JESD8-15)

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STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18)

(From JEDEC Board Ballots JCB-02-36, JCB-02-37, JCB-02-55, JCB-02-56, JCB-02-57, JCB-02-83, JCB-02-119, and JCB-03-40 formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range, nominally 0 V to 1.8 V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages. The V_{DD} value is not specified in this standard; however V_{DD} and V_{DDQ} will have the same voltage level in many cases.

1.1 Standard Structure

The standard is defined in four clauses:

The first clause defines pertinent supply voltage requirements common to all compliant ICs.

The second clause defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The third clause specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments.

The fourth clause specifies requirements for differential signaling.

The full input reference level (V_{REF}) range specified is required on each IC in order to allow any SSTL_18 integrated circuit to receive signals from any SSTL_18 output driver.

1.2 Rationale and assumptions

The SSTL_18 standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage.

Actual selection of the resistor values is a system design decision and beyond the scope of this standard. However in order to provide a basis, the driver characteristics will be derived in terms of a typical 50 Ω environment.

While driver characteristics are derived from a 50 Ω environment, this standard will work for other impedance levels. The system designer will be able to vary impedance levels, termination resistors and supply voltage and be able to calculate the effect on system voltage margins. This is accomplished precisely because drivers and receivers are specified independently of each other. The standard defines a reference voltage V_{REF} which is used at the receivers as well as a voltage V_{TT} to which termination resistors are connected. In typical applications, V_{REF} and V_{TT} are nominally equal to $V_{DDQ}/2$.

2 Supply voltage and input logic levels

The standard defines both the ac and dc input signal values. Making this distinction is important for the design of the high gain, differential receivers that are required. The ac values indicate the voltage levels at which the receiver must meet its timing specifications. The dc values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the ac value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the dc threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform “ringing”. The relationship of the different levels is shown in Figure 1. An example of ringing is illustrated in the waveform.

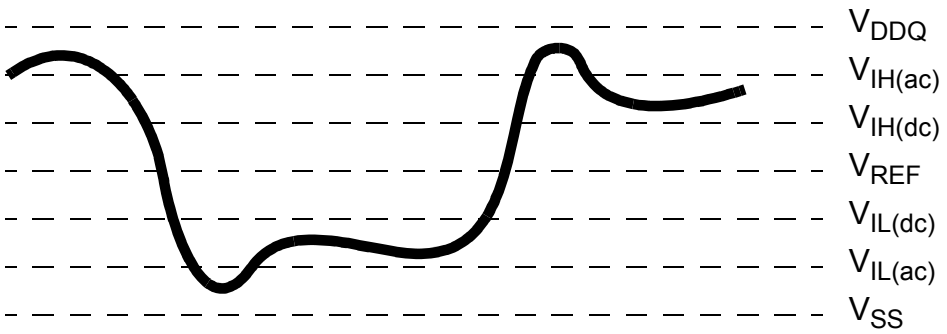

Figure 1 — SSTL_18 Input Voltage Levels

2.1 Supply Voltage Levels

Table 1 — Supply Voltage Levels

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{DDQ}	Output supply voltage	1.7	1.8	1.9	V	
V_{REF}	Input reference voltage	833	900	969	mV	1, 2
V_{TT}	Termination voltage	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3

NOTE 1 The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be (50 +/- 1)% * V_{DDQ} of the transmitting device, e.g., V_{REF} min = 0.49 * V_{DDQ} min and V_{REF} max = 0.51 * V_{DDQ} max. V_{REF} is expected to track variations in V_{DDQ}.

NOTE 2 Peak to peak ac noise on V_{REF} may not exceed +/- 2% of $V_{REF(dc)}$.

NOTE 3 V_{TT} is expected to track V_{REF} of the receiving device.

2.2 Input logic levels

Table 2 — DC input logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(dc)}$	dc input logic high	V_{REF} + 125	V_{DDQ} + 300	mV	1
$V_{IL(dc)}$	dc input logic low	-300	V_{REF} - 125	mV	1

NOTE 1 Within this standard, it is the relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device that determines noise margins. However, in the case of $V_{IH(dc)}$ max (i.e., input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented that supports SSTL_18 inputs but has no SSTL_18 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 2.2 V (V_{DDQ} max + 300 mV).

Table 3 — AC input logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(ac)}$	ac input logic high	V_{REF} + 250	-	mV	
$V_{IL(ac)}$	ac input logic low	-	V_{REF} - 250	mV	

2.3 AC test conditions

The ac input test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.0 V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the ac input level. This is illustrated in Figure 2.

Table 4 — AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1, 4
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1, 2
SLEW	Input signal minimum slew rate	1.0	V/ns	3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test. Table 1 identifies the V_{REF} range supported in SSTL_18.

NOTE 2 Compliant devices must still meet the $V_{IH(ac)}$ and $V_{IL(ac)}$ specifications under actual use conditions.

NOTE 3 The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in Figure 2, consistent with the specifications of Tables 2 and 3. This is not a monotonicity requirement: ringing is still allowed as shown in Figure 1.

NOTE 4 ac test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis that the device will meet its timing specifications under all supported voltage conditions.

2.3 AC test conditions (cont'd)

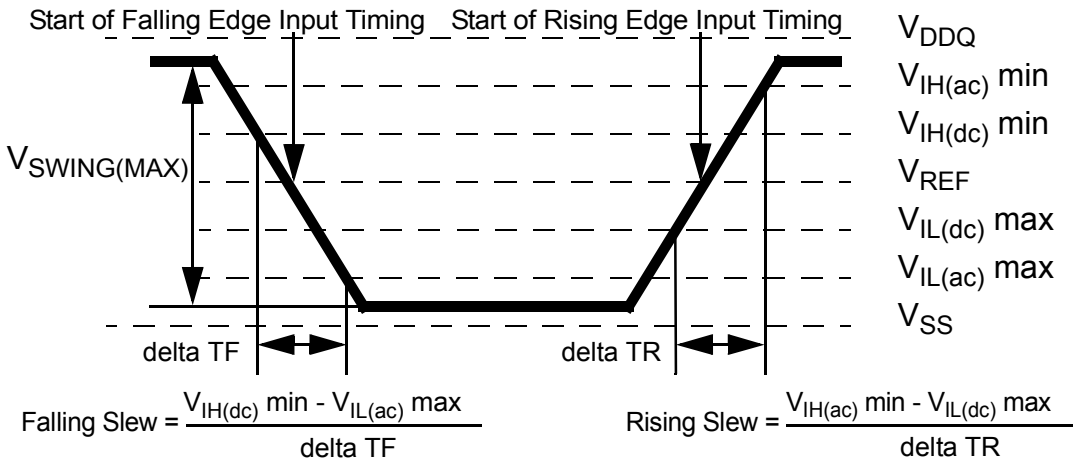

Figure 2 — AC Input Test Signal Waveform

3 SSTL_18 Output Buffers

3.1 Overview

This specification sets minimum requirements for output buffers such that when they are applied within the range of power supply voltages specified in SSTL_18 and are used in conjunction with SSTL_18 input receivers, then the input receiver specifications can be met or exceeded. The specifications are quite different from traditional specifications, where minimum values for V_{OH} and maximum values for V_{OL} are set that apply to the entire supply range. In SSTL_18, the input voltage provided to the receiver depends on the driver as well as on the termination voltage and termination resistors. Figure 3 shows the typical dc environment that is presented to the output buffer.

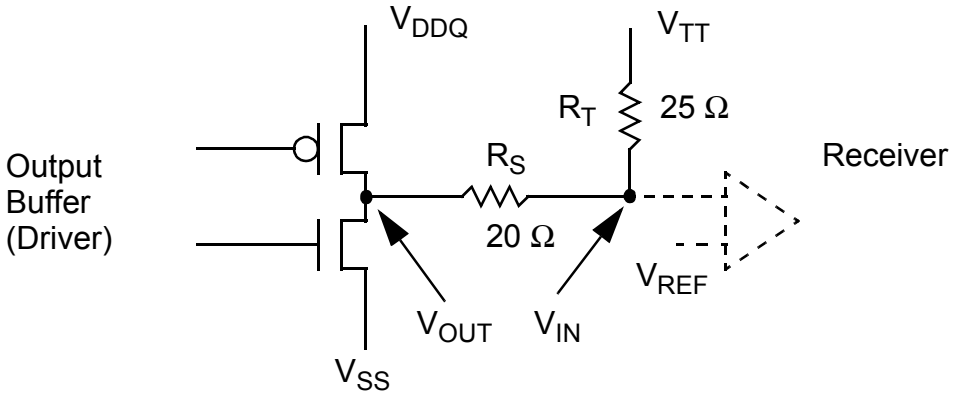

Figure 3 — Typical output buffer (driver) environment

In this environment, MOS output devices are deep into their triode region, so SSTL_18 driver characteristics are specified to ensure a driver output resistance (R_{ON}) no greater than 21 Ω at the minimum V_{DDQ}. It is understood that MOS devices are not perfectly linear, but designers are expected to scale up as needed to ensure that they meet the required operating points.

3.2 SSTL_18 output buffers

3.2.1 Push-pull output buffer for symmetrically double parallel terminated loads with series resistor (V_{TT} = 0.5 * V_{DDQ})

Table 5 — Output dc current drive

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{OH(dc)}$	Output minimum source dc current	-13.4	-	mA	1, 3, 4
$I_{OL(dc)}$	Output minimum sink dc current	13.4	-	mA	2, 3, 4

NOTE 1 V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

NOTE 2 V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 Ω for values of V_{OUT} between 0 V and 280 mV.

NOTE 3 The dc value of V_{REF} applied to the receiving device is set to V_{TT}

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 Ω load line to define a convenient driver current for measurement.

3.2.2 SSTL_18 output ac test conditions

This testing regimen is used to verify SSTL_18 output buffers (push-pull output buffers designed for symmetrically double parallel terminated loads with series resistor).

This clause is added to set the conditions under which the driver ac specifications can be tested. The test circuit is assumed to be similar to the circuit shown in Figure 4. The ac test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 6 assumes that ± 335 mV must be developed across the effectively 25 Ω termination resistor at V_{IN} (13.4 mA * 25 Ω = 335 mV). With a series resistor of 20 Ω this translates into a minimum requirement of 603 mV swing relative to V_{TT}, at the output of the device
(13.4 mA * 45 Ω = 603 mV).

3.2 SSTL_18 output buffers (cont'd)

3.2.2 SSTL_18 output ac test conditions (cont'd)

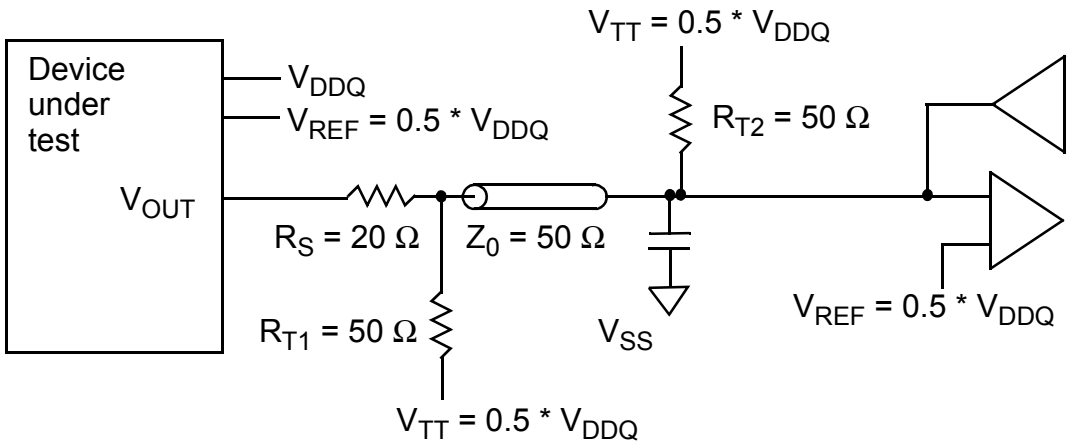

Figure 4 — Example of SSTL_18 symmetrically double parallel terminated output load with series resistor

Table 6 — AC Test Conditions

Symbol	Condition	Value	Units	Notes
V_{OH}	Min. required output pull-up under ac test load	V_{TT} + 603	mV	
V_{OL}	Max. required output pull-down under ac test load	V_{TT} - 603	mV	
V_{OTR}	Output timing measurement reference level	0.5 * V_{DDQ}	mV	1

NOTE 1 The V_{DDQ} of the device under test is referenced.

3.3 SSTL_18 noise margin

SSTL_18 output devices are characterized for a linear 21 Ω maximum output resistance (R_{ON}). The noise margin at the receiver under worst-case conditions is thus calculated as follows:

Assume R_S = 20 Ω and R_T = 25 Ω.

V_{DDQ} min = 1.7 V

V_{REF} min = 0.49 * V_{DDQ} min = 833 mV

$V_{TT} = V_{REF}$ min + 40 mV = 873 mV

$V_{IN} = V_{TT} * (R_{ON} + R_S)/(R_{ON} + R_S + R_T)$ = 873 mV * 41 Ω / 66 Ω = 542 mV

$V_{REF} - V_{IN}$ = 833 mV - 542 mV = 291 mV

$V_{IN(ac)}$ min = 250 mV (from Table 3).

3.3 SSTL_18 noise margin (cont'd)

As described, the receiver sees an input of 291 mV and only requires $V_{IN(ac)}$ min = 250 mV, for a gross margin of 41 mV. System designers may allocate this margin as judgment dictates. An SSTL_18 driver meeting these conditions while driving low would have the operating point:

$I_{OUT} = I_{OL} = (V_{TT} - V_{IN})/R_T = (873\ mV - 542\ mV) / 25\ \Omega = 13.24\ mA$

$V_{OUT} = V_{OL} = V_{IN} - I_{OUT} * R_S = 542\ mV - 13.24\ mA * 20\ \Omega = 277.2\ mV$

A similar calculation may be done for the case where the receiver is driven high. In either case, the resulting values are shifted along a 21 Ω load line to establish the output dc current drive requirements given in Table 5.

4 Other applications (For reference only)

The specifications for SSTL_18 are based on an environment comprising both series and parallel terminating resistors. In this non-binding section, some derived applications are shown. Clearly it is not the intention to show all possible variations in this standard.

4.1 Push-pull output buffer for source series and single parallel terminated loads, single destination

Applications exist where a signal source may reside at some distance from a single load. In this case, it may be advantageous to series terminate the signal source and parallel terminate at the load. An example of this situation is shown in Figure 5.

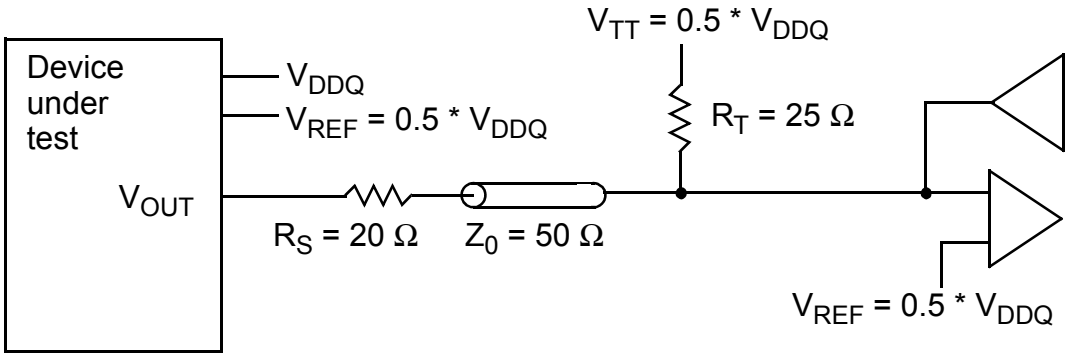

Figure 5 — Example of SSTL_18 symmetrically single parallel terminated output load with series resistor, single or lumped load shown

4.2 Push-pull output buffer for source series and single parallel terminated loads, multi-drop bus

Particularly in memory systems, a signal source may reside at some distance from several relatively closely spaced loads. In this case, it may be advantageous to series terminate the signal source and parallel terminate at or beyond the load farthest from the source. An example of this situation for two loads is shown in Figure 6.

4.2 Push-pull output buffer for source series and single parallel terminated loads, multi-drop bus (cont'd)

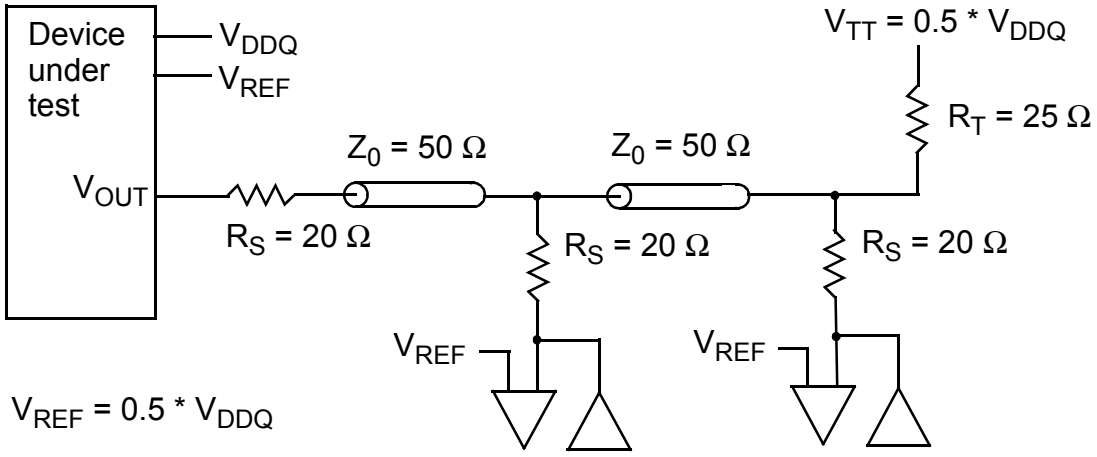

Figure 6 — Example of SSTL_18 symmetrically single parallel terminated output load with series resistor, multi-drop bus

4.3 Push-pull output buffer for source series terminated loads

In some applications the system designer may wish to terminate at the signal source rather than at the end of the transmission line. One advantage of this approach is that there is no need for a V_{TT} power supply. An example is shown in Figure 7. A larger value of R_S than that shown in the Figure may be chosen in order to provide a better termination of the reflected wave.

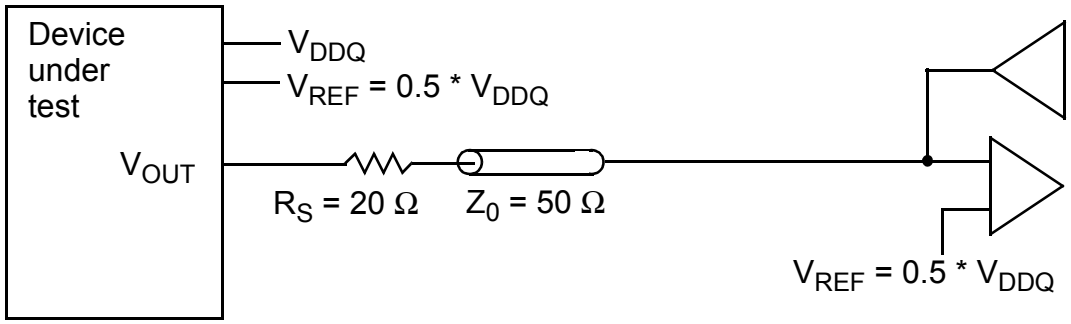

Figure 7 — Example of SSTL_18 source series terminated load

4.4 Push-pull output buffer for symmetrically single parallel terminated loads

Sometimes the system application requires longer transmission lines that will only be terminated at one end. An example of this may be address drivers on a memory board. An example is shown in Figure 8.

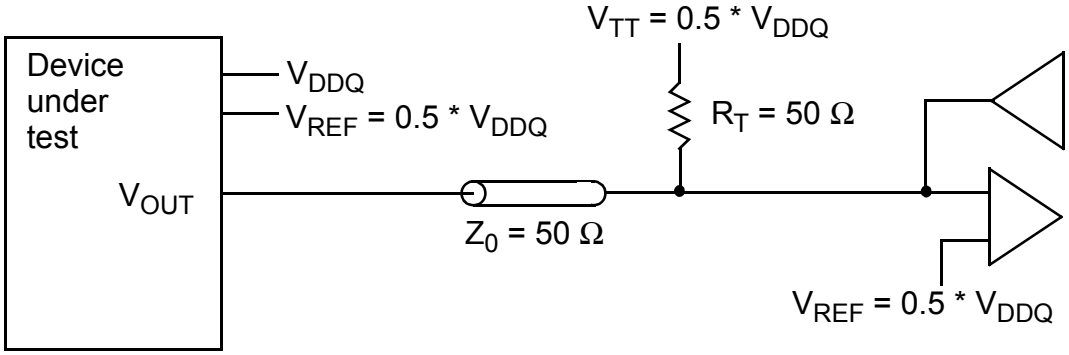

Figure 8 — Example of SSTL_18 symmetrically single parallel terminated load

4.5 Push-pull output buffer for symmetrically double parallel terminated loads

Finally, the system designer may require a bus system which must be terminated at both sides. However, the drivers are connected directly onto the bus so there are no stubs present. In that case, the designer may decide to eliminate the series resistors entirely as shown in Figure 9.

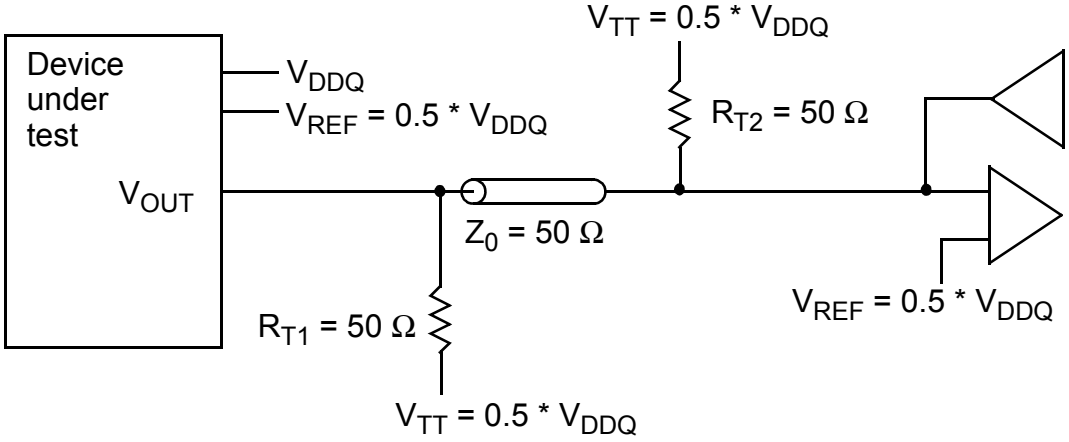

Figure 9 — Example of SSTL_18 symmetrically double parallel terminated load

4.6 Reference load for timing measurements

The reference load for timing measurement of SSTL_18 output drivers is shown in Figure 10.

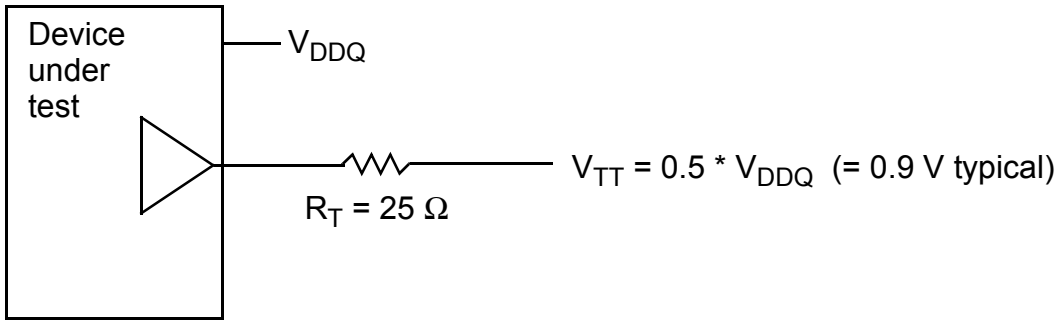

Figure 10 — Reference load for timing measurements

5 Differential signals

5.1 Overview

The following specifications describe differential signalling in SSTL_18 based systems. This is particularly relevant to DDRII DRAM clocks and data strobes, but the specification is intended to address any usage of SSTL_18 differential signals.

5.2 Differential input parameters

Table 7 — Differential dc input logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IN(dc)}$	dc input signal voltage	-0.3	V_{DDQ} + 0.3	V	1
$V_{ID(dc)}$	dc differential input voltage	0.25	V_{DDQ} + 0.6	V	2

NOTE 1 $V_{IN(dc)}$ specifies the allowable dc excursion of each differential input.

NOTE 2 $V_{ID(dc)}$ specifies the input differential voltage $|V_{TR}-V_{CP}|$ required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complementary" input level. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$ from Table 2.

5.2 Differential input parameters (cont'd)

Table 8 — Differential ac input logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{ID(ac)}$	ac differential input voltage	0.5	V_{DDQ} + 0.6	V	1
$V_{IX(ac)}$	ac differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

NOTE 1 $V_{ID(ac)}$ specifies the input differential voltage $|V_{TR}-V_{CP}|$ required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal. The minimum value is equal to $V_{IH(ac)}$ - $V_{IL(ac)}$ from Table 3.

NOTE 2 The typical value of $V_{IX(ac)}$ is expected to be about 0.5 * V_{DDQ} of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ}. $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross. See Figure 11.

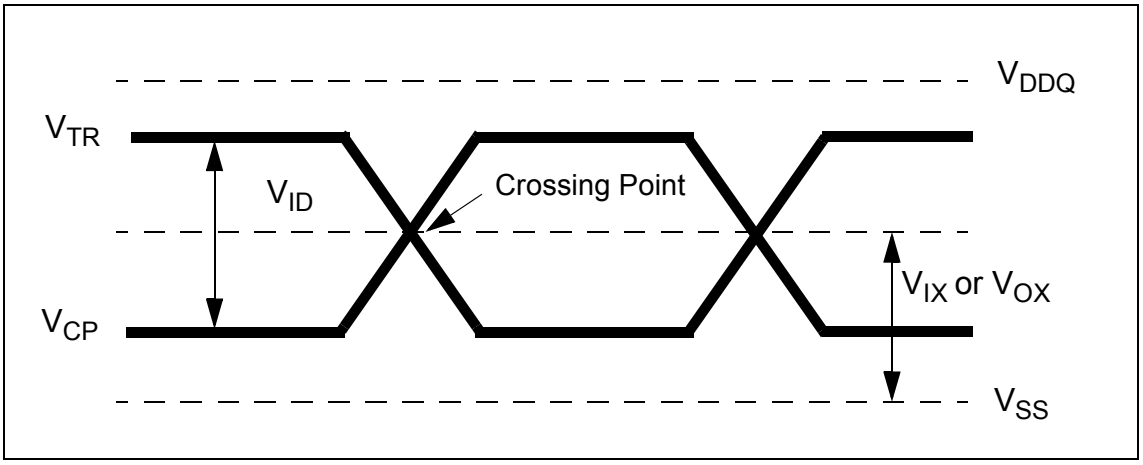

Figure 11 — SSTL_18 differential signal levels

5.3 AC test conditions

The differential ac test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.0 V peak-to-peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the differential ac input level. This is illustrated in Figure 12.

Table 9 — Differential AC Input Test Conditions

Symbol	Parameter	Min.	Max.	Units	Notes
V_r	Input timing measurement reference level	V_{IX} (cross point)		V	1
V_{SWING}	Input signal peak to peak swing voltage	-	1.0	V	2
SLEW	Input signal slew rate	1.0	-	V/ns	3

NOTE 1 In all cases, input waveform timing is referenced to the crossing point level (V_{IX}) of two input signals (V_{TR} and V_{CP}) applied to the device under test, where V_{TR} is the “true” input signal and V_{CP} is the “complementary” input signal. Table 8 identifies the $V_{IX(ac)}$ range supported for SSTL_18 differential inputs.

NOTE 2 A 1.0 V input pulse level is specified to allow consistent, repeatable test results in an automatic test equipment (ATE) environment. Compliant devices must meet the $V_{ID(ac)}$ specification under actual use conditions. See Table 8.

NOTE 3 The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges, consistent with Figure 2 and Tables 2 and 3 of this specification.

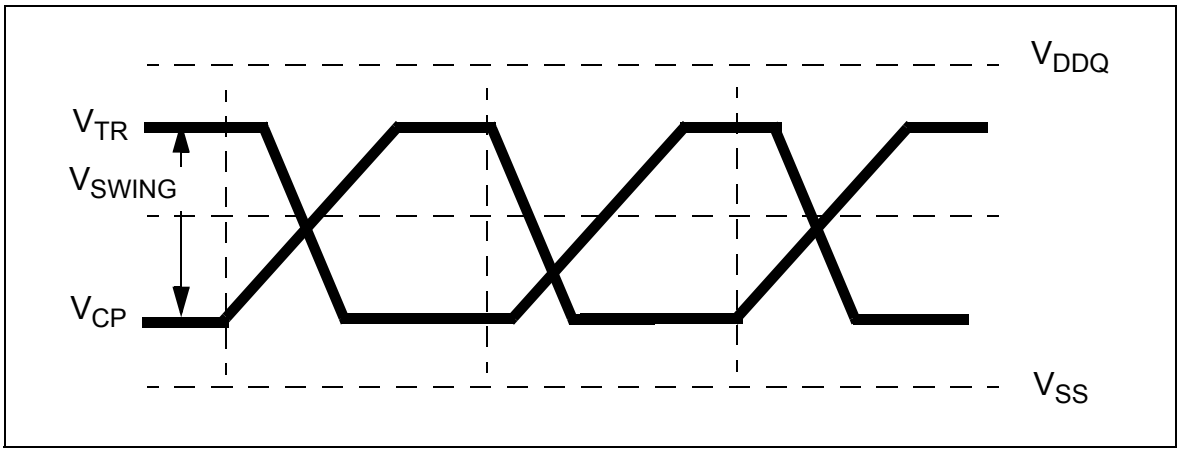

Figure 12 — Differential ac input test signal wave form

5.4 Differential output parameters

Differential outputs may be created using either true differential drivers or by combining pairs of SSTL_18 compliant, single-ended drivers driven from true and complementary signals. As a result, differential output parameters are assumed to be identical to those for single-ended outputs as given in Section 3, except where additional specifications are provided in Table 10.

Table 10 — Differential AC Output Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{OX(ac)}$	ac differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

NOTE 1 The typical value of $V_{OX(ac)}$ is expected to be about 0.5 * V_{DDQ} of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ}. $V_{OX(ac)}$ indicates the voltage at which differential output signals must cross. See Figure 11.

5.5 Example of SSTL_18 differential signals (Reference Only)

For reference only, Figure 13 shows differential inputs independently terminated with 25 Ω resistors. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ must satisfy Table 5.

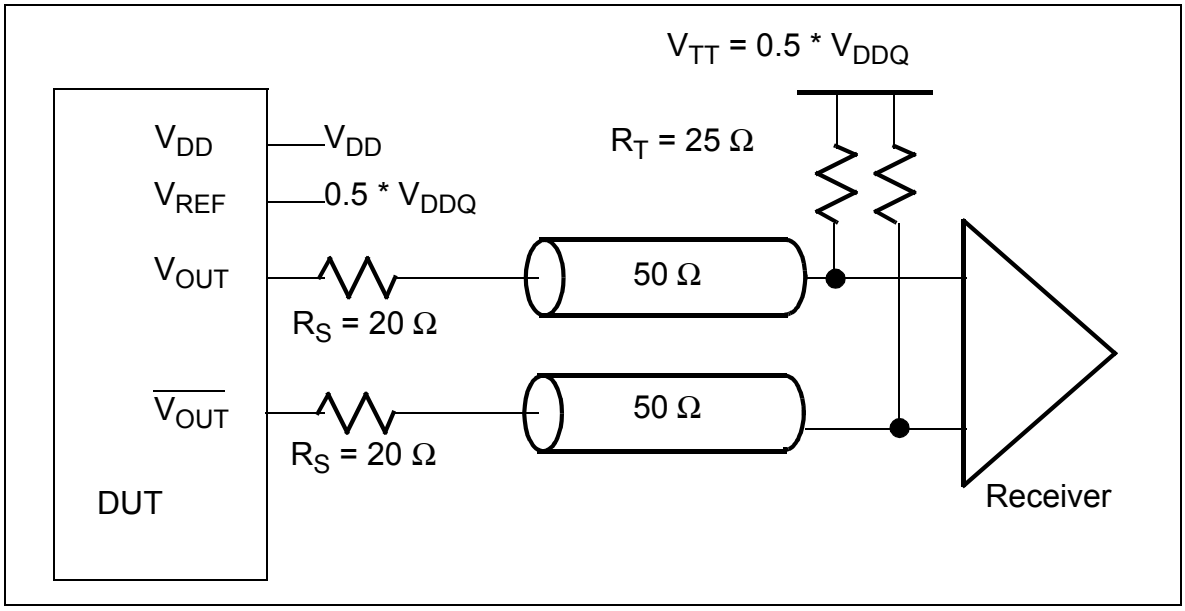

Figure 13 — Example of SSTL_18 differential signalling using series resistors and independent parallel termination resistors.

5.6 Example of SSTL_18 differential clock signals (Reference Only)

For reference only, Figure 14 shows a differential clock with a 100 Ω differential termination resistor. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ must satisfy Table 5.

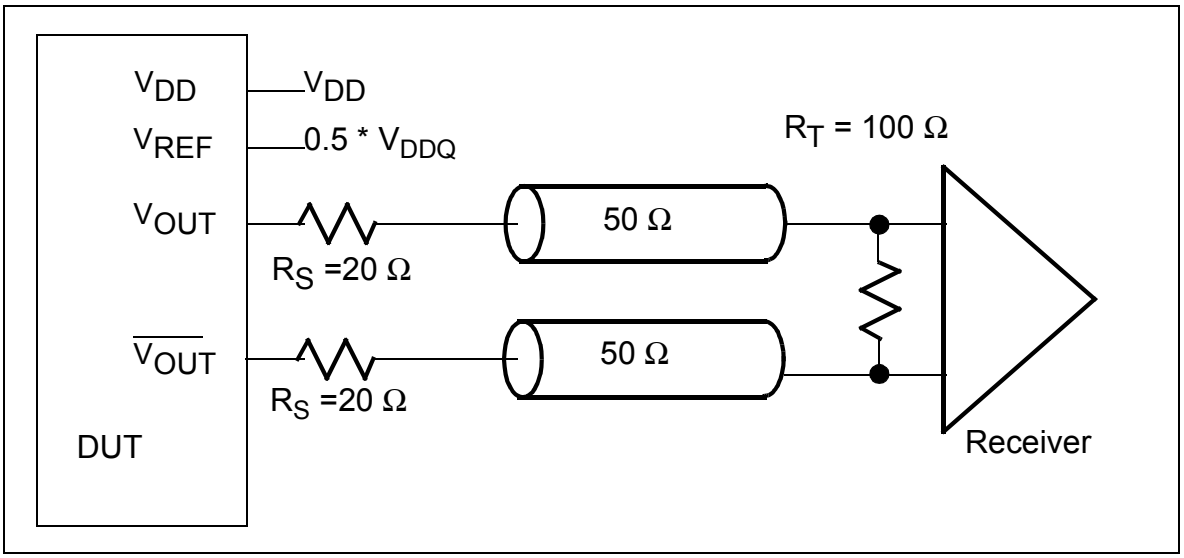

Figure 14 — Example of SSTL_18 differential signalling using series resistors and a differential termination resistor.

Table 11 — V_{ISO} Specifications (Reference Only)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ISO}	Input signal offset voltage	0.5 * V_{DDQ}		V	1
ΔV_{ISO}	Differential common mode stability	-	+200	mV	2

NOTE 1 The value of V_{ISO} is expected to be $(|V_{TR}+V_{CP}|)/2$ in case of each differential pair directly terminated by a 100 Ω resistor, where V_{TR} is the "true" input signal voltage and V_{CP} is the "complementary" input signal voltage, respectively. See Figure 15.

NOTE 2 ΔV_{ISO} is the allowed variation in the input signal offset voltage, V_{ISO}. See Figure 15.

5.6 Example of SSTL_18 differential clock signals (Reference Only) (cont'd)

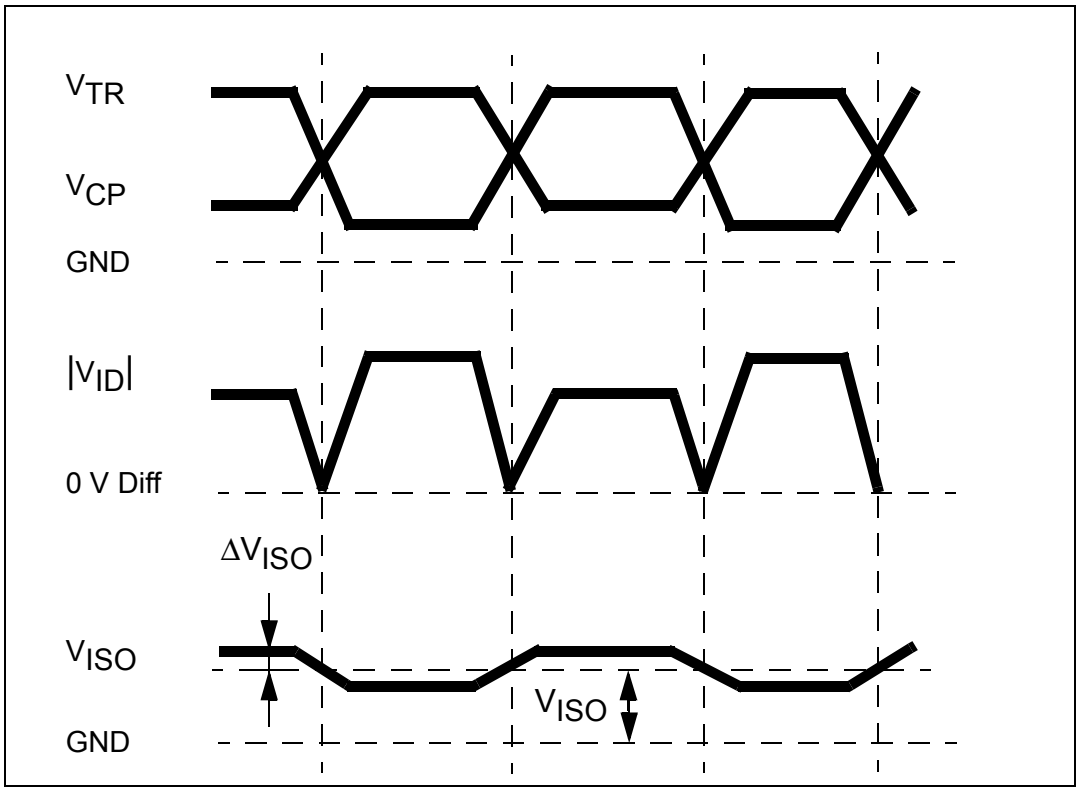

Figure 15 — Input signal offset voltage (Reference Only)

6 Annex A (informative) Differences between JESD8-15A and JESD8-15

This table breifly describes most of the changes made to entries that appear in this standard, JESD8-15A, compared to its predecessor, JESD8-15 (October 2002). If the change to a concept involves any words added or deleted, it is included. Punctuation changes may not be included.

Location	Description of Change
Page 2, 1st paragraph, 5th sentence	deleted 'for a sufficient period (see t_s below)'
Page 2, Figure 1	Deleted all references to t_s
Page 2	Deleted paragraph of text below Figure 1
Page 10	Added subclause 4.6
Page 10	Added Figure 10
Page 11 - 15	Original referencs to Figures 10 - 14 in subclause 5.2 through 5.6 were modified (incremented) to account for the addition of Figure 10.

Standard Improvement Form **JEDEC JESD8-15A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

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Submitted by

Name: _____ Phone: _____

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