Theory, Practice, and Fundamental Performance Limits of High-Speed Data Conversion Using Continuous-Time Delta-Sigma Modulators

by

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A Ph.D. thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy

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November 20, 1998

The undersigned recommend to the Faculty of Graduate
Studies and Research acceptance of the thesis

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Acknowledgments

For research inspiration, thanks to Omid Shoaei and Lars Risbo for their thought-provoking Ph.D. theses, Joe Jensen and Gopal Raghavan at HRL for their paper which got me interested in high-speed $\Delta\Sigma$M, and big thanks to Weinan Gao for discussions on theory and for allowing me access to his circuit design for simulation and testing purposes which resulted in a much more practical and relevant final thesis for me. I am grateful to him.

At Nortel, thanks to Robert Hadaway for access to the SiGe process, Sorin Voinigescu and Dave Marchesan for assistance with layout and simulation, Etienne Bernard and Marie Quinn for die cutting, José Macedo and Glen Tiegs for packaging suggestions, Icy Jackson for packaging the test chips, and big thanks to Dr. Peter Schvan for all his help getting me access to the building and computer system and for allowing me to use the SPICE files for his original prototype.

For modulator testing, thanks to Sergiy Uhanov and Nagui Mikhail for help with procuring and calibrating measurement equipment, big thanks to Joe Jensen and Gopal Raghavan at HRL for letting me capture bit streams on their high-speed oscilloscope, and biggest thanks to Philip J. Lauzon for his tireless design, redesign, and assembling of printed circuit boards.

Most of all, thanks to my supervisor, Martin Snelgrove, for seeing me through six years of graduate school and encouraging me, and to Melissa Fritz for putting up with my schedule during the last year and supporting me.

Abstract

We consider the design of high-speed continuous-time delta-sigma modulators for analog-to-digital conversion. Many of the nonidealities that affect performance in discrete-time modulators do likewise in continuous-time modulators, yet there are three additional important considerations unique to continuous-time modulators. The first, excess loop delay, is the time delay between the quantizer clock and the output of the feedback, which affects stability and dynamic range; its effect can be reduced by employing return-to-zero-style DACs and feedback coefficient tuning. The second, clock jitter, whitens the output spectrum in the quantization noise notch and lowers SNR; a carefully-designed VCO will alleviate its effects for all but very wideband or high-resolution modulators. The third, quantizer metastability, also whitens the output spectrum and lowers SNR; it is essential to use a three half-latch quantizer over a simple master/slave design to provide extra regeneration, and even then it is best not to clock faster than about 5% of maximum transistor switching speed. A design procedure is given for band pass modulators whose intended application is conversion of analog signals at one quarter of the sampling frequency, and a fabricated 4GHz modulator for 1GHz signal conversion is simulated, tested, and redesigned to improve its performance from 6 bits to 10 bits. Finally, the appropriateness of high-speed continuous-time delta-sigma modulation is considered for various applications.

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List of Abbreviations and Symbols

Abbreviations

A/D	Analog-to-digital
ADC	Analog-to-digital converter; analog-to-digital conversion
AGC	Automatic gain compensation
BJT	Bipolar junction transistor
BP	Band pass
BV_{CEO}	Collector-emitter breakdown voltage with base open
CM	Common-mode
CT	Continuous time
DAC	Digital-to-analog converter
DEM	Dynamic element matching
DFT	Discrete Fourier transform
DNL	Differential nonlinearity
DPW	DAC pulse width
DR	Dynamic range
$\Delta\Sigma$M	Delta-sigma modulator; delta-sigma modulation
DSP	Digital signal processing
DT	Discrete time

ECL	Emitter-coupled logic
FFT	Fast Fourier transform
GB	Gain-bandwidth
HBT	Heterojunction bipolar transistor
HNRZ	Half-delayed non-return-to-zero
HRZ	Half-delayed return-to-zero
IBN	In-band noise
i.i.d.	Independent and identically-distributed
IIP_3	Input third-order intercept point
INL	Integral nonlinearity
LNA	Low-noise amplifier
LP	Low pass
M/S	Master/slave
MSA	Maximum stable amplitude
NRZ	Non-return-to-zero
NTF	Noise transfer function
OOBG	Out-of-band gain
OSR	Oversampling ratio
pdf	Probability distribution function
RHS	Right-hand side
rms	Root mean square
RK4	Fourth-order Runge-Kutta numerical integration
RZ	Return-to-zero
SC	Switched capacitor

SFDR	Spurious-free dynamic range
S/H	Sample and hold
SI	Switched current
SiGe	Silicon germanium
SNDR	Signal-to-noise-plus-distortion ratio
SNR	Signal-to-noise ratio
SQNR	Signal-to-quantization-noise ratio
STF	Signal transfer function
VCO	Voltage-controlled oscillator
ZCT	Zero-crossing time

Roman Symbols

Equation and figure numbers in the list below refer to equations or figures where an example of the use of the symbol may be seen.

a_k	(2.12) Coefficient of $x(n-k)$
A	(Figure 7.10) Imbalance of transistors in multi-tanh block
A_0	(3.1) Op amp dc gain
A_0	Resonator center frequency gain
A_{clk}	(7.38) Clock voltage magnitude
A_i	(5.1) Gain of block $\hat{G}_i(s)$
b	Input tone bin number
b_k	(2.12) Coefficient of $y(n-k)$
B_i	(4.27) Zero-placement feedback coefficients
c_k	(2.12) Coefficient of $u(n-k)$

C	(2.15) Capacitance
C	(7.13) BP rsonator tank capacitance
C_μ	Base-collector capacitance
D	Number of emitter diodes in multi-tanh block
e	(Figure 2.2) Quantization noise in linear model
$e(n)$	(5.11) Jitter-induced error sequence
$E(z)$	(2.1) $\mathcal{Z}$-transform of e
f	Frequency
f_c	(5.21) Carrier frequency
f_{max}	Transistor unity power gain frequency
f_n	(5.22) Offset from f_c at which phase noise is measured
f_N	(2.4) Nyquist frequency
f_s	(2.4) Sampling frequency
f_T	(4.12) Transistor unity current gain frequency
g_m	(2.15) Transconductance
$G(z)$	(2.11) DT prefilter transfer function
$\hat{G}(s)$	(2.14) CT prefilter transfer function
G_g, G_q	(7.13) Transconductance of gain and Q-tuning blocks
$\hat{G}_i(s)$	(5.1) Generalized CT gain block
$h(n)$	(4.3) DT loop transfer function impulse response
$\hat{h}(t)$	(4.3) CT loop transfer function impulse response
$H(z)$	(2.1) DT loop transfer function
$\hat{H}(s)$	(2.14) CT loop transfer function
$H(z, \tau_d)$	(4.19) DT loop transfer function of CT $\hat{H}(s)$ with excess loop delay τ_d

I_{Dout} (Figure 7.26) DAC output current

I_g (7.13) Gain transconductor output current

I_k (7.33) Feedback DAC current

I_{le} (Figure 7.21(b)) Current through R_{le}

I_q (7.13) Q-enhancement transconductor output current

I_{tail} (Figure 7.10) Tail current in multi-tanh block

k Boltzmann's constant

k_1, k_2 (2.15) Second-order LP $\Delta\Sigma$M feedback parameters

k_2, k_4 (Figure 7.2) BP modulator feedback parameters

k_i (4.27) General feedback coefficients

k_{h2}, k_{h4} (Figure 7.2) HRZ feedback coefficients in BP modulator

k_{ni} (4.37) NRZ feedback coefficients

k_{r2}, k_{r4} (Figure 7.2) RZ feedback coefficients in BP modulator

$\bar{k}_{r2}$, $\bar{k}_{r4}$, $\bar{k}_{h2}$, $\bar{k}_{h4}$ (7.19) Nominal feedback current levels

k_{ri}, k_{hi} (4.26) RZ/HRZ feedback coefficients

K (Figure 2.10) Number of averaged periodograms

l Loop filter pole multiplicity

l (7.43) Metal length in μm

L (7.13) BP resonator tank inductance

L_{par} (7.43) Parasitic metal inductance in nH

L_p (7.3) Equivalent tank parallel inductance

L_s (7.3) Equivalent tank series inductance

m (Figure 2.6) Order of $\Delta\Sigma$M loop filter

n (2.6) Sampling instant number, $t = nT_s$

n_c	(5.21) VCO phase noise
n_t	(4.12) Number of transistors in feedback path
N	(2.6) Length of output bit sequence
NTF(z)	(2.2) Noise transfer function
p	(3.1) Leaky integration proportionality constant
$p_x(\alpha)$	(Figure 6.9(b)) pdf of quantizer input voltage
$\hat{P}(f)$	CT-domain power spectrum
$P(n)$	(2.7) DT-domain power spectrum, $n = 0, 1, \ldots, N/2$
P_n	(2.9) Total noise power in baseband
Q	Quality factor
Q_L	(7.2) Inductor quality factor
Q_{res}	Resonator quality factor
Q_n	Bipolar transistor n
R	(7.13) Resistance of inductor in resonant tank
$\hat{r}_D(t)$	(4.3) Time domain feedback DAC impulse response
$\hat{R}_D(s)$	(4.2) Frequency domain feedback DAC impulse response
R_{DAC}	(Figure 7.26) DAC current-source resistance
R_{ef}	(Figure 7.21) Emitter follower resistance
R_{in}	Input resistance
R_{la}	(Figure 7.21(b)) Latch amplifier load resistance
R_{le}	(Figure 7.21(b)) Latch current-source transistor emitter resistance
R_p	(7.3) Equivalent tank parallel resistance
R_{pa}	(Figure 7.21(a)) Preamp amplifier load resistance
R_{par}	Parasitic metal resistance

R_{pe} (Figure 7.21(a)) Preamp current-source transistor emitter resistance

R_s (7.3) Equivalent tank series resistance

s Continuous-time frequency variable, $s = \sigma + j\omega$

s_k (4.6) kth pole of $\hat{H}(s)$

STF(z) (2.2) Signal transfer function

t Time

Δt_{jitt} (7.39) Time jitter

t_n (5.4) Time at sample n including jitter

T Absolute emperature

T_s Sampling period

u (2.12) DT input to $\Delta\Sigma$M

$\hat{u}$ (2.15) CT input to $\Delta\Sigma$M

u_{min}, u_{max} (7.5), (7.6) Minimum, maximum BP modulator input signals

$U(z)$ (2.1) $\mathcal{Z}$-transform of u

$\hat{U}(s)$ (2.14) Laplace transform of $\hat{u}$

$\overline{v_{nc}}$ (7.41) Clock transistor input-referred noise voltage

$\overline{v_{ng1}}$ (7.4) Input-referred noise for G_{g1}

Δv_{noi} (7.39) Total clock waveform noise

v_{sl} Slope of latch input voltage relative to full scale

v_x Latch input voltage relative to full scale

V_{BUF} (Figure 7.24) Modulator output swing control voltage

V_{CB} (Figure B.3(a)) Latch current control voltage

V_{CC} Power supply voltage

V_{CDB} (Figure 7.17) V_{IB} control voltage

V_{clk} (7.38) Clock voltage waveform

V_G (Figure 7.17) Voltage to generate G_g

V_{h2}, V_{h4} HNRZ/HRZ DAC control voltages

V_{IB} (Figure 7.17) Q-tuning multi-tanh block common-mode voltage

V_{k+}, V_{k-} (Figure 7.26) DAC control voltages

V_{Lmid} (Figure 7.21(b)) Intermediate latch voltage

V_{Lout} (Figure 7.21(b)) Latch output voltage

V_{n2}, V_{n4} NRZ DAC control voltages

V_{Pin} (Figure 7.21(a)) Preamp input voltage

V_Q (Figure 7.17) Voltage to generate G_q

V_{r2}, V_{r4} RZ DAC control voltages

V_{rd} (Figure 6.5) Differential regeneration voltage

w (7.43) Metal width in μm

$w(n)$ (2.8) Spectral windowing function

x (2.12) DT input to quantizer

x_2, x_4 (Figure 7.2) Band pass resonator outputs

$\hat{x}$ (4.1) CT input to quantizer

x_i (5.3) Output of gain block $\hat{G}_i(s)$

$\hat{x}_1$ (2.15) CT output of first integrator in double integration modulator

$\hat{x}_2$ (2.15) CT output of second integrator in double integration modulator

$X(z)$ (2.11) $\mathcal{Z}$-transform of x

$\hat{X}(s)$ (2.14) Laplace transform of $\hat{x}$

X_2 (7.13) Laplace transform of x_2

y (2.12) DT output of $\Delta\Sigma$M

$\hat{y}$	(Figure 4.2) CT output of $\Delta\Sigma$M
$Y(n)$	(2.6) DFT of y
$Y(z)$	(2.1) $\mathcal{Z}$-transform of y
$\hat{Y}(s)$	(2.14) Laplace transform of $\hat{y}$
z	(2.1) Discrete-time frequency variable, $z = \exp(sT)$
z_k	(4.6) kth pole of $H(z)$

Greek Symbols

(α, β)	(4.4) DAC pulse interval
β	Random variable for jitter distribution
β_n	(5.4) Jitter at sample n
Δ	Difference between adjacent quantizer output levels
δy	Difference between successive output samples, $y(n) - y(n-1)$
ϵ_{g1}, ϵ_{g2}	(7.7) Nonlinearity coefficients of G_{g1}, G_{g2}
$\bar{\epsilon}_{g2}$	(7.26) Normalized ϵ_{g2}
ϵ_{q1}, ϵ_{q2}	Nonlinearity coefficients of G_{q1}, G_{q2}
$\bar{\epsilon}_{q1}$, $\bar{\epsilon}_{q3}$	(7.25), (7.27) Normalized ϵ_{q1}, ϵ_{q3}
$\|\varepsilon\|_2$	(6.5) RMS least-squares matching error
$\|\varepsilon\|_\infty$	(6.5) Maximum least-squares matching error
γ_k	(7.21) DAC feedback current scale factor
κ	(Figure 4.6) Linearized quantizer gain
ρ_d	(4.11) Excess loop delay as a fraction of T_s, i.e., τ_d/T_s
ρ_r	DAC pulse rise time as a fraction of T_s, i.e., τ_r/T_s
σ	Standard deviation

σ_β	(5.12) Standard deviation of β
$\sigma_{\delta y}$	(5.12) Standard deviation of δy
σ_e	(5.12) Standard deviation of $e(n)$
σ_x	Standard deviation of $x(n)$
σ_{x_2}, σ_{x_4}	(7.22) Standard deviation of x_2, x_4
τ	Op amp dominant pole time constant
τ_d	(4.11) Excess loop delay
τ_r	DAC pulse rise time
τ_{rg}	Latch regeneration time constant
ω_0	Center frequency of band pass resonator
ω_i	(5.2) Center frequency of gain block $\hat{G}_i(s)$

Chapter 1

Introduction

1.1 Motivation

The late 1990s will perhaps be remembered as the start of the "system on a chip"-style of design and manufacturing: those engaged in building products for certain markets, cellular radio being a major one, are keen to cut costs and therefore gain a competitive edge by integrating all system functions onto a single substrate with as few external components as possible. This task is made much easier if analog signals, which is how any real-world quantity must inevitably be represented, are converted to digital form for on-chip processing. This helps in two main ways: digital signals are less susceptible to corruption by circuit noise and process variations, and more digital signal processing circuitry can be integrated into the same die area than analog circuitry. Thus, it is clear that analog-to-digital converter (ADC) circuits play an important role in modern integrated systems.

The three main performance measures of an ADC are its resolution (usually number of bits), its speed (how many conversions it does per second), and its power consumption, where customarily it is desired that the first two of these be maximized and the third minimized. There are many different styles of circuit that perform ADC; one particular style that has received a good deal of attention in the last fifteen years is the delta-sigma modulator (DSM or $\Delta\Sigma$M) [Nor97]. These circuits have found their niche in applications requiring very high resolution at low speeds (e.g., 20

bits at 500Hz [Tho94]) and audio converters (16 or more bits at 44kHz [Kwa96]), and they often work with very modest power budgets (2.3mW for an audio coder [vdZ97]). It is fair to say that for high resolution and/or low power at fairly low speeds (up to a few hundred kHz), delta-sigma modulation is the best ADC architecture choice.

The vast majority of $\Delta\Sigma$Ms have been built with discrete-time (DT) circuitry, very often switched-capacitor circuits. If circuit waveforms are to be allowed adequate settling time, the speed at which DT circuits are clocked must be restricted. These restrictions can be relaxed by employing continuous-time (CT) circuitry in place of DT circuitry. We noted last paragraph that DT $\Delta\Sigma$Ms already enjoy resolution and power advantages over other styles of ADC; perhaps CT $\Delta\Sigma$Ms could retain these advantages while operating at higher speeds? This question has been given increasing attention in the last few years as the need for high-resolution ADC at ever-higher speeds grows.

It is this same question that we address in this thesis. We shall see that the practice of building CT $\Delta\Sigma$Ms for high-speed conversion has proved more difficult than anticipated—they operate correctly, but they achieve lower resolution than their lower-speed counterparts. We study the reasons for this in the present work. Past work has identified some of the problems in specific architectures, but here we generalize these results to many architectures, explore the effect of some previously unidentified nonidealities, and explain as much as possible about what can be done to overcome their effects. Where feasible, we give simple formulas for prediction of performance limits. This thesis contains a moderate amount of emphasis on theory, but every effort is made to tie the theory to practice. This is made easier because we have an actual high-speed part to test.

1.2 Contributions

The introductory chapters of this thesis present summaries of the published literature in the following subjects:

- $\Delta\Sigma$M performance measurement;
- a $\Delta\Sigma$M nonideality literature survey;

- a CT $\Delta\Sigma$M literature survey.

The first and third of these are not summarized elsewhere to the author's knowledge and so are useful overviews, while the second is discussed in [Nor97, Chap. 11] for DT modulators but extended here for CT modulators. Thereafter follows the original material listed here.

1. The phenomenon of "excess loop delay" in $\Delta\Sigma$Ms has been identified as an important non-ideality in past work, though the study has been scattered among several papers. Here, we collect all the information into one place, use an improved mathematical technique, and apply it to previously-unstudied circuit architectures.

2. The effect of clocking a CT $\Delta\Sigma$M with an on-chip VCO having a certain phase noise specification is quantified for the first time.

3. A new method of system identification is proposed and illustrated for CT $\Delta\Sigma$Ms.

4. Quantizer metastability is identified as a mechanism of performance loss in CT $\Delta\Sigma$Ms and its effect characterized.

5. The tradeoffs and parameter selection criteria in the design of $f_s/4$ fourth-order band pass modulators are outlined and an explicit design procedure formulated.

6. Simulation and measurement results are presented on a fabricated fourth-order band pass modulator with a 4GHz clock. As well, design improvements which appear to better the performance significantly are suggested.

There are also many illustrative examples throughout the following chapters that clarify the concepts presented.

1.3 Organization

Chapter 2 introduces the concept of delta-sigma modulation, lists some of the fundamental modulator design choices, explains how modulator performance is measured, and briefly discusses time-domain simulation of $\Delta\Sigma$Ms.

Chapter 3 summarizes some issues surrounding the implementation of $\Delta\Sigma$Ms. We survey the literature that characterizes the effect of certain nonidealities in DT $\Delta\Sigma$Ms and explain how these apply to CT $\Delta\Sigma$Ms, then we list and briefly describe the important papers in CT $\Delta\Sigma$M. Finally, a summary of the performance achieved in published high-speed CT $\Delta\Sigma$Ms is given.

Chapter 4 is about excess loop delay in CT $\Delta\Sigma$Ms, which is delay between the clock edge and the effect of the output bit as seen at the feedback. We first expound on the equivalence between ideal DT and CT modulators, then explain what loop delay does to this equivalence, illustrating the performance lost in different modulator orders and architectures. As well, we look at methods for overcoming this performance loss.

Chapter 5 characterizes the effect of quantizer clock jitter on ideal CT $\Delta\Sigma$M performance and looks at the effect of clocking a CT $\Delta\Sigma$M with a practical integrated VCO with a given phase noise characteristic.

Chapter 6 analyzes quantizer metastability and its effect on high-speed CT $\Delta\Sigma$Ms and proposes what can be done to alleviate the performance loss it causes.

Chapter 7 presents design guidelines, analysis, simulation results, and test results for a fourth-order 4GHz band pass $\Delta\Sigma$M fabricated with SiGe HBTs for conversion of narrowband 1GHz analog signals to digital. We also redesign key portions of the modulator and estimate the performance improvement that would result.

Chapter 8 concludes the thesis with a discussion of the appropriateness of CT $\Delta\Sigma$M for applications requiring high-speed ADC and makes recommendations for future work.

Chapter 2

$\Delta\Sigma$M Concepts

In this chapter we explain what a delta-sigma modulator is and how it can be used for analog-to-digital conversion along with some of the basic design choices in $\Delta\Sigma$M design. We move on to how the performance of a $\Delta\Sigma$M is measured. Finally, we discuss some aspects of the time-domain simulation of $\Delta\Sigma$Ms, distinguishing discrete-time modulator simulation from continuous-time.

2.1 A Brief Introduction to $\Delta\Sigma$M

An overview of the $\Delta\Sigma$M concepts relevant for this work will be presented here. If it seems too cursory, the reader may turn to any of a number of excellent summary articles [Hau91, Can92b, Azi96, Can97] for a more detailed treatment.

2.1.1 Operating Principles

A $\Delta\Sigma$M ADC has three important components, depicted in Figure 2.1:

1. A *loop filter* or *loop transfer function* $H(z)$
2. A clocked quantizer
3. A feedback digital-to-analog converter (DAC)

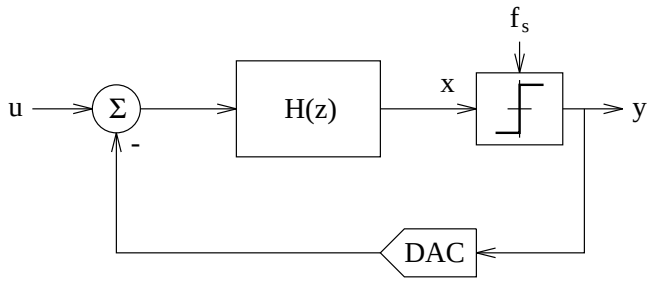


Figure 2.1: Basic components of a ΔΣM for ADC.

The quantizer is a strongly-nonlinear circuit in an otherwise linear system, which makes the behavior of ΔΣMs very complicated to investigate analytically [Gra90]. The basic idea of ΔΣ modulation is that the analog input signal is modulated into a digital word sequence with a spectrum that approximates that of the analog input well in a narrow frequency range and has the quantization noise "shaped" away from this range. An intuitive qualitative understanding of how this happens can be had by *linearizing* the circuit as shown in Figure 2.2. The quantizer is replaced by an adder

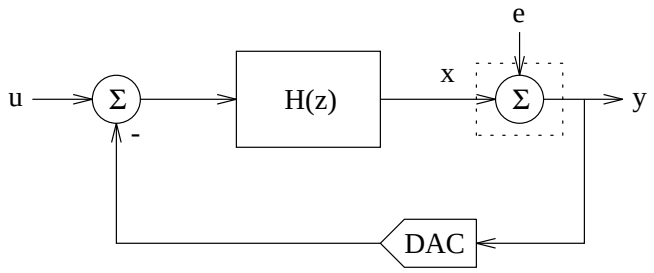


Figure 2.2: Linearizing the quantizer in a ΔΣM.

and we pretend that the quantization noise is "generated" by an input e which is independent of the circuit input u. The output y may now be written in terms of the two inputs u and e as

$$Y(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \quad (2.1)$$

$$= \mathrm{STF}(z)\cdot U(z) + \mathrm{NTF}(z)\cdot E(z) \quad (2.2)$$

where $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ are the so-called *signal transfer function* and *noise transfer function*. From (2.1) we see that the poles of $H(z)$ become the zeros of $\mathrm{NTF}(z)$, and that for any frequency

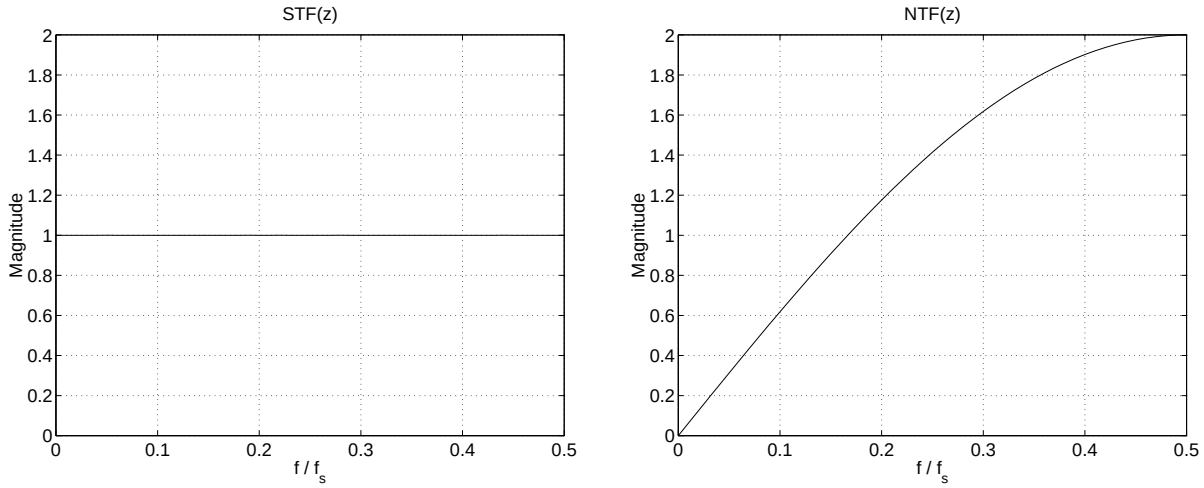


Figure 2.3: STF(z) and NTF(z) for circuit of Example 2.1.

where $H(z) \gg 1$,

$$Y(z) \approx U(z).$$

In other words, the output resembles the input most closely at frequencies where the gain of $H(z)$ is large.

Example 2.1: Consider the system of Figure 2.1 with a simple integrator $H(z) = 1/(z-1)$ as the loop filter and a one-bit quantizer which produces output bits with values ± 1. From (2.1) we can calculate

$$\text{STF}(z) = z^{-1},\ \text{NTF}(z) = 1 - z^{-1}. \tag{2.3}$$

These are depicted graphically in Figure 2.3 with $z = \exp(j2\pi f T_s)$. We have $H(z) \to \infty$ at dc (i.e., at $f = 0$), which means input signals near dc should be reproduced faithfully in the output bit stream. In fact, $|\text{STF}(z)| = 1$ everywhere, so we at least expect the *magnitude* of an input at any frequency to be reproduced at the output. As well, NTF$(z) \to 0$ at dc, and it increases away from dc; hence, the quantization noise is "shaped away from dc".

If we implement the system mathematically, simulate it in Matlab, and look at the power spectrum of the output bit stream, we obtain the plot shown in Figure 2.4. In

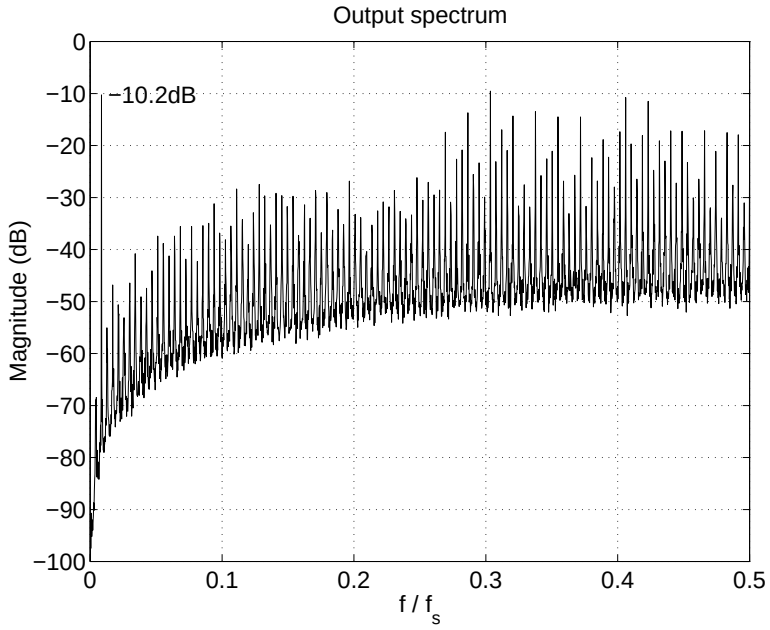


Figure 2.4: Simulated output bit stream power spectrum.

this example, the input tone had an amplitude of 0.434V and a frequency of $(8.545 \times 10^{-3})f_s$. Relative to the output levels of ± 1, we expect, and observe, an output signal power of $20\log_{10}(0.434/\sqrt{2}) = -10.2$dB. The quantization noise spectrum follows NTF(z) qualitatively at least, going to zero at dc and increasing away from dc, but it clearly contains tones spaced at an interval related to the input frequency. The usual assumption when linearizing the quantizer as in (2.1) is that the quantization noise spectrum is white, as well as uncorrelated with the input; while the former is often true, the latter is never exactly true though the correlation is often so complex as to be all but impossible to determine. The linearization is thus not really valid, but it often gives correct qualitative predictions of modulator performance. However, we usually require *quantitative* accuracy, and thus for the most part we eschew linearization throughout this thesis. □

Note what is implied in this example: the quantization noise is reduced only in a small bandwidth, that is, a bandwidth much smaller than the sampling frequency f_s. If we wish to obtain high

converter resolution, then the signal must be bandlimited to a value much smaller than f_s. This means that for a signal with Nyquist rate f_N, we require $f_N \ll f_s$, which is the same as saying we must sample much *faster* than the Nyquist rate. ΔΣMs, therefore, are so-called *oversampled converters*, with an *oversampling ratio* defined as

$$\text{OSR} \equiv f_s / f_N. \tag{2.4}$$

How is the high-speed low-resolution quantizer output converted to multibit output samples at the Nyquist rate? A complete block diagram of a ΔΣM ADC is shown in Figure 2.5; it includes

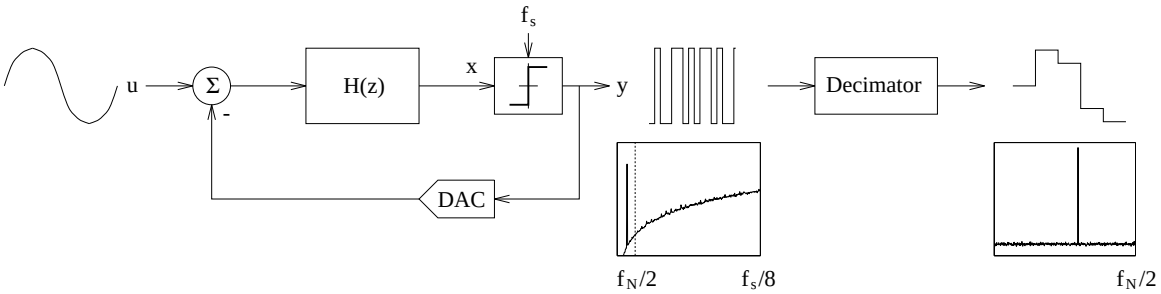


Figure 2.5: Complete ΔΣM ADC block diagram including decimator.

a modulator followed by a circuit called a *decimator*. The decimator's purpose is twofold: it *decimates*, i.e., reduces in frequency, the high-rate bit stream *and* removes everything outside the desired band with a filter. Typical time domain and frequency domain waveforms at the modulator and decimator outputs are shown in the figure.

We do not go into detail regarding the design of the decimator, instead preferring to concentrate on designing a ΔΣM to obtain an output bit stream with desirable properties. Decimator design is reasonably well-understood and is covered in [Can92a]. As is customarily done in work about ΔΣM, we shall assume that the modulator output is filtered by a brick-wall filter with a gain of 1 in the signal band and 0 elsewhere.

2.1.2 Design Choices

There is a myriad of design choices for ΔΣMs. Very briefly, the major ones are listed and described here.

Order of $H(z)$ and oversampling ratio

Example 2.1 featured a single integrator, a first-order transfer function, for $H(z)$. In general, the order of $H(z)$ (which must be strictly proper to ensure causality) is the maximum power of z in the denominator. It is possible to use a second-, third-, or even higher-order $H(z)$ as a loop filter; generally, a converter of order m is built as a cascade of m integrators usually surrounded with feedforward and feedback coefficients [Cha90] as depicted in Figure 2.6.

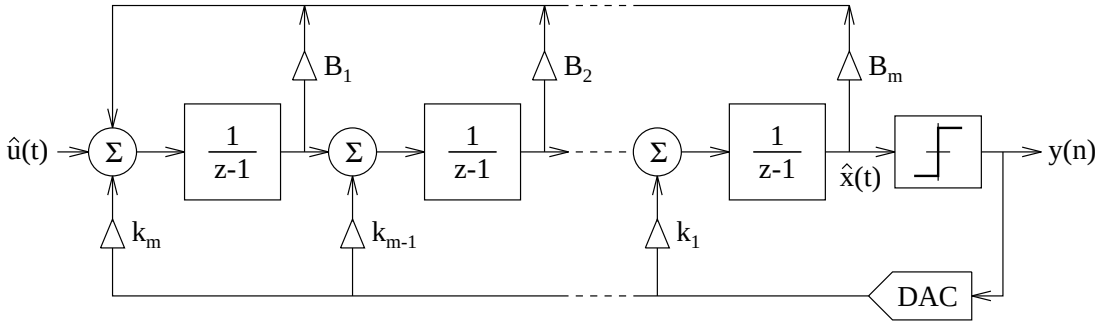


Figure 2.6: General mth-order low pass ΔΣM structure.

In a given application, the signal bandwidth f_N is usually fixed. Sampling faster than the Nyquist rate is *always* beneficial for improving the signal-to-noise ratio (SNR) in an ADC because the quantization noise inside the signal band is reduced by 3dB per octave of oversampling; in an order-m ΔΣM, this improvement can be shown to be $6m + 3$dB/oct [Can92b] because the noise is shaped by the loop filter. Thus, a high-order modulator is desirable because of the huge increase in converter dynamic range (DR) obtained from each doubling of the OSR.

Not surprisingly, using a high-order modulator has drawbacks. First, the stability of the overall system with $H(z)$ above order two becomes conditional: input signals whose amplitudes are below but close to full scale (to be defined later) can cause overload at the output of the integrators closer to the quantizer, which degrades DR [Sch93]. As well, the placement of the poles and zeros of $H(z)$ becomes a complicated problem, though many solutions have been proposed in the literature (e.g., [Ris94] among others). Furthermore, the technology in which the circuit is implemented and the circuit architecture itself will limit the maximum-achievable sampling rate and hence, from (2.4), the OSR. Finally, the design of the decimator increases in complexity and area for larger

oversampling ratios. Typical values of OSR lie in the range 32–256, though circuits with OSRs outside this range have been fabricated [Bai96, Nys96].

Quantizer resolution

It is possible to replace the single-bit quantizer of Example 2.1 with a multibit quantizer, e.g., a flash converter [Ada86]. This has two major benefits: it improves overall ΔΣM resolution and it tends to make higher-order modulators more stable. Furthermore, nonidealities in the quantizer (e.g., slightly misplaced levels or hysteresis) don't degrade performance much because the quantizer is preceded by several high-gain integrators, hence the input-referred error is small [Hau86]. Its two major drawbacks are the increase in complexity of a multibit vs. a one-bit quantizer, and that the feedback DAC nonidealities are directly input-referred so that a slight error in one DAC level corrupts converter performance greatly. There exist methods to compensate for multibit DAC level errors (e.g., [Gal96], [Lar88]). These aren't needed in a single-bit design because one-bit quantizers are inherently linear [Sch93].

Low pass vs. band pass

Integrators have poles at dc, and hence building $H(z)$ from integrators will shape noise away from dc. ΔΣMs where the quantization noise has a high pass shape are built with low pass loop filters and hence are denoted *low pass* (LP) converters. If we were to build $H(z)$ out of *resonators*, the noise would tend to be shaped away from the resonant frequency. The quantization noise then has a band stop shape because the loop filter is band pass, and the resulting ΔΣMs are called *band pass* (BP) converters [Sch91]. A common type of band pass converter is built starting with a low pass $H(z)$ and performing the substitution $z^{-1} \rightarrow -z^{-2}$; this produces a converter with noise shaped away from $f_s/4$ with identical stability properties performance as the low pass prototype, though the order is doubled [Sho96].

A typical application of such a converter is the conversion of an RF or IF signal to digital for processing and heterodyning in the digital domain, as depicted in Figure 2.7. The spectrum at the output of the converter is shown in the figure—the quantization noise is large everywhere except

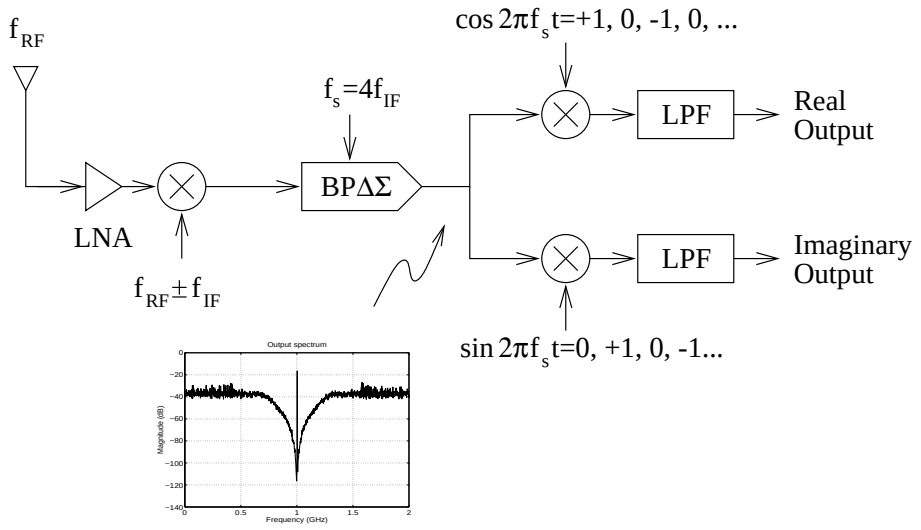


Figure 2.7: Typical radio receiver application for a band pass ΔΣM.

in a narrow band near 1GHz. Mixing to baseband digitally for I and Q channel recovery becomes particularly easy when the sampling frequency is chosen to be four times the input signal frequency because sine and cosine are sequences involving only ± 1 and 0, so simple digital logic can replace a complicated multiplier circuit. In general, the ability of a ΔΣM to perform narrowband conversion at a frequency other than dc makes them particularly attractive for radio applications; furthermore, CT ΔΣMs can be made fast enough to allow conversion of signals into the hundreds of MHz and beyond[1].

OSR for BP converters is defined as half the sampling frequency divided by the bandwidth of interest [Nor97, Chap. 9]; thus, an $f_s/4$ converter with a signal occupying the frequency range $(f_s/4 - f_s/32, f_s/4 + f_s/32)$ has a bandwidth of $f_s/16$, and hence OSR $= 8$.

Discrete- vs. continuous-time

We have been writing the loop transfer function $H(z)$ in the discrete-time (DT) domain. The majority of ΔΣMs in the literature are implemented as discrete-time circuits such as switched-

[1]This is not the only possible architecture: we might digitize directly at the RF rather than at the IF, although the noise figure of the ΔΣM might be too high to achieve the desired system dynamic range. We might also mix more than once prior to the modulator.

capacitor (SC) [Bai96] or switched-current (SI) [Ned95] circuits. It is possible to build the loop filter as a *continuous-time* (CT) circuit $\hat{H}(s)$, for example with transconductors and integrators [Jen95]. It is this kind of circuit in which we are interested in this thesis for it will usually be possible to clock a CT ΔΣM at a much higher rate than an SC or SI design in the same technology.

Single stage vs. multi-stage

Many modulators employ a single quantizer with multiple feedback loops leading to various points inside the forward modulator path, and these are called *multiloop* ΔΣMs. It is possible to build stable high-order modulators out of two or more low-order modulators where later modulators' inputs are the *quantization noise* from previous stages. Such ΔΣMs are called *multistage*; they were originally dubbed "MASH" structures, where MASH is an acronym deriving somehow from Multistage Noise-Shaping [Hay86]. In Figure 2.8, a first-order modulator's quantization noise is

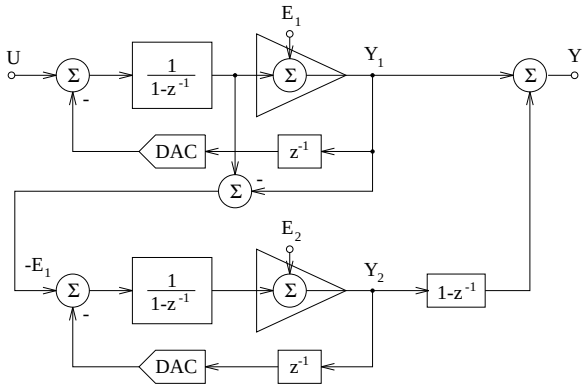


Figure 2.8: A multistage ΔΣM.

shaped by another first-order modulator:

$$\begin{aligned} Y_1 &= U + (1 - z^{-1})E_1 \\ Y_2 &= -E_1 + (1 - z^{-1})E_2. \end{aligned}$$

When Y_2 is differentiated and added to Y_1, we find

$$Y = Y_1 + (1 - z^{-1})Y_2$$

$$\begin{aligned} &= U + (1 - z^{-1})E_1 - (1 - z^{-1})E_1 + (1 - z^{-1})^2 E_2 \\ &= U + (1 - z^{-1})^2 E_2. \end{aligned} \tag{2.5}$$

Thus, the first-order noise is canceled in the output and the modulator achieves second-order quantization noise shaping. In principle, this can be extended to mth order noise shaping while preserving unconditional stability since each first-order ΔΣM is unconditionally stable. In practice, mismatches between components in the stages result in imperfect noise cancellation [Mat87].

To the author's knowledge, all published MASH ΔΣMs to date have been DT. It is possible to do CT MASH, but the only place it is discussed is [Nor97, Chap. 6]. As such, we will consider only single-stage modulators in this thesis.

2.2 Performance Measures

We have mentioned certain A/D converter performance measures such as dynamic range and signal-to-noise ratio, but we have yet to explain how to determine them for a ΔΣM. This section does just that by combining information from a literature survey about the subject with the author's practical experience.

2.2.1 Power Spectrum Estimation

A ΔΣM is a *noise-shaping converter*: the quantization noise is shaped away from the desired frequency band. We are thus interested in the frequency domain representation of the time domain output bits. More specifically, we care about the power spectrum of the output bits. The most common tool for finding power spectra is the discrete Fourier transform or DFT.

Suppose we have N uniformly-sampled data points $y(n) = \hat{y}(t)|_{t=nT_s}$, $n = 0 \ldots N-1$, $y(n) \in \mathbf{R}$. We will be using the so-called *periodogram* to estimate the power spectrum of $y(n)$. The DFT (which can be a *fast Fourier transform* or FFT when N is a power of two, which it frequently is) of $y(n)$ is given by

$$Y(n) = \sum_{k=0}^{N-1} y(k) e^{j2\pi kn/N},\ n = 0 \ldots N-1 \tag{2.6}$$

and the periodogram is defined as [Pre92]

$$\begin{aligned} P(0) &= \frac{1}{N^2}|Y(0)|^2 \\ P(n) &= \frac{1}{N^2}[|Y(n)|^2 + |Y(N-n)|^2],\ n = 1 \ldots (\tfrac{N}{2} - 1) \\ P(N/2) &= \frac{1}{N^2}|Y(N/2)|^2. \end{aligned} \tag{2.7}$$

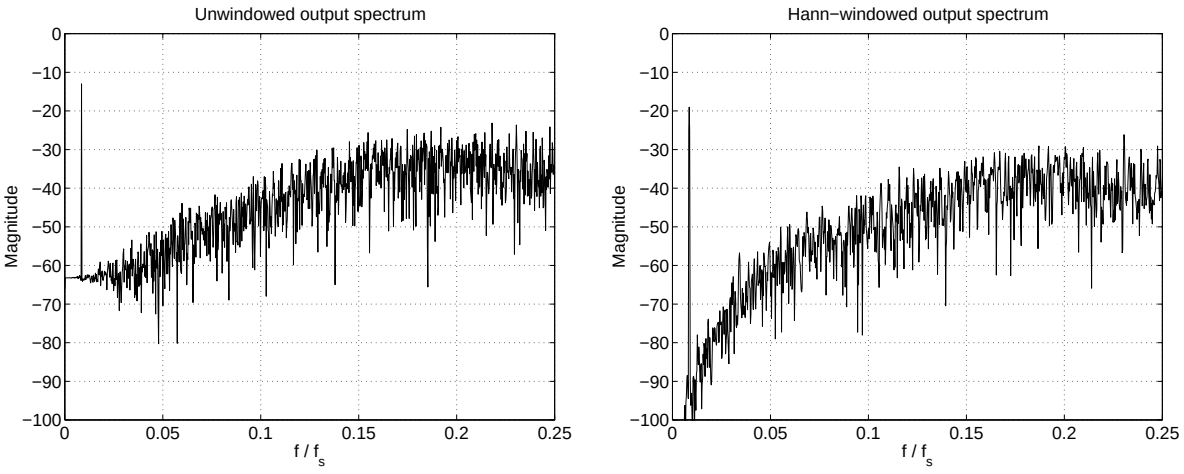
This power spectrum is defined at $N/2 + 1$ uniformly-spaced frequency points between 0 and the Nyquist rate $f_s/2$. Thus, each frequency *bin* is of width f_s/N. An example plot of $10 \log_{10} P$ from (2.7) was shown in Figure 2.4 in Example 2.1. Evidently, P is rms power: our input had magnitude -7.2dB and its power in the spectrum is -10.2dB. In this thesis, when we refer to the "spectrum", we mean the power spectrum as found from the periodogram.

A periodogram is a discrete representation of the spectrum of a discrete (sampled) signal, but in the real world power spectra are continuous functions of continuous signals. The discretization gives rise to two problems in periodograms, the first of which is usually denoted *spectral leakage* or simply *leakage*, and the second of which relates to uncertainty. We discuss both and how to alleviate them below.

Leakage and windowing

If there exists a tone in the input signal at a frequency that does not fall exactly in the center of a frequency bin, then leakage will result: instead of a sharp "spike" in one sepctrum bin, the tone will become spread over several adjacent bins. This can be understood by realizing that we can only take the FFT of a finite stretch of data (i.e., at a finite number of points); this is akin to taking the FFT of an infinite stretch of data multiplied by a rectangular window that is 1 for the duration of the finite stretch and 0 elsewhere. In the frequency domain, this corresponds to convolving an infinite power spectrum with the Fourier transform of a rectangle, namely, $(\sin x)/x$. The amount of leakage is determined by the spectrum of this function.

The severity of leakage may be reduced by *windowing* the data, which means multiplying it by a *windowing function* before taking its FFT. This has the effect of convolving the spectrum with a function other than $(\sin x)/x$. [Har78] lists many examples of windows; in the time domain, they



(a) (b)

Figure 2.9: Effect of windowing: (a) unwindowed output spectrum, (b) windowed output spectrum.

generally peak at 1 near the center of the data and fall to 0 in various ways near the edges. We prefer to use a *Hann window* (often incorrectly called a *Hanning window*), also called a *raised cosine* window because of the formula that describes it:

$$w(n) = \frac{1}{2}\left[1 - \cos\left(\frac{2\pi n}{N}\right)\right], n = 0, \ldots, N-1. \tag{2.8}$$

Example 2.2: In the simulation of ΔΣMs, it is easy (and recommended) to choose an input sinusoid with a frequency exactly in the center of a bin by making its frequency a multiple of f_s/N. Thus, leakage from the input tone is not usually problematic. Moreover, discrete tones arising from output limit cycles also usually fall exactly in the center of frequency bins. One case where they don't occurs when simulating a low pass ΔΣM and the mean of $y(n)$ is nonzero. This creates a dc component in $P(n)$ and also "misaligns" the output limit cycles such that there is leakage into all the low-frequency bins. We shall see that this turns out to give an unfairly-pessimistic SNR estimate.

Windowing greatly alleviates the problem. Figure 2.9(a) illustrates what happens when $N = 4096$ output bits from a second-order modulator have an average value of $2/N = -66.2$dB: the spectrum near dc flattens out to -63.2dB. Taking that same

output bit stream and first multiplying it by a Hann window before taking the FFT yields Figure 2.9(b): now, the noise-shaping behavior is clearly evident down to dc. The author prefers a Hann window because the input tone only becomes smeared over its immediately adjacent bin on each side; compare this to Blackman or Welch windows, commonly used by other authors, which smear the tone over several adjacent bins. This is of concern for calculating SNR as we shall see in Example 2.4. □

Uncertainty and averaging

The second reason why periodograms are inaccurate is as follows: the periodogram at a single frequency $P(n)$ is an estimate of a continuous function $\hat{P}(f)$ over a frequency range f_s/N centered at f_n. It turns out the estimate $P(n)$ has a standard deviation of 100% of the "actual" value. However, by taking K successive sets of N output bits, finding the periodogram of each, and *averaging* them, the standard deviation in each frequency bin is reduced by $\sqrt{K}$ [Pre92].

Example 2.3: Figure 2.10 is a striking illustration of the effect of averaging on the output power spectrum of a second-order ΔΣM. The upper-left graph shows the FFT of $N = 4096$ output bits; the upper-right graph depicts the average of $K = 4$ successive sets of N output bits. The following graphs are for $K = \{16, 256, 1024, 16384\}$; the graphs become smoother and smoother as the variance in each frequency bin is reduced. Moreover, the detail of the tones near $f_s/2$ is enhanced.

To generate the graph for $K = 16384$ we must calculate $N \times K \approx 67 \times 10^6$ output bits, and that takes about 12 minutes with a C program on an unloaded 170MHz Sparc Ultra. We do not usually need that large a K; it was provided merely as an illustration. 256 would certainly suffice for most purposes. □

2.2.2 Signal to Noise Ratio (SNR)

One of the most important performance measures of a ΔΣM is its signal-to-noise ratio (SNR). From this we may calculate other important performance measures such as its dynamic range

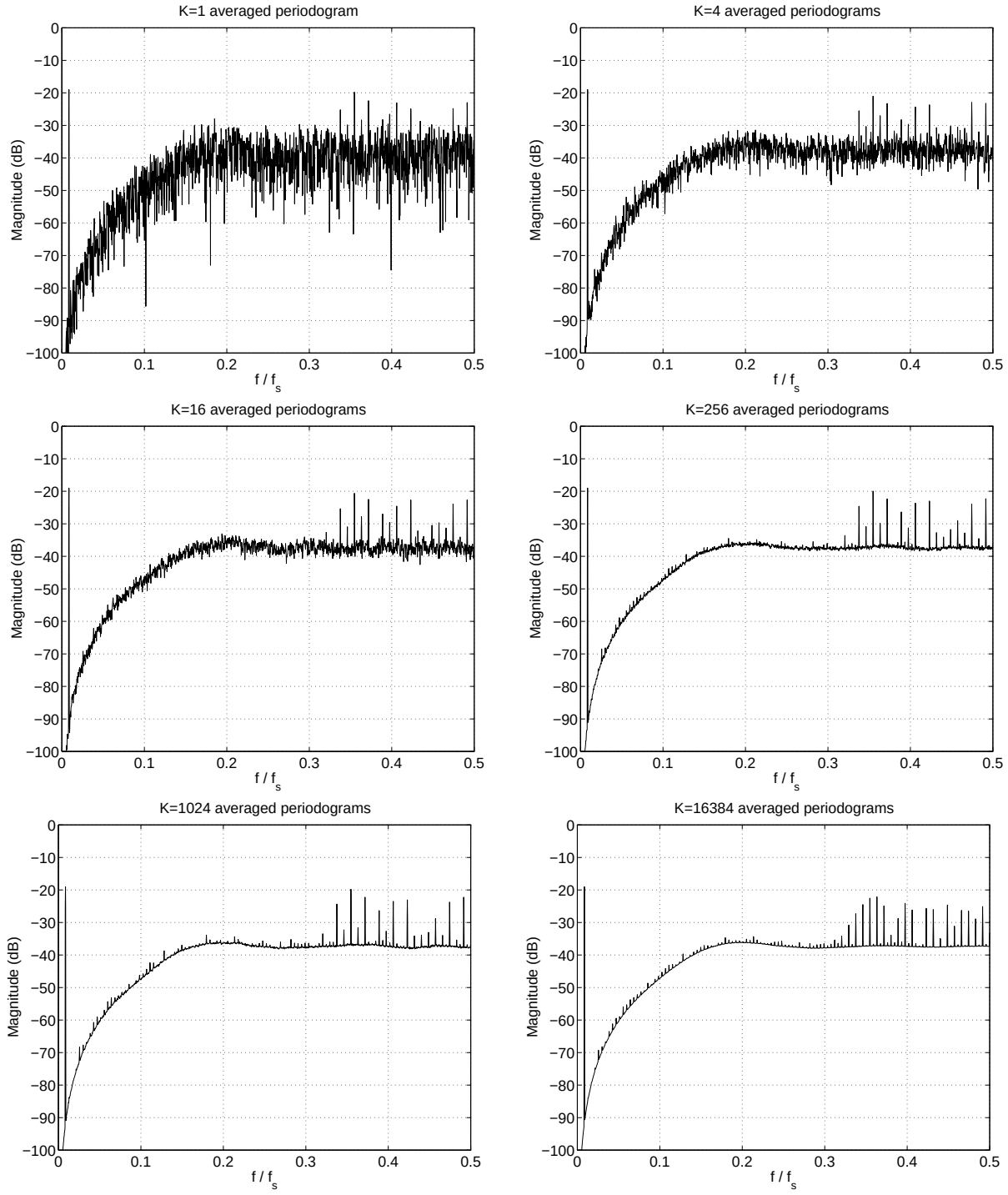


Figure 2.10: Effect of averaging on spectrum variance.

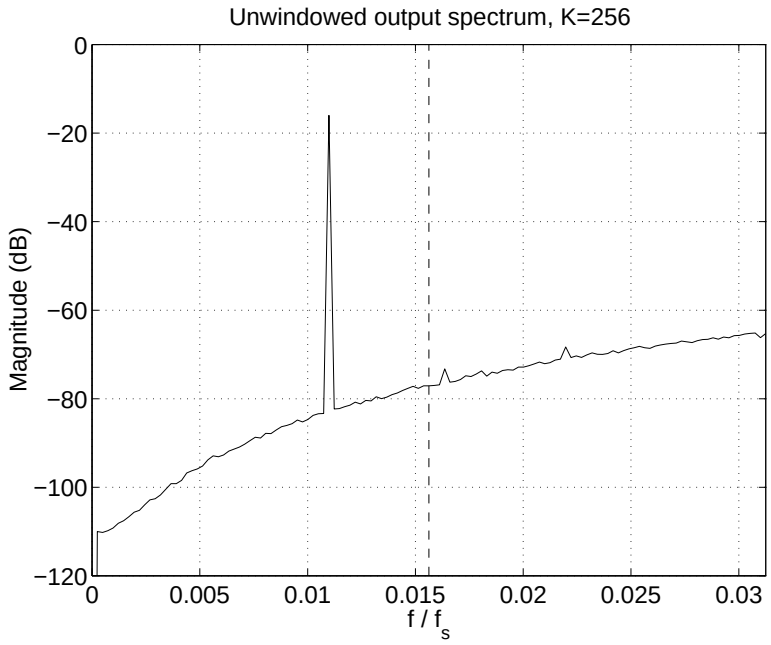


Figure 2.11: Unwindowed averaged periodogram near dc.

(DR) and peak SNR (SNR_{max}).

To find the SNR in a Nyquist-rate converter, we would divide the signal amplitude by the integrated noise from 0 to $f_N/2$ [Kes90a], which is the same frequency as $f_s/2$. A ΔΣM is an oversampled converter, however, so we do the same calculation over the bandwidth from 0 to $f_N/2$, which is now $f_s/(2 \cdot \text{OSR})$. As noted earlier, this assumption is the same as having the modulator followed by a brick-wall low pass filter which cuts off sharply at $f_N/2$. That being said, we are about to see that there remain a number of subtleties in this calculation.

Example 2.4: Consider a 4096-point simulation of a second-order modulator. With $K = 256$ averaged periodograms, the spectrum near dc appears as in Figure 2.11. The input tone is -13dB and it occurs in bin $b = 45$, which is $0.01099 f_s$. Let us try to calculate the SNR for OSR $= 32$.

We must integrate the noise between 0 and $f_s/64$, which is shown by the dashed line in Figure 2.11. This corresponds to bin numbers 0 through $4096/64 = 64$. Pre-

sumably, the noise power we're interested in can be found from

$$P_n = \sum_{i=0}^{64} P(i) - P(b). \tag{2.9}$$

However, do we include bin 64 in the calculation, or exclude it? In other words, should we find the noise for $0 \leq f \leq f_s/64$, or $0 \leq f < f_s/64$? Moreover, what should we do about the bin containing the signal? Do we subtract it as in (2.9) and leave it at that, or perhaps add the geometric mean of the power in the surrounding bins to P_n to make up for the missing bin?

Table 2.1 addresses some of these considerations, as well as the effect of K (the

Table 2.1: Comparison of SNR calculation methods. Including the bin at $f_s/(2 \cdot \text{OSR})$ lowers SNR by 0.3dB, while trying to account for the tone bin lowers it further by 0.1dB.

K	$\sum_{i=0}^{63} P(i) - P(b)$	$\sum_{i=0}^{64} P(i) - P(b)$	$\sum_{i=0}^{64} P(i) - P(b) + \sqrt{P(b-1)P(b+1)}$
1	$50.86,\ \sigma = 1.01$	$50.53,\ \sigma = 0.85$	$50.46,\ \sigma = 0.86$
4	$49.81,\ \sigma = 0.62$	$49.49,\ \sigma = 0.62$	$49.40,\ \sigma = 0.60$
16	$50.03,\ \sigma = 0.32$	$49.64,\ \sigma = 0.28$	$49.56,\ \sigma = 0.28$
64	$49.87,\ \sigma = 0.22$	$49.55,\ \sigma = 0.19$	$49.47,\ \sigma = 0.19$
256	$49.93,\ \sigma = 0.22$	$49.60,\ \sigma = 0.22$	$49.52,\ \sigma = 0.22$

number of averaged periodograms) on the calculated SNR. For ten different runs at each K value, the SNR was calculated by dividing $P(b)$ by the quantity listed at the top of each table column and taking $10\log_{10}$ of the result. The table lists the average and standard deviation σ of the ten SNR values, all in dB. First, we note that including bin 64 lowers SNR by 0.3dB or so, while adding the geometric mean of the bins around the tone makes another 0.1dB of difference. Second, we note that σ is higher for small K—that is, the variance in calculated SNR between different runs is greater when we do less averaging. Third, calculated SNR drops by a full dB between $K = 1$ and $K = 256$.

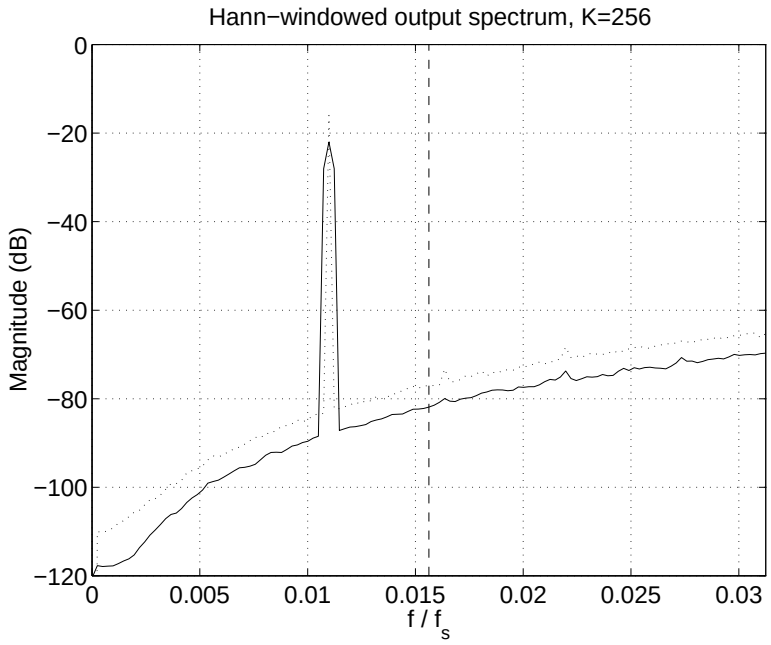


Figure 2.12: Hann-windowed averaged periodogram near dc.

Adding to this is the confusion about what happens when we window the periodograms. Figure 2.12 is another run with $K = 256$, but now a Hann window is applied to the data before finding its spectrum; the dotted line is the data from Figure 2.11 reproduced for reference. In Figure 2.11, the tone was only in one bin, and its power was $P(b) = -15.99$dB. Now, we find the tone spreads over three bins, and $P(b-1) + P(b) + P(b+1) = -20.25$dB. The unwindowed SNR for bins 0 to 64 excluding bin b was 49.66dB; the Hann-windowed SNR for bins 0 to 64 excluding bins $b-1$ to $b+1$ is 50.57dB.

The difference of -4.26dB in tone power can be explained as follows. The periodogram of (2.7) is normalized such that the signal power in time and frequency are equal (i.e., Parseval's theorem holds). Since the output sequence is composed of ± 1, the power in time is 1; we can easily verify that $\sum_{i=0}^{N/2+1} P(i) = 1$ in Matlab. A Hann window turns out to scale the total power by 0.375, and $10\log_{10}(0.375) = -4.2597$—exactly the difference seen in the tone power. The total baseband noise seems to have

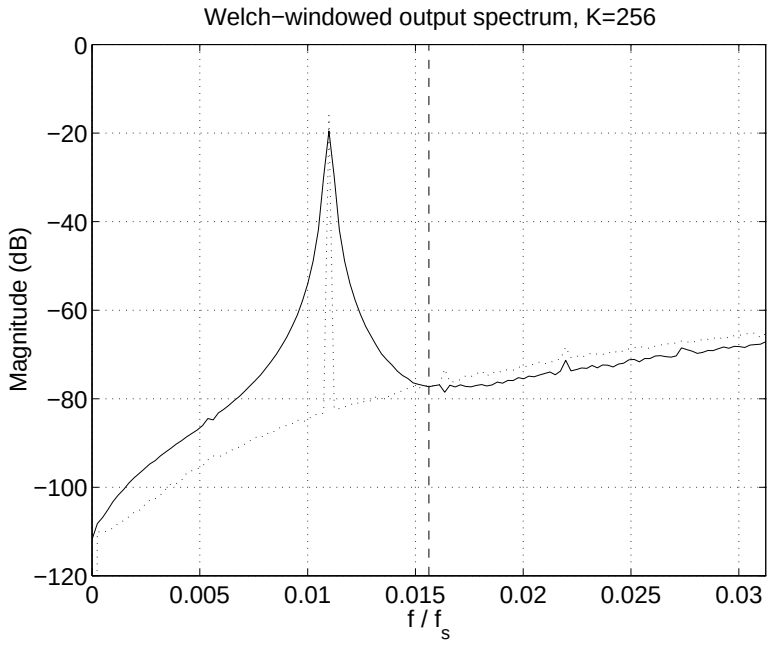


Figure 2.13: Welch-windowed averaged periodogram near dc.

been reduced by $50.57 - 49.66 + 4.26 = 5.15$dB. It is not so easy to explain numerically where the extra $5.15 - 4.26 = 0.91$dB of noise reduction by windowing comes from, though qualitatively we expect the reduction because windowing reduces leakage problems.

Finally, as alluded to in Example 2.2, a Hann window is vastly preferable for SNR calculations over many other windows. Figure 2.13 shows what a Welch window does to the baseband spectrum with the unwindowed spectrum plotted for reference. The tone has been smeared over so many bins that it becomes impossible to know where the noise begins. We only have 64 bins in which to find the noise, and too many of them get corrupted by smearing for a meaningful SNR calculation. □

The preceding example illustrates that SNR can vary by about 1dB depending on how the calculation is done. This suggests that specifying SNR to more than one decimal place is pointless, and even the first decimal place might not be very meaningful. Unfortunately, the example does little to clear up confusion about the “right” way to calculate SNR; papers in the literature rarely

seem to be specific. We arbitrarily adopt the definition in the first column of Table 2.1, where we neglect the tone bin(s) and the final FFT bin.

Some authors refer to signal-to-quantization-noise ratio (SQNR), where only quantization noise power is counted as noise, as distinct from signal-to-noise-and-distortion ratio (SNDR or SINAD), where both quantization noise power *and* the power in any output harmonics of the input signal are counted. We use SNR to mean SNDR—our SNR calculations will include any power in harmonics of the input signal caused by distortion. We shall examine some of the things that can create input signal harmonics in the output spectrum presently.

2.2.3 Other Performance Measures

Dynamic range

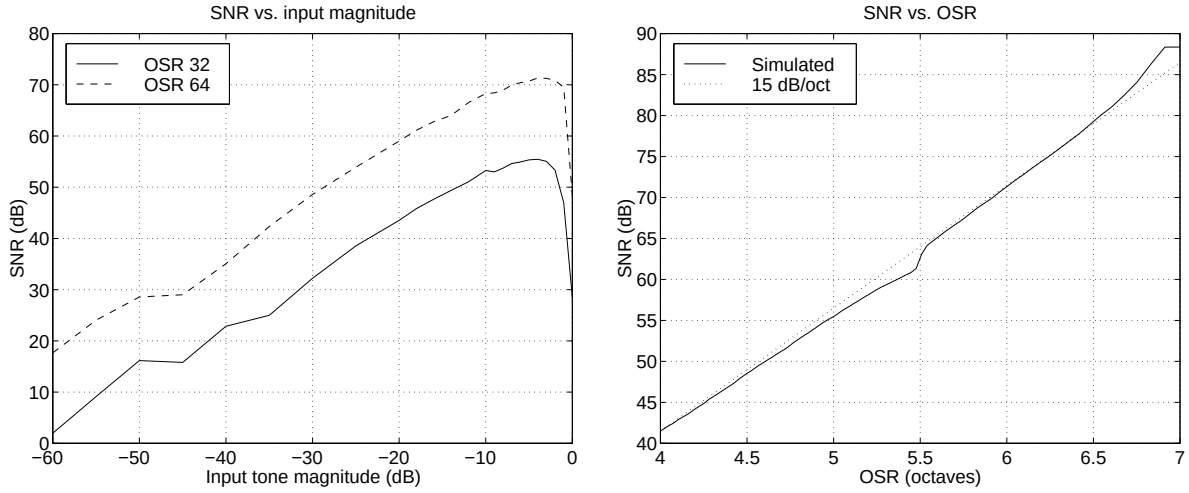
The dynamic range range of a $\Delta\Sigma$M, often specified in decibels, is equivalent to the resolution of the modulator as an ADC. We can convert from resolution in dB to resolution in bits by relating a $\Delta\Sigma$M to a Nyquist-rate converter using [Ben48]

$$\text{DR(bits)} = (\text{DR(dB)} - 1.76)/6.02. \tag{2.10}$$

To actually find the DR for a given modulator, SNR is plotted against input amplitude. The input amplitude range which gives SNR ≥ 0 is precisely the DR.

Example 2.5: For a second order low pass $\Delta\Sigma$M, Figure 2.14(a) shows the SNR as a function of input amplitude for two different OSRs, 32 and 64. We call this kind of graph a *dynamic range plot*. The slope of each curve is 1dB/dB except for large input amplitudes where the SNR stays constant or decreases with input amplitude. For small inputs, the SNR is limited by the in-band noise, while at large inputs, the SNR starts to become affected by input signal harmonics. Figures 2.15(a) and (b) show the baseband output spectrum for inputs of -6dB and -2dB, respectively. Signal harmonics are clearly present for the larger input.

Extrapolating to SNR $= 0$ for small inputs indicates the DR for OSR $= 32$ is 62dB, or about 10 bits from (2.10), and for OSR $= 64$ the DR is 77dB (about 12.5 bits). We



(a) (b)

Figure 2.14: Performance of ideal double integration ΔΣM.

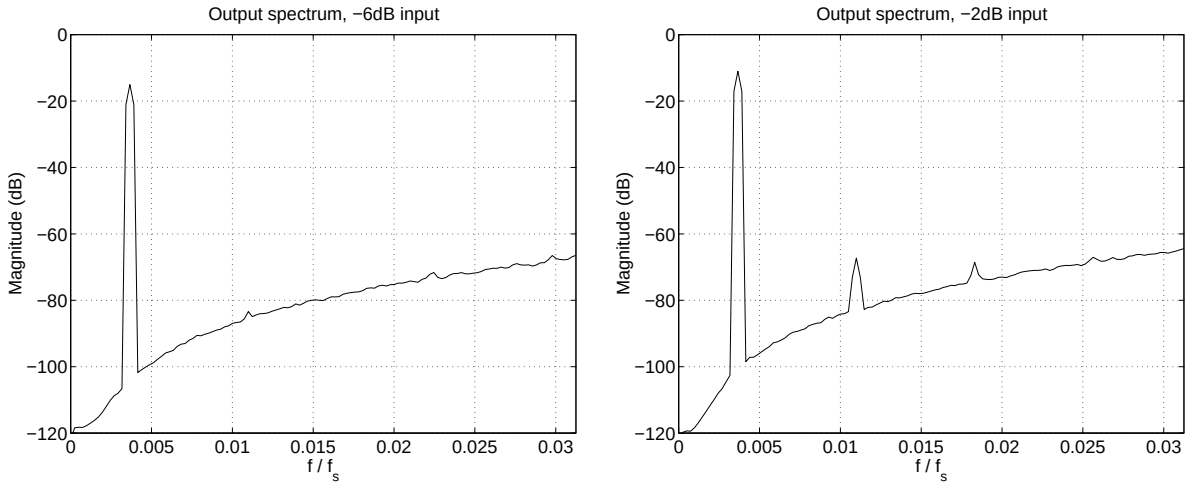
said earlier that at a fixed input amplitude SNR improves as $6m + 3$dB per octave of oversampling, where m is the order of the modulator. Figure 2.14(b) demonstrates the truth of this for a -4dB input tone. □

Full scale amplitude

In the previous example we referred to the input as being in dB, but what we did not make explicit is that it is dB relative to full scale[2]. How is "full scale" defined for a ΔΣM? The answer is not always obvious. In many cases, a full-scale input is one whose magnitude equals the maximum magnitude of the quantizer feedback, assuming a quantizer whose output is centered at 0 (which it almost always is). For an input larger than this, the feedback will not be able to keep the modulator stable; we refer to this as *overloading the modulator*.

Example 2.6: In the previous example, the quantizer was feeding back ± 1. When the input was a tone with peak amplitude 0.1V, it transpired that the tone appeared in

[2]It would probably be less confusing if the units of the input signal were explicitly specified as "dBrel" or something similar to indicate that it is dB relative to some maximum. However, most of the literature refers to "dB", so we do the same here.



(a) (b)

Figure 2.15: Increase in baseband harmonics for inputs near full scale: (a) -6dB input, (b) -2dB input.

the output spectrum with magnitude -23.01dB, which corresponds to a peak amplitude of $-20\text{dB} = 0.1\text{V}$. We can deduce that 1V is the full-scale input level in that example. An input larger than 1V will overload the modulator. Inputs close to 1V cause graceful degradation of SNR due to increased spectral harmonic content, as we saw in Figure 2.15. □

Example 2.7: Figure 2.16 shows a typical implementation of a second-order low

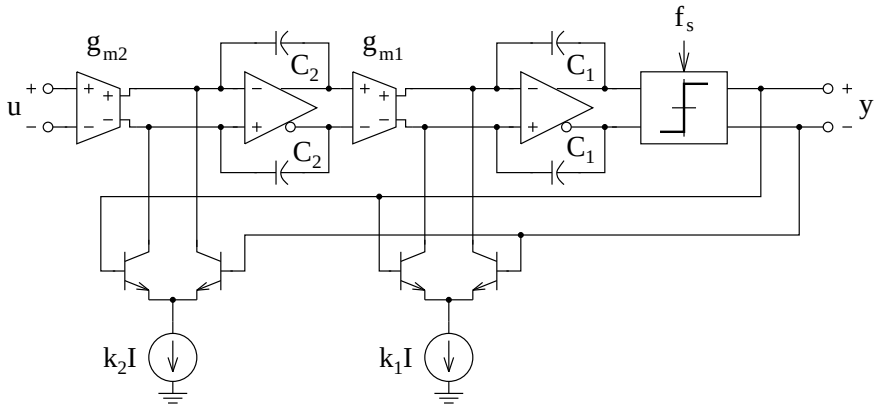


Figure 2.16: InP second-order CT ΔΣM by Jensen et al.

pass CT ΔΣM for high-speed ADC. The input signal is fed through a transconductor g_{m1}, and at the transconductor output node, there is a feedback current of magnitude k_2. The current $g_{m1}u$ can be no larger than k_2 without overloading the modulator; therefore, the full-scale input signal magnitude is k_2/g_{m1}. Typical component values might be $k_2 = 0.4$mA and $g_{m1} = 1$mA/V, so a 0.4V input signal would appear at the output as 0dB when the output bits are ± 1. □

For certain more complicated modulator structures we will encounter later, the full-scale input range will need to be found from simulation rather than calculation.

Maximum SNR and maximum stable amplitude

Maximum SNR, SNR_{max} (sometimes called "peak SNR"), is easily found from a DR plot as the peak of the SNR vs. input amplitude curve. It turns out that the second-order low pass ΔΣM is stable all the way up to an input amplitude of 0dB [Wan92]. It also turns out that higher-order modulators usually become unstable before 0dB is reached; this instability usually manifests itself in clipping of the final integrator output which causes the quantizer to produce a long consecutive sequence of the same output bit. This means the signal encoding properties of the modulator become poor [Ris94] and hence SNR is degraded. The maximum stable amplitude (MSA) is, then, the largest input amplitude which keeps the final integrator output bounded "most of the time". It, too, can be found from a DR plot as the maximum input amplitude for which SNR ≥ 0.

Spurious free dynamic range

Nyquist-rate ADCs sometimes specify a rating for spurious free dynamic range (SFDR) [Kes90b]. To measure SFDR, we apply a tone at the ADC input and look for the largest *spur* between 0 and $f_N/2$, where a spur is a tone visible above the noise floor. In theory, we must do this for all input frequencies and phases to find the very worst-case spur. Then, SFDR is the largest magnitude difference between the amplitudes of the input tone and the largest spur in dB, over all input tone amplitudes.

The importance of SFDR depends on the application. In some applications, a good SFDR is more important than a good DR. In radio systems, for example, it might be important to keep the amplitude of spurious tones low since nonlinearities might cause them to intermodulate and corrupt the desired signal, while the total amount of in-band noise might not matter so much. SFDR measurements aren't often quoted for oversampling converters such as ΔΣMs, though they sometimes are [Jen95]. Realistically, an SFDR measurement can only be performed on an actual circuit rather than in simulation because it requires many different input amplitudes, frequencies, and phases. We will usually neglect SFDR in our examination of CT ΔΣMs until we come to Chapter 7 where we can explicitly measure it for a fabricated design.

2.3 Simulation Methods

To characterize the performance of a ΔΣM, we take the spectrum of its output bit stream. How do we actually generate this output bit stream in a simulation? Because of the nonlinear quantizer, determining the output bits analytically is very difficult. As a result, time-domain simulation of the modulator is the usual method. In the simulation of just about any system, there exists a tradeoff between *realism* and *simulation time*: as we model the behavior of a system more accurately, the length of time required to generate simulation results increases. Let us first consider our simulation options for DT ΔΣMs, a subject which has received a considerable amount of attention in the literature, followed by those for CT ΔΣMs [Che98a].

2.3.1 Discrete-Time Modulator Simulation

An ideal DT ΔΣM can be described by a discrete-time system of equations. For the general modulator in Figure 2.17 which includes input prefiltering [Ris94], we can write a linear equation for the quantizer input in terms of the circuit input and quantizer output

$$X(z) = G(z)H(z)U(z) - H(z)Y(z). \tag{2.11}$$

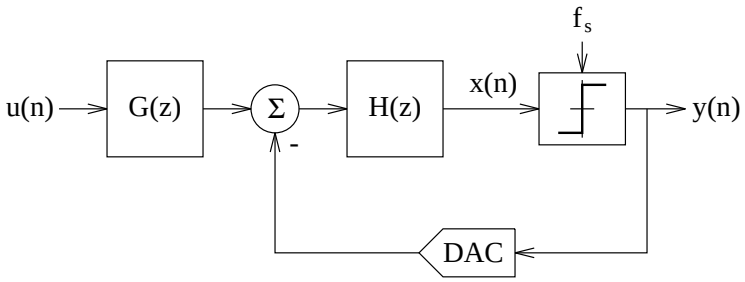


Figure 2.17: A general DT ΔΣM including input prefiltering.

$G(z)$ and $H(z)$ are rational functions of z, with $G(z)$ proper and $H(z)$ strictly proper. It is a trivial matter to take the inverse $\mathcal{Z}$-transform of (2.11), which leaves an expression for $x(n)$, the quantizer input now, in terms of past samples of (u, x, y):

$$x(n) = \sum_{k=1}^{m} a_k x(n-k) + \sum_{k=1}^{m} b_k u(n-k) + \sum_{k=1}^{m} c_k y(n-k). \tag{2.12}$$

$\{a_k, b_k, c_k\}$ are constants that can be found from $G(z)$ and $H(z)$. For each $x(n)$ found from (2.12), we find $y(n)$ by assuming an ideal quantizer; in the case of a single-bit quantizer,

$$y(n) = \begin{cases} +1, & x(n) \geq 0 \\ -1, & x(n) < 0. \end{cases} \tag{2.13}$$

Applying (2.12) and (2.13) for $n = 1, \ldots, N$ in a high-level language such as Matlab [Han98] or C gives a very rapid method for determining the output bit stream.

Rapidity is one thing, but realism is another. A practical circuit will likely not be represented by its ideal equations. Eventually, we will have a transistor-level description of a circuit whose behavior we would like to simulate, and we will most likely turn to a full-circuit simulator such as SPICE or Eldo. While such a simulation is likely to be able to model most if not all of the pertinent nonidealities which affect circuit performance, we will often be stuck waiting for hours or even days while generating enough output bits for an FFT. A detailed discussion of these nonidealities appears in Chapter 3.

Fortunately, there exists more than one "middle-ground" approach, where we achieve reasonable accuracy while still maintaining acceptably-fast simulation speed. Several programs (Simulink

under Matlab [Sim96], SPW [SPW92], and Ptolemy [Pto97] among them) allow a system to be defined at the block diagram level graphically, with the function of each block controlled by the user. This allows both rapid, user-friendly prototyping of ΔΣM systems along with the inclusion of nonidealities (such as finite integrator output swing and quantizer hysteresis) by using the appropriate blocks in the simulation. In a similar manner, full-circuit simulation programs like SPICE and Eldo[3] often allow the specification of a circuit with *macromodels*, where a block is modeled as an ideal version of itself instead of as a transistor-level description. Better still, ideal blocks can be replaced one at a time with transistor-level descriptions, which allows the user to see the effect of nonidealities in each individual block on overall modulator performance while keeping the simulation speed faster than for a complete transistor-level circuit.

Even better still, there exist special-purpose programs written specifically for the simulation of DT ΔΣMs. Both MIDAS [Wil92] and TOSCA [Lib93] are examples of programs which can simulate and extract key performance parameters from otherwise ideal ΔΣMs as well as DT ΔΣMs which include important nonidealities such as finite op amp gain, finite switch on-resistance, and clock feedthrough. A program by Medeiro et al. [Med95] goes even further: the user specifies modulator parameters such as required resolution, clock rate, and power consumption, and then the program can design and automatically produce the circuit layout for a complete SC modulator which meets the specifications.

Clearly, a first-time DT ΔΣM designer has plenty of options for generating an output bit sequence relatively quickly while still including the effects of relevant nonidealities.

2.3.2 Continuous-Time Modulator Simulation

The situation for CT ΔΣMs is perhaps not as good, most likely because there has been considerably less attention devoted to the design of CT ΔΣMs. Nonetheless, there are several choices. As with DT ΔΣMs, we may represent an ideal CT ΔΣM with a frequency domain equation akin to (2.11),

$$\hat{X}(s) = \hat{G}(s)\hat{H}(s)\hat{U}(s) - \hat{H}(s)\hat{Y}(s), \tag{2.14}$$

[3]Eldo is perhaps more suited to discrete-time block-level simulation than SPICE.

where we use the continuous frequency variable s rather than the discrete one $z = \exp(sT_s)$ and T_s is the sampling frequency. Taking the inverse Laplace transform of (2.14) does not lead to as easily-implementable an equation as that which resulted from the discrete case (2.12), so for time-domain simulation, we must represent the system as a series of coupled first-order differential equations and solve them using numerical integration.

Example 2.8: For the modulator in Figure 2.16, the equations describing circuit behavior are

$$\begin{aligned} C_1 \frac{d\hat{x}_1}{dt} &= g_{m1}\hat{u}(t) + k_2\hat{y}(t) \\ C_2 \frac{d\hat{x}_2}{dt} &= g_{m2}\hat{x}_1(t) + k_1\hat{y}(t) \end{aligned} \tag{2.15}$$

and the single-bit quantizer is described by (2.13). Implementing these equations in a numerical integration program is perhaps slightly more tedious than solving the difference equations, but it is still not terribly difficult. □

It happens that because of the clocked quantizer inside the CT loop, an ideal CT modulator has a DT equivalent. Thus, there exists a mapping between the s-domain description of a ΔΣM and the z-domain which can be exploited to increase simulation speed and give intuitive understanding of modulator behavior. We leave a more detailed discussion of this until the time when we actually make use of it in Chapter 4.

Once again, ideal CT ΔΣM behavior is one thing and the behavior of a real circuit is another. As with DT modulators, full-circuit simulation of CT modulators is painfully slow when each block is described down to the transistor level. Also as in the DT case, macromodel simulation is an attractive option for reducing simulation time while incorporating key nonidealities: a CT ΔΣM is first described with ideal blocks in a full-circuit simulator, then nonidealities can be added gradually to observe the effect on performance. Often, graphical block diagram simulators (such as those listed in the previous section) can also simulate CT systems, so this too is a choice for CT ΔΣMs.

As far as specialized CT ΔΣM simulation tools go, the literature seems not to mention large-scale efforts. Frequently [Bro90, Cha92, Ush94, Che98a] special-purpose programs in a high-level language such as C are written in the course of studying modulator performance. Opal [Opa96]

has built a fairly general framework based on the CT/DT equivalence mentioned above, but to this author's knowledge, there is no equivalent of a program like TOSCA for CT ΔΣMs.

Rapid and realistic simulation of CT ΔΣMs is a central underlying theme of this thesis. We will be making use of various simulation techniques as we delve into detail, and we will describe them more as we need to make use of them.

2.4 Summary

Delta-sigma modulation is a technique which combines filtering and oversampling to perform analog-to-digital conversion: the noise from a low resolution quantizer is shaped away from the signal band prior to being removed by filtering. High-speed conversion can be accomplished by using a continuous-time filter inside the delta-sigma loop, and we are interested in this for its potential applicability to radio receiver and other high frequency circuits. Performance of a ΔΣM is determined by taking the spectrum of a sequence of output bits generated from time-domain simulation of the modulator; it is characterized with some of the usual ADC performance measures such as DR and SNR, while omitting others which have no meaning in ΔΣMs such as DNL and INL. How to actually perform the time-domain simulation is a matter of considerable import in oversampled converters because they will usually require many more output samples than a Nyquist rate ADC before performance can be measured.

Chapter 3

$\Delta\Sigma$M Implementation Issues

The theory of ideal delta-sigma modulators is quite well-understood [Nor97, Chap. 4–5]. The purpose of this chapter is twofold: first, to summarize the papers from the published literature which discuss the effects of commonly-encountered nonidealities on the performance of $\Delta\Sigma$Ms, and second, to list the important literature papers regarding CT $\Delta\Sigma$M specifically, of which there are considerably fewer than those that discuss DT $\Delta\Sigma$Ms. We close this latter section with a summary of the performance achieved in published high-speed CT $\Delta\Sigma$Ms.

3.1 Nonidealities in $\Delta\Sigma$Ms

There are certain considerations that apply to the design of both DT *and* CT modulators. First of all, the problem of choosing the CT loop transfer function $\hat{H}(s)$ can be formulated in the DT domain, where $H(z)$ is chosen using any one of the numerous suggestions in the literature and then transformed to the appropriate $\hat{H}(s)$. We will see several examples of this in Chapter 4. Additionally, there are certain nonidealities which adversely affect the performance of DT $\Delta\Sigma$Ms which have a similar effect in CT $\Delta\Sigma$Ms. In this section, we take it as given that how to select a transfer function to achieve a given performance is understood; we survey the literature on the performance effect of nonidealities in delta-sigma modulation and summarize the results that are germane to the design of single-stage CT $\Delta\Sigma$Ms. A version of this summary for DT $\Delta\Sigma$Ms

appears in [Nor97, Chap. 11]; we extend it here to include CT ΔΣMs.

3.1.1 Op Amps

Not all modulators include op amps, though many do. If an op amp inside a ΔΣM deviates from ideal, performance is invariably worsened. We consider various types of commonly-encountered op amp problems here.

Finite op amp gain

Probably the most widely-studied nonideal effect is that of finite op amp dc gain [Hau86, Bos88, Cha90, Fee91, Can92b, Cha92]. An ideal integrator has a DT transfer function $F(z) = 1/(z-1)$; it can be shown that an integrator built from an op amp with dc gain A_0 results in a transfer function

$$F(z) = \frac{1}{z - p(1 - 1/A_0)} \tag{3.1}$$

where p is a constant. Finite op amp gain causes *leaky integration*: the NTF zeros are moved off the unit circle towards $z = 0$, which reduces the amount of attenuation of the quantization in the baseband and therefore worse SNR. The equivalent problem in a BP modulator occurs when the resonators have finite Q.

A good rule of thumb which applies to both DT and CT ΔΣMs is that the integrators should have $A_0 \approx$ OSR, the oversampling ratio [Hau86, Bos88, Cha92, Can92b, Ber96]. If this holds, the SNR will be only about 1dB worse than if the integrators had infinite dc gain [Bos88]. In [Jen95], which is a CT ΔΣM using the circuit in Figure 2.16, it was shown that the parameter which limited the baseband noise floor was $A_0 R_{in} C$, where A_0 and R_{in} are the gain and input impedance of the op amp and C is the integrating capacitor. That is, the baseband noise went from shaped to white at a frequency given by $f = (2\pi A_0 R_{in} C)^{-1}$, so once again, high A_0 is beneficial.

Finite bandwidth (nonzero settling time)

Usually, it is assumed that an op amp can be modeled as a single-pole system with time constant τ [Hau86, Bos88, Cha90, Med94]. [Bos88] notes that for many sampled-data analog filters, the

unity-gain bandwidth of an op amp must be at least an order of magnitude higher than the sampling rate; [Gre86] says it should be five times higher.

This requirement is greatly relaxed in DT $\Delta\Sigma$Ms. Both [Med94] and [Bai96] contend that incomplete integrator settling is the same as a gain error, which results in increased baseband quantization noise. However, [Hau86] finds that even with a settling error as large as 10%, as long as it is a *linear* error, 14-bit performance can be achieved. The fabricated design in [Bos88] exhibited negligible performance loss for $\tau \leq T_s/2$. It thus seems that τ can be on the order of T_s for acceptable performance. Chan [Cha92] found something similar for a CT $\Delta\Sigma$M: op amp bandwidths could be as low as f_s, the sampling frequency, and still give negligible performance loss.

Finite slew rate

Generally, in DT circuits we are worried about slewing of the *input* signal. A DT $\Delta\Sigma$M, however, is oversampled, which means the input signal is slow compared to the sampling rate; thus, what concerns us is slewing of *internal* signals (most particularly op amp outputs). It might appear that slew-rate limiting of these signals should not make any difference on top of that made by imperfect settling—so long as the outputs are "close enough" to the correct values after a full clock period, why does it matter whether they approach these values by slewing rather than linear settling? In fact, it *does* matter because op amp slewing is a *nonlinear* settling process [Cha90], and this introduces input signal harmonics in the output spectrum which degrades SNDR [Med94]. In [Bos88], a large increase both in quantization noise and harmonic distortion was observed when the slew rate dropped below $1.1\Delta/T_s$, where Δ is the difference between adjacent quantizer output levels. Note well, however, that this is an *extremely* relaxed requirement compared with non-oversampled circuits—slew rate is one of many parameters in which $\Delta\Sigma$Ms are quite tolerant of imperfections.

We show by example that a similar thing happens in CT $\Delta\Sigma$Ms.

Example 3.1: Typical integrator and quantizer output waveforms for an ideal CT double integration modulator with a small dc input are depicted in Figure 3.1. The

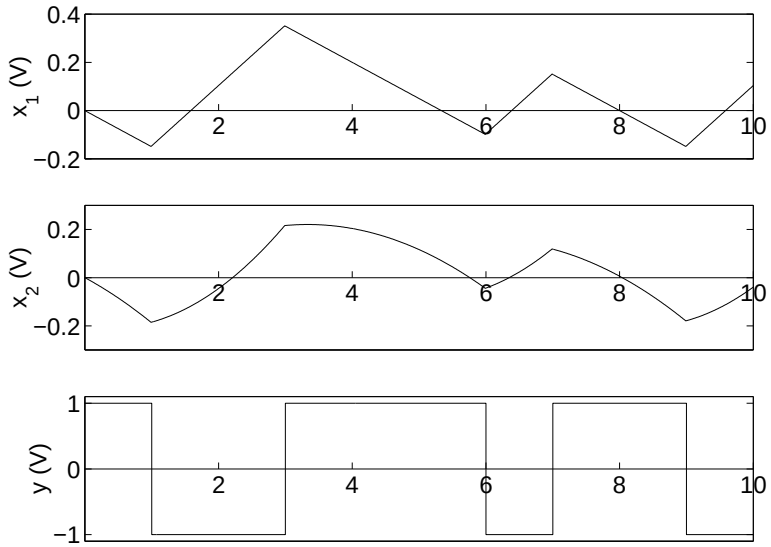


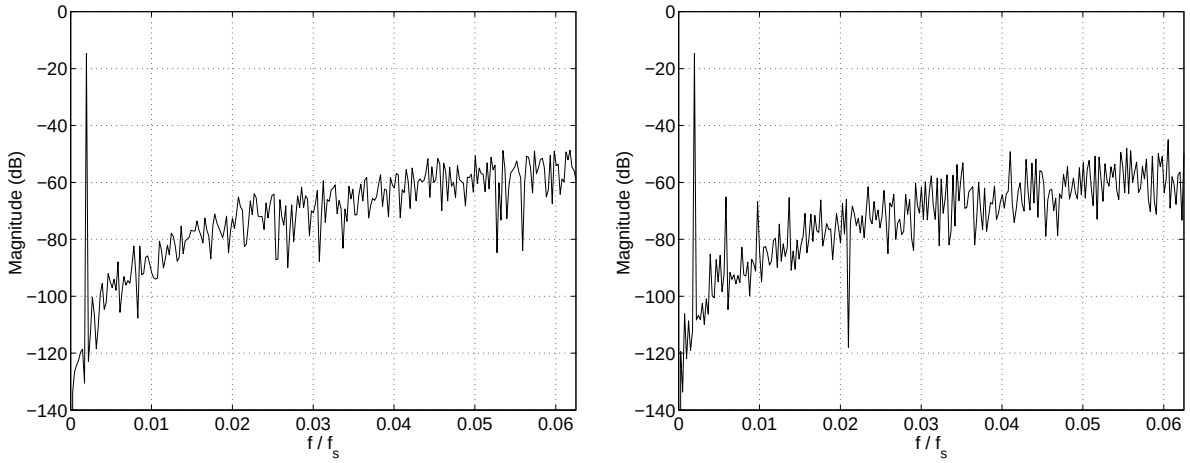
Figure 3.1: Typical integrator output and quantizer waveforms.

first integrator operates on the sum of two currents, a constant one determined by the quantizer bit and a nearly-constant one from the input (which in general is slowly-varying compared to the sampling clock). Hence, the integrator output $\hat{x}_1(t)$ appears as a straight line. The output $\hat{x}_2(t)$ is the integral of the sum of $\hat{x}_1(t)$ (a straight line) and the output bit (a constant), so it has a parabolic shape.

A typical output spectrum for the ideal modulator appears as in Figure 3.2(a). For the modulator parameters chosen, the maximum slew rate required for the $f_s = 1$GHz sampling clock is about 0.35V/ns. If we limit the slew rate to 0.25V/ns, the graph in Figure 3.2(b) results. We see both a slight increase in baseband quantization noise *and* a large increase in harmonic distortion. Clearly, avoiding slew-rate limiting in CT ΔΣMs is as important as in DT circuits, though doing so is not usually difficult. □

Limited output swing

An mth-order ΔΣM has m states whose values at sampling instants completely determine modulator behavior. It is usually the case that the integrator output voltages are precisely the system



(a) (b)

Figure 3.2: Output spectra using op amps with (a) no slew-rate limiting, (b) slew-rate limiting.

states. Therefore, if the integrators are built with op amps whose output swing is not large enough to produce the required state values, modulator behavior will be altered. Both [Hau86] and [Bos88] illustrate that clipping the integrators results in severe baseband noise penalties. Fortunately, this problem has been very well-studied, and it is not difficult to scale the parameters in a ΔΣM to avoid clipping op amp outputs (e.g., [Cha90] among others). Circuit noise considerations yield a practical lower limit on how small signal swings can be.

Gain nonlinearity

If the gain of the op amp depends in a nonlinear manner on the op amp input voltage, harmonic distortion of large input signals appears in the output spectrum [Bos88, Med94, Dia94, Ber96]. It is difficult to give general results for how much nonlinearity can be tolerated; op amp gain should be made as independent of input signal level as possible, though the amount of independence required depends on the desired modulator resolution. Gain nonlinearity in the op amp nearest the input stage has the greatest effect because later-stage gain nonlinearities are divided by the (large) gains of earlier stages when referred to the input [Bos88]; this fact is important in both DT and CT ΔΣMs.

3.1.2 Mismatch and Tolerance

A traditional notion about ΔΣMs (as compared with Nyquist-rate ADCs) is that they often need not have matching or tolerances better than the desired resolution of the converter. This is true for mismatch among components in the forward loop (i.e., in the loop filter), but not true for DAC level mismatch.

Component mismatch and tolerance

In SC ΔΣMs, a mismatch between sampling and integrating capacitors in an SC integrator stage results in a gain error [Reb89, Baz96] whose effects we can treat in a manner similar to [Bos88]. There exist layout techniques to keep integrated capacitors matched quite well [Reb89]; as well, using large capacitors and/or clever circuit architectures can alleviate problems [Baz96]. To give an idea of the required tolerances, in a particular 90dB SC converter, it was found 5% error in individual coefficients of the loop filter led to performance losses of only 1–3dB [Cha90]. Sensitivity to tolerance obviously depends on the exact circuit architecture, so it is difficult to generalize. However, for a typical CT ΔΣM, matching requirements are unlikely to be terribly stringent, just as was found in [Cha90].

Multibit DAC level mismatch

ΔΣMs frequently employ a one-bit quantizer for two reasons: it is easy to build, and because a feedback DAC with only two levels is inherently linear [Sch93]. If we choose to build our modulator with a multibit quantizer, then we require a multibit DAC, and now any errors in the spacing between DAC levels are directly input-referred. Thus, it would appear the resolution of the overall modulator depends directly on the DAC matching.

Fortunately, there exist techniques called *dynamic element matching* where mismatched DAC elements are “shuffled” so that different elements are used each time the same output code occurs. A survey of this area alone is quite interesting, though for brevity and relevance reasons we omit it. The most important papers which discuss DEM techniques are [Car87, Bai95, Kwa96, Jen98, Shu98], and [Nor97, Chap. 8] contains a good summary of present knowledge in the area. This

same chapter also goes into digital-post correction schemes which can also compensate for multibit DAC errors. All DAC error correction schemes could in theory be applied just as well to CT designs, something we discuss more in §4.5.

3.1.3 Quantizers

Just as $\Delta\Sigma$Ms are tolerant of mismatch, so too are they tolerant of common quantizer imperfections [Hau90]. The quantizer is preceded by several high-gain stages, so dc offsets (or level spacing errors in a multibit quantizer) are negligible once input-referred. Of course, the comparator must be "fast enough" to resolve its input signal to the desired logic level; there is some discussion on this point for DT designs in [Hau90], and for CT designs, not much has been said. We devote considerable attention to this important point in Chapter 6 of this thesis.

It transpires that for one-bit quantizers, hysteresis is not terribly problematic. Boser [Bos88] shows that hysteresis may be as severe as 0.1Δ (one tenth of the step size) with negligible performance loss in his SC circuit, though Chan [Cha92] found a requirement of 0.01Δ in his CT circuit. We consider hysteresis in Chapter 6, and we discover that CT $\Delta\Sigma$Ms are very tolerant of it.

3.1.4 Circuit Noise

In simulation, the in-band noise floor in a $\Delta\Sigma$M output spectrum is determined by quantization noise only in an ideal modulator. Certain nonidealities like DAC level mismatch (discussed above) and clock jitter (discussed below) can also contribute to in-band noise in a simulation. In manufactured circuits, often it is the input-referred electronic circuit noise that limits performance [Bos88].

Once again, circuit noise depends on the circuit architecture. In a typical SC $\Delta\Sigma$M, noise comes from three main sources [Dia92a, Dia92b].

1. Switch resistance means the voltage sampled onto the input capacitor has uncertainty kT/C [Gre86] where k is Boltzmann's constant, T is absolute temperature, and C is the capacitance. Depending on resolution, this might require relatively large input capacitors—for particularly high-resolution converters, integrating such capacitors onto a chip might be prob-

lematic [dS90]. Off-chip capacitors could be used, or using a CT integrator as the first stage with DT integrators for later stages also works [dS90].

2. The thermal noise of the first op-amp must be kept small. It is inversely proportional to the transconductance g_m of the input MOS differential pair, which can be controlled by sizing the input devices appropriately [Gre86].

3. MOS transistors also have so-called $1/f$ noise [Gre86], where low-frequency noise increases as 10dB/dec with decreasing frequency. This can be overcome with so-called *chopper stabilization* [Gre86, dS90] where the $1/f$ noise is cleverly modulated to the sampling frequency and thus filtered out by the decimator. As well, it is unlikely that $1/f$ noise would affect a band pass $\Delta\Sigma$M, since then the baseband would be away from low frequencies.

We leave a discussion of thermal noise in typical CT $\Delta\Sigma$Ms for Chapter 7 where we present test results on an actual fabricated circuit.

3.1.5 Other Nonidealities

There are a few other nonidealities which have been studied in connection with $\Delta\Sigma$Ms. Two effects which matter in SC designs, but not in CT designs, are nonzero switch "on" resistance and signal-dependent charge injection. The first of these limits the maximum modulator clock rate because of the RC time constant involving the switches and the sampling capacitor [Hau90], hence small-resistance switches are often important. The second disturbs the voltage on the sampling capacitors, though it can be circumvented with techniques such as differential circuitry [Bos88], additional clock phases [Bos88, Baz96], and bottom-plate sampling [Baz96].

Designing the first stage

We have already alluded to this in the previous subsections, but we say it explicitly here: the first stage is the most important to design well in terms of its thermal noise, linearity, matching, etc. This is because nonidealities in later stages, when input-referred, are divided by the total gain

preceding them. By design, each stage in a ΔΣM has a high gain in the signal band, so stages two and beyond have a reduced influence at the input, but the first stage does not. Thus, in a DT ΔΣM, considerable effort must be spend designing the first op amp [Yuk87] while requirements on later op amps may be relaxed. Likewise, the first transconductor in a CT ΔΣM is the most important for overall thermal noise and linearity [Jen95, Mor98]. A mismatch in the input differential pair transistors leads to an offset which results in a dc term in the output spectrum; special care must be taken in converters where dc is not removed by the decimator.

Component nonlinearity

Earlier we mentioned nonlinearity in the first stage op amp gain characteristic adds harmonic distortion. The same thing happens if components near the input are nonlinear. For example, [Hau86] shows how a voltage-sensitive first integrating capacitor degrades performance in a typical SC ΔΣM. In [Jen95], the input transconductor in their CT ΔΣM uses a differential pair degenerated with an emitter resistor to set g_m; it is observed that the linearity of this resistor which is the key to the linearity of the whole circuit. If the first integrating capacitor is slightly nonlinear, harmonics of the input signal appear in the output spectrum—the resulting spectrum looks similar to the one in Figure 3.2(b). Usually, component linearity requirements are more stringent than component tolerance requirements.

Clock jitter

How important is timing jitter in the quantizer clock in a ΔΣM? Compared to a Nyquist-rate converter, Harris [Har90] found ΔΣMs had a tolerance to white jitter improved by the oversampling ratio for the same jitter variance. Boser [Bos88] found the same thing, but he also noted that because jitter noise falls as $1/\text{OSR}$ while quantization noise falls as $1/\text{OSR}^{2m+1}$, modulators with high OSRs are more likely to be performance-limited by jitter. Van der Zwan [vdZ96] presents an argument that CT ΔΣMs are more sensitive to jitter than DT ΔΣMs; we will take this issue up in Chapter 5 when we consider in detail the problem of clock jitter in CT ΔΣMs.

3.2 Important CT ΔΣM Papers: A Survey

No study of CT ΔΣM would be complete without a review of the significant papers in the literature on the subject. We present a chronological listing of these papers as unearthed by the author in an extensive literature survey with a brief description of each, and we then summarize the performance achieved in tests of actual fabricated circuits.

3.2.1 Paper List

[Ino62], [Ino63] The first of these papers is where ΔΣM was first published, though there was a patent granted to Cutler a couple of years earlier [Cut60]. The second paper contains some analysis of a CT ΔΣM with both a single and double integrator. In particular, the 9dB and 15dB of SNR improvement per octave of oversampling for the first- and second-order modulators are derived. They build circuits for both and verify the predicted performance, and apply the circuits to the encoding of video signals.

Following this paper, over the next twenty years there were not many papers on ΔΣM because integrated MOS processes were still expensive. As they became cheaper, the DSP required in the decimator became cheaper, and hence ΔΣMs began to receive more interest.

[Can85] It is this paper which really sparked interest in ΔΣM as a method for ADC. It is widely cited as the source for the so-called *double integration* ΔΣM, although in fact [Ino63] predates it. Such a ΔΣM contains two cascaded integrators and implements $\text{NTF}(z) = (1 - z^{-1})^2$, i.e., double differentiation of the quantization noise. We denote this modulator the *standard [low pass] second-order* ΔΣM since, as we shall see, there have been many subsequent implementations of it. This paper is the first to derive the DT/CT loop filter equivalence

$$H(z) = \frac{2z - 1}{(z - 1)^2} \quad \leftrightarrow \quad \hat{H}(s) = \frac{1 + 1.5sT_s}{s^2T_s^2} \tag{3.2}$$

for a feedback DAC that emits full-period pulses, and a CT ΔΣM circuit was built based on this equivalence.

[Koc86] This is also a double integration CT ΔΣM, following Candy's lead. With a 15MHz clock, the achieved performance was 77dB over a 120kHz bandwidth and a power consumption of 20mW—certainly not poor even by today's standards.

[Ada86] Miles ahead of its time, this paper describes a fourth-order four-bit (i.e., with a four-bit quantizer) CT ΔΣM that achieves 18 bits of resolution at 24kHz. The crucial issue of DAC waveform asymmetry (i.e., differing rise and fall times at the DAC output) is first discussed here. This will be mentioned again in Chapter 4.

[Gar86] Floyd Gardner's paper is the first to describe the *impulse-invariant transformation* between CT and DT as an alternative to the (perhaps more common) bilinear transform. We mentioned its existence in §2.3.2 and we will make use of it in Chapter 4.

[Pea87], [Sch89], [Gai89] The idea of band pass ΔΣM was, to the author's knowledge, first suggested in the first of these papers, though it can hardly be said that those proceedings are widely available. In *Electronics Letters*, Schreier and Snelgrove first introduced the idea to a wider audience in the second paper listed; unbeknownst to them at the time, a U.S. patent had been granted to Gailus et al. a few months earlier, as the third citation shows.

[Gos88], [Gos90] These papers were the first to point out that a delay between the sampling clock edge and DAC pulse edge affects the performance of a CT ΔΣM. We shall denote this delay as *excess loop delay*, and as we shall see in Chapter 4, it turns out to have a major impact on the design of CT ΔΣMs.

[Bro90] This was an early paper on how to simulate DT systems in CT. It used a third-order CT ΔΣM as an example and showed how to simulate its behavior both in C and SABER. The bilinear transform was used to map between z and s domains, though we prefer the impulse-invariant transformation.

[Hor90] Another paper very advanced for its time and often overlooked, it also discusses excess loop delay in CT ΔΣM and is the first to suggest the use of the modified $\mathcal{Z}$-transform to account for loop delay in the design of high-order CT ΔΣMs. While [Gos88] showed that a

certain amount of loop delay is beneficial to a first-order CT ΔΣM, this paper extended the results to higher-order CT ΔΣMs.

[Asi91] Although no circuit was actually designed here, this is an early paper that considers some issues in the design of very fast CT ΔΣMs. For a standard second-order CT ΔΣM clocking at 500MHz in GaAs, the authors examine the effect on SNR of finite op amp dc gain, gain-bandwidth product, and signal swing, and small nonlinearities in the op amp, and conclude that a 10-bit converter could be built to work at this speed.

[Com91] This is one of the few CT ΔΣM papers that doesn't use op amps: it is a CMOS current-steering design. Nothing much similar has appeared in the literature to this author's knowledge since its publication.

[Thu91] At the time this paper was published, the idea of band pass ΔΣM was relatively new. This paper is the first to use the impulse-invariant transformation to design a continuous-time BP ΔΣM. They designed a loop transfer function with nonoptimal noise shaping; it took [Sho94] to explain how to overcome this.

[Cha92] The authors talk about design issues of a standard second-order CT ΔΣM in GaAs for 500MHz clocking, including finite op amp dc gain and gain-bandwidth product, and quantizer hysteresis and delay. They then fabricate and test a prototype whose poor performance is attributed to poor comparator sensitivity. However, the circuit was one of the first to demonstrate the feasibility of integrating high-speed CT ΔΣMs.

[Can92b] This is the first of two IEEE Press books published about ΔΣM. It is a compendium of Candy and Temes' opinion of the important papers in ΔΣM up until early 1990. This author recommends owning a copy to anyone working in ΔΣM design since most or all important early papers may be found in this convenient reference.

[Hal92] This is another early high-speed modulator, this time in 2μm CMOS clocking at 150MHz. It describes a standard second-order CT ΔΣM and achieves 10-bit resolution at an OSR of 128.

[Wan92] It had long been suspected that the standard double integration ΔΣM is stable for dc inputs up to the rails. This paper proves it using a geometrical argument about the bounds of internal states.

[Tro93] These authors designed a BP CT ΔΣM on an analog-digital FPGA. As in [Thu91], they didn't implement the correct $H(z)$...

[Sho94] ...it was in this paper that a correct method for designing band pass CT ΔΣMs based on the impulse-invariant transform was explained.

[Ush94] This paper isn't terribly interesting except for the fact that they model the quantizer as a steep tanh function for simulation purposes, which allows them to write and simulate linear differential equations for a ΔΣM. Little seems to have been made of this since then.

[Ris94] Lars Risbo's doctoral thesis is unique. Motivated by his desire to build the best-sounding CD player possible, he examines stability and design methods for high-order single-bit ΔΣMs in ways that are highly innovative and original. Sadly, his ideas will likely be appreciated by few because they are almost too clever: it took this author three separate attempts over one year to grasp much of what Risbo says. Nonetheless, this is a reference work to be taken seriously for anyone wishing a deep understanding of ΔΣMs. His Appendix C contains some discussion of clock jitter in CT ΔΣMs, a topic we cover at length in Chapter 5.

[Fen94], [Nar94], [Jen94] Three high-speed CT ΔΣMs appeared at the GaAs Integrated Circuits Symposium in 1994. The first listed clocked at 500MHz, the second at 2GHz, and the third at 4GHz; the first two are standard second-order low pass GaAs designs while the third is a first-order low pass InP design. All three designs suffered from moderate amounts of harmonic distortion in the baseband.

[Jen95] We spent considerable time studying this paper. It describes the building of a standard second-order CT ΔΣM using InP double heterostructure HEMTs clocking at 3.2GHz for

converting a 50MHz baseband signal and 71dB SFDR is achieved. A circuit diagram of their modulator was shown in Figure 2.16 on page 25.

[Mit95] The authors of this paper simulate, but don't build, a first-order CT ΔΣM in CMOS that dissipates only 3mW at a clock speed of 128MHz.

[Sho96], [Sho97] Omid Shoaei's excellent Ph.D. thesis is, to date, the definitive work on high-speed CT ΔΣM. It is required reading for anyone working in the area. Shoaei attempted to build a 250MHz fourth-order band pass CT ΔΣM for conversion of narrow band signals at 62.5MHz, but the final performance was thwarted by unexpectedly high fabrication tolerances and a lack of common-mode feedback circuitry in his transconductors. Shoaei's work will be referred to extensively throughout this thesis. The first citation is the thesis itself, and the second is a journal paper which summarizes the thesis.

[Erb96] This brief paper describes a silicon bipolar standard second-order CT ΔΣM clocking at 1.28GHz. The performance is at best 8 bits, though the paper's length permits very little detail to be given. It is implied that the authors use a circuit architecture similar to that in Figure 2.16.

[Sch96a] This paper explains how to design a CT ΔΣM by transforming it to a DT ΔΣM design problem using the impulse-invariant transform. While [Sho96] deals with the problem in pole-zero form, [Sch96a] represents the modulator in state-space.

[Opa96], [Don97], [Don98b], [Don98a] Opal's 1996 work focuses on the rapid simulation of clocked CT systems in the DT domain. Since then, a student of his, Yikui Dong, has written several papers about rapidly simulating nonideal effects in CT ΔΣMs, most particularly thermal noise. Such a tool is extremely useful, and the simulation results look plausible, but unfortunately no experimental validation of their results has been provided to date.

[vdZ96], [vdZ97] These nice papers present fourth-order CT ΔΣMs with very low power. The first is a 0.2mW voice band coder, the second a 2.3mW audio coder. Both achieve about 15

bits of performance. [vdZ96] also contains some discussion about tradeoffs between DT and CT designs.

[Ben97], [Gao97a] As noted, excess loop delay in a CT ΔΣM worsens performance. Both these papers talk about how to compensate for loop delay with appropriate feedback and tuning. We will be examining this further in Chapter 4.

[Rag97] Written by the authors of [Jen95], this paper describes Figure 2.16 with an additional transconductor element to turn the low pass modulator into a mildly band pass one with a noise notch tunable from 0 to 70MHz and a 4GHz sampling clock. A claim of 92dB SNR is made for a very narrow bandwidth corresponding to an OSR of around 5000.

[Che97] It is believed that this is the first mention of the performance effects of quantizer metastability in CT ΔΣMs. It was written by the author, and a large amount of new material along these lines is given in Chapter 6.

[Nor97] This is the second IEEE Press book about ΔΣM. Instead of a compilation of papers, the editors commissioned various authors to write chapters in their areas of expertise on many aspects of ΔΣM theory, design, and simulation. It, too, is highly recommended as a reference work for anyone in the area—the book has acquired the moniker “the orange Bible”.

[Miy97], [Olm98] In these papers, a 5GHz HEMT modulator was designed for a 50MHz bandwidth, and 7-bit performance was achieved. It must be noted, however, that this performance was achieved with a signal band that did not extend below 6MHz; this was apparently to avoid further SNR degradation by the $1/f$ noise of the devices.

[Jay97] Following [Jen95], these authors make a fourth-order BP CT ΔΣM clocking at 3.2GHz with an 800MHz center frequency. They achieve 7-bit performance in a 25MHz band, though they estimate with proper design this could be raised to 10 bits. We arrive at a similar conclusion for our 4GHz modulator in Chapter 7.

[Gao97b], [Gao98b] These papers present an aggressive 4GHz CT second-order band pass design in 25GHz Si bipolar technology for direct conversion of 950MHz analog signals. In a very narrow bandwidth, 10-bit performance was achieved.

[Che98a], [Che98b] The author presented these papers at ISCAS 1998 in Monterey. The first deals with simulating CT ΔΣMs, something we covered briefly in the previous chapter, and the second deals with the nonideal effects of excess loop delay, clock jitter, and quantizer metastability on the performance on CT ΔΣMs. This thesis is in large part an expansion of the second paper: we devote one chapter to each of these three key nonidealities.

[Gao98a] Preliminary test results on a fourth-order 4GHz CT band pass modulator in a 40GHz SiGe HBT technology are presented in this paper. We greatly extend these results in Chapter 7 of this thesis.

[Oli98] In this paper the effect of jitter in the DAC pulse width of return-to-zero-style first- and second-order modulators is studied. The authors conclude, as [Che97] did earlier, that jitter in the width of the DAC pulse is not noise-shaped and hence degrades performance. However, their new result is that a second-order modulator provides first-order shaping of pulse *starting time* jitter; hence, they propose using a monostable multivibrator as a quantizer, which produces fixed pulse widths even in the presence of variable pulse start time.

[Mor98] This is the first paper to the author's knowledge which contains a high-speed design of order three. This circuit contains two separate modulators for I and Q channels with integrated mixers, similar in architecture to Figure 2.7 only where the mixing is done as part of the first stage of the modulator so that the modulators themselves are low pass. In a 50MHz bandwidth, 35dB SNR was achieved.

3.2.2 High-Speed CT ΔΣM Performance Summary

Table 3.1 summarizes the order and type of the high-speed CT ΔΣM designs surveyed, where "1LP" means first-order low pass, "2BP" means second-order band pass, etc. The majority of the

Table 3.1: High-speed CT ΔΣM published performance.

Paper	Technology	Type	f_s	OSR	DR (dB)	SNR (dB)
[Cha92]	1μm GaAs D MESFET	2LP	200MHz	100	58	50
[Hal92]	2μm CMOS	2LP	150MHz	128	63	57
[Fen94]	0.5μm GaAs HEMT	2LP	500MHz	100	60	55
[Nar94]	1.4μm GaAs HBT	2LP	2GHz	20	43	37
[Jen95]	2.0μm InP DHBT	2LP	3.2GHz	32	49	50
[Mit95]	1.2μm CMOS	1LP	128MHz	128	60	57
[Sho96]	0.8μm Si BiCMOS	2BP	200MHz	500	50	46
[Erb96]	Si BJT	2LP	1.28GHz	64	–	45
[Rag97]	2.0μm InP DHBT	2LP/BP	4GHz	64	44	41
[Gao97b]	0.5μm Si BJT	2BP	3.8GHz	10000	60?	49
[Jay97]	AlGaAs/GaAs HBT	4BP	3.2GHz	64	42	41
[Olm98]	0.4μm InGaP/InGaAs HEMT	2LP	5GHz	50	51	39
[Gao98a]	0.5μm SiGe HBT	4BP	4GHz	500	62	53
[Mor98]	0.5μm SiGe HBT	3LP	1.6GHz	16	–	35

designs are implementations of the standard double-integration modulator with a loop filter given by (3.2), $H(z) = (2z-1)/(z-1)^2$. The two second-order BP modulators are for converting analog signals at one quarter of the sampling frequency to digital; ideally, they have the same performance and stability as a first-order LP design. The two fourth-order BP designs are also $f_s/4$ designs, and they have the same performance and stability as a double-integration $\Delta\Sigma$M. Thus, all the high-speed designs listed except the last one are first- or second-order. For each clock rate f_s and OSR, DR and SNR_{max} are also listed.

The performance of an ideal first- or second-order modulator can be found from DT simulation as we did in Example 2.5 or from [Sch93, Fig. 7]. Based on these, an approximate formula for the achievable performance in a double integration modulator is

$$\text{DR} \approx 15\log_2(\text{OSR}) - 13 \text{ dB}, \ \text{SNR}_{\text{max}} \approx 15\log_2(\text{OSR}) - 20 \text{ dB}. \tag{3.3}$$

Table 3.2 shows how each of the published 2LP/4BP modulators compares to (3.3). Generally,

Table 3.2: Performance in published double integration CT$\Delta\Sigma$Ms relative to ideal simulation.

Modulator	[Cha92]	[Hal92]	[Fen94]	[Nar94]	[Jen95]
f_s (GHz)	0.2	0.15	0.5	2.0	3.2
OSR	100	128	100	20	32
DR loss (dB)	29	29	27	9	13
Useful OSR	18.7	24.0	21.0	11.9	15.1
Modulator	[Erb96]	[Rag97]	[Jay97]	[Olm98]	[Gao98a]
f_s (GHz)	1.28	4.0	3.2	5.0	4.0
OSR	64	64	64	50	500
DR loss (dB)	25?	33	35	21	59
Useful OSR	15.1	9.5	8.5	14.9	16.6

we see performance falling far short of ideal, particularly for OSRs of 64 or more. Frequently in papers that publish output spectra it is clear that the signal band is filled with white, rather than shaped, noise. Thus, doubling the OSR results only in a 3dB DR improvement instead of 15dB

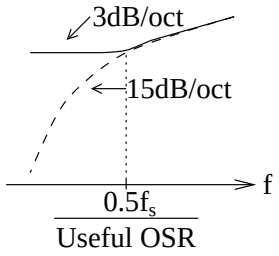


Figure 3.3: Ideal vs. real spectra in double integration modulators.

for an ideal second order ΔΣM as depicted in Figure 3.3. We could extrapolate backwards to the approximate point where noise shaping ends and white noise begins as

$$\text{Useful OSR} \approx \text{OSR} \div 2^{\text{DR loss}/12}. \tag{3.4}$$

This is termed "useful OSR" because it is the OSR for which noise shaping ceases, and it is listed in the table for each modulator.

Clearly, there is little benefit in using OSR > 15 for GHz-speed modulators. It is surprising how consistent this number is, even with quite different clock speeds and semiconductor processes. The problem is not with CT ΔΣMs in general—[Ada86], for example, achieved DR $= 105$dB in a 20kHz band—it is with *high speed* CT ΔΣMs. It might be that all these modulators are limited simply by thermal noise; the same thermal noise spec would cause 30dB more noise in a 20MHz band than in a 20kHz band, so a 4GHz modulator would be more likely to be thermal-noise limited than a 4MHz modulator with the same OSR. Still, there are a number of other possibilities which we explore in the coming chapters.

3.3 Summary

Published high-speed CT ΔΣMs achieve poor performance compared to an ideal modulator. We spend the remainder of this thesis investigating the performance-limiting nonidealities in high-speed CT ΔΣM design.

Chapter 4

Excess Loop Delay

Consider once again the high-speed double-integration modulator from Figure 2.16 [Jen95] reproduced in Figure 4.1. The quantizer is a latched comparator whose output drives differential

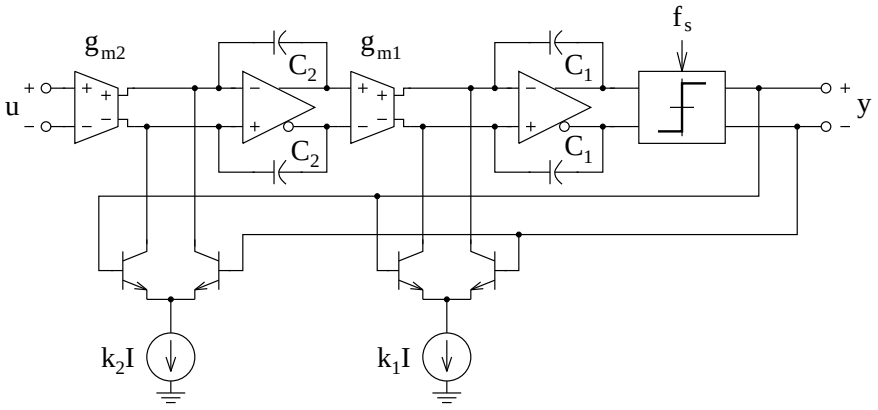


Figure 4.1: Example of high-speed double integration CT ΔΣM.

pair DACs; their output currents sum with the transconductor outputs. Ideally, the DAC currents respond immediately to the quantizer clock edge, but in practice, the transistors in the latch and the DAC have a nonzero switching time. Thus, there exists a delay between the quantizer clock and DAC current pulse. It is this delay that we call *excess loop delay*, or simply *excess delay* or *loop delay*. There is really no analogous problem in DT modulators; perhaps the closest thing is incomplete settling, which we discussed in §3.1.1.

Excess delay has been studied in the literature before; a brief summary of past work is appropriate. Gosslau and Gottwald [Gos88, Gos90] found that excess delay of 25% actually improves the DR of a 1LP CT $\Delta\Sigma$M. Horbach [Hor90] confirmed this and extended the results to higher-order LP modulators, showing that excess delay is detrimental to their performance. Chan [Cha92] found a full sample of feedback delay in his 2LP modulator caused 10dB of SNR loss. Shoaei [Sho96] found excess delay problematic in 2BP and 4BP modulators. Gao et al. [Gao97a] propose feedback coefficient tuning and demonstrate that it alleviates delay problems in a 4BP modulator, while Benabes et al. [Ben97] add an extra feedback loop to a 2LP modulator for the same purpose.

One of the aims of this chapter is to unify and summarize the past work in the area, but we also contribute new material. First, most authors use the modified $\mathcal{Z}$-transform for studying excess delay, but we explain here why this is inappropriate and demonstrate a preferred method. Second, we consider higher-order LP and BP modulators in much more detail than has previously appeared. We also consider multibit modulators, something which seems not to have been done in the past. Ideas from this chapter have appeared partially in [Che98b], and the chapter has been accepted almost verbatim in its entirety for journal publication [Che99b].

4.1 Preliminaries

A general CT $\Delta\Sigma$M is depicted in Figure 4.2[1]. The CT input $\hat{u}(t)$ (possibly prefiltered by $\hat{G}(s)$)

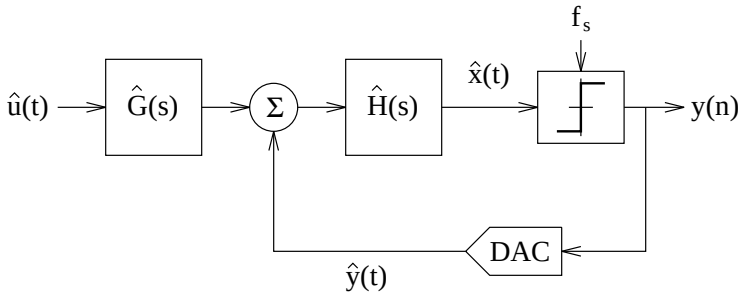


Figure 4.2: General CT $\Delta\Sigma$M block diagram.

[1]We have made a slight change from Figure 2.1: the DAC output is now added to the input instead of subtracted. This is a trivial difference which will invert the sign of $H(z)$, but otherwise leave modulator behavior identical.

is applied to a modulator with a CT loop filter $\hat{H}(s)$ whose output we denote $\hat{x}(t)$. The quantizer samples this signal at frequency f_s, or equivalently with period T_s; this produces a DT output signal $y(n) = \hat{y}(nT_s)$, which is fed back through a DAC.

4.1.1 CT/DT Modulator Equivalence

It is useful to begin by explaining how to find the equivalent DT loop filter $H(z)$ for a given CT loop filter $\hat{H}(s)$ (we first mentioned this equivalence in §2.3.2). Why does such an equivalent exist? Because the quantizer in a CT $\Delta\Sigma$M is clocked, which means there is an *implicit* sampling action inside the modulator, and sampled circuits are DT circuits. We can make the sampling explicit by placing the sampler immediately prior to the quantizer as depicted in the upper left diagram of Figure 4.3—this does not change the behavior of the modulator. If we want to know how this is

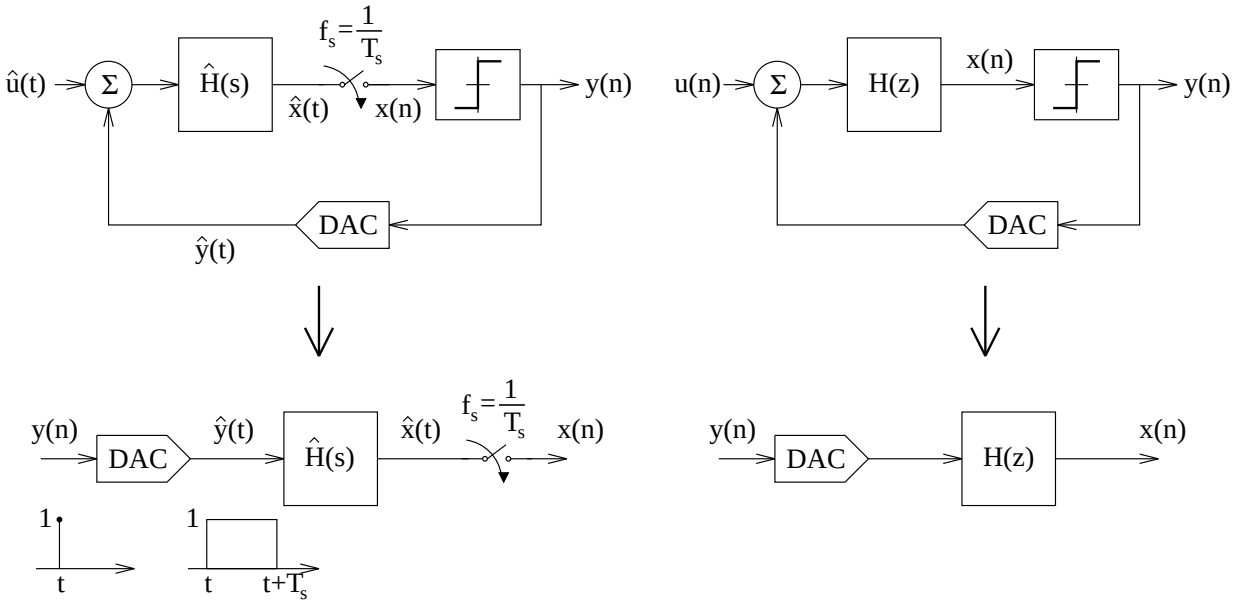


Figure 4.3: Open-loop CT $\Delta\Sigma$M and its DT equivalent.

equivalent to a DT modulator, shown in the upper right of Figure 4.3, then it is illustrative to zero both inputs and open both loops around the quantizer. This leads to the bottom two diagrams of Figure 4.3.

In the CT open-loop diagram, the quantizer output $y(n)$ is a DT quantity, and we may think of the DAC as a "discrete-to-continuous converter": it makes a CT pulse $\hat{y}(t)$ from the output sample $y(n)$. This pulse is filtered by $\hat{H}(s)$ (the CT loop filter) to produce $\hat{x}(t)$ at the quantizer input, which is then sampled to produce the DT quantizer input $x(n)$. The input and output of both the CT and DT open-loop diagrams are thus discrete-time quantities. A CT modulator would produce the same sequence of output bits $y(n)$ as a DT modulator if the inputs to the quantizer in each were identical at sampling instants:

$$x(n) = \hat{x}(t)|_{t=nT_s}. \tag{4.1}$$

This would be satisfied if the impulse responses of the open loop diagrams in Figure 4.3 were equal at sampling times, leading to the condition [Thu91]

$$\mathcal{Z}^{-1}\{H(z)\} = \mathcal{L}^{-1}\{\hat{R}_D(s)\hat{H}(s)\}|_{t=nT_s}, \tag{4.2}$$

or, in the time domain [Sho96],

$$h(n) = [\hat{r}_D(t) * \hat{h}(t)]|_{t=nT_s} = \int_{-\infty}^{\infty} \hat{r}_D(\tau)\hat{h}(t-\tau)d\tau|_{t=nT_s} \tag{4.3}$$

where $\hat{r}_D(t)$ is the impulse response of the DAC. Since we are requiring the CT and DT impulse responses to be the same, the transformation between the two is called the *impulse-invariant transformation* [Gar86].

Without loss of generality, we shall simplify the discussion by normalizing the sampling period to $T_s = 1$ second for the remainder of this chapter.

4.1.2 Usefulness of Equivalence

Knowledge of the equivalence allows us to perform CT $\Delta\Sigma$M loop filter design in the DT domain using any design technique we choose, for example, NTF prototyping [Nor97, Chap. 4]. Once we have chosen $H(z)$, we may find the $\hat{H}(s)$ to implement the CT modulator with identical behavior, given a certain type of DAC pulse. For simplicity, we assume a perfectly rectangular DAC pulse of magnitude 1 that lasts from α to β, i.e.,

$$\hat{r}_{(\alpha,\beta)}(t) = \begin{cases} 1, \ \alpha \le t < \beta, \ 0 \le \alpha < \beta \le 1 \\ 0, \ \text{otherwise.} \end{cases} \tag{4.4}$$

Table 4.1 lists the s-domain equivalents for z-domain $H(z)$ poles of orders one through three. These were found by solving (4.2) in the symbolic math program Maple [Red94] where the Laplace transform of (4.4) is

$$\hat{R}_{(\alpha,\beta)}(s) = \frac{\exp(-\alpha s) - \exp(-\beta s)}{s}. \tag{4.5}$$

It is found that a z-domain pole of multiplicity l at z_k maps to one at s_k with the same multiplicity, with

$$s_k = \ln z_k. \tag{4.6}$$

Therefore, to use the table, $H(z)$ is first written as a partial fraction expansion, then we apply the transformations in the table to each term and recombine them to get the equivalent $\hat{H}(s)$. Poles at dc (i.e., $z_k = 1$) end up giving $0^l/0^l$ as the numerator of the s-domain equivalent, which necessitates l applications of l'Hôpital's rule; this has been done in the right column of Table 4.1. The table extends the work in [Sho96] to general (α, β) and also to third-order z-domain poles.

Example 4.1: Many designs use DACs with an output pulse which remains constant over a full period, which we shall term a *non-return-to-zero* (NRZ) DAC. For this type of DAC, $(\alpha, \beta) = (0, 1)$ in (4.4). Moreover, we saw that many of the high-speed designs in Table 3.1 were second-order LP designs; these differentiate the quantization noise twice so that NTF$(z) = (z-1)^2$ and

$$H(z) = \frac{-2z + 1}{(z-1)^2}. \tag{4.7}$$

Writing this in partial fractions yields

$$H(z) = \frac{-2}{z-1} + \frac{-1}{(z-1)^2}. \tag{4.8}$$

Thus $z_k = 1$, which means $s_k = 0$ from (4.6). Applying the first row of Table 4.1 to the first term of (4.8) and the second row to the second term with $(\alpha, \beta) = (0, 1)$ gives

$$\hat{H}(s) = \frac{-2}{s} + \frac{-1 + 0.5s}{s^2} \tag{4.9}$$

$$= -\frac{1 + 1.5s}{s^2}. \tag{4.10}$$

Table 4.1: s-domain equivalences for z-domain loop filter poles.

z-domain pole	s-domain equivalent	Limit for $z_k = 1$
$\frac{y_0}{z-z_k}$	$\frac{r_0}{s-s_k} \times \frac{y_0}{z_k^{1-\alpha}-z_k^{1-\beta}}$ $r_0 = s_k$	$\frac{r_0}{s-s_k}$ $r_0 = \frac{y_0}{\beta-\alpha}$
$\frac{y_0}{(z-z_k)^2}$	$\frac{r_1 s+r_0}{(s-s_k)^2} \times \frac{y_0}{z_k(z_k^{1-\alpha}-z_k^{1-\beta})^2}$ $r_1 = q_1 s_k + q_0$ $r_0 = q_1 s_k^2$ $q_1 = z_k^{1-\beta}(1-\beta) - z_k^{1-\alpha}(1-\alpha)$ $q_0 = z_k^{1-\alpha} - z_k^{1-\beta}$	$\frac{r_1 s+r_0}{(s-s_k)^2}$ $r_1 = \frac{1}{2}\frac{(\alpha+\beta-2)y_0}{\beta-\alpha}$ $r_0 = \frac{y_0}{\beta-\alpha}$
$\frac{y_0}{(z-z_k)^3}$	$\frac{r_2 s^2+r_1 s+r_0}{(s-s_k)^3} \times \frac{y_0}{z_k^2(z_k^{1-\alpha}-z_k^{1-\beta})^3}$ $r_2 = \frac{1}{2}q_2 s_k - q_1$ $r_1 = -q_2 s_k^2 + q_1 s_k + q_0$ $r_0 = \frac{1}{2}q_2 s_k^3$ $q_2 = (1-\beta)(2-\beta)(z_k^{1-\beta})^2$ $+ (1-\alpha)(2-\alpha)(z_k^{1-\alpha})^2$ $+ [\beta(\beta+3) + \alpha(\alpha+3)$ $- 4(1+\alpha\beta)]z_k^{1-\alpha}z_k^{1-\beta}$ $q_1 = (\frac{3}{2}-\beta)(z_k^{1-\beta})^2 + (\frac{3}{2}-\alpha)(z_k^{1-\alpha})^2$ $+ (\alpha+\beta-3)z_k^{1-\alpha}z_k^{1-\beta}$ $q_0 = (z_k^{1-\alpha} - z_k^{1-\beta})^2$	$\frac{r_2 s^2+r_1 s+r_0}{(s-s_k)^3}$ $r_2 = \frac{1}{12}\frac{y_0}{\beta-\alpha}[\beta(\beta-9)$ $+ \alpha(\alpha-9) + 4\alpha\beta + 12]$ $r_1 = \frac{1}{2}\frac{(\alpha+\beta-3)y_0}{\beta-\alpha}$ $r_0 = \frac{y_0}{\beta-\alpha}$

As noted in §3.2.1, (4.10) was first derived by Candy [Can85] as the CT equivalent of the DT double integration modulator in (4.7). □

Our CT/DT transformations are based on expressing the loop filter in pole-zero form, though this is not the only way to do it. Schreier [Sch96a] uses state-space representation, and others [Sho96, Gao97a] use pole-zero with the modified $\mathcal{Z}$-transform to account for excess delay, something we avoid here for reasons which will be explained below. As well, we only deal with loop filter equivalence, which affects the noise transfer function in the linearized $\Delta\Sigma$M model. There are some subtleties regarding the signal transfer function [Sho96, Sch96a] which we simplify by assuming a signal transfer function of 1 in the signal band. This assumption is approximately valid for most designs.

4.1.3 Effect of Excess Loop Delay

As noted in the introduction, excess loop delay arises because of nonzero transistor switching time, which makes the edge of the DAC pulse begin *after* the sampling clock edge. We assume that excess loop delay can be expressed by

$$\tau_d = \rho_d T_s \tag{4.11}$$

which is depicted for an NRZ DAC pulse in Figure 4.4. The sampling instant is $t = 0$. The value

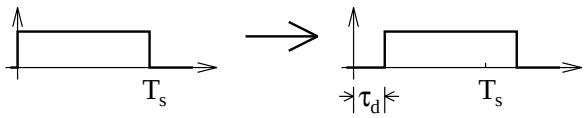


Figure 4.4: Illustration of excess loop delay on NRZ DAC pulse.

of τ_d depends on the switching speed of the transistors f_T, the quantizer clock frequency f_s, and the number of transistors in the feedback path n_t, as well as the loading on each transistor. As a crude approximation, we may assume all transistors switch fully after $1/f_T$, in which case

$$\rho_d \approx \frac{n_t f_s}{f_T}. \tag{4.12}$$

τ_d could end up being a significant fraction of T_s depending on the parameters in (4.12).

Example 4.2: In the design in Figure 4.1, suppose we desire 12-bit DR in a 50MHz bandwidth. This will require an OSR of about 50 [Sch93], which means we must clock at $f_s = 50(2 \cdot 50) = 5$GHz. If the quantizer is an ECL-style latched comparator, its output differential pair must switch; the DAC must also switch, and thus $n_t = 2$. In a $f_T = 30$GHz process, therefore,

$$\rho_d \approx \frac{2 \cdot 5}{30} = 33\% \tag{4.13}$$

is the amount of excess delay predicted by (4.12). □

Excess loop delay is problematic because it alters α and β, which means it affects the equivalence between $\hat{H}(s)$ and $H(z)$. We can calculate the effect mathematically by using Table 4.2 which lists the z-domain equivalents for s-domain $\hat{H}(s)$ poles of orders one through three. As with Table 4.1, these were calculated with the help of Maple and (4.2). An s-domain pole of multiplicity l at s_k maps to one at z_k with the same multiplicity, with

$$z_k = \exp s_k. \tag{4.14}$$

Poles at $s_k = 0$ give numerators of $0^l/0^l$, as before, and the rightmost column gives the formulae that result when l'Hôpital's rule is applied l times.

Example 4.3: Suppose we have designed $\hat{H}(s)$ from (4.10) assuming NRZ DAC pulses, but that we have excess loop delay τ_d, so that in actuality we have NRZ DAC pulses delayed by τ_d as in Figure 4.4. Now, we have $(\alpha, \beta) = (\tau_d, 1 + \tau_d)$. The formulae in Table 4.2 only apply for a pulse with $\beta \leq 1$, but we needn't worry: it is possible to write a τ_d-delayed NRZ pulse as

$$\hat{r}_{(\tau_d, 1+\tau_d)}(t) = \hat{r}_{(\tau_d, 1)}(t) + \hat{r}_{(0, \tau_d)}(t-1), \tag{4.15}$$

that is, as a linear combination of a DAC pulse from τ_d to 1 *and* a one-sample-delayed DAC pulse from 0 to τ_d as shown in Figure 4.5. Writing (4.10) in partial fractions gives

$$\hat{H}(s) = \frac{-1.5}{s} + \frac{-1}{s^2}. \tag{4.16}$$

Table 4.2: z-domain equivalences for s-domain loop filter poles.

s-domain pole	z-domain equivalent	Limit for $s_k = 0$
$\frac{r_0}{s-s_k}$	$\frac{y_0}{z-z_k} \times \frac{r_0}{s_k}$ $y_0 = z_k^{1-\alpha} - z_k^{1-\beta}$	$\frac{y_0}{z-z_k}$ $y_0 = r_0(\beta - \alpha)$
$\frac{r_0}{(s-s_k)^2}$	$\frac{y_1 z+y_0}{(z-z_k)^2} \times \frac{r_0}{s_k^2}$ $y_1 = z_k^{1-\beta}[1 - s_k(1-\beta)]$ $- \; z_k^{1-\alpha}[1 - s_k(1-\alpha)]$ $y_0 = z_k^{2-\alpha}(1 + s_k\alpha)$ $- \; z_k^{2-\beta}(1 + s_k\beta)$	$\frac{y_1 z+y_0}{(z-z_k)^2}$ $y_1 = \frac{r_0}{2}[\beta(2-\beta) - \alpha(2-\alpha)]$ $y_0 = \frac{r_0}{2}(\beta^2 - \alpha^2)$
$\frac{r_0}{(s-s_k)^3}$	$\frac{y_2 z^2+y_1 z+y_0}{(z-z_k)^3} \times \frac{r_0}{s_k^3}$ $y_2 = z_k^{1-\beta}[-1 + s_k(1-\beta) + \frac{s_k^2}{2}(1-\beta)^2]$ $- \; z_k^{1-\alpha}[-1 + s_k(1-\alpha) + \frac{s_k^2}{2}(1-\alpha)^2]$ $y_1 = z_k^{2-\beta}[2 - s_k(1-2\beta)$ $+ \; \frac{s_k^2}{2}(-1 - 2\beta + 2\beta^2)]$ $+ \; z_k^{2-\alpha}[2 - s_k(1-2\alpha)$ $+ \; \frac{s_k^2}{2}(-1 - 2\alpha + 2\alpha^2)]$ $y_0 = z_k^{3-\alpha}(1 + s_k\alpha + \frac{s_k^2}{2}\alpha^2)$ $- \; z_k^{3-\beta}(1 + s_k\beta + \frac{s_k^2}{2}\beta^2)$	$\frac{y_2 z^2+y_1 z+y_0}{(z-z_k)^3}$ $y_2 = r_0[\frac{1}{6}(\beta^3 - \alpha^3)$ $- \; \frac{1}{2}(\beta^2 - \alpha^2) + \frac{1}{2}(\beta - \alpha)]$ $y_1 = r_0[\frac{1}{3}(\beta^3 - \alpha^3)$ $- \; \frac{1}{2}(\beta^2 - \alpha^2) - \frac{1}{2}(\beta - \alpha)]$ $y_0 = \frac{r_0}{6}(\beta^3 - \alpha^3)$

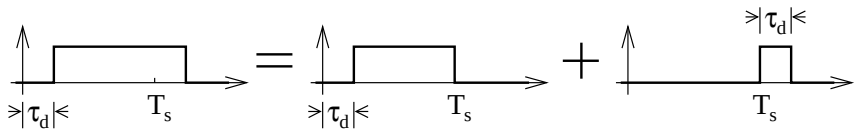


Figure 4.5: Delayed NRZ pulse as a linear combination.

Applying Table 4.2 to each term of (4.16), for each of the two DAC pulses in (4.15), yields

$$\frac{-1.5}{s} \rightarrow \frac{-1.5(1-\tau_d)}{z-1} + z^{-1}\frac{-1.5\tau_d}{z-1} \tag{4.17}$$

$$\begin{aligned}\frac{-1}{s^2} &\rightarrow \frac{(-0.5+\tau_d-0.5\tau_d^2)z+0.5(-1+\tau_d^2)}{(z-1)^2} \\ &+ z^{-1}\frac{\tau_d(-1+0.5\tau_d)z-0.5\tau_d^2}{(z-1)^2}.\end{aligned} \tag{4.18}$$

Adding (4.17) and (4.18) gives

$$H(z,\tau_d) = \frac{(-2+2.5\tau_d-0.5\tau_d^2)z^2+(1-4\tau_d+\tau_d^2)z+(1.5\tau_d-0.5\tau_d^2)}{z(z-1)^2}. \tag{4.19}$$

We can quickly verify that for $\tau_d = 0$, (4.19) turns into (4.7) as it should. However, for $\tau_d \neq 0$, the equivalent $H(z)$ is no longer (4.7).

If instead of Table 4.2 we use the modified $\mathcal{Z}$-transform on (4.7), the result is [Gao97a]

$$H_{MZ}(z,\tau_d) = \mathcal{Z}_m\left[\mathcal{Z}^{-1}\left[\frac{-2z+1}{(z-1)^2}\right]\right] = \frac{(-2+2\tau_d)z^2+(1-3\tau_d)z+\tau_d}{z(z-1)^2}, \tag{4.20}$$

which is similar to (4.19) but not identical. The modified $\mathcal{Z}$-transform assumes the delay happens at the output of $\hat{H}(s)$ (at the quantizer *input*), but in our method we assume the delay happens prior to the DAC pulse (at the quantizer *output*). The literature does not distinguish between these two cases, but they are clearly different. More importantly, our assumption represents reality more closely—the delay is after the quantizer in an actual circuit—so our method is superior to the modified $\mathcal{Z}$-transform. □

We treat pulses as rectangular because it allows exact closed-form solutions in the CT/DT equivalence calculations. Other authors [Ben97] treat pulses as trapezoidal or as having exponential

rising behavior, which is more realistic but which does not lead to exact solutions as easily. A real circuit will likely exhibit DAC pulse shapes more complicated still. The key point is, excess delay always alters the numerator coefficients of the equivalent $H(z)$, and it turns out that using rectangular pulses yields results that are similar to those found using more realistic pulse shapes.

4.2 Double Integration Modulator

How well does a modulator with a loop filter given by (4.19) perform? To study the effects of excess loop delay, Matlab code was written to perform the transformations in Tables 4.1 and 4.2 numerically. The output bit stream from a modulator was determined by solving the difference equation $X(z) = G(z)H(z)U(z) + H(z)Y(z)$ in the time domain with a C program for given $G(z)$ and $H(z)$. The virtue of using the transformations is it allows us to simulate in the DT domain, a process usually significantly more rapid than simulating using $\hat{H}(s)$ in the CT domain[2].

Since first-order modulators with excess delay have been studied already [Gos88] and are of limited practical use due to an excessive presence of harmonics in the output spectrum, we confine ourselves to modulators of orders two and above. In this section, we commence with the double-integration $\Delta\Sigma$M: how is its DR affected by excess delay? We said in §2.2.3 that DR is defined as the difference between the smallest and largest input levels (in dB) which give SNR ≥ 0. At low input levels, SNR is limited by in-band quantization noise (IBN), while a large-enough input level eventually compromises the stability of the modulator. There exists a maximum stable input amplitude (MSA); DR may be found from IBN and MSA, as we explain below.

4.2.1 Root Locus

The easiest way to grasp the effect of excess delay is to linearize the quantizer as was done in §2.1.1 and look at the stability of the noise transfer function. There is, however, a subtlety we ignored in

[2]Though we provide no experimental verification of the results throughout this chapter, we find simulation of Figure 4.1 in Eldo using ideal circuit components and a variable delay in the feedback path gives results that are consistent with those presented in this section. Simulations take much longer with Eldo, however.

Figure 2.1: the gain of a one-bit quantizer isn't well-defined. That is, we could insert a positive gain κ immediately in front of the quantizer and not affect the performance of the circuit—quantizer inputs would be scaled, but their signs remain unchanged, hence the sequence of ± 1 would be identical. Making κ explicit is usually done (Figure 4.6) in the linear model, which results in

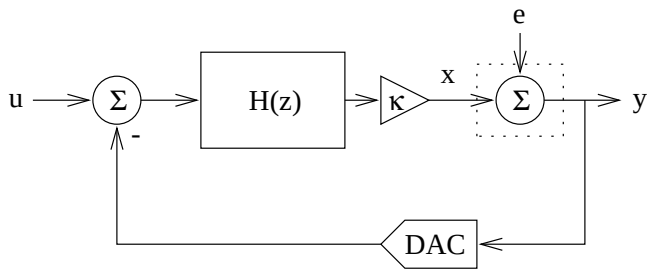


Figure 4.6: Linearized $\Delta\Sigma$M with one-bit quantizer arbitrary gain κ.

NTF$(z, \tau_d) = (1 + \kappa H(z, \tau_d))^{-1}$. Figure 4.7 shows that for $\kappa = 1$ and increasing ρ_d, the poles of NTF(z, τ_d) move towards the unit circle, eventually moving outside at $\rho_d \approx 0.31$. Any choice of $\kappa > 0$ shows a similar movement of poles from their initial positions towards the unit circle; this implies modulator stability worsens as delay increases. Time-domain simulation shows that it takes $\rho_d \approx 0.65$ to make the modulator unstable. The root locus incorrectly predicted $\rho_d = 0.31$ for instability because $\kappa = 1$ was not satisfied in the simulation. How to measure or choose κ is a nontrivial matter [Ris94, Chap. 6] and we do not explore it in detail here; we attempted to use the linear model for characterizing delay with little success. Suffice it to say that it at least makes a *qualitative* prediction that stability worsens with increasing loop delay.

4.2.2 In-Band Noise

In practical terms, we care about how much performance is lost due to excess delay. Figure 4.8(a) shows an output spectrum near dc: 256 16384-point Hann-windowed periodograms with random initial conditions were averaged, and the input signal is a 0.1V sine wave. As the delay increases from 0% up to 60%, we see that the noise floor rises slowly. Integrating the IBN for zero input as a function of τ_d produces Figure 4.8(b): for delays below about 20%, IBN stays roughly constant,

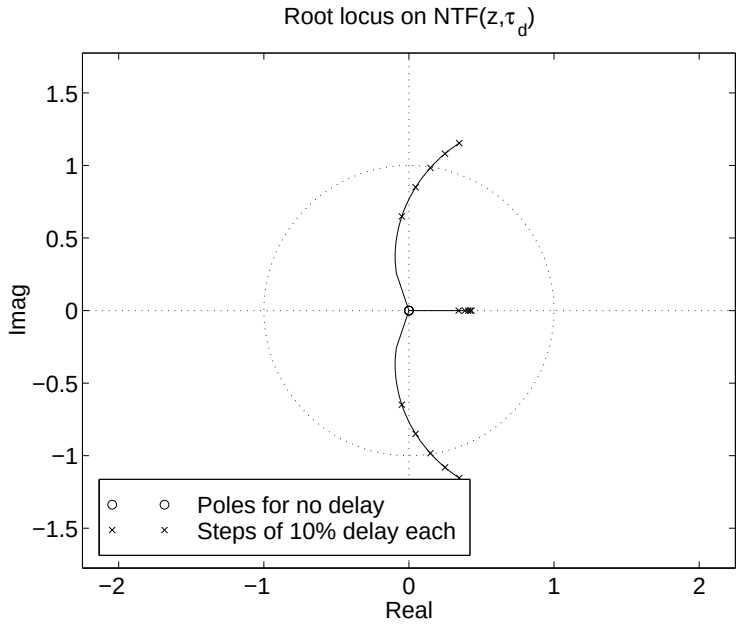


Figure 4.7: Effect of loop delay on root locus of NTF(z, τ_d).

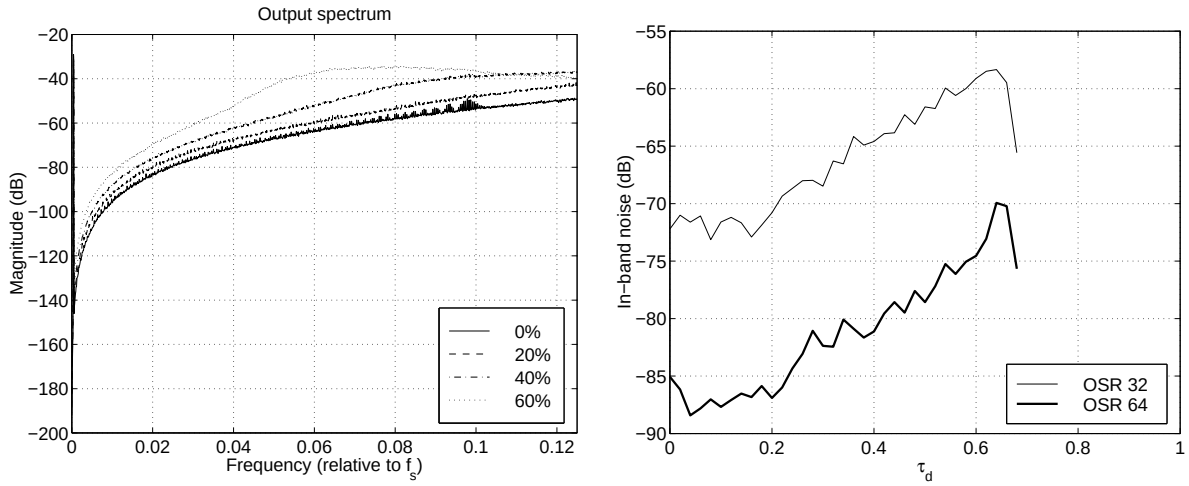
but rises as delay increases[3]. If the excess delay exceeds about 65%, the modulator goes unstable. In this chapter, instability is defined to have occurred if the quantizer input magnitude exceeds 10 before the end of a simulation for 1000 successive simulations with random initial states. A similar definition was used in [Ris94].

The smallest input signal for which SNR $= 0$dB is exactly the IBN, adjusted for the gain of the window (0.375 for Hann, or 4.26dB) and the fact that periodograms measure rms power (3.01dB). For example, the IBN for $\tau_d = 0$ and OSR $= 64$ is -85.06dB, and so we predict that an input magnitude of approximately

$$-85.06 + 4.26 + 3.01 = -77.79\text{dB} \tag{4.21}$$

is needed to get SNR $= 0$dB. In simulation, we find the input magnitude that leads to 0dB SNR to be about -77dB.

[3]The non-monotonicity on the tails of the IBN graphs and certain later DR graphs is not a real effect: it is an artifact of doing simulations with zero input and no dither. Otherwise, the general trends indicated by the curves are accurate.



(a) (b)

Figure 4.8: (a) Output spectrum from double integration CT $\Delta\Sigma$M (b) in-band noise for zero input as a function of loop delay.

4.2.3 Maximum Stable Amplitude

Second, how does the MSA change with loop delay? To determine the MSA, we once again follow Risbo [Ris94]: we apply a ramp input whose amplitude increases slowly from 0 to 1 over 10^5 time steps; when the quantizer input magnitude exceeds 10, the input level at that instant is the MSA. A traditional method [Sch93] involves applying a low-frequency sine wave at the input and running for hundreds of thousands of cycles to check that the modulator remains stable, then increasing the amplitude and repeating the simulation until the maximum amplitude for which the modulator remains stable is found. We find Risbo's method gives approximately the same answer while requiring many fewer simulation runs.

Performing this test for 200 runs with random initial conditions yields the graph in Figure 4.9. The modulator is stable for inputs of up to 0.92 for no excess delay, but this falls more or less linearly to near zero at about 50% delay. An unstable modulator has SNR $= -\infty$, so the MSA is precisely the largest input for which SNR > 0. For example, at $\tau_d = 0$, the MSA is

$$20 \log_{10} 0.92 = -0.72\text{dB}. \tag{4.22}$$

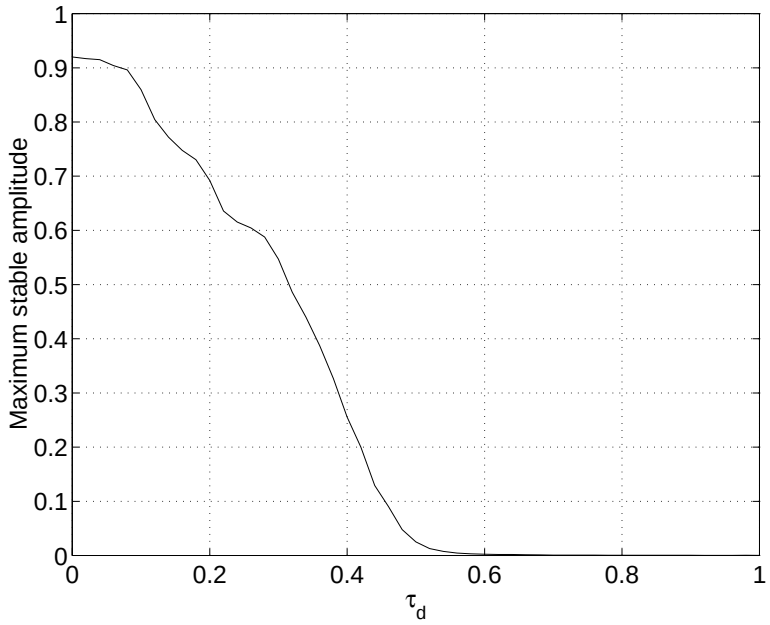


Figure 4.9: Maxmimum stable amplitude for double integration CT $\Delta\Sigma$M.

4.2.4 Dynamic Range

We can combine the previous two results to plot the modulator's DR against delay in Figure 4.10. DR is the difference between MSA and adjusted IBN; for example, at $\tau_d = 0$, equations (4.21) and (4.22) give

$$\text{DR} = -0.72 - (-77.79) = 77.07\text{dB}. \tag{4.23}$$

This is converted to bits using (2.10) and the result is plotted for $0 \leq \tau_d \leq 1$ in Figure 4.10.

Example 4.4: Example 4.2 estimated a loop delay of 33% in (4.13) for OSR $= 50$. We see from Figure 4.10 that even with OSR $= 64$ it would not be possible to achieve the desired resolution at 33% delay: we could only obtain DR $= 11$ bits. To achieve 12 bits at OSR $= 64$, we must have no more than about 20% excess loop delay. For a 50MHz bandwidth, OSR of 64 means clocking at 6.4GHz, and from (4.12), we see that the transistors must have $f_T > 32$GHz or so. □

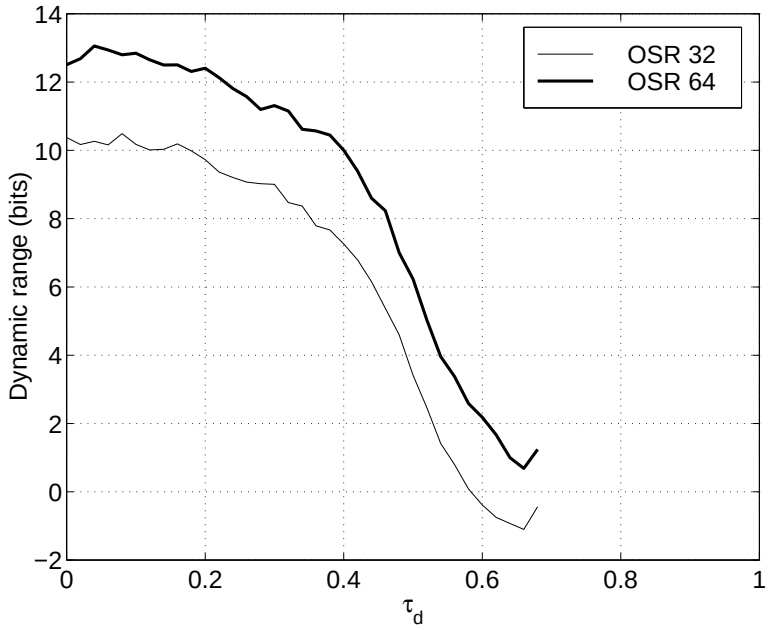


Figure 4.10: Dynamic range for double integration CT $\Delta\Sigma$M.

4.3 $f_s/4$ Fourth-Order Band Pass Modulator

We saw in Figure 2.7 that BP modulators with center frequency $f_s/4$ are potentially useful in radio receivers; indeed, several circuits [Sin95, Gao97b, Jay97, Gao98a] have been built with this application in mind. We noted in §2.1.2 that taking a low pass NTF(z) with a quantization noise notch at dc and performing the substitution $z^{-1} \rightarrow -z^{-2}$ gives a BP NTF(z) with a noise notch at $f_s/4$, one-quarter the sampling frequency, with double the order and identical stability properties to the LP prototype. The substitution can be applied to the loop filter $H(z)$ to yield the same result. Applying this to the double integration modulator (4.7) gives

$$H_{LP}(z) = \frac{-2z^{-1} + z^{-2}}{(1 - z^{-1})^2} \rightarrow H_{BP}(z) = \frac{2z^{-2} + z^{-4}}{(1 + z^{-2})^2}. \tag{4.24}$$

This contains two double poles at $z_k = \pm j$; we could find the equivalent $\hat{H}_{BP}(s)$ by applying the results in Table 4.1 to a partial fraction expansion of (4.24).

Example 4.5: Doing this for NRZ DAC pulses yields

$$\hat{H}_{BP}(s) = \frac{-1.0354s^3 + 1.0652s^2 - 1.3210s + 4.5661}{(s^2 + (\frac{\pi}{2})^2)^2}. \tag{4.25}$$

How do we build a circuit to implement this? Historically, LP DT modulators have been built as a cascade of integrators $z^{-1}/(1 - z^{-1})$ [Cha90], and building an $f_s/4$ BP DT modulator simply requires replacing the integrator blocks directly with resonator blocks $-z^{-2}/(1 + z^{-2})$. It is likewise possible to build LP CT modulators as a cascade of integrators $1/s$—the block diagram for Figure 4.1 is shown in Figure 4.11. However, simply replacing integrators with resonators $As/(s^2 + \omega^2)$, $\omega = \pi/2$ as in

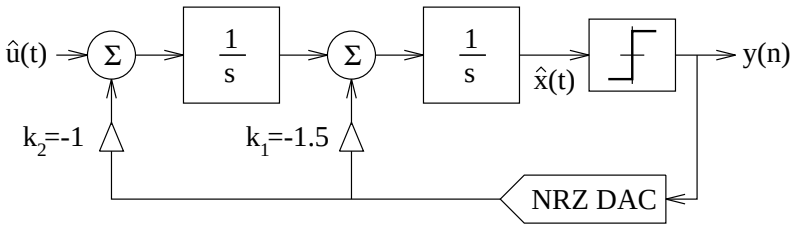


Figure 4.11: Block diagram for LP CT ΔΣM from Figure 4.1.

Figure 4.12 does *not* build (4.25): the numerator of $\hat{H}_{BP}(s)$ for Figure 4.12 does not

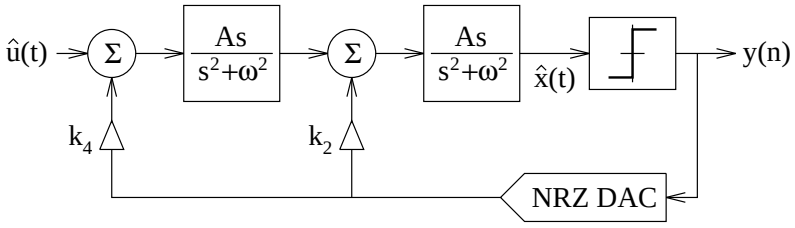


Figure 4.12: Block diagram for BP CT ΔΣM with integrators replaced by resonators that cannot implement desired equivalent $H(z)$.

contain an s^2 or s^0 term, yet each is required in (4.25). Early designs [Thu91] suffered from this problem. □

One solution is to use resonators with a low pass term included in the numerator: $(As + B)/(s^2 + \omega^2)$. A second elegant solution first proposed in [Sho94] and [Sho95] is to use resonators

$As/(s^2+\omega^2)$ with two different types of feedback DAC, leading to the so-called *multi-feedback architecture* in Figure 4.13. There, the DACs are return-to-zero (RZ), which has $(\alpha, \beta) = (0, 0.5)$ in

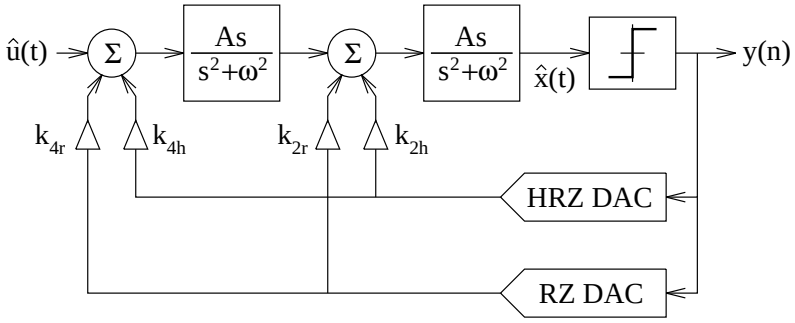
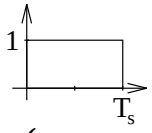


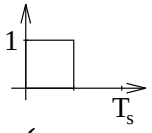
Figure 4.13: Multi-feedback BP CT ΔΣM architecture.

(4.4), and half-delayed return-to-zero (HRZ) $(\alpha, \beta) = (0.5, 1)$. The three types of DAC mentioned so far are depicted in Figure 4.14. All are easy to fabricate in an ECL-style latched comparator, a



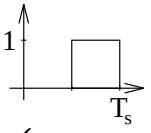
$$\hat{r}_{NRZ}(t) = \begin{cases} 1, & 0 \le t < T_s \\ 0, & \text{otherwise} \end{cases}$$

$$\hat{R}_{NRZ}(s) = \frac{1 - e^{-sT_s}}{s}$$



$$\hat{r}_{RZ}(t) = \begin{cases} 1, & 0 \le t < T_s/2 \\ 0, & \text{otherwise} \end{cases}$$

$$\hat{R}_{RZ}(s) = \frac{1 - e^{-sT_s/2}}{s}$$



$$\hat{r}_{HRZ}(t) = \begin{cases} 1, & T_s/2 \le t < T_s \\ 0, & \text{otherwise} \end{cases}$$

$$\hat{R}_{HRZ}(s) = e^{-sT_s/2}\frac{1 - e^{-sT_s/2}}{s}$$

Figure 4.14: Common DAC pulse types.

typical circuit diagram of which is shown in Figure 4.15. By diode-connecting the final differential pair rather than cross-coupling them [Gao98a], an RZ rather than an NRZ waveform is output. In the multi-feedback architecture, we could have used any two of NRZ, RZ, and HRZ, or for that matter any other two different pulses, but those three types are easiest to build in a practical circuit.

The numerator of $\hat{H}_{BP}(s)$ implemented in Figure 4.13 can be set by altering the k coefficients.

Example 4.6: We wish to find how to set the ks so that the equivalent $H_{BP}(z)$ is that in (4.24); this is done by converting $\hat{H}_{BP}(s)$ to the z-domain using Table 4.2 for each DAC separately, then linearly combining the results and solving for the ks. It can

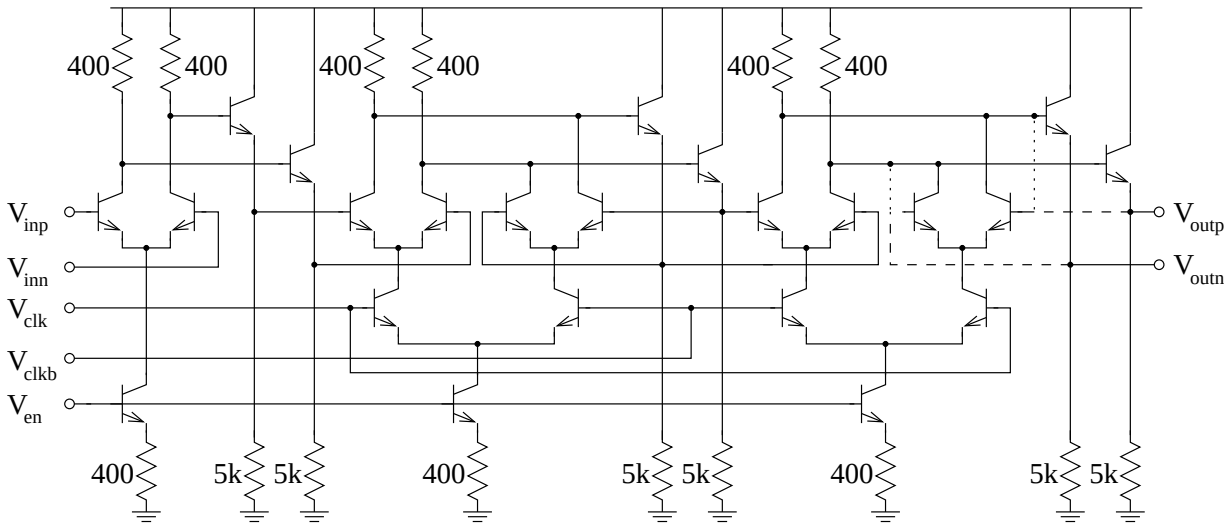


Figure 4.15: ECL-style latched comparator with preamplification for enhanced resolution at high speed. For an NRZ comparator, connect the final differential pair via the dashed lines; for RZ, connect the dotted lines instead.

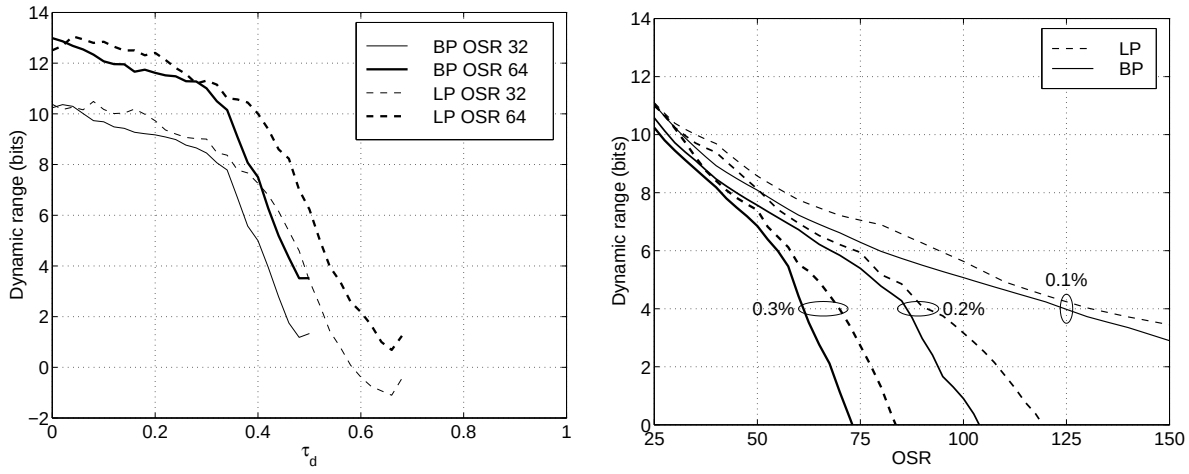
be calculated that

$$\{k_{r4}, k_{r2}, k_{h4}, k_{h2}\} = \{-1.08678, -2.13388, 0.45016, 1.48744\} \tag{4.26}$$

are the k values that implement (4.24) when the CT modulator uses RZ and HRZ DACs. □

How does excess delay affect this design? Both leading DAC edges become delayed by τ_d. Exactly the same simulations were carried out for this BP modulator as were done in the previous section (IBN and MSA), only instead of using a dc input to find the MSA, a sine wave input at $f_s/4$ whose amplitude increases from 0 to 1 over 10^5 time steps is used. Again, this method is rapid, and we find it to gives similar results to using a sine wave input with fixed amplitudes and frequencies near $f_s/4$, simulating for many cycles to see if the modulator remains stable, then increasing the amplitude and repeating the simulation.

The resulting DR as a function of τ_d is plotted in Figure 4.16(a); for comparison, the results from Figure 4.10 for the double integration modulator are overlaid with dashed lines. Interestingly, the two designs perform the same until about about 30% excess delay, at which point the BP design becomes more severely affected; the exact reason for this is unclear to the author. It goes unstable



(a) (b)

Figure 4.16: (a) Dynamic range for multi-feedback BP CT $\Delta\Sigma$M, with comparison to double integration results. (b) Same graph with OSR as independent variable; numbers on curves are $\tau_d \times f_N$.

for about 50% excess delay. These results do not change if a different pair of DAC pulses are selected. Figure 4.16(b) plots the same results only with OSR as the independent variable; the parameter on the curves is the product of τ_d and f_N, the Nyquist rate. Thus, for example, a modulator with a desired $f_N = 2$MHz and a fixed delay of $\tau_d = 1$ns has $\tau_d \times f_N = 10^{-3} = 0.1\%$, and the DR at a given clock speed $f_s \equiv \text{OSR} \cdot f_N$ may be found from the graph.

Previous examinations of this modulator [Sho96, §3.1.4], [Gao97a] which found 25% delay required for instability made two errors. First, the modified $\mathcal{Z}$-transform was used which led to an incorrect $H_{BP}(z, \tau_d)$. Second, simulations were carried out with a large fixed-amplitude tone, which fails to take into account the changing modulator MSA with increasing delay.

4.4 Higher-Order Modulators

We now turn to the effects of excess loop delay for low pass CT $\Delta\Sigma$Ms of order higher than two. This has been examined cursorily using the modified $\mathcal{Z}$-transform in [Hor90], but nowhere else to the author's knowledge. The architecture we will consider is a generalization of Figure 4.11

which was first shown in Figure 2.6, reproduced here with CT integrators in Figure 4.17. It is

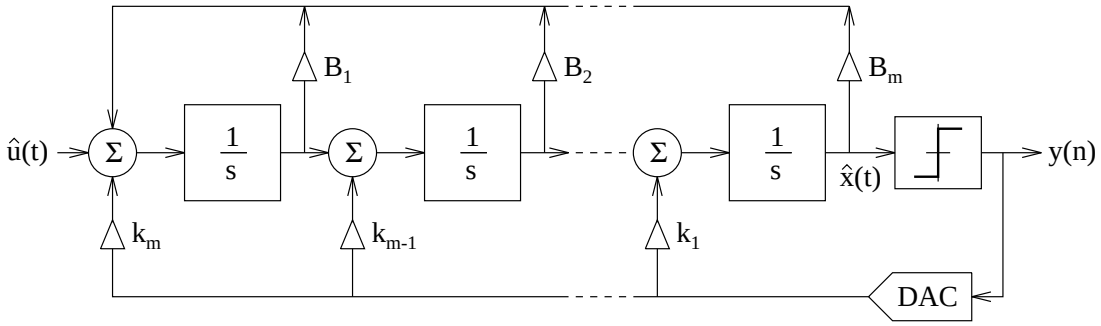


Figure 4.17: Block diagram for general high-order LP CT ΔΣM .

straightforwardly realizable in VLSI with transconductors, integrators, and differential pair DACs as in Figure 4.1. The loop filter realized by this architecture for $m \geq 2$ is

$$\hat{H}(s) = \frac{\sum_{i=1}^{m} (\frac{1}{s})^i [k_i - \sum_{j=1}^{i-1} k_{i-j} B_j]}{1 - \sum_{i=1}^{m} B_i (\frac{1}{s})^i}. \tag{4.27}$$

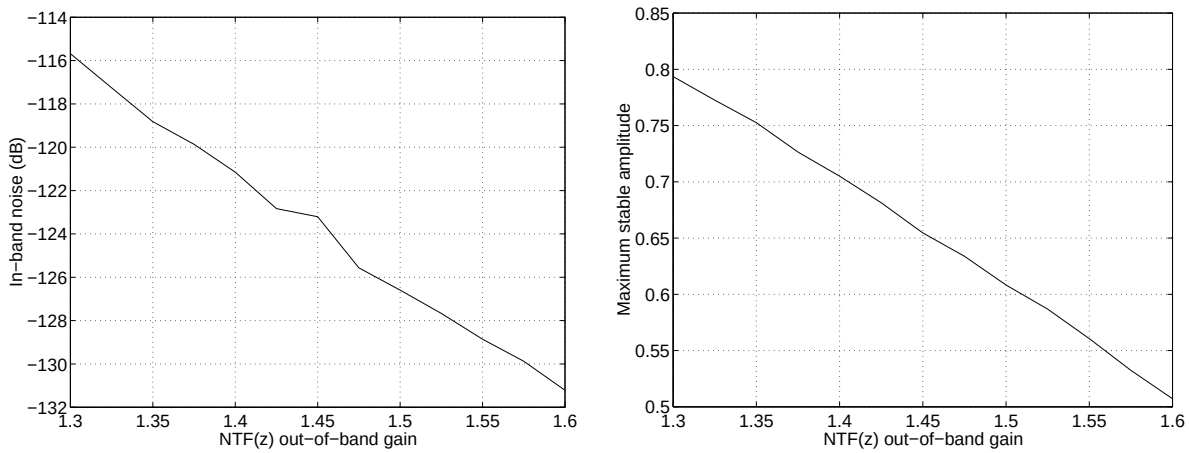
(4.27) shows that the purpose of the B_is is to allow us to implement NTF(z) zeros at places other than dc (i.e., $z = 1$).

Four types of high-order modulators were designed using NTF prototyping. The NTFs used had

- Third-order Butterworth poles, all zeros at $z = 1$;
- Third-order Butterworth poles, optimally-spread zeros;
- Fourth-order Butterworth poles, optimally-spread zeros;
- Fifth-order Chebyshev poles, optimally-spread zeros.

The spread-zero modulators had zeros placed according to [Sch93] so that IBN would be minimized for a given OSR. Modulators with out-of-band gains (OOBGs) of 1.3, 1.4, 1.5, and 1.6 were all designed—higher OOBG means lower IBN at the price of MSA [Nor97, Chap. 4].

Example 4.7: We demonstrate this quickly for a fifth-order Chebyshev modulator with zeros spread assuming OSR $= 64$. Figure 4.18(a) shows that IBN falls from



(a) (b)

Figure 4.18: Effect of out-of-band-gain on fifth-order Chebyshev modulator: (a) IBN, (b) MSA.

-116dB for OOBG $= 1.3$ down to -131dB for OOBG $= 1.6$. At the same time, MSA falls from about 0.79 to about 0.51. Note that IBN is plotted on a logarithmic scale but MSA is on a linear scale; DR increases from 17.4 to 19.3 bits over that range of OOBG. □

The DR as a function of excess loop delay for NRZ DAC pulses and OSRs of both 32 and 64 are summarized in the graphs in Figure 4.19. The results are most intriguing. The modulators with OOBG $= 1.3$ remain stable even for one full sample excess delay, and moreover they only suffer a dynamic range loss of between two and three bits. This contrasts starkly with the results for the second-order LP and fourth-order BP circuits. Increasing OOBG results in modulators which have generally better resolution at no delay, but which become unstable for less excess delay. This makes perfect sense: higher OOBG means a generally less-stable $H(z)$, and in fact we see the τ_d needed for instability is roughly inversely proportional to OOBG. This suggests that higher-order modulators enjoy an advantage over the lower-order ones: the existence of a parameter, OOBG, which we may select according to our resolution *and* excess delay imperviousness requirements, though only extremely recently has anyone published a high-speed CT $\Delta\Sigma$M design with an order higher than two (recall [Mor98] in Table 3.1). To be fair, one *can* vary the OOBG in a second-order

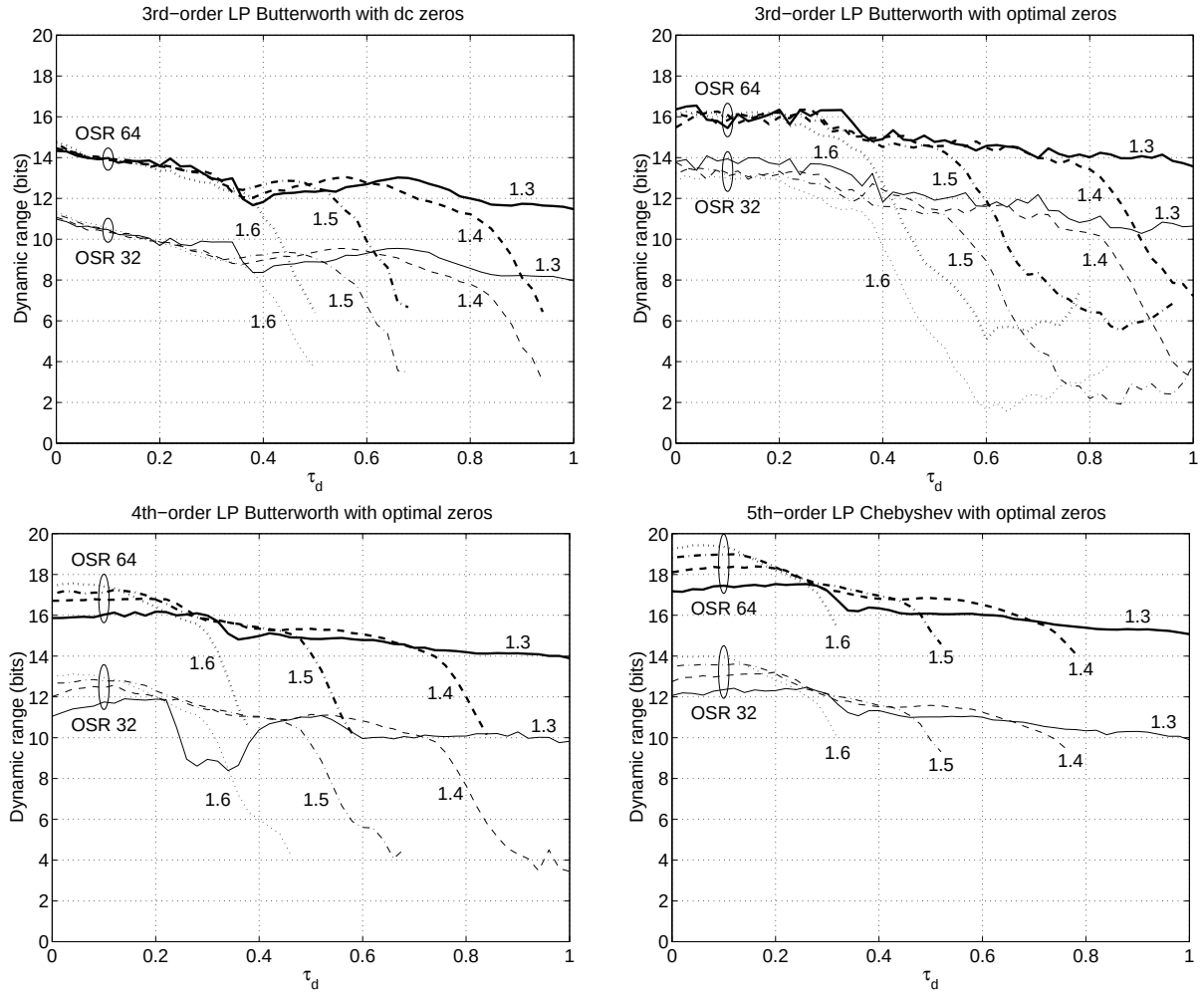


Figure 4.19: Dynamic range for high-order LP CT ΔΣMs. Numbers on curves are OOBG values.

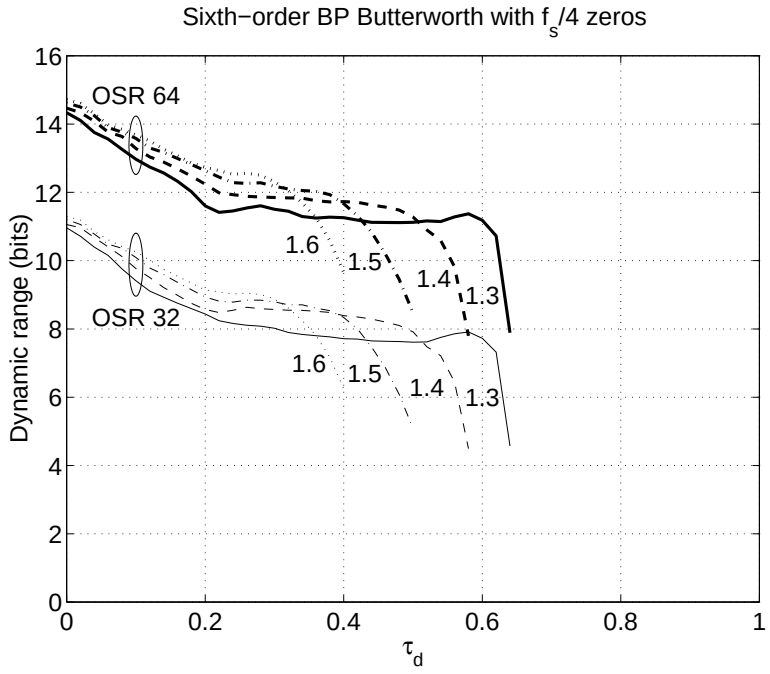


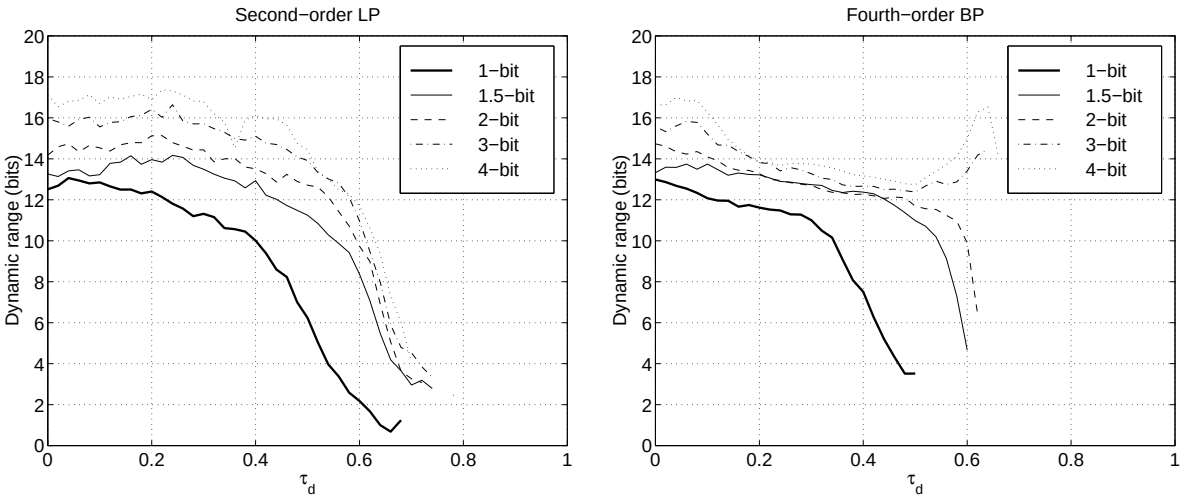
Figure 4.20: Dynamic range for sixth-order BP CT $\Delta\Sigma$M. Numbers on curves are OOBG values.

LP $\Delta\Sigma$M, but it is rarely done in practise.

For interest's sake, a sixth-order $f_s/4$ BP design was also tested by taking the low pass NTF with third-order Butterworth poles and three dc zeros and transforming it to a band pass design using $z^{-1} \rightarrow -z^{-2}$. This can be implemented using the multi-feedback architecture in Figure 4.13 with a third resonator and an additional feedback coefficient for each DAC. DR is plotted against τ_d in Figure 4.20. Comparing these curves to those of the equivalent third-order LP design (the upper-left graph of Figure 4.19) illustrates behavior like that in Figure 4.16: the BP curves have the same shape as those of the LP curves for low excess delay, but they become unstable sooner as excess delay increases. Significantly, the LP modulator with OOBG $= 1.3$ was stable for a full sample of excess delay, while the same BP modulator is only stable up until $\tau_d = 0.65$.

In conclusion, LP modulators of order higher than two let us choose OOBG as an anti-delay measure at the cost of resolution. High-order multi-feedback BP modulators do likewise, though their immunity to excess delay isn't as good as in their LP counterparts[4]. It is believed that these

[4]The Matlab code written to do the transformations was unfortunately not sophisticated enough to handle BP



(a) (b)

Figure 4.21: Modulators with multibit quantizers: (a) second-order LP, (b) fourth-order BP.

results are new. Finally, in fairness, even though the resolution of some of the ideal modulators in Figure 4.19 exceeds 16 bits, it is unlikely that GHz-speed modulators would achieve such a high resolution because other nonidealities such as thermal noise and clock jitter will almost surely limit performance more than quantization noise [Dia92a]. We will discuss these in the chapters to come.

4.5 Modulators with a Multibit Quantizer

Thus far, this study has simulated $\Delta\Sigma$Ms employing a single-bit quantizer. It is known that multibit quantizers in DT designs improve stability, particularly for high-order designs [Nor97, Chap. 8]. If the previous section is any guide, we can hope for an improvement in the immunity of CT designs with a multibit quantizer to excess delay. The author has not seen this studied elsewhere.

There is some improvement, but not a lot. Figure 4.21(a) shows the DR against excess delay for the second-order LP modulator for OSR $= 64$, while Figure 4.21(b) is for the fourth-order BP modulator. The thick lines are from Figure 4.10 and Figure 4.16, the results for a 2-level (1-bit)

modulators with non-coincident NTF zeros, though it seems reasonable to assume the results for such modulators would echo those seen in Figure 4.20.

quantizer, and the other lines are for 3-, 4-, 8-, and 16-level (1.5-, 2-, 3-, and 4-bit) quantizers. Generally, DR improves with quantizer resolution as expected, and furthermore the τ_d range over which the modulators remain stable improves a little with increasing quantizer resolution. Similar results are seen for the high-order LP modulators as for the second-order LP modulator. We see the fourth-order BP circuit can be stable for τ_d close to 0.7 with a 4-bit quantizer compared to 0.5 for a 1-bit quantizer. Again, similar results are seen for the sixth-order BP modulator.

We noted in §3.1.2 the traditional problem in multibit designs: any level mismatches in the multibit feedback DAC are directly input-referred, thereby limiting the achievable performance. Implementing either DEM or digital post-correction on the same chip as the modulator might be a problem because both would require digital circuitry switching at f_s, which would cause a great deal of switching noise that might couple through the substrate into the forward modulator circuitry and degrade performance. Moreover, DEM would mean switching circuitry in the feedback path, which would add excess delay. Multibit quantizers are attractive both for stability and for reducing jitter sensitivity [Ada98], something we consider further next chapter, though no one has yet attempted to build a high-speed CT $\Delta\Sigma$M with a multibit quantizer probably because of the difficulties just mentioned.

4.6 Compensating for Excess Loop Delay

We have seen that it is possible to make a modulator immune to excess delay by choosing its OOBG appropriately. However, there exist methods of actually compensating for delay. We turn now to discussing them for single-bit designs, though the results are equally applicable to multibit designs. We explore some past proposals in more detail than previously reported and also suggest some new methods.

4.6.1 DAC Pulse Selection

In §4.2, we considered the second-order LP $\Delta\Sigma$M with NRZ DAC pulses. A problem with this kind of pulse is that any excess loop delay $\tau_d > 0$ causes $\beta > 1$, which means the end of the pulse

extends beyond $t = 1$. We saw in equations (4.15) through (4.19) that this increases the order of the resulting equivalent $H(z)$: in (4.19), $H(z)$ has the two poles at $z = 1$, but it acquires an additional pole at $z = 0$ for $\tau_d > 0$. Thus, the second-order modulator we tried to build actually has a *third* order loop filter[5]. In general, in any CT modulator with enough excess delay to push the falling DAC pulse edge past $t = 1$, the order of the equivalent DT loop filter is one higher than the order of the CT loop filter. Thus, a multi-feedback BP modulator using either an NRZ or HRZ pulse increases in order, as do the higher-order LP modulators from §4.4 with NRZ DACs. Another way to think about this increase in order is that it adds intersymbol interference: the DAC pulse from a previous symbol overlaps the current one.

If we were to use DAC pulses with $\beta < 1$, then the pulses would extend past $t = 1$ only if the condition

$$\tau_d > 1 - \beta \tag{4.28}$$

held. This suggests the following for the second-order LP modulator in Figure 4.11: if we used an RZ DAC instead of an NRZ DAC, $H(z)$ would remain second-order for $\tau_d \leq 0.5$. If we knew exactly what τ_d was, we could select the feedback coefficients $\{k_2, k_1\}$ to get exactly the equivalent $H(z)$ from (4.7).

Example 4.8: For Figure 4.11, the loop filter is

$$\hat{H}(s) = \frac{k_2 + k_1 s}{s^2}. \tag{4.29}$$

Applying Table 4.2 to the partial fraction expansion of this for $(\alpha, \beta) = (\tau_d, \tau_d + 0.5)$ gives

$$H(z, \tau_d) = \frac{[4k_1 + k_2(3 - 4\tau_d)]z + [-4k_1 + k_2(1 + 4\tau_d)]}{8(z-1)^2}. \tag{4.30}$$

We wish for this to equal (4.7); equating powers of z in the numerator and solving yields

$$\{k_2, k_1\} = \{-2, -\frac{5}{2} - 2\tau_d\}. \tag{4.31}$$

[5]For small τ_d, the NTF has a pole and a zero close to one another which almost cancel, so the design appears approximately second-order in that case.

Thus, for a given $\tau_d \leq 0.5$ and RZ DAC pulses, we can make our $\hat{H}(s)$ match exactly the desired $H(z)$ by *tuning* the parameter k_1. In the particular circuit of Figure 4.1, this is accomplished by changing the value of the current source in the rightmost differential pair DAC. □

It has long been recognized that it is sensible to use RZ DAC pulses in low pass CT $\Delta\Sigma$Ms [Ada86, Com91, Cha92, Nar94, Mit95]. Apart from the immunity to excess delay it afford us, an RZ DAC also alleviates intersymbol interference problems caused by asymmetric DAC pulse rise and fall times [Ada86]. However, the differential circuit architecture of Figure 4.1 also avoids this asymmetry even with NRZ pulses [Jen95].

4.6.2 Feedback Coefficient Tuning

As we have noted, if there exists enough excess delay to push the falling edge of a DAC pulse past $t = 1$, the modulator order increases by one. Therefore, there will be $m + 1$ coefficients in the numerator of the equivalent $H(z)$; with only m feedback coefficients k, the system is not fully controllable via these ks alone. Previous examinations of loop delay in $f_s/4$ BP $\Delta\Sigma$Ms (notably [Sho96, §3.1.4] and [Gao97a]) have studied the system in Figure 4.13 using the modified $\mathcal{Z}$-transform and found the number of parameters in the numerator is m. The multi-feedback architecture achieves a numerator coefficient of 0 for the z^{-1} term only because of perfect cancellation in the $\tau_d = 0$ case. For $\tau_d \neq 0$ the cancellation is ruined so the coefficient of z^{-1} is nonzero, yet the modified $\mathcal{Z}$-transform incorrectly finds it to remain zero. There are actually $m + 1$ rather than m numerator coefficients for $f_s/4$ BP modulators with excess delay.

Even though delay causing $\beta > 1$ means the system cannot be controlled perfectly with the ks, *some* degree of control can be exercised. We demonstrate the helpfulness of this on the fourth-order multi-feedback modulator in Figure 4.13.

Example 4.9: Suppose there is a fixed excess delay of $\tau_d = 35\%$: Figure 4.16 shows that for OSR $= 64$, a DR of 9.9 bits is achieved using the nominal k values in (4.26). It is found that IBN $= -78$dB and MSA $= 0.34$ at this τ_d.

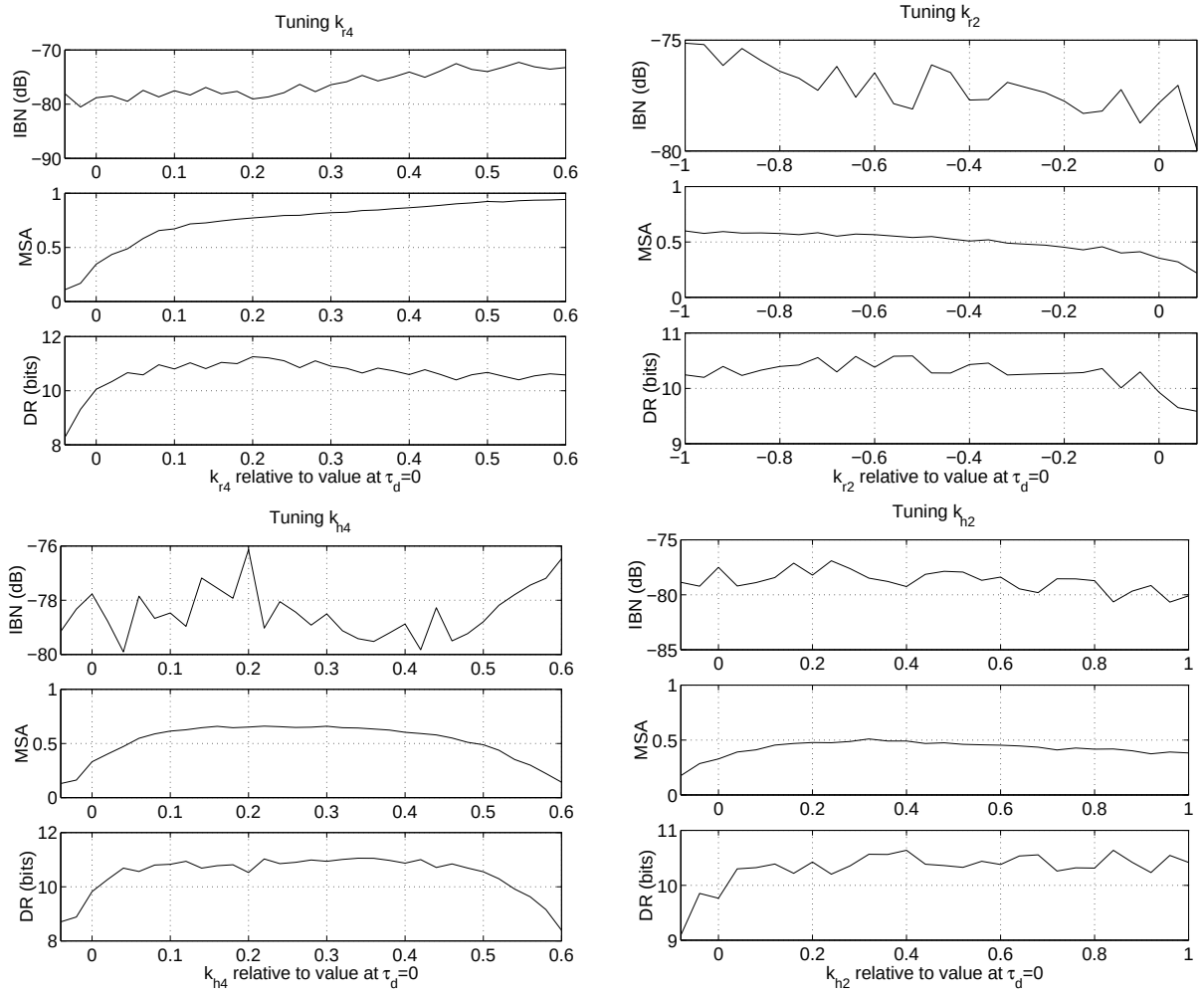


Figure 4.22: Fourth-order $f_s/4$ BP CT $\Delta\Sigma$M performance at $\rho_d = 35\%$ delay with feedback coefficient tuning.

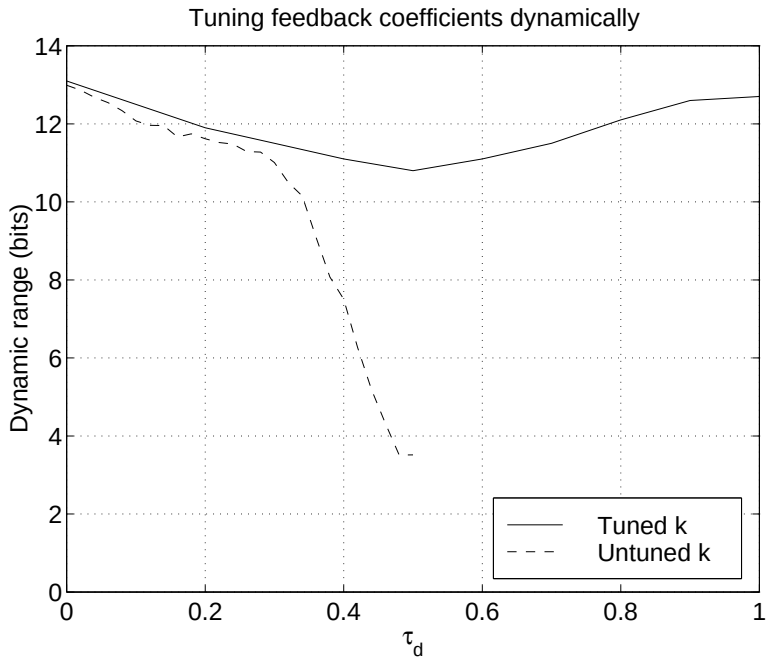


Figure 4.23: Multi-feedback BP modulator dynamic range with k tuning.

Figure 4.22 shows how the performance of the modulator is affected when the ks are tuned one at a time away from their nominal values. By adopting a steepest-descent tuning approach where each k is tuned iteratively until the DR is maximized, we find that it is possible to improve the DR from 9.9 bits to 11.3 bits, still at $\tau_d = 0.35$. The IBN and MSA are both improved, IBN to -79dB and MSA to 0.74. The k values which give this performance are approximately

$$\{k_{r4}, k_{r2}, k_{h4}, k_{h2}\} = \{-0.87, -1.83, 0.48, 1.89\}. \tag{4.32}$$

The tuned k performance is still not as good as the 13 bits achieved at no excess delay in Figure 4.16, but it is an improvement compared to the untuned k performance. □

An interesting thing happens when we tune the ks to maximize performance over a wide range of excess delay values. To wit:

Example 4.10: Figure 4.23 compares the modulator DR for untuned k parameters

from Figure 4.16 and tuned k parameters where the steepest-descent algorithm was applied for several different values of excess delay between 0 and 1. We see that it is possible to find k values which keep the modulator stable for the entire range of τ_d. What is perhaps more surprising is that performance worsens up to 50% excess delay, but then actually starts to improve again until there is a full sample delay, whereupon the performance becomes as good as it was for no delay at all! How can this apparently incongruous result be true?

Recall $H_{BP}(z)$ in (4.24): the numerator was $2z^{-2} + z^{-4}$. The z^{-2} means there is a two-sample delay in the feedback; every $\Delta\Sigma$M must have at least one sample of delay in order to be causal. We found the equivalent $\hat{H}_{BP}(s)$ in (4.25); the two-sample delay is implicit in this equation. Note that

$$H_{BP}(z) = \frac{2z^{-2} + z^{-4}}{(1+z^{-2})^2} = z^{-1}\frac{2z^{-1} + z^{-3}}{(1+z^{-2})^2}. \tag{4.33}$$

This suggests we could place a digital latch that provides one sample of delay (z^{-1}) prior to the DACs, and then find the equivalent $\hat{H}_{BP}(s)$ for the $H(z)$ with numerator $2z^{-1} + z^{-3}$. In other words, we have two choices for building a two-sample delay into the CT feedback loop: by matching to an $H(z)$ with two delays in the numerator, *or* by providing a latch which adds one delay and matching to an $H(z)$ with one delay in the numerator. These are denoted, respectively, the *zero* and *one digital delay* schemes in [Sho96]. This choice is peculiar to $f_s/4$ BP modulators; it does not exist for LP modulators or BP modulators at a different frequency because they invariably have a nonzero z^{-1} term in the numerator, and therefore $H(z)$ would become non-causal if we were to factor out a z^{-1} as we did in (4.33).

For each scheme, it is possible to find analytically the feedback ks which implement the desired $H(z)$:

$$\{k_{r4}, k_{r2}, k_{h4}, k_{h2}\} = \begin{cases} \{-1.0868, -2.1339, 0.4502, 1.4874\}, & \text{zero digital delay,} \\ \{-0.4502, -0.6339, 1.0868, 2.9874\}, & \text{one digital delay,} \end{cases} \tag{4.34}$$

where the first set of ks is from (4.26). The reason for the identical DR performance observed at both $\tau_d = 0$ and $\tau_d = 1$ is now clear: for $\tau_d = 1$, the optimal ks are those in the second row of (4.34), and the steepest-descent algorithm turns out to converge to values close to those. For $0 < \tau_d < 1$, the ks for optimal DR lie in between the zero and one digital delay values—compare, for example, (4.32) for $\tau_d = 0.35$ to (4.34)—though unfortunately the relationship between τ_d and the ks which optimize DR is not linear. For example, for $\tau_d = 0.5$, picking k values that lie exactly half way between the values in (4.34) leads to DR $= 9.2$ bits, though the steepest-descent algorithm found k values to make a modulator with DR $= 10.8$ bits. □

Figure 4.23 is strong encouragement to design the ks to be tunable, possibly even for on-line calibration against process and temperature variations. How to design a tuning algorithm to maximize DR that works on-chip, perhaps even while the modulator is operating, is an interesting topic for future research.

4.6.3 Additional Feedback Parameters

If $\beta > 1$ causes the modulator order to increase from m to $m + 1$, and we only have m feedback coefficients, then it stands to reason that employing an additional feedback should restore full controllability to the system. This has been suggested in [Ben97]: in the block diagram of Figure 4.11, a third NRZ feedback was added whose output goes directly to a summing node after the second integrator (that is, immediately prior to the quantizer). To use this approach in a circuit architecture like Figure 4.1, where the quantizer input must be a voltage but summation is done with currents, we would have to add a transconductor followed by a current-to-voltage converter in between the second op amp and quantizer.

We can avoid adding components in the forward $\Delta\Sigma$M path by using an additional feedback with a *different* kind of DAC pulse. This is akin to the multiple feedbacks in the multi-feedback BP circuit, but it is believed that this has not been suggested previously for delay compensation in LP modulators.

Example 4.11: Consider again Figure 4.11: let us denote its NRZ feedback parameters $k_{n2} = k_2$ and $k_{n1} = k_1$, and let us suppose there is a third feedback which goes to the same summing node as k_{n1}: an HRZ DAC with coefficient k_{h1}. The z-domain equivalents for the NRZ pulses with excess delay have already been found in (4.17) and (4.18); to generalize them to feedbacks k_{n1} and k_{n2} instead of -1.5 and -1 is a trivial change to those equations. For an HRZ pulse delayed by τ_d, the z-domain equivalent is

$$\frac{k_{h1}}{s} \rightarrow \frac{k_{h1}(0.5-\tau_d)}{z-1} + z^{-1}\frac{k_{h1}\tau_d}{(z-1)}. \tag{4.35}$$

Combining this with (4.17) and (4.18) yields

$$H(z) = \frac{y_2 z^2 + y_1 z + y_0}{z(z-1)^2} \tag{4.36}$$

where $\{y_2, y_1, y_0\}$ are expressions involving $\{k_{n2}, k_{n1}, k_{h1}, \tau_d\}$. We wish for the numerator of this to equal $-2z^2 + z$ from (4.7), and Maple can be used to solve symbolically for the k values:

$$\begin{array}{rcl} k_{n2} & = & \frac{\tau_d^2+2}{\tau_d^2-2}, \\ k_{n1} & = & \frac{-\tau_d^4+4\tau_d^3-12\tau_d^2+10\tau_d+4}{\tau_d^2-2}, \\ k_{h1} & = & \frac{\tau_d^4-4\tau_d^3+13\tau_d^2-12\tau_d-2}{\tau_d^2-2}. \end{array} \tag{4.37}$$

Therefore, given the excess delay τ_d, we can get exactly the $H(z)$ in (4.7) by tuning the feedbacks to the values given in (4.37).

We could also use an HRZ pulse fed back to the first summer; this would give us different equations from (4.37), but it would still be possible to achieve the $H(z)$ in (4.7). However, we could *not* use an RZ pulse in place of an HRZ pulse. This is because for $\tau_d \leq 0.5$, the RZ pulse would not contribute to y_0 in (4.36): only k_{n2} and k_{n1} would, and thus to set $y_0 = 0$ (as (4.7) dictates) would require $k_{n2} = k_{n1} = 0$, which renders the feedback inoperational. □

How do we add an additional parameter to the BP multi-feedback architecture for delay compensation? Interestingly, adding an NRZ pulse to Figure 4.13 turns out not to work. This is because

an NRZ pulse is a linear combination of RZ and HRZ pulses, so its feedback parameters are not independent. An independent pulse is needed—for example a pulse with $(\alpha, \beta) = (0.25, 1)$ in combination with any two of NRZ, RZ, and HRZ—but generating a pulse other than these latter three might be nontrivial at high speed.

4.7 Summary

Excess loop delay in a CT $\Delta\Sigma$M is a delay between the sampling clock edge and the change in output bit as seen at the feedback point in the modulator. It arises because of the nonzero switching time of the transistors in the feedback path, and is significant because it alters the equivalence between the CT and DT representations of the loop filter, $\hat{H}(s)$ and $H(z)$. Its effect on performance is noticeable if the sampling clock speed is an appreciable fraction (10% or more) of the maximum transistor switching speed; this is becoming more likely nowadays as desired conversion bandwidths increase and delta-sigma modulation with an aggressively-high clock rate relative to the transistor switching speed is considered for the converter architecture.

If excess delay is not designed for, then as excess delay increases as a fraction of the clock period, second-order LP and fourth-order $f_s/4$ BP modulators will suffer in terms of in-band noise, maximum stable input amplitude, and dynamic range. Higher-order LP designs seem more robust if designed using NTF prototyping because there is a parameter, the out-of-band gain, which can be selected to give some immunity to excess delay. Higher-order BP designs are also more robust than lower-order ones, but a multi-feedback $f_s/4$ BP design is always found to be less immune to excess delay than the corresponding LP design. The use of a multibit quantizer is somewhat helpful, though incorporating the usually-needed correction circuitry for a feedback DAC with mismatched levels is nontrivial for high-speed designs.

It is sensible—nay, imperative—to recognize the presence of excess delay and take it into account in the design process. Choosing the right DAC pulse shape in combination with tuning of the feedback parameters (either in the design phase or automatically on-line) can greatly mitigate the performance loss due to delay. In fact, taking excess delay into account renders it effectively a

nonproblem. Our study has contributed a number of useful new results: we use a transformation method which treats the delay as occurring after the quantizer, not before as the modified $\mathcal{Z}$-transform does; we consider both the change in noise *and* MSA with delay; we show how delay affects high-order designs, as well as multibit designs; and we demonstrate compensation methods based on RZ DAC pulses and additional feedbacks using independent DAC pulses.

Chapter 5

Clock Jitter

Timing jitter in the quantizer clock, usually called clock jitter, is an important mechanism of performance degradation in CT $\Delta\Sigma$Ms. It is a more severe problem than in DT designs for a reason that can be understood as follows. On the left of Figure 5.1, a typical circuit voltage waveform for

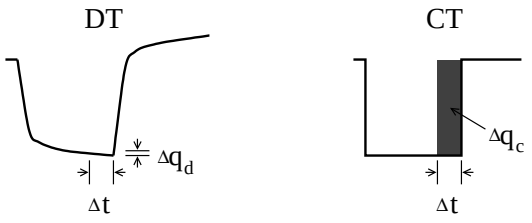


Figure 5.1: Clock jitter effect in DT vs. CT design.

an SC DT $\Delta\Sigma$M is depicted. Most of the charge transfer occurs at the start of the clock period so that the amount of charge Δq_d lost due to a timing error is relatively small. By contrast, the right of Figure 5.1 shows the DAC output currents in a CT circuit such as Figure 4.1; here, charge is transferred at a constant rate over a clock period, and so charge loss Δq_c from the same timing error is a larger proportion of the total charge. Moreover, in a DT design, jitter in the input sample-and-hold (S/H) clock means only the input waveform is affected. In a CT design, the sampling occurs at the quantizer rather than the input, which means the jitter affects the sum of the input plus quantization noise—a signal with considerably more power than the input alone. Hence, CT $\Delta\Sigma$Ms are more sensitive to clock jitter than DT designs [vdZ96].

Clock jitter causes a slight random variation in the amount of charge fed back per clock cycle. Put another way, it is akin to adding a random phase modulation to the output bit stream. In an oversampled converter, the spectrum of the output stream is very noisy outside the (narrow) signal band; a random phase modulation causes the noise outside the signal band to fold into the signal band, raising the converter noise floor and degrading its resolution. The aim of this chapter is to quantify this degradation given a phase noise specification for a typical on-chip VCO so that given the desired resolution of a fully-integrated delta-sigma data converter with an on-chip clock, the maximum-allowable phase noise for a given clock frequency might be determined. The majority of past work [Har90], [Dia92a, §4], [Ris94, §C.4.3], [vdZ96, §II.C] treats jitter as white; our treatment of nonwhite jitter in §5.3 is believed to be the first comprehensive one. This chapter and the next have been accepted for publication as a journal paper [Che99a].

5.1 Preliminaries

We introduce the architecture of the modulators used in this study and describe the method used to simulate their behavior.

5.1.1 Modulator Architecture

A block diagram of the architecture is shown in Figure 5.2. It is similar to Figure 4.17, only more

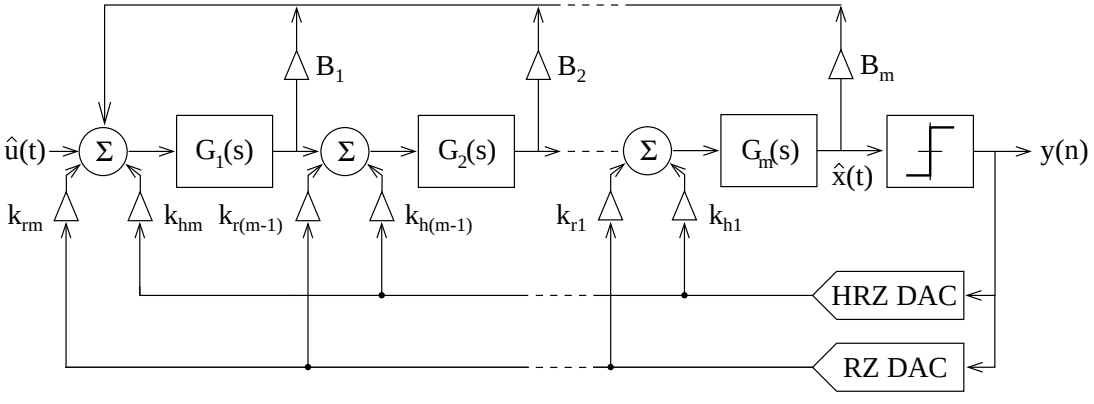


Figure 5.2: Block diagram for general CT ΔΣM architecture.

generalized. Each of the gain blocks $G_i(s)$ will typically be the same except possibly for the gains; thus, for a low pass modulator, the blocks can be represented with continuous-time integrators

$$G_i(s) = \frac{A_i}{sT_s} \tag{5.1}$$

and for a band pass modulator, they will be resonators

$$G_i(s) = \frac{A_i s T_s}{s^2 T_s^2 + \omega_i^2}. \tag{5.2}$$

Without loss of generality, we will sometimes assume the sampling frequency is $f_s = 1$Hz, which simplifies the notation in (5.1) and (5.2) by making $T_s = 1$. Modulator behavior is unchanged so long as the proper scaling is applied to all circuit parameters.

The quantizer drives two separate DACs of the RZ and HRZ varieties whose levels at feedback points are set by coefficients $\{k_{rm}, k_{r(m-1)}, \ldots, k_{r1}\}$ and $\{k_{hm}, k_{h(m-1)}, \ldots, k_{h1}\}$, respectively. A modulator with an NRZ DAC can be effected by setting $k_{ri} = k_{hi}$, while one with an RZ DAC only would have all $k_{hi} = 0$. We have both types of DAC in Figure 5.2 separately tunable for when we wish to implement multi-feedback BP modulators.

5.1.2 Simulation Method

The time-domain state equations are coded in a C program and integrated numerically using a variable time step fourth-order Runge-Kutta (RK4) method [Pre92]. For example, for an LP modulator with gain blocks given by (5.1), the state equations are

$$\frac{1}{A_i}\frac{dx_i}{dt} = \begin{cases} B_1 x_1 + \cdots + B_m x_m + k_m y + u, & i = 1 \\ x_{i-1} + k_{m+1-i} y, & i = 2, \ldots, m \end{cases} \tag{5.3}$$

where $k_i = k_{ri}$ during the first half of a period and $k_i = k_{hi}$ during the second half. At every clocking instant, the quantizer output is evaluated; the power spectrum of N output bits is calculated by the program using the periodogram of the FFT, and periodograms from any number of runs with random initial states may be averaged to yield a fairly smooth spectrum from which the SNR may be found.

Moreover, certain nonidealities of interest in this chapter are implemented. In particular:

- the sampling instant can be affected by jitter;
- the DAC pulses can be delayed to model the finite speed of the transistors in the feedback path, and they can have nonzero rise time to model the finite gain of the transistors;
- the quantizer can exhibit hysteresis and/or metastability.

This latter item will be important in Chapter 6; in this chapter a quantizer with no metastability is assumed. Other nonidealities such as integrators with finite dc gains (or resonators with finite Qs) and finite gain block output swing could also be modeled without much difficulty.

The principal advantage of using C is that it runs very fast compared to, for example, block-diagram level simulation in a circuit simulator like SPICE, though it is slower to code. Presently we show that we can get acceptable agreement between the program and a transistor-level simulation in SPICE with several orders of magnitude increase in simulation speed. The effort spent on the coding will appear justified.

5.2 Effect of Clock Jitter on an Ideal CT $\Delta\Sigma$M

Let us start with a review of the theory for white jitter. Suppose the sampling times are given by

$$t_n = nT_s + \beta_n,\ n = 0, 1, \ldots, N-1 \tag{5.4}$$

and for the moment, let the β_n be i.i.d. random variables with variance σ_β^2. As noted in the introduction, the effect of sample time jitter is to modulate the out-of-band noise in the output spectrum into the signal band. This fills in the ideally infinitely-deep quantization noise notch with white noise, which lowers the SNR and hence the converter resolution. Let us quantify this statement for a couple of different cases.

5.2.1 LP Modulators with NRZ Feedback

Figure 5.2 can simulate low pass modulators with NRZ feedback by making the gain blocks integrators as in (5.1) and setting $k_{ri} = k_{hi} = k_i$. If all the integrators have gain $A_i = 1$, the loop filter

implemented by the circuit for $m \geq 2$ is (4.27):

$$\hat{H}(s) = \frac{\sum_{i=1}^{m} (\frac{1}{s})^i [k_i - \sum_{j=1}^{i-1} k_{i-j} B_j]}{1 - \sum_{i=1}^{m} B_i (\frac{1}{s})^i}. \tag{5.5}$$

We can choose a loop filter $H(z)$ in the DT domain using any method we please and transform it to the equivalent $\hat{H}(s)$ as we did in Chapter 4. It is then a trivial matter to pick k_i and B_i in (5.5).

Example 5.1: We have already noted that the standard double-integration modulator has a DT loop transfer function $H(z)$ and equivalent CT $\hat{H}(s)$ for NRZ DAC pulses given by

$$H(z) = \frac{-2z+1}{(z-1)^2} \leftrightarrow \hat{H}(s) = \frac{-1.5s-1}{s^2} \tag{5.6}$$

where $T_s = 1$ for simplicity. For integrators with gains $\{A_1, A_2\} = \{1, 1\}$,

$$\{k_2, k_1\} = \{-1, -1.5\},\ \{B_1, B_2\} = \{0, 0\} \tag{5.7}$$

are found from (5.5). □

Example 5.2: A third-order modulator designed using NTF prototyping where NTF(z) has Butterworth poles, an out-of-band gain of 1.5, and zeros spread to minimize quantization noise in the signal band assuming OSR $= 32$ can be found to have $H(z)$ and $\hat{H}(s)$ for NRZ DAC pulses given by

$$\begin{aligned} H(z) &= \frac{-0.7874z^2 + 1.3085z - 0.5569}{z^3 - 2.9942z^2 + 2.9942z - 1} \\ \leftrightarrow \quad \hat{H}(s) &= \frac{-0.6702s^2 - 0.2407s - 0.0458}{s^3 + 0.0058s}. \end{aligned} \tag{5.8}$$

Choosing all integrator gains to be 1 yields

$$\begin{aligned} \{k_1, k_2, k_3\} &= \{-0.0831, -0.5021, -1.4659\}, \\ \{B_1, B_2, B_3\} &= \{0, -5.7830 \times 10^{-3}, 0\}. \end{aligned} \tag{5.9}$$

If we were interested in actually building this, we might find the range of these values (from 0.5×10^{-3} up to 1.5) too wide to be practical. Choosing the integrator gains as

$\{A_1, A_2, A_3\} = \{0.2, 0.2, 1\}$ instead gives a smaller spread in the resulting k_i and B_i. Rewriting (5.5) for $A_i \neq 1$ and solving gives

$$\{k_1, k_2, k_3\} = \{-1.0479, -1.2033, -0.6702\},$$
$$\{B_1, B_2, B_3\} = \{0, -0.1446, 0\}. \tag{5.10}$$

Of course, for the purposes of simulation, either will work. □

Performing the same calculation for fourth-order Butterworth pole and fifth-order Chebyshev pole NTFs both with out-of-band gain 1.5 and optimally-spread zeros, and simulating those systems with different values of jitter standard deviation σ_β, results in the output spectra shown in Figure 5.3. These are 256 averaged 8192-point Hann-windowed periodograms whose x axes span a frequency range from 0 to $f_s/32$. The input tone was -20dB relative to full scale in bin 19 ($2.32 \times 10^{-3} f_s$). The β_n were normally-distributed. We indeed see the deep notch in the quantization noise gradually filled in with white noise with a power proportional to $10 \log_{10}(\sigma_\beta / T_s)^2$.

This behavior can be explained by considering Figure 5.4. The output bit stream with jitter shown in the top diagram is equivalent to the sum of an unjittered bit stream (the middle diagram) and a stream of pulses, which we call the *error sequence*, resulting from the jitter (the bottom diagram). By the linearity of the FFT, the output spectrum of the top signal must be the sum of the spectra of the bottom two signals. The error sequence can be written as [Ris94]

$$e_{NRZ}(n) = [y(n) - y(n-1)] \frac{\beta_n}{T_s} \tag{5.11}$$

where $y(n)$ is the nth output bit. For wideband uncorrelated jitter, this error will be almost white, in which case we may write

$$\sigma_e^2 \approx \sigma_{\delta y}^2 \times \frac{\sigma_\beta^2}{T_s^2}, \tag{5.12}$$

in other words, the variance of the error sequence is the product of the variance of $\delta y \equiv y(n) - y(n-1)$ and the jitter variance relative to the clock period. For N output bits, we expect the noise per periodogram bin to be

$$10 \log_{10} \left(\frac{2\sigma_{\delta y}^2 \cdot 2\sigma_\beta^2}{N T_s^2} \right) - 7.27\text{dB} \tag{5.13}$$

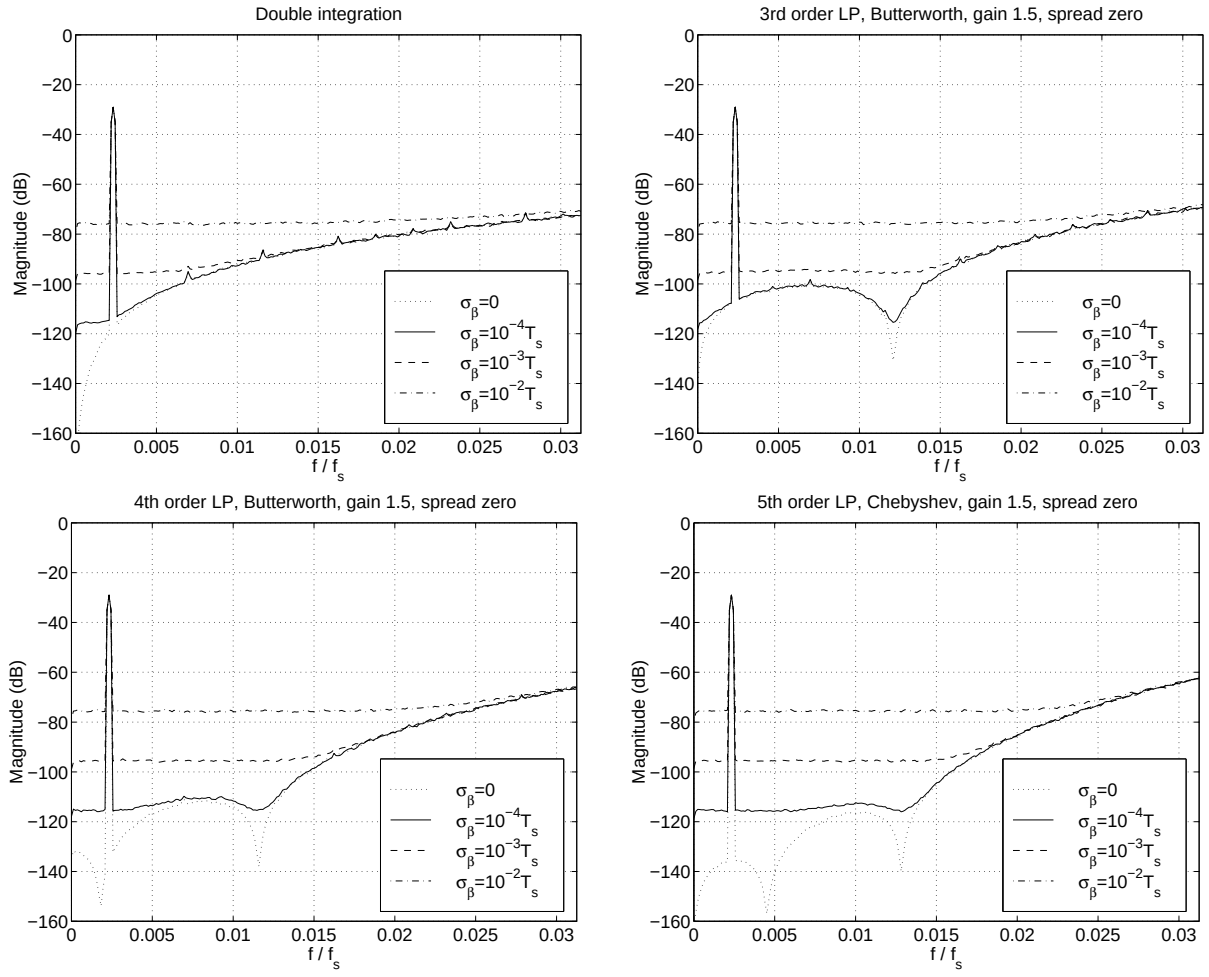


Figure 5.3: Output spectra for NRZ LP modulators with clock jitter.

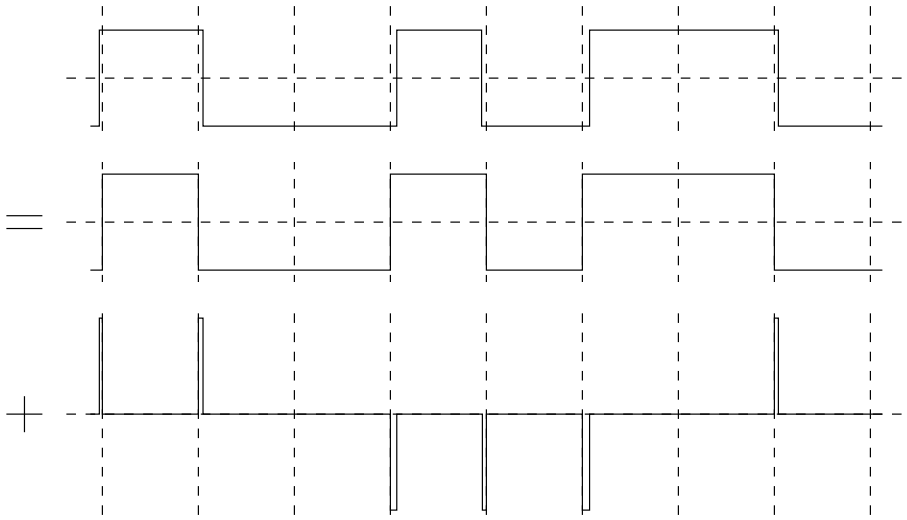


Figure 5.4: Equivalent representations of a jittered bit stream.

Table 5.1: Simulated and calculated LP NRZ modulator performance for $\sigma_\beta = 10^{-2}T_s$ in Figure 5.3.

Modulator	$\sigma_{\delta y}$	Baseband noise per bin		SNR for OSR $= 32$	
	Simulated	Simulated	Calculated, eq. (5.13)	Simulated	Calculated, eq. (5.14)
Double integration	1.674	-75.8dB	-75.9dB	27.5dB	27.6dB
3rd order Butterworth	1.750	-75.6dB	-75.5dB	27.3dB	27.2dB
4th order Butterworth	1.739	-75.5dB	-75.6dB	27.4dB	27.2dB
5th order Chebyshev	1.731	-75.5dB	-75.6dB	27.5dB	27.3dB

where the factors of 2 in the numerator arise because we are taking the one-sided power spectrum and where 7.27 is the sum of $10\log_{10} 2 = 3.01$dB (the power spectrum is rms power) and $10\log_{10} 0.375 = 4.26$dB (0.375 is the gain of a Hann window). Moreover, if the SNR in baseband is completely limited by white jitter noise rather than noise-shaped quantization noise, we can write [Ris94]

$$\text{SNR}_{NRZ} = 10\log_{10} \frac{\text{OSR} \cdot V_{in}^2/2}{\sigma_{\delta y}^2 (\frac{\sigma_\beta}{T_s})^2} \text{dB}. \tag{5.14}$$

Table 5.1 shows the agreement between calculated and simulated values of (5.13) and (5.14) for the four modulators in Figure 5.3. The theory for low pass NRZ modulators is confirmed by our

simulation.

5.2.2 Modulators with RZ and/or HRZ Feedback

It is possible to build LP modulators that use feedback other than NRZ, for example, RZ feedback. Indeed, as we saw last chapter, RZ DAC waveforms are beneficial for reducing intersymbol interference and excess delay problems, so we might prefer them over NRZ DACs. As well, multi-feedback BP modulators use both RZ and HRZ DACs in the same circuit. How does jitter affect the spectrum of a modulator using RZ (and possibly HRZ) DACs? This problem has not previously been considered; it is believed that the material here is new. Let us first choose circuit coefficients for typical modulators.

Example 5.3: The CT loop filter $\hat{H}(s)$ for a double integration LP modulator with RZ DAC pulses can be found from $H(z)$ to be

$$H(z) = \frac{-2z+1}{(z-1)^2} \leftrightarrow \hat{H}(s) = \frac{-2.5s-2}{s^2}. \tag{5.15}$$

Picking the integrator gains to be 1 and the B_is to be zero leaves

$$\{k_2, k_1\} = \{-2, -2.5\}, \tag{5.16}$$

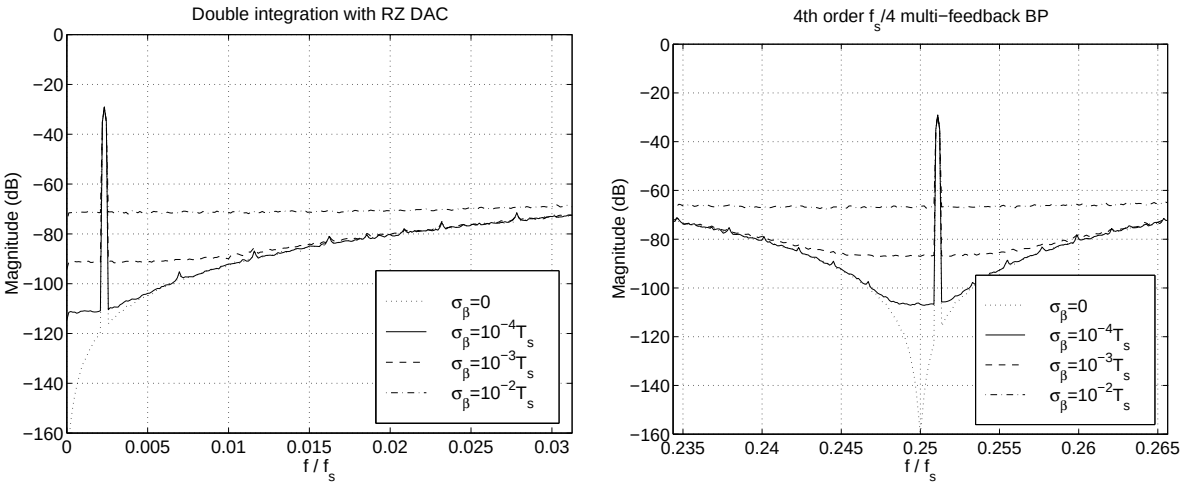
which we found in (4.31) for $\tau_d = 0$. □

Example 5.4: We considered the design of a fourth-order $f_s/4$ BP modulator in Example 4.6 already. The feedback coefficients for resonators in (4.26) were

$$\{k_{r2}, k_{r1}, k_{h2}, k_{h1}\} = \{-1.0868, -2.1339, 0.4502, 1.4874\}, \tag{5.17}$$

and these are correct for resonators with gains $\{A_1, A_2\} = \{\pi/2, \pi/2\}$ and $\omega_0 = \pi/2$ in (5.2). □

Output spectra for simulations of each system are shown in Figure 5.5. Once again, these are 256 averaged 8192-point Hann-windowed periodograms. For a jitter standard deviation $\sigma_\beta =$



(a) (b)

Figure 5.5: Output spectra for (a) LP RZ and (b) BP RZ/HRZ modulators.

$10^{-2}T_s$, we found a baseband noise of -75.8dB per bin in the double integration NRZ modulator, while for the double integration RZ modulator in Figure 5.5(a) the value is -71.3dB, and for the BP modulator in Figure 5.5(b) the value is -66.7dB. Where do the new values come from?

Figure 5.6 shows the same bit sequence $\{+1, +1, -1, +1, -1\}$ as output by the same modulator

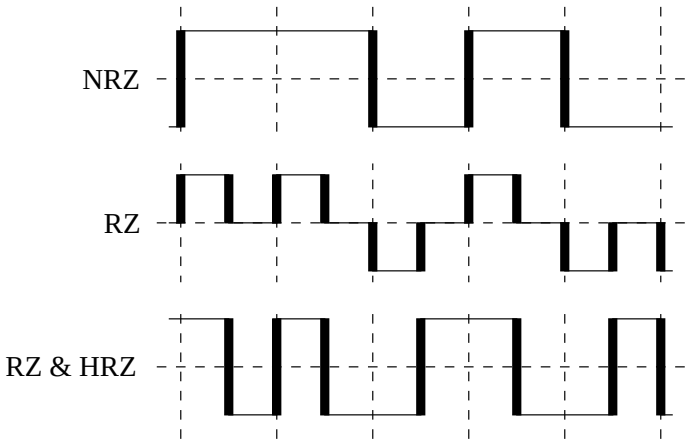


Figure 5.6: Error sequence energy in different types of modulator.

with three different DACs: NRZ, RZ, and a combination of both RZ and HRZ DACs. The solid rectangles show edges which are affected by jitter. We may distinguish the three cases as follows.

- In an NRZ modulator, jitter only matters when the output changes sign—the error sequence $e_{NRZ}(n)$ is nonzero only at those times, c.f. (5.11). The energy in the error sequence is proportional to $\delta y^2 = [y(n) - y(n-1)]^2 = 4$ for a modulator with ± 1 outputs. For the double integration NRZ modulator in Table 5.1 we found $\sigma_{\delta y} = 1.673$, and the formula for variance is
$$\sigma^2_{\delta y} = \frac{\sum \delta y^2 - \frac{(\sum \delta y)^2}{N}}{N-1} \approx \frac{4N_{\delta y}}{N} \tag{5.18}$$
for large N where $N_{\delta y}$ is the actual number of output bit transitions. We have $\sigma^2_{\delta y} = 2.80$ and can estimate $N_{\delta y}/N = \sigma^2_{\delta y}/4 = 0.70$ for that modulator.

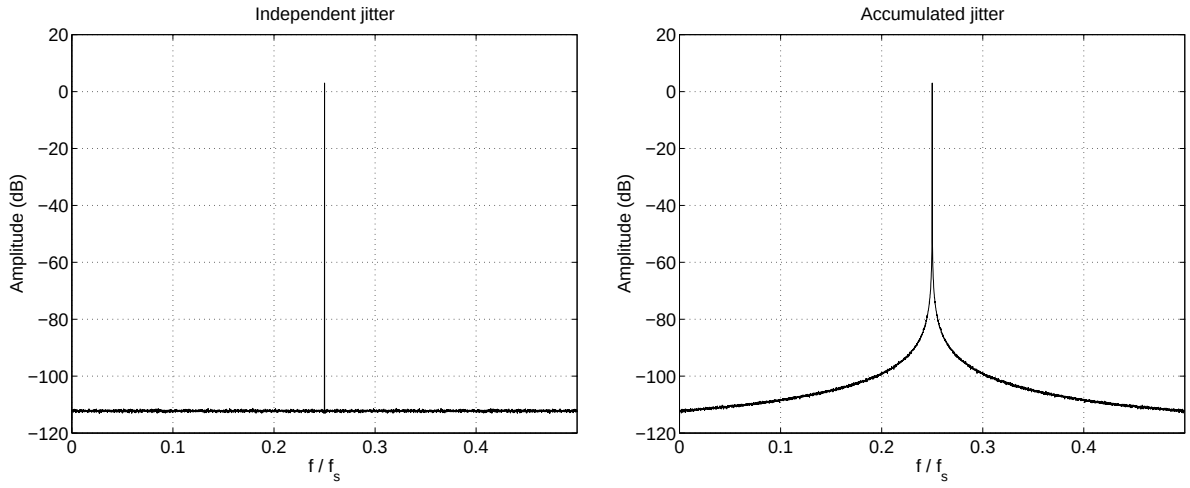
- In an RZ modulator, both the rising and the falling edge of the pulse occur *every* clock cycle, so jitter affects a total of $2N$ edges. The energy per edge is $[\pm 1 - 0]^2 = 1$, one quarter as much as in the NRZ case. But now, energy is being transferred over only half a clock cycle; σ_β is therefore twice as large relative to the energy transfer period in an RZ modulator.

- In a modulator employing RZ and HRZ pulses of opposite sign, as is the case in a multi-feedback BP modulator, there are now N edges at half clock cycles when going from the RZ to the HRZ pulse, and edges at half cycles where the output bits $y(n-1)$ and $y(n)$ are the same. These edges have energy 4 as in the NRZ case, and σ_β is twice as large relative to the energy transfer period as in the RZ case. In simulation, we find $\sigma_{\delta y} = 1.405$ for the BP modulator, so that $N_{\delta y}/N = 0.494$ from (5.18). The total number of edges is then $N + N(1 - N_{\delta y}/N) = 1.506$.

Taking all this into account, we may estimate an effective value of $\sigma^2_{\delta y}$ in (5.12):

$$\sigma^2_{\delta y} = \begin{cases} \frac{0.70N \times 4}{N} & = & 2.80, & \text{NRZ} \\ \frac{2N \times 1}{N} \times 2^2 & = & 8.00, & \text{RZ} \\ \frac{1.506N \times 4}{N} \times 2^2 & = & 24.10, & \text{RZ \& HRZ.} \end{cases} \tag{5.19}$$

Therefore, we expect the RZ LP modulator to be $10\log_{10}(8.00/2.80) = 4.6$dB worse than the NRZ LP modulator and the BP modulator to be $10\log_{10}(24.10/2.80) = 9.3$dB worse than the NRZ LP modulator. This is very close to what we observed (4.5dB and 9.2dB) in Figure 5.5. As a rule of thumb, clock jitter lowers SNR by 6dB (1 bit) in RZ/HRZ vs. NRZ modulators.



(a) (b)

Figure 5.7: Unwindowed spectra of sine wave carriers sampled with jitter: (a) independent jitter, (b) accumulated jitter.

5.3 Clocking with a VCO

Although it is interesting didactically, the analysis in §5.2 is not terribly relevant in practice. The problem is, if we are trying to use a high-speed CT $\Delta\Sigma$M in a practical circuit it will likely be clocked on-chip with an integrated VCO. Sampling instants as given in (5.4) are not what a real VCO provides—the jitter instants β_n from a VCO are not well-modeled as i.i.d. random variables. Figure 5.7(a) shows 256 averaged 8192-point unwindowed periodograms of a sine wave carrier sampled by an ideal S/H four times per period (i.e., $f_c = f_s/4$) with a jittered clock given by (5.4) and $\sigma_\beta = 10^{-4}T_s$. That kind of jitter, which we will denote *independent jitter*, adds white noise skirts to the carrier. A VCO produces skirts that are nonwhite.

5.3.1 Modeling VCO Phase Noise

We can modify (5.4) to produce nonwhite skirts fairly easily using a result due to Berkovitz and Rusnak [Ber92]. Suppose the sampling instants are instead given by

$$t_n = nT_s + \sum_{i=0}^{n} \beta_i,\ n = 0, 1, \ldots, N-1 \tag{5.20}$$

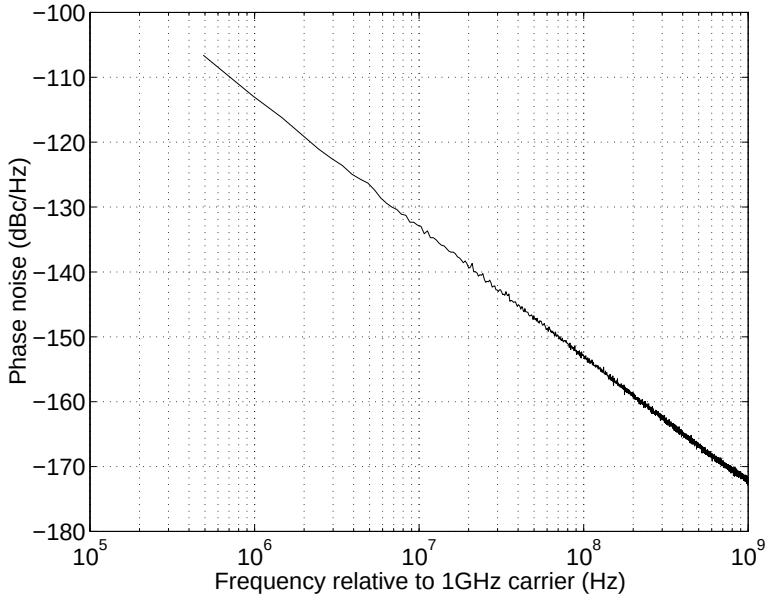


Figure 5.8: Phase noise plot for accumulated jitter sampling of sine wave.

where β_i are still i.i.d. We denote this *accumulated jitter* because it contains a running sum, and a sine wave sampled four times per period with a jittered clock given by (5.20) has the spectrum shown in Figure 5.7(b). Plotting the magnitude of the skirts relative to the carrier with a logarithmic frequency scale, as is customarily done in a VCO phase noise plot, yields the graph in Figure 5.8, where we have assumed the sine wave has a frequency of $f_c = 1$GHz. The sideband power has a $1/f^2$ dependence—exactly as is the case in an integrated VCO [Haj98]. A VCO also has a $1/f^3$ region close to the carrier, and a white noise floor far from the carrier, but (5.20) at least gives a reasonable approximation of a VCO phase noise over frequencies an intermediate distance from the carrier. Phase noise in a VCO is usually specified as n_c dBc/Hz at an offset f_n from the carrier f_c. Happily, this f_n is usually in the $1/f^2$ region of the phase noise.

A typical achievable value of n_c is [Lee66, Dau98]

$$n_c = -100 + 20 \log_{10} f_c \text{ dBc/Hz at 100kHz offset} \tag{5.21}$$

for f_c in GHz. How can we relate this to σ_β? We are interested in the case of $f_c = f_s$, since for clocking a $\Delta\Sigma$M, all that matters is the jitter of the zero crossings of the carrier, yet we are

constrained mathematically in a periodogram to $f_c < f_s/2$. However, it is found that altering the ratio f_c/f_s moves the phase noise in Figure 5.8 proportionally to $10\log_{10} f_c/f_s$, so we can use this to extrapolate to $f_c = f_s$. After some experimentation with normally-distributed β_n, it is found that using

$$\sigma_\beta^2 \approx \frac{f_n^2 \times 10^{n_c/10}}{2f_c} \tag{5.22}$$

gives a phase noise of n_c relative to the carrier at f_n offset from f_c.

Therefore, we can simulate the effect of clocking a $\Delta\Sigma$M with a VCO meeting a certain phase noise spec by using sampling instants with accumulated jitter (5.20) and a variance given by (5.22).

5.3.2 Effect of Accumulated Jitter on Performance

Example output spectra for four different types of modulator are depicted in Figure 5.9. These are the third-order Butterworth NRZ, fifth-order Chebyshev NRZ, double integration RZ, and fourth-order $f_s/4$ multi-feedback BP $\Delta\Sigma$Ms from Figures 5.3 and 5.5. All simulations used $\sigma_\beta = 10^{-2}T_s$, and for contrast both independent *and* accumulated jitter spectra are plotted compared to unjittered spectra.

There are two traits in the accumulated jitter spectra worth noting. First, accumulated jitter whitens the in-band spectrum in much the same way as independent jitter—this is not unexpected because *any* clock spectral impurities will randomly modulate out-of-band noise into the signal band. The white noise floor seems to be between about 1–5dB lower for accumulated jitter compared to independent with the same σ_β; for a given modulator, simulations shows this number is about constant for any values of σ_β, input frequency, and input amplitude. Second, the dash-dot lines on each graph show the spectrum of a sine wave with the same frequency as the input tone that has been sampled by a S/H circuit clocked with the same clock as the quantizer. The skirts on the tone appear directly in the output spectrum so long as they are higher than the white noise floor. This, too, is logical.

Note the significance of the observation in §5.3.1 that the height of the skirts is proportional to $10\log_{10} f_c/f_s$: as the input tone moves to higher frequencies, the skirts become higher relative to the tone. Thus, an LP modulator with a large tone close to the upper in-band frequency edge will

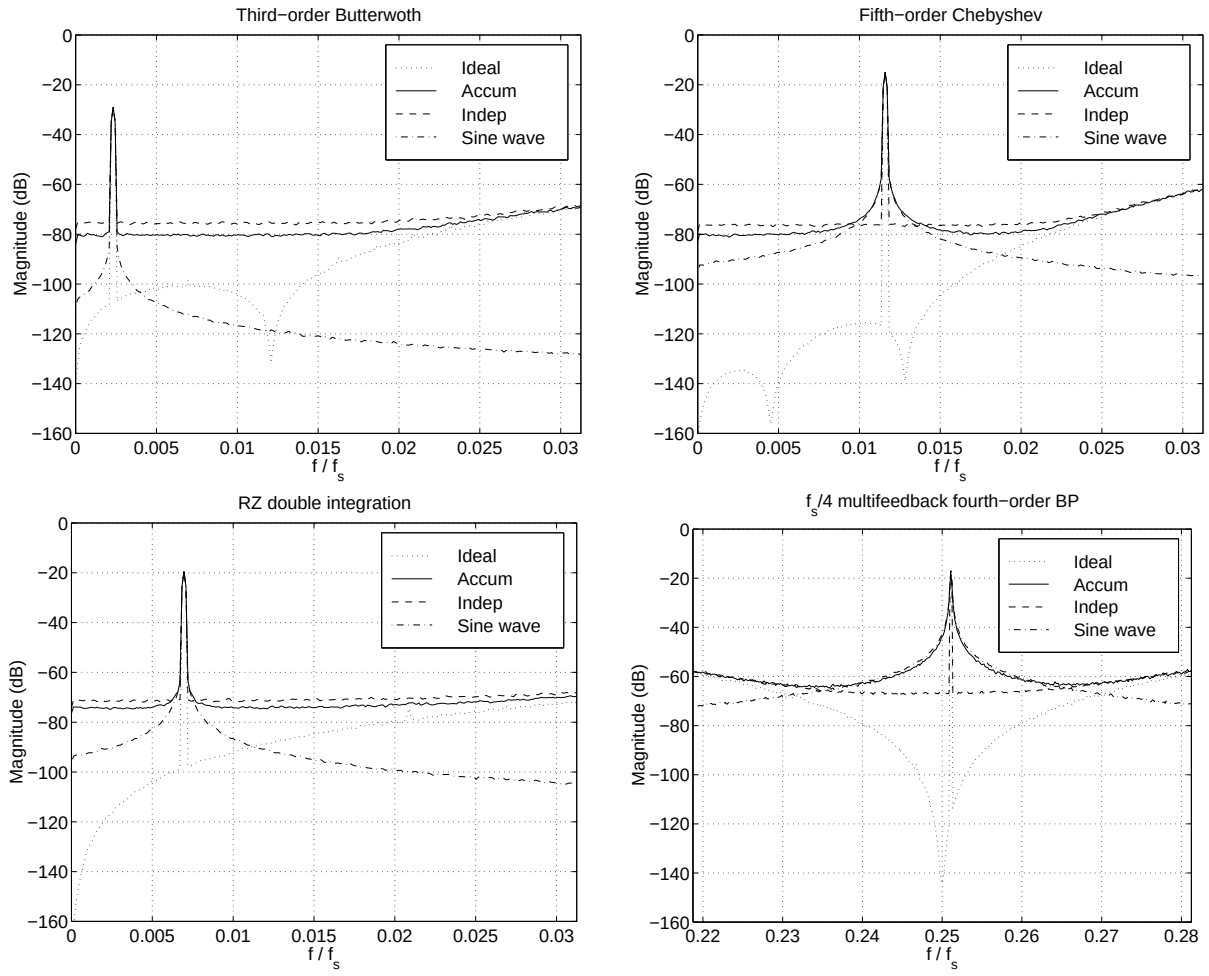


Figure 5.9: Comparison of $\Delta\Sigma$M spectra for independent and accumulated jitter, including spectrum of single tone at output of jittered S/H.

Table 5.2: Performance effects of real VCO clocking on practical modulators.

Modulator	σ_β/T_s	OSR	Ideal clock		VCO clock	
			DR	Peak SNR	DR	Peak SNR
1GHz 3rd order Butterworth	2.236×10^{-5}	32	73.2dB	73.3dB	69.6dB	69.6dB
		64	93.5dB	93.8dB	90.5dB	89.2dB
2GHz 5th order Chebyshev	3.155×10^{-5}	32	82.6dB	82.8dB	79.8dB	79.1dB
		64	114.5dB	100.7dB	101.6dB	92.1dB
3.2GHz double integration [Jen95]	3.953×10^{-5}	32	62.7dB	56.3dB	62.6dB	56.3dB
		64	78.8dB	71.3dB	79.0dB	71.4dB
4GHz 4th order BP [Gao98a]	4.451×10^{-5}	32	63.2dB	56.4dB	63.2dB	52.7dB
		64	77.5dB	70.2dB	77.3dB	55.3dB

have higher skirts and hence lower peak SNR than if the tone were close to dc. Moreover, the $f_s/4$ BP modulator's performance is affected much more severely than any of the LP modulators, as is apparent in the graphs. Shoaei observed skirts in the output spectrum of a BP modulator [Sho96, §8.4], so he too was apparently using accumulated jitter, though his study is not nearly as detailed as ours.

The σ_β used in Figure 5.9 is unrealistically high for a practical VCO; it was used simply as an illustration. In Table 5.2, we have shown how more realistic σ_β values would affect the performance of real high-speed CT $\Delta\Sigma$Ms. We have characterized the dynamic range (DR) and peak SNR of four modulators:

- a 1GHz-clocking third-order LP design with NRZ DAC pulses and Butterworth pole placement in the NTF with gain 1.5 and spread zeros;
- a 2GHz fifth-order LP design with NRZ DAC pulses and Chebyshev pole placement in the NTF with gain 1.5 and spread zeros;
- the 3.2GHz double integration modulator published in [Jen95], which has NRZ DAC pulses; and

- the 4GHz fourth-order BP multi-feedback modulator from [Gao98a] with a noise notch at $f_s/4 = 1$GHz.

For each modulator, we used (5.21) to pick a reasonable value of n_c given f_s, and (5.22) to find σ_β. Then, DR and peak SNR were measured from simulation of each modulator at two different OSRs, 32 and 64. The modulators were simulated both with ideal (unjittered) and VCO (jittered) clocks, and the input tone for the LP modulators is close to the upper band edge so that jitter skirts will be most pronounced[1].

Looking at the table, we may make the following comments. The ideal modulators have DR and SNR limited by quantization noise only; for the modulators clocked with a VCO, the question is, does jitter noise impose additional performance limitations? For the double integration modulator, the answer is no: performance is still quantization-noise limited for the realistic value of σ_β used. For high-order modulators and/or high OSRs, the likelihood of being jitter-noise limited increases, as is particularly clear in the fifth-order modulator with OSR $= 64$: more than two full bits of DR are lost at this clock frequency. As well, modulators with center frequencies away from dc suffer more greatly from jitter performance degradation, as we expect from Figure 5.9—note that maximum SNR for the BP modulator is 4dB worse than ideal at OSR $= 32$ and 15dB worse at OSR $= 64$.

An interesting thing happens when we combine the equations in this chapter to derive the maximum-achievable DR for a VCO-clocked modulator with a phase-noise spec given by (5.21). We assume that the in-band noise is completely white; the full calculation appears in §A.1 and the result is equation (A.10),

$$\text{Maximum DR (bits)} \approx 19 - 0.5 \log_2 f_N, \tag{5.23}$$

[1]A quick check of the absolute σ_β values in the table makes them appear suspicious: for example, the 4GHz modulator has $T_s = 250$ps and $\sigma_\beta/T_s = 4.451 \times 10^{-5}$, which means $\sigma_\beta = 11.1$fs. A typical Gbit-rate data generator specs edge jitter at a value of a few ps, two to three orders of magnitude higher than this σ_β. However, it must be remembered that we are using accumulated jitter, (5.20), not white. This means the clock phase over hundreds of cycles wanders significantly relative to a coherent reference; it is trivial to show that after N clock cycles, the phase is a Gaussian random variable with variance $N\sigma_\beta^2$. The σ_β/T_s values in the table are correct for a phase noise given by (5.21).

where f_N is the Nyquist rate expressed in MHz. This depends *only* on desired conversion bandwidth—it is independent of clock frequency so long as the VCO conforms to (5.21)! As an example, a 32MHz converter has $f_N = 64$MHz, and (5.23) says VCO jitter will limit the performance to no more than 16 bits in this band. But this is far more than the resolution achieved by the fast modulators in Table 3.2. Clearly, VCO phase noise is unlikely to be the limiting factor in a high-speed modulator.

To conclude, the quality of integrated VCOs for cellular radio applications is good enough that the DR of only very high-resolution wideband LP $\Delta\Sigma$Ms would likely be affected. Fast BP designs might be more problematic in terms of the peak SNR lost due to jitter skirts appearing on the output tone. For [Gao98a] which does band pass conversion at 1GHz, we might think we can address this by downconverting to a frequency of a couple hundred MHz and doing the ADC there instead where the jitter skirts in a $\Delta\Sigma$M would be less severe; however, we must remember that the downconversion operation itself must be done with a jittered clock, and this introduces skirts on the tone in the mixing process.

5.4 Summary

Clock jitter adds a random phase modulation to the output bit stream which degrades performance by whitening the quantization noise notch. Past treatments of jitter in CT $\Delta\Sigma$Ms have generally treated jitter as wideband uncorrelated white noise, but this is not realistic for the case of a $\Delta\Sigma$M clocked with an on-chip VCO which has nonwhite phase noise skirts. This can lead not only to in-band noise whitening, but also to skirts on the input tone in the output spectrum. We distill the calculations into a single equation, (5.23), which allows us to estimate the maximum DR that would result if $\Delta\Sigma$M performance was limited entirely by VCO phase noise. From it, we conclude that for conversion bandwidths into the tens of MHz it is unlikely that typical VCO phase noise would be severe enough to cause a noticeable DR degradation in a typical integrated low-order LP CT $\Delta\Sigma$M, though high-bandwidth high-order LP designs might present more of a problem and BP designs suffer in terms of SNR_{max} due to the higher skirts at higher input signal frequencies.

Chapter 6

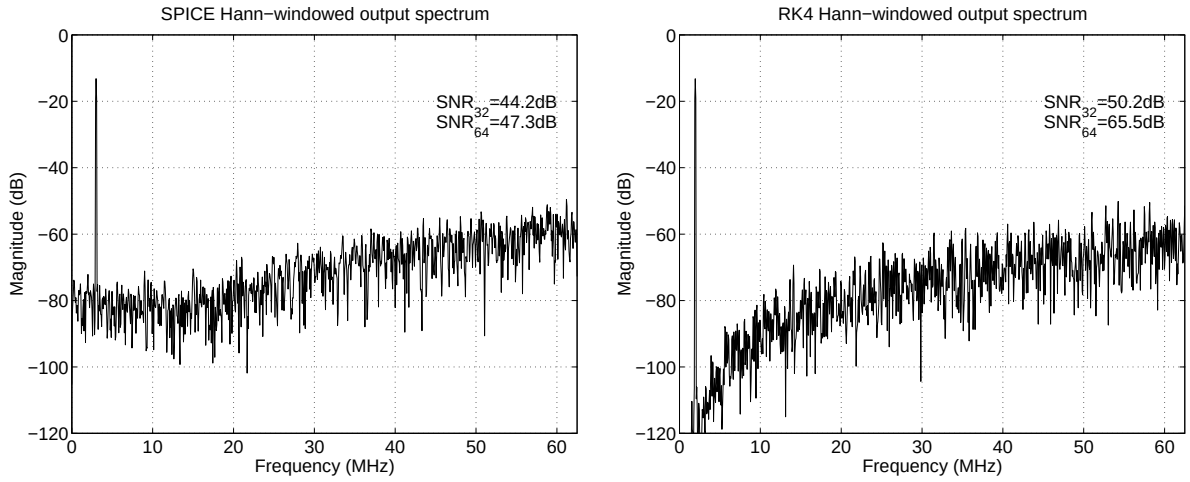
Quantizer Metastability

Even with a perfectly uniform sampling clock, it is nonetheless possible for there to exist a variation in the feedback charge. This happens because a real quantizer contains a regenerative circuit with a finite regeneration gain. Therefore, quantizer inputs with a magnitude near zero will take longer to resolve than inputs with a large magnitude—this is the classic problem of metastability in digital latches. In a $\Delta\Sigma$M, the input to the quantizer is decorrelated from the modulator input to the degree that it appears random; hence, the times when the quantizer input is near zero also appear random. This means that at certain unpredictable sampling instants, slightly more charge is transferred for the previous clock period and slightly less for the next period. As with clock jitter, the effect is to modulate out-of-band noise into the signal band and degrade converter resolution.

This was first identified by the author in [Che97]. The aim of this chapter is to greatly expand on those results, which were only for a double integration modulator: we wish to generalize them to different orders of modulator and study methods to overcome the effects of quantizer metastability.

6.1 Background

Before going too deep, we first chronicle how the importance of metastability was discovered. This is to introduce a new method of simulating CT $\Delta\Sigma$Ms, another idea first published by the author [Che98a].



(a) (b)

Figure 6.1: Typical output spectra for (a) SPICE prototype, (b) C program using the same parameters.

6.1.1 Initial Observations

The author was studying an industrial high-speed double integration CT $\Delta\Sigma$M [Sch96b], an early prototype of which was very similar in design to the modulator in Figure 4.1. The prototype clocked at $f_s = 1$GHz; a 16000-point Hann-windowed spectrum from a transistor-level SPICE simulation is shown in Figure 6.1(a). The input tone was -4dB, and the SNR achieved for an OSR of 32 was 44.2dB. From (3.3), an ideal double integration $\Delta\Sigma$M achieves $\text{SNR}_{\text{max}} = 56$dB, and this happens at an input level of around -4dB. Therefore, the prototype appeared nonideal by about two bits. Moreover, at an OSR of 64, the SNR only improved 3dB to 47.3dB—this shows that the baseband noise is white rather than shaped at 15dB per octave of oversampling, as we would expect for a second-order $\Delta\Sigma$M. A C program was written to model the SPICE circuit, including such things as finite op amp gain and input resistance, nonzero excess delay, and nonzero DAC pulse rise time. A typical spectrum for the same input conditions appears in Figure 6.1(b). The spectrum looks similar except towards dc, where it continues to descend at 15dB/oct. Both modulators had an unjittered clock, and past experience with SPICE taught us that it didn't seem reasonable to attribute the SPICE results to, e.g., roundoff error. Why does the spectrum of the SPICE simulation become white?

6.1.2 z-Domain Extraction

The new simulation method exploits the bidirectionality of the DT/CT equivalence explained in §4.1. For the general DT modulator in Figure 2.17 on page 28, we had a time-domain expression for the quantizer input $x(n)$ in (2.12), reproduced here:

$$x(n) = \sum_{k=1}^{m} a_k x(n-k) + \sum_{k=1}^{m} b_k u(n-k) + \sum_{k=1}^{m} c_k y(n-k). \tag{6.1}$$

Recall that we are using the impulse-invariant transformation for DT/CT equivalence, which enforces the condition (4.1):

$$x(n) = \hat{x}(t)|_{t=nT_s}. \tag{6.2}$$

Thus, (6.1) must hold for a CT modulator at sampling instants:

$$\hat{x}(nT_s) = \sum_{k=1}^{m} \left[a_k \hat{x}((n-k)T_s) + b_k \hat{u}((n-k)T_s) + c_k \hat{y}((n-k)T_s) \right]. \tag{6.3}$$

This suggests the following: if we simulate a CT $\Delta\Sigma$M and extract $\{\hat{x}(nT_s), \hat{u}(nT_s), \hat{y}(nT_s)\}$, then we ought to be able to find $\{a_k, b_k, c_k\}$ such that (2.15) is satisfied. This will give us the DT equivalent for the CT modulator.

Example 6.1: During the 16000-clock cycle SPICE simulation of the prototype, the values of $\hat{x}$, $\hat{u}$, and $\hat{y}$ at sampling instants were printed out. Using a least-squares fitting approach in Matlab, the following best-fit DT difference equation was found for the group of 50 consecutive samples of $\hat{x}(nT_s) = x(n)$ beginning at sample 700:

$$\begin{aligned} x(n) &= 1.9835x(n-1) - 0.9886x(n-2) + 0.2319u(n-1) \\ &\quad - 0.2083y(n-1) + 0.0511y(n-2) + 0.0462y(n-3), \end{aligned} \tag{6.4}$$

$$\|\varepsilon\|_\infty = 19.43\text{mV}, \quad \|\varepsilon\|_2 = 4.914\text{mV}. \tag{6.5}$$

The fit is not perfect, as evidenced by the nonzero $\|\varepsilon\|_\infty$ and $\|\varepsilon\|_2$ values in (6.5), which are (respectively) the maximum and rms errors between the best-fit $x(n)$ in (6.4) and the $\hat{x}(nT_s)$ from SPICE. $x(n)$ spans a range of about ± 500mV, so the rms error $\|\varepsilon\|_2$ is about 1% of the full-scale range of $x(n)$.

Taking the $\mathcal{Z}$-transform of (6.4) and using (2.11), we find the loop transfer function to be

$$H(z) = 0.1042\frac{-2.0000z^{-1} + 0.4906z^{-2} + 0.4436z^{-3}}{1 - 1.9835z^{-1} + 0.9886z^{-2}}. \tag{6.6}$$

Thus, the z-domain extraction method allows us to see the $H(z)$ actually implemented (as opposed to the $H(z)$ we thought we had implemented) in a CT $\Delta\Sigma$M. (6.6) is quite a bit different from the $H(z) = (-2z^{-1} + z^{-2})/(1 - z^{-1})^2$ we desire in a double integration $\Delta\Sigma$M. First, the ratio of the z^{-1}/z^{-2} numerator coefficients is closer to -4 than -2, and z^{-3} is nonzero. Second, from (2.2) the poles of $H(z)$ are the zeros of NTF(z), and factoring the denominator of (6.6) gives poles $z = 0.994\angle\pm 4.1°$. Ideally, this would be $z = 1\angle 0°$. Using the group of 50 samples starting at sample 7000 yields a best-fit $x(n)$ of

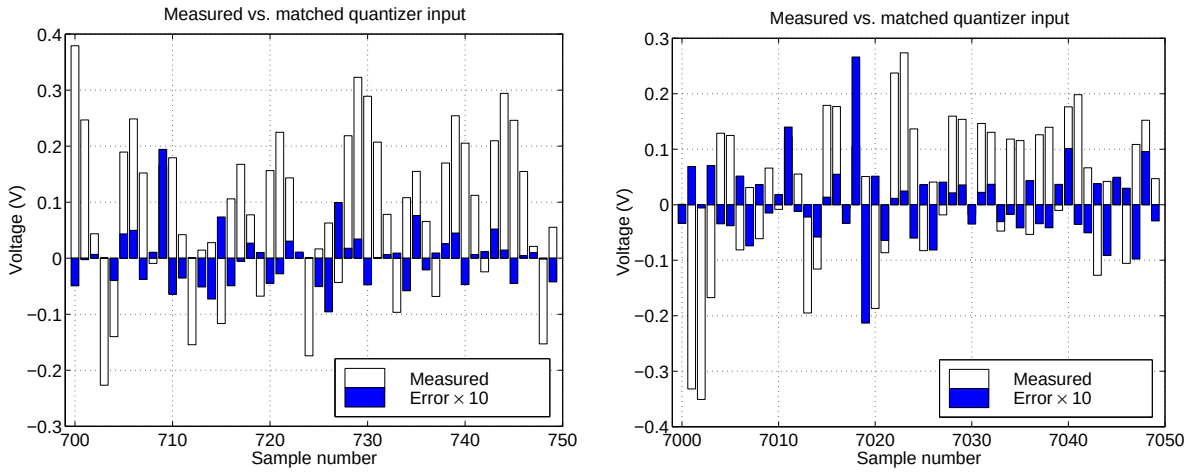
$$\begin{aligned} x(n) &= 1.9587x(n-1) - 0.9832x(n-2) + 0.2241u(n-1) \\ &\quad - 0.2027y(n-1) + 0.0501y(n-2) + 0.0468y(n-3), \end{aligned} \tag{6.7}$$

$$\|\varepsilon\|_\infty = 26.62\text{mV}, \quad \|\varepsilon\|_2 = 7.061\text{mV}. \tag{6.8}$$

The NTF zeros are now found to be $0.992\angle\pm 9.0°$. The magnitude is similar to that found from (6.6), but the angle has changed from 4.3° to 9.0°. The coefficients of the best-fit equation seem sensitive to the group of samples chosen. □

6.1.3 Examining the Errors

For the groups of samples in Example 6.1, Figure 6.2 illustrates the SPICE values of $\hat{x}(nT_s)$ with clear bars, and the errors (the solid bars, magnified for ease of viewing) between $\hat{x}(nT_s)$ and the best-fit Matlab equations $x(n)$ in (6.4) and (6.7). At samples 709 and 710 in Figure 6.2(a), there is a large error followed by an error of opposite sign; the same is true at samples 7018 and 7019 in Figure 6.2(b). Resimulating with more detail produced the same problem at samples 179 and 180 and the circuit waveforms in Figure 6.3. We noticed the matching errors of opposite sign coincided with *additional* excess delay at sample 178: the nominal excess delay in this design is $\rho_d \approx 0.20$, but at sample 178 in Figure 6.3, the delay is $\rho_d \approx 0.30$. Recall that the second integrator



(a) (b)

Figure 6.2: Examples of z-domain extraction from SPICE data.

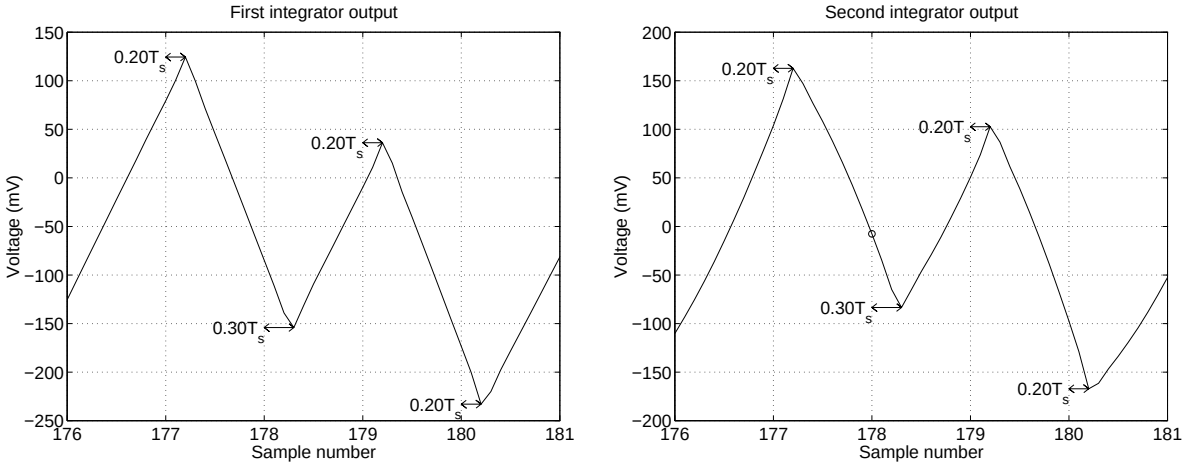
output in Figure 4.1 is precisely $\hat{x}$, the quantizer input; notice that in Figure 6.3(b), the voltage at sample 178 (illustrated by the small circle) is close to zero. It is this which causes the extra delay: small quantizer inputs lead to longer regeneration times, which leads to increased excess delay. Figure 6.4 plots excess delay against quantizer input magnitude for many sampling instants and proves the point.

6.1.4 Usefulness of z-Domain Extraction

It was because of the z-domain extraction method that we stumbled upon the significance of metastability in CT $\Delta\Sigma$Ms. Some general comments about the usefulness of the method are in order. First, the good things:

- It requires relatively few samples to work, and hence relatively little simulation: for example, 50 samples are enough for a good least-squares fit. These 50 samples could be the first 50 rather than later sequences of 50 as we used in Example 6.1, which means we can apply it with a quick SPICE simulation rather than a lengthy one.

- It works on data from any simulation program, SPICE or otherwise, which can print out



(a) (b)

Figure 6.3: First and second integrator output waveforms from SPICE showing additional excess delay at sample 178.

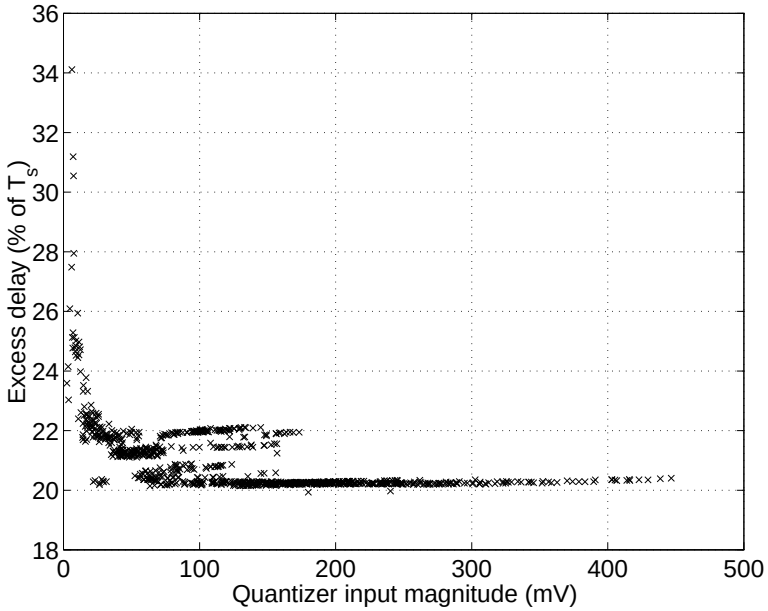


Figure 6.4: Effect of finite quantizer gain on excess loop delay.

circuit values at sampling times.

- It turns out to be good at modeling certain types of nonideality, such as DAC waveforms with delay or nonzero rise time, well.
- It allows us to determine the $H(z)$, and consequently the NTF(z), actually implemented. This could be useful as a design check on NTF(z).

The bad things are:

- Guesswork as to which terms to include on the RHS of the fitting equation is sometimes required to find a fit with a small error.
- Certain types of nonidealities, such as nonlinear integrating capacitors (or, indeed, quantizer metastability—it was this that was predominantly to blame for the largish matching errors in (6.5) and (6.8)), seem difficult or impossible to model exactly. This might be improved with a better selection of fitting terms.

We had, perhaps naively, hoped to be able to use the method to supplant CT simulation altogether: with a perfect z-domain fit, one could simply simulate a CT modulator using the difference equation. Instead, the method seems appropriate to use *in conjunction with*, rather than in place of, full-circuit CT simulation. We should also mention that it can be, and was successfully, used in an SC modulator to identify clipping integrator outputs as the reason for poor performance, so it can be applied to DT simulations as well.

6.2 Latches and Metastability

Published high-speed CT $\Delta\Sigma$Ms tend to be bipolar-only circuits with a one-bit quantizer. A typical quantizer for such circuits was shown in Figure 4.15, reproduced here as Figure 6.5. As we said earlier, the transistors in the dotted box can be reconnected to produce RZ instead of NRZ waveforms. The dashed box contains the four transistors responsible for regeneration: when the circuit is enabled, the voltage difference V_{rd} at the bases of the emitter follower transistors is amplified by

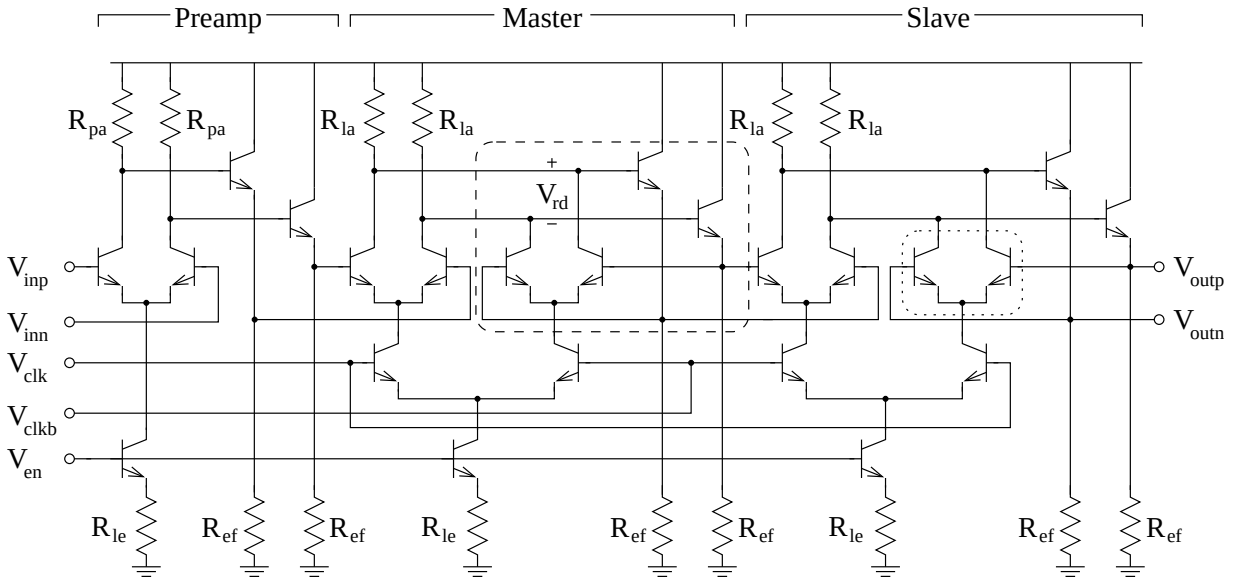


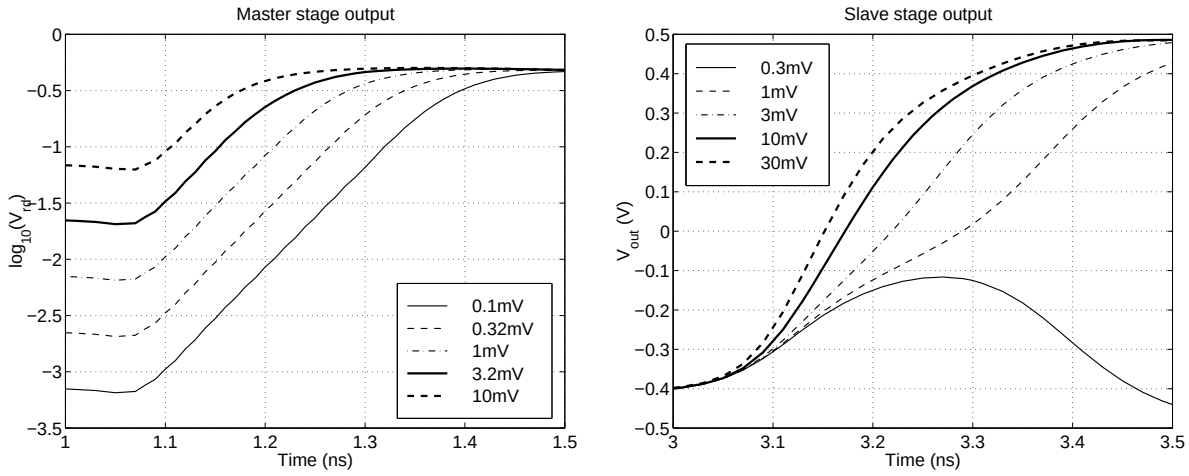
Figure 6.5: Typical high-speed CT $\Delta\Sigma$M master-slave latched comparator with preamplifier.

positive feedback until the maximum positive (digital $+1$) or negative (digital -1) voltage difference is reached. In an ideal latch there exists a third output state, the *metastable* state, where the inputs are balanced resulting in a 0V differential output signal. This state is unstable in that a slight perturbation (e.g., from circuit noise) will push the latch towards one of its stable states, hence the metastable state itself is never observed in practice.

6.2.1 Digital Circuits vs. $\Delta\Sigma$Ms

The usual analyses of metastability in digital latches [Vee80, Hor89] treat the regenerative circuit as a single-pole system where the voltage difference at $t = 0$ increases exponentially with a time constant inversely proportional to the gain-bandwidth (GB) product of the system. Such a treatment is valid here: Figure 6.6(a) is a SPICE transistor-level simulation of just the master portion of Figure 6.5 with input voltages given in the legend box. The differential pair amplifies the input voltage in the first half clock cycle, then the regenerative quad is enabled at $T = 1$ns and the value V_{rd} rises exponentially ($\log V_{rd}$ is a straight line) until near the output voltage limit.

In digital circuits, the usual question to be answered is, what is the probability that the latch



(a) (b)

Figure 6.6: Output of (a) master stage, (b) slave stage.

output is a valid digital level at time t given a certain setup time? In CT $\Delta\Sigma$Ms, we are interested in a different question. Figure 6.6(b) plots the output of an M/S latch whose input is first driven negative to make the latch output -1, then slightly positive to the value in the legend box. Note that the time when the latch output crosses zero on its way to $+1$ varies as a function of the positive input voltage (and that very small positive inputs cause the latch to produce a glitch). This output voltage drives the DACs, and variations in its zero-crossing time (ZCT) have exactly the same effect as quantizer clock jitter—random edge variations modulate out-of-band noise into the signal band and whiten the spectrum. Thus, the question that concerns us is, what is the exact shape of the DAC output waveform? Most particularly, how does its ZCT vary for quantizer input voltages changing sign between clock periods?

When we initially studied this problem we were hoping to find an analytic answer to the question using methods along the lines of those published in papers on CMOS latches. However, we encountered a number of difficulties that meant a formula eluded us. First, published papers generally solve for one variable (the probability that the output is a valid digital level) based on one parameter (the setup time); in our work, we care about *two* variables (the ZCT and also the rise time) as a function of *two* parameters (the input voltage and its slope). Second, papers on CMOS

latches generally look just at the latch output; in our case, while the latch output is important in its own right, we are really more interested in the *DAC* output waveform. The latch output drives an emitter follower which drives the DAC differential pair, so there are additional stages whose behavior must be characterized.

Surely neither of these difficulties means an analytic approach is outright impossible. The work in [Hoh84] treats a latch with a multivibrator input stage, which is more complicated than what most papers treat and could perhaps be adapted for our purposes. However, we eventually decided to adopt an empirical solution to the problem. We must accept the danger that useful insights which would otherwise have come out will be obscured.

6.2.2 Characterization Method for $\Delta\Sigma$Ms

We determine the ZCT and rise time characteristics of a given latch from simulation. A transistor-level SPICE file describing the complete feedback circuit from latch input to feedback output is composed. The input to the latch is a piecewise-linear wave which first goes negative to drive the feedback output negative, then positive with slope v_{sl} so that at the next clocking instant the latch input is a specified value v_x. For many different (v_x, v_{sl}) pairs, the ZCT relative to the previous sampling instant (which we call $\tau_d = \rho_d T_s$ for "delay time") and the feedback output rise time (which we call $\tau_r = \rho_r T_s$ for "rise time") are calculated. It is assumed that the curves would be the same for a falling output wave, i.e., that the circuit is differential and hence symmetric. If this did not hold, it would be possible to characterize ρ_d and ρ_r both for rising and falling latch inputs.

Example 6.2: The process is illustrated in Figure 6.7, which is for an M/S latch like Figure 6.5 except with no preamplifier stage. The clock rate is $f_s = 500$MHz ($T_s = 2$ps), and the transistors have a switching speed of about $f_T = 12$GHz. In the upper graph, we see $(v_x, v_{sl}) = (0.2, 0.6)$ for the input wave V_{in} at $t = 0$. The latch output goes through an emitter follower to a differential pair DAC whose collectors have been terminated with resistors. It is the differential resistor voltage that we plot as V_{out} in the bottom graph. We calculate $(\rho_d, \rho_r) = (0.0860, 0.0386)$ and this is plotted

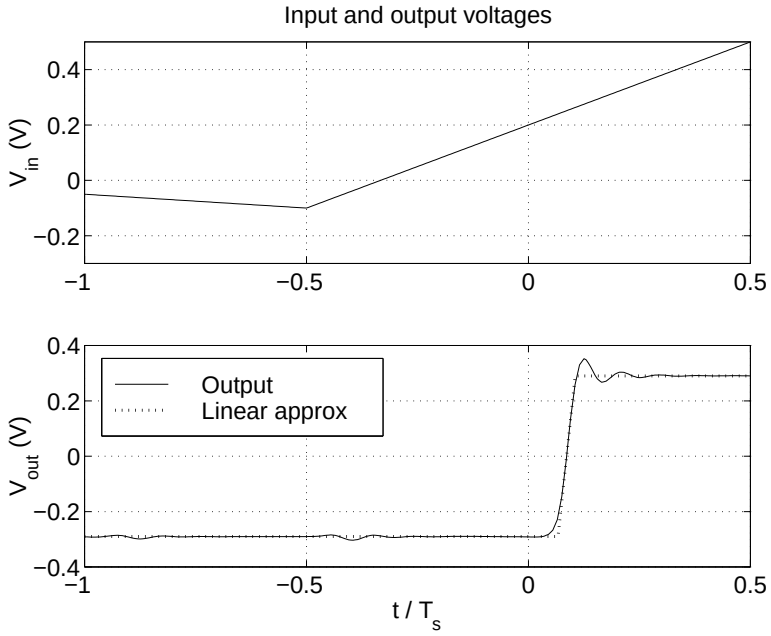


Figure 6.7: SPICE input and output waveforms with linear approximation to output.

as the dotted line in the bottom graph; the approximation to the actual waveform is quite good.

Our input wave is such that we are characterizing the quantizer by driving it hard one way, which makes it emit a "strong pulse", then weakly the other way, which makes a "weak pulse". Experience shows that this is by far the most common case—rarely is the quantizer input of a real modulator such that the quantizer would emit two weak pulses in a row. □

Using Perl [Wal96] helps greatly to automate the procedure for many (v_x, v_{sl}) pairs. Curves for ρ_d and ρ_r for our M/S latch and DACs from Example 6.2 are plotted in Figure 6.8. These curves indicate that for inputs close to zero, both the ZCT and the rise time increase, c.f. Figure 6.6(b). Moreover, for small enough inputs, no zero crossing is measured, which is what we saw with the glitch in Figure 6.6(b) for $V_{in} = 0.3$mV—this is an example of quantizer hysteresis. And, as the input passes through v_x with higher slopes, delayed zero crossings and hysteresis happen for larger values of v_x. These curves have been normalized so that v_x is relative to the expected full-scale

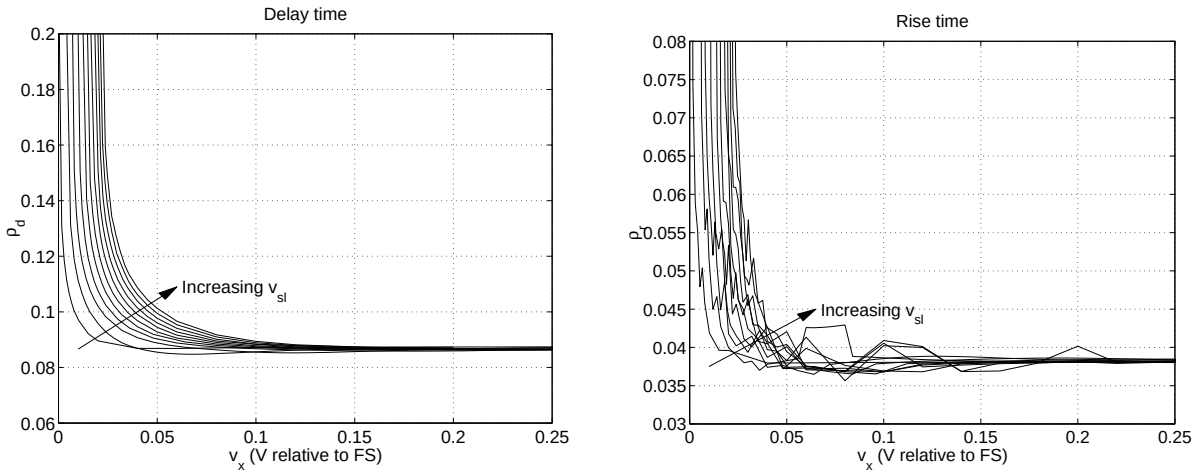


Figure 6.8: Example of numerically-characterized ρ_d and ρ_r values.

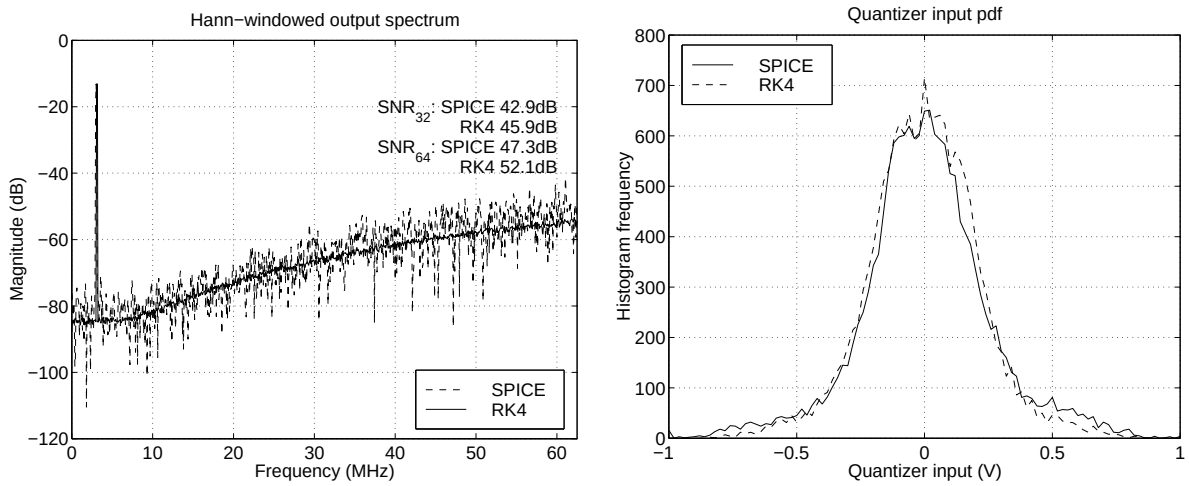
quantizer input, which for our example circuit happens to be ± 1V. v_{sl} values are normalized to full scale volts per clock period and swept from 0 to 2. $v_{sl} = 2$ corresponds to a straight line quantizer input that goes from positive to negative full-scale over one clock period. Typically the maximum quantizer slope can be observed to be about half this much, though the quantizer input isn't usually a perfectly straight line (recall x_2 in Figure 3.1). Nonetheless, $v_{sl} = 2$ should be larger than most practically-occurring slopes.

The data from Figure 6.8 is used as input to the RK4 simulation program from Chapter 5; at each clocking instant, the program calculates (v_x, v_{sl}) and uses linear interpolation to find (ρ_d, ρ_r), which are then used to set the feedback pulse's delay time and rise time. Essentially, we are employing the technique of *behavioral modeling* [Cur95].

6.2.3 Validation of Quantizer Model

How good is the behavioral model? In other words, how well do the results from our $\Delta\Sigma$M simulator using the behavioral quantizer model agree with those from full-circuit simulation?

Example 6.3: The comparator and feedback circuitry of the prototype double integration modulator in §6.1 designed in an $f_T = 25$GHz process clocking at $f_s = 1$GHz were characterized as described in Example 6.2, and as many of the pa-



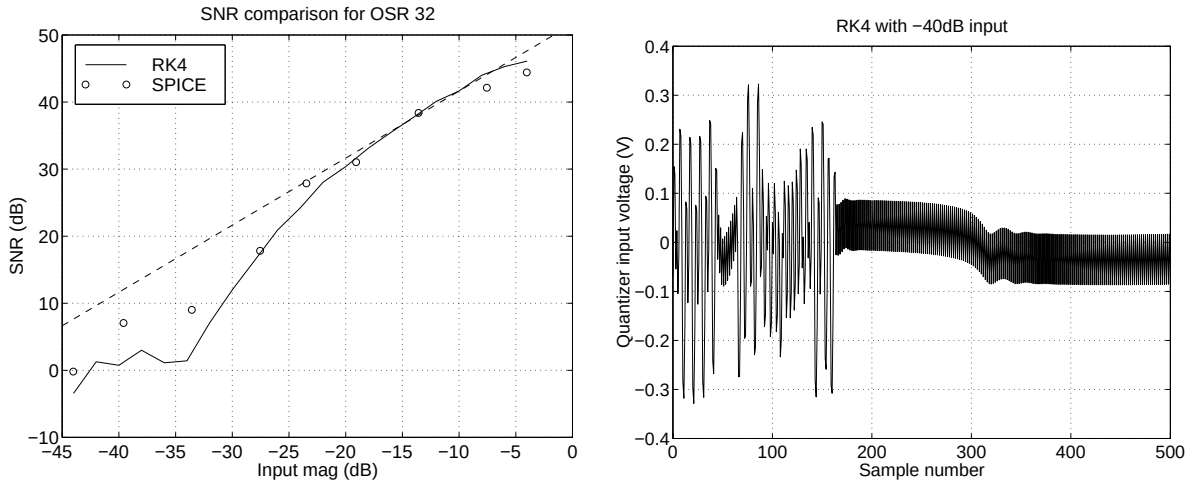
(a) (b)

Figure 6.9: Comparison of SPICE and Runge-Kutta simulation programs: (a) output spectra, (b) quantizer input pdfs.

rameters from the actual circuit as possible (such as finite integrator gain and input resistance) were included in an input file to the RK4 simulator. For a -4dB input at 3.1MHz, output spectra for a 16384-point SPICE simulation and 64 averaged 16384-point periodograms from the RK4 simulation are shown in Figure 6.9(a). The spectrum details agree quite well, and there is acceptable agreement between calculated SNR values at OSR $= 32$ and 64, as shown on the graph. The RK4 program predicts a slightly lower white noise floor due to metastability than SPICE. Figure 6.9(b) shows a histogram of the quantizer input pdf $p_x(\alpha)$ from each simulator, and good agreement is seen—we are modeling the behavior and voltage levels in the real circuit quite well.

A dynamic range plot is shown in Figure 6.10(a). The RK4 values of SNR were found from 32 averaged 4096-point periodograms, and in SPICE each value was found from a single 4096-point simulation. The agreement between the two is quite good, and it is worth noting that while each RK4 simulation of 128k output bits took about 30 seconds, a single 4096-bit SPICE simulation took over four hours. □

Behavioral models are meant to increase simulation speed while maintaining accuracy, and we see that our quantizer model scores well on both counts.



(a) (b)

Figure 6.10: Comparison of SPICE and Runge-Kutta simulation programs: (a) dynamic range plot, (b) quantizer input limit cycle for low magnitude input.

Example 6.4: We made an interesting discovery in the course of this work: the effect of metastability for small input magnitudes. The dashed line in Figure 6.10(a) has slope 1dB/dB, which is the expected slope of the SNR vs. input magnitude curve. This slope is observed in simulation for large input amplitudes, but as input amplitude decreases, we achieve SNR $= 0$ for an input magnitude of -42dB, whereas the dashed line predicts SNR $= 0$ at -52dB input. With a -40dB modulator input, observation of the quantizer input as a function of time reveals the behavior shown in Figure 6.10(b): up to about sample 160, the quantizer behaves as it should, but then the modulator enters a $\{+1, -1\}$ limit cycle from which it does not escape at a later time. Clearly, the modulator output no longer encodes the input signal at this point. The author observed this behavior in both RK4 and SPICE simulations.

It is known [Fee91] that integrators with finite gain can cause such behavior. However, it was found in RK4 simulations with a metastable quantizer that the behavior occurred even with ideal (i.e., infinite-gain) integrators. It was thought that perhaps a quantizer with hysteresis alone (i.e., with *constant* ρ_d and ρ_r) might also cause the

$\Delta\Sigma$M to exhibit the behavior, but this was not found to be the case with infinite-gain integrators. Therefore, it appears that quantizer metastability can result in worsened sensitivity of an otherwise ideal CT $\Delta\Sigma$Ms to small input levels.

It should be noted that the metastability is indeed being excited in Figure 6.10(b). From samples 160 to 300 or so the bottom envelope of the quantizer input is near zero, which activates the metastability. It "escapes" from this mode of behavior only to have the *top* of the envelope approach zero and activate the metastability at sample 320. The metastability is excited alternately by the envelope top and bottom every few hundred cycles. □

This result is of grave significance because it implies using a single large-amplitude tone to estimate modulator resolution is insufficient: one might predict a DR based on an incorrect assumption of a slope of 1dB/dB down to SNR $= 0$. To the author's knowledge, this is a previously unpublished result.

Admittedly, there is no absolute guarantee that changing the quantizer circuit will mean the agreement between behavioral and SPICE simulation remains good. However, we have more than one reason to be confident that our behavioral model has identified the key issues. First, we have good agreement not just on SNR, but on output spectrum details and quantizer input pdf too. Second, the behavioral model correctly predicted the limit cycle behavior, a result which was unknown a priori. For the remainder of this chapter we use only the behavioral model for circuit performance measurements.

6.3 Real Quantizer Performance Effects

The design of CT $\Delta\Sigma$Ms is usually done assuming an ideal quantizer, which has no hysteresis and makes a decision instantly. The characteristics of such a quantizer are plotted in Figure 6.11(a): ρ_d is always zero no matter how small v_x is. Practical quantizers suffer from three nonidealities which can be distinguished as follows:

1. Excess delay, Figure 6.11(b), means a vertical shift of the quantizer curve; more excess

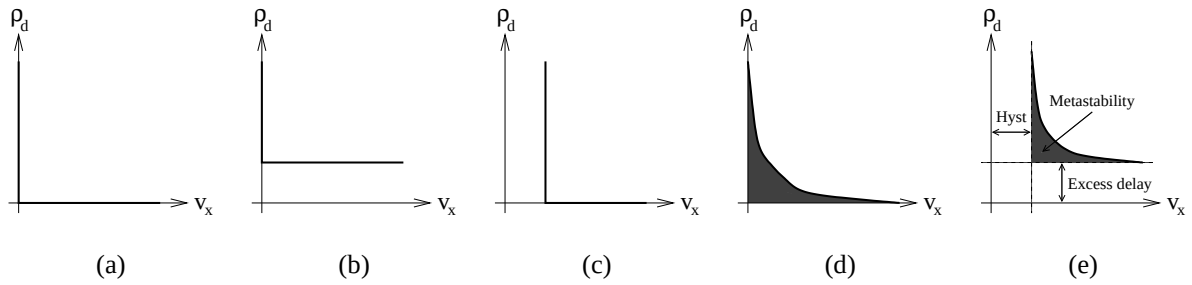
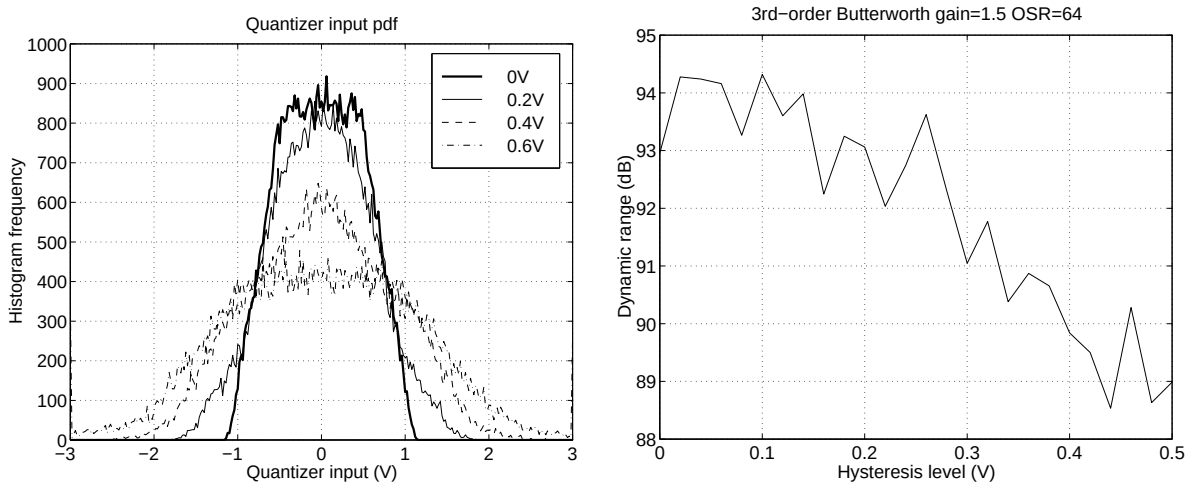


Figure 6.11: Quantizer characteristics: (a) ideal, (b) excess delay, (c) hysteresis, (d) metastability, (e) practical. Metastability severity is proportional to the area of the shaded region.

delay means a greater vertical shift. As we noted in Chapter 4, the effect of excess delay is to increase in-band noise and lower MSA which in combination compromise overall modulator DR.

2. Hysteresis, Figure 6.11(c), causes a horizontal shift of the curve proportional to the amount of hysteresis. From §3.1.3, quantizer hysteresis in an otherwise ideal system adds noise power in the baseband for LP modulators [Bos88]. An example of its effects for the third-order LP Butterworth $\Delta\Sigma$M studied in Chapter 5 is depicted graphically here. In Figure 6.12(a), we see $p_x(\alpha)$ becoming wider with hysteresis; this is expected because as long as the quantizer output bit remains the same, the circuitry inside the loop will continue integrating in the same direction, enlarging signal swings. In a modulator whose integrator outputs clip, hysteresis introduces harmonic distortion; moreover, too large an internal signal excursion range leads only to *gradual* instability and hence DR loss, as shown in Figure 6.12(b)—hardly any performance is lost even for large hysteresis. By contrast, [Cha92] found 1% hysteresis caused significant performance loss, though this is at odds with other publications and our own results.

3. Metastability, Figure 6.11(d), means that the sharp corner in the ideal quantizer characteristics becomes smooth instead. The severity of the metastability is related to the amount of area underneath the curve: curves with a more abrupt corner have less area under them and hence less metastability.



(a) (b)

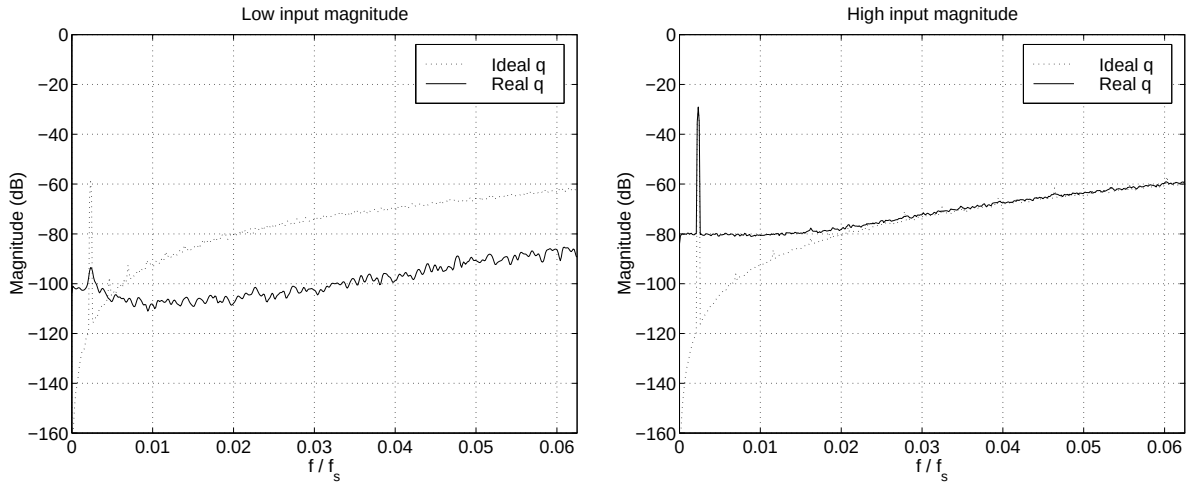
Figure 6.12: Quantizer hysteresis in third-order Butterworth modulator: (a) quantizer input pdf, (b) modulator dynamic range.

A real quantizer has all three effects simultaneously, Figure 6.11(e), as we saw in Figure 6.8. Along with the losses already caused by excess delay and hysteresis, metastability introduces two additional performance-limiting effects. First, at low input amplitudes, there is the output limit cycle behavior mentioned in Example 6.4 and depicted in Figure 6.13(a) for a double integration modulator. Second, at higher input amplitudes spectral whitening occurs due to the *variability* of ρ_d mentioned in §6.1.3. A typical spectrum is depicted in Figure 6.13(b).

Example 6.5: The DR impact of using the quantizer characteristics in Figure 6.8 on several kinds of LP $\Delta\Sigma$M is shown in Figure 6.14. In order to make the comparison fair, the modulators had their feedbacks scaled so that they all had the same quantizer input pdf standard deviation of $\sigma_x = 1/3$[1]. We observe the following:

- An ideal modulator exhibits $6m+3$dB/oct improvement of SNR with OSR, where m is the modulator order. A modulator with a metastable quantizer will, for large enough OSR, be limited to a mere 3dB/oct improvement because the noise

[1]Since $p_x(\alpha)$ is roughly Gaussian [Bos88], fixing σ_x assures roughly the same distribution of abscissae in the quantizer characteristic in Figure 6.8, and hence a roughly-comparable ordinate distribution.



(a) (b)

Figure 6.13: Typical output spectra from double integration $\Delta\Sigma$M with a real quantizer: (a) low input amplitude, (b) high input amplitude.

notch in the output spectrum is filled in with white noise. For the quantizer from Example 6.2, going from OSR $= 32$ to OSR $= 64$ (shown by the dash-dot lines) gives us only 3dB SNR improvement. This means the DR at OSR $= 64$ for all modulators is cut drastically by a full factor of two.

- The dashed lines show modulators with hysteresis and fixed

$$(\rho_d, \rho_r) = (8.6\%, 3.9\%);$$

compared with the ideal modulator, DR is hardly compromised at all, perhaps 0–3dB depending on the modulator order.

- The limit cycle behavior in $\Delta\Sigma$Ms with metastable quantizers mentioned earlier seems only to affect the lower-order modulators: the higher-order modulators have 1dB/dB slope all the way down to low input magnitudes, except perhaps for a slight dip near -35dB.

Metastability clearly has a major impact on the DR of these high-speed CT $\Delta\Sigma$Ms. □

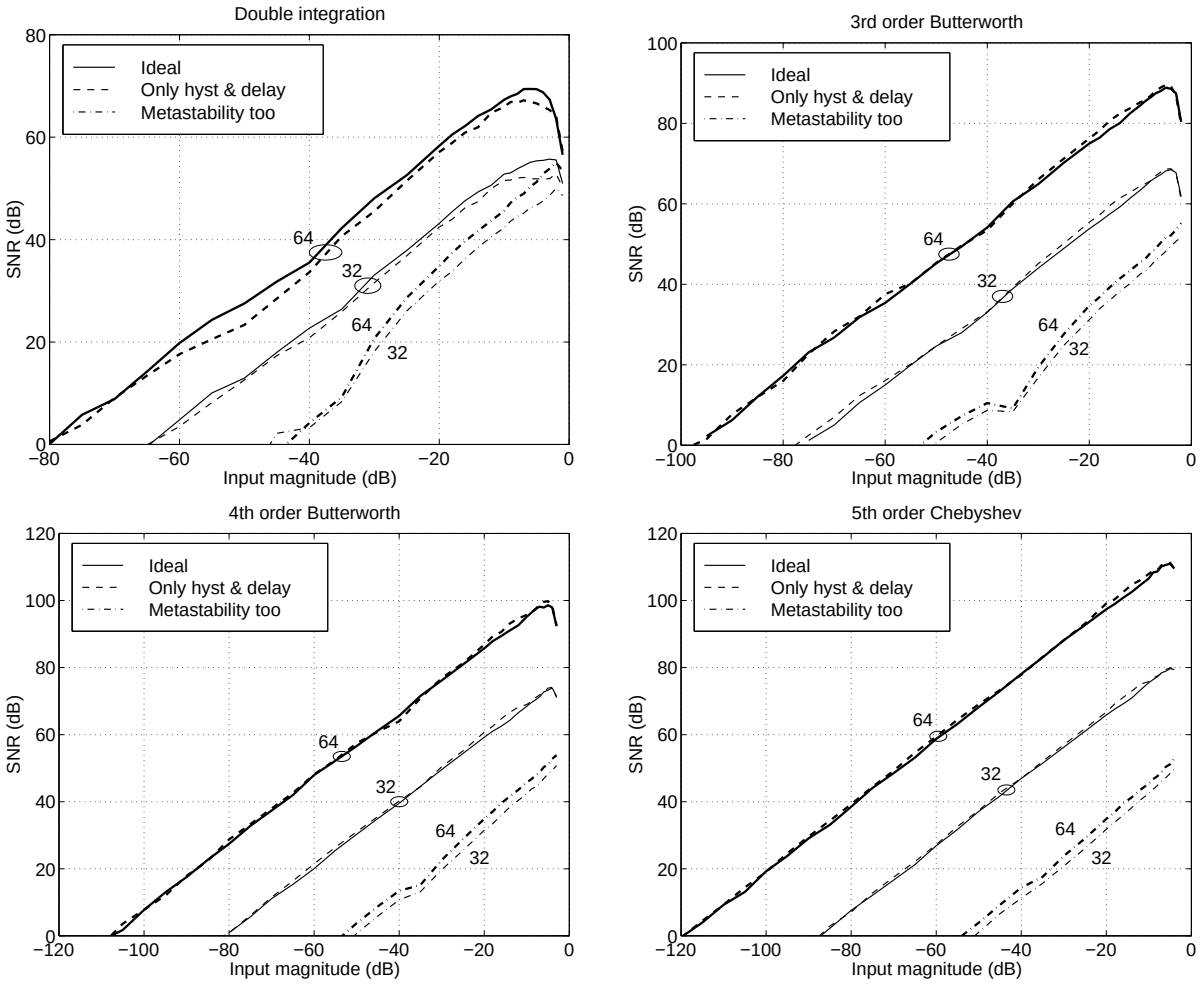
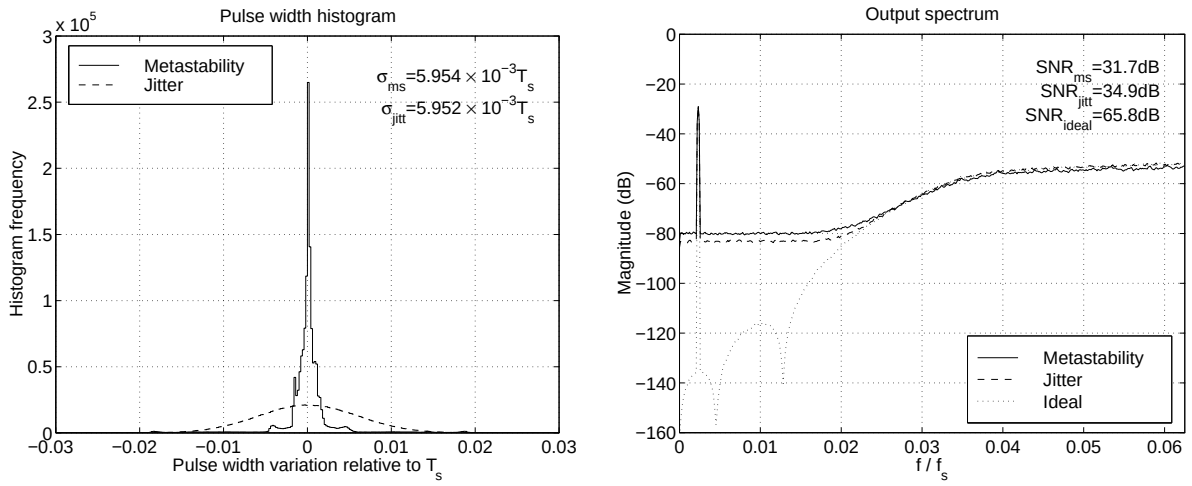


Figure 6.14: Dynamic range plots. Numbers on curves are OSR values.



(a) (b)

Figure 6.15: Comparison of clock jitter to quantizer metastability: (a) DAC pulse width variation histogram, (b) output spectrum.

There is a relationship between performance lost by metastability and that lost by clock jitter which can be explained as follows.

Example 6.6: We know that random variation in DAC pulse width (DPW) fills the output spectrum noise notch with white noise. The solid line in Figure 6.15(a) shows a histogram of DPW variation for the fifth-order modulator with an ideal sampling clock and a metastable quantizer with characteristic given by Figure 6.8. The standard deviation of this distribution is $\sigma_{ms} = 5.95 \times 10^{-3} T_s$. To get the same DPW variance from a modulator with an ideal quantizer and a clock with independent jitter, we must set the jitter variance to

$$\sigma_\beta = \sigma_{ms}/\sqrt{2}. \tag{6.9}$$

This results in the dashed-line histogram in Figure 6.15(a). Note that $\sigma_{jitt} \approx \sigma_{ms}$. Since the DPW variance is about the same in both cases, §5.2 taught us that the spectrum whitening should also be about the same. Figure 6.15(b) illustrates this to be the case: the SNR value for the modulator with the metastable quantizer is 31.7dB, while that for the modulator with clock jitter is 34.9dB. The noise floors are close but not

identical because the distribution of the DPW histogram for a metastable quantizer is not particularly Gaussian. Even still, the agreement is quite good. □

Clock jitter is not identical to metastability because clock jitter does not cause the limit cycle behavior observed in Example 6.4 for low input amplitudes; it is the white noise levels that are roughly the same in both for large-enough input amplitudes. Though the DRs might differ, the peak SNR measured in both would come out about the same.

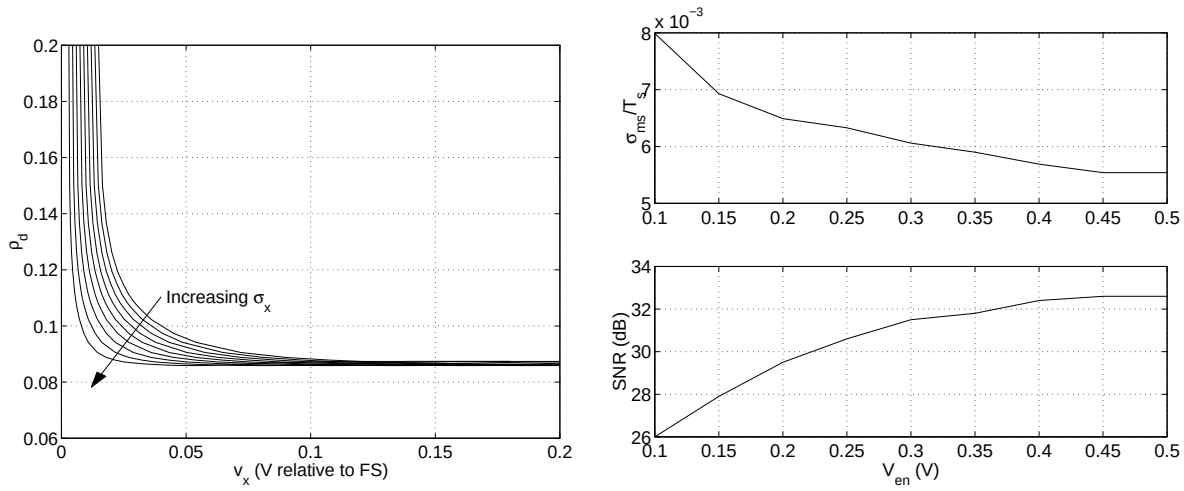
6.4 Mitigating Metastability Performance Loss

How can we overcome the performance penalties imposed by quantizer metastability? Several answers to this question suggest themselves when we consider the source of the loss: the variations in the DPW caused by finite quantizer regeneration. We observed at the start of §6.3 that this variance σ_{DPW} is related to the area under the metastability curve in Figure 6.11(e), or equivalently the "sharpness" of the corner in the curve. What approaches might we take to reduce its area or sharpness?

6.4.1 Parameter Scaling

The first thing we might think of is to scale the modulator parameters to enlarge the quantizer input standard deviation σ_x. This works as follows: we know that if the magnitude of the quantizer input is small, then the ZCT increases. For the quantizer in Figure 6.8, inputs which cause increased ZCT are approximately those for which $|v_x| < 100$mV. By increasing σ_x, we widen the range of possible quantizer inputs so that the probability of $|v_x| < 100$mV is decreased. Alternately, we may think of this as scaling the v_x axis by compressing the metastability curves towards the ρ_d axis. This reduces the effective area under a given curve and hence reduces σ_{DPW}.

Example 6.7: Example 6.5 used $\sigma_x = 0.33$. We illustrate the effect of choosing σ_x ranging from 0.1 up to 0.5 in Figure 6.16. In Figure 6.16(a), the metastability curve for $v_{sl} = 0.6$ is plotted as a function of σ_x; we can see the corner of the curve



(a) (b)

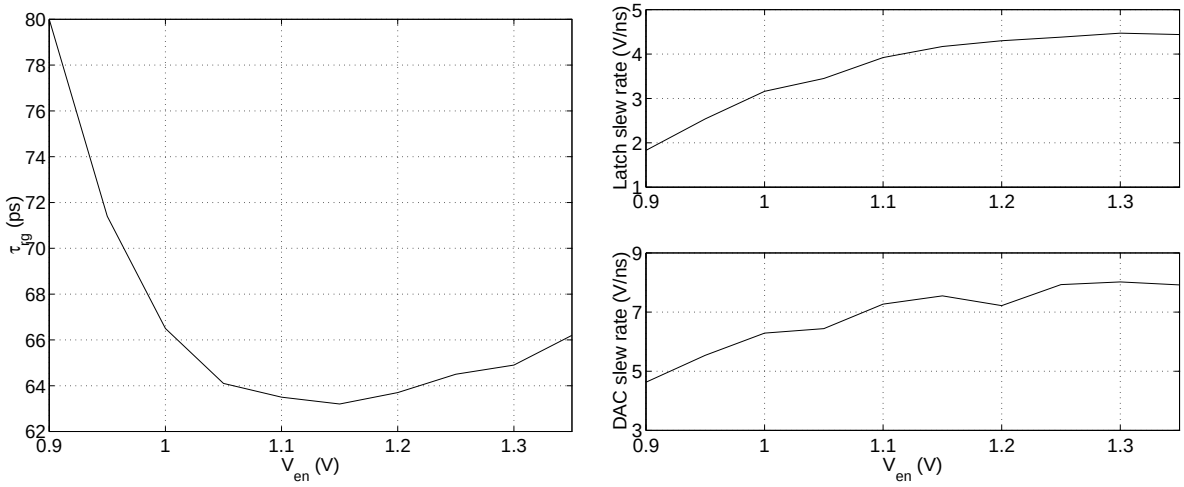
Figure 6.16: (a) Quantizer metastability curves and (b) modulator performance as a function of σ_x.

becoming sharper as $\sigma_x$increases, which leads to more favorable σ_{ms}/T_s and SNR in Figure 6.16(b). □

Generally, it is a good idea to have the quantizer input span as large a range as possible. The range can be increased by, for example, choosing smaller integrating capacitors and larger feedback currents. Circuit constraints will ultimately limit the maximum achievable range; for our case, the quantizer input can swing about $\pm$1V differential while still keeping all transistors operating in their forward active regions. Having too small a swing range is to be avoided because as we see in Figure 6.16(b) it quickly becomes detrimental for SNR.

6.4.2 Regeneration Time

In §6.2.1, we said that the regeneration time of a latch is inversely proportional to the GB product of the regeneration circuit. If we were to increase this GB product, the corners of the metastability curves would become sharper as follows: the slope of the curves in Figure 6.6(a) would increase, which in turn would, we hope, mean that it would take a *smaller* input level v_x for the curves in Figure 6.6(b) to exhibit increased delay—in other words, for the set of v_x values in that legend box,



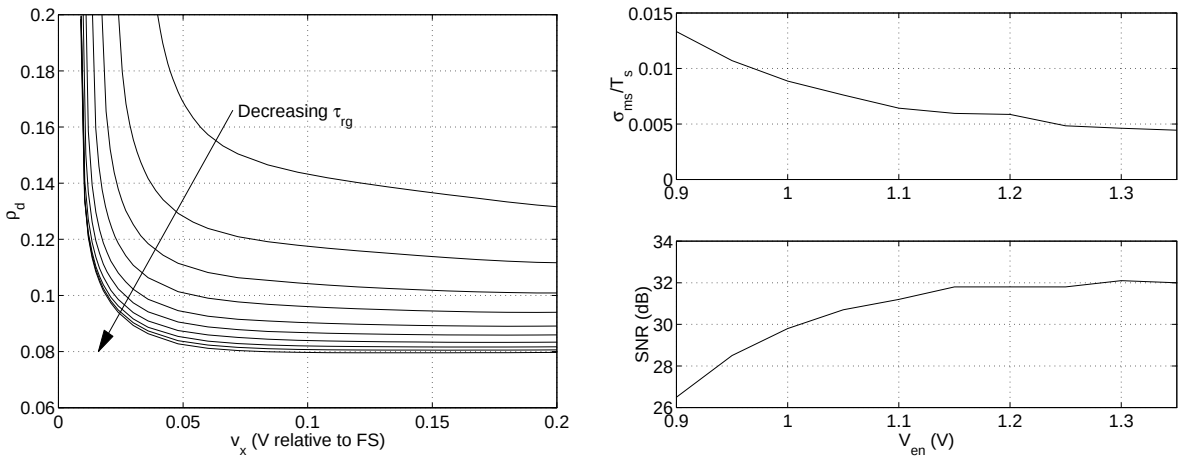
(a) (b)

Figure 6.17: Effect of V_{en} on (a) regeneration time, (b) slew rates at latch output and DAC output.

the rising output edges would be bunched more closely together. In turn, the curves in Figure 6.8 would rise towards infinity more abruptly, i.e., the corner becomes more pronounced.

Example 6.8: One way to affect the regeneration time constant τ_{rg} of the latch in Figure 6.5 is to change the current in the regenerative quad; this is accomplished by altering the voltage V_{en}. To keep the comparison reasonable, we will adjust V_{en} and R_{la} simultaneously to keep the latch output voltage swing at around ± 300mV. Sweeping V_{en} over the range 0.90V to 1.35V and extracting τ_{rg} from simulation yields the curve of Figure 6.17(a): as is usual with ECL circuits, there exists a current/load resistor combination which minimizes rise time which for this latch occurs at about $V_{en} = 1.15$V. While fast linear settling is important, surely as important for ZCT is the nonlinear settling behavior, i.e., slewing. Figure 6.17(b) plots the slew rates at both the latch output (top) and DAC output (bottom) as a function of V_{en}.

Figure 6.18(a) shows quantizer metastability curves for $v_{sl} = 0.6$ as V_{en} changes. There is some sharpening of the corner with increased V_{en}, but as an added bonus also lower ρ_d and hysteresis. Just as diminishing returns are apparent there, so too are they



(a) (b)

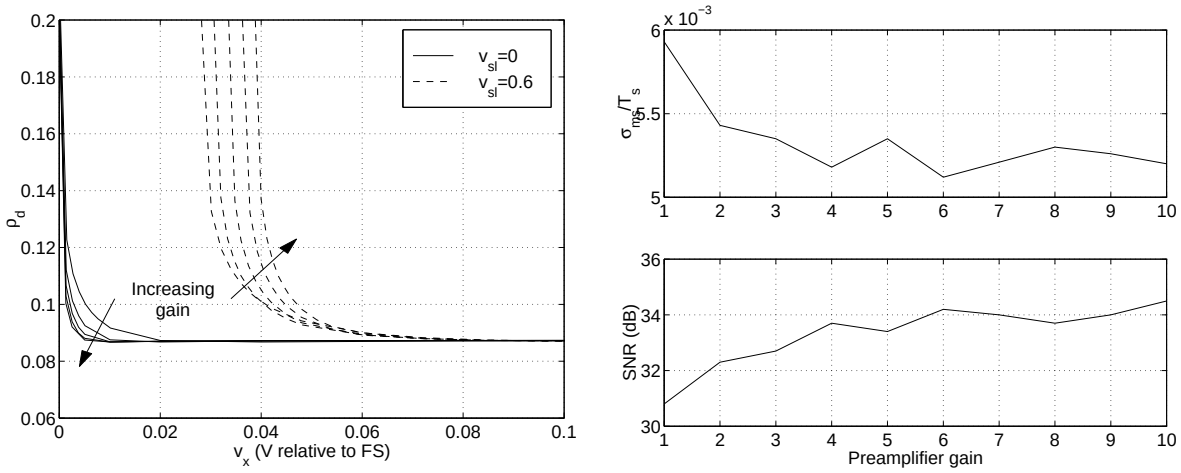
Figure 6.18: (a) Quantizer metastability curves and (b) modulator performance as a function of τ_{rg}.

in Figure 6.18(b) where the SNR is plotted against V_{en}. The optimum SNR does not quite occur where τ_{rg} is a minimum—very minor improvements are obtained as V_{en} is raised further because of the increase in slew rate. □

Ensuring adequate regeneration is a good idea in a $\Delta\Sigma$M's latch. Setting V_{en} very high might use more power than necessary to achieve a given SNR, so there exists a tradeoff between power consumption and SNR, though we could use smaller transistors whose peak speed occurs at lower bias current.

6.4.3 Preamplification

A third thing we can try is using a latch with a preamplifier. This is similar to signal scaling in §6.4.1 but not identical because we actually insert a new circuit element into the forward path. How do we choose its gain? Traditional analyses show that for cascaded amplifiers there exists an optimum gain per stage that maximizes the overall amplifier GB product and hence the amplifier speed. Depending on the assumptions made, the optimum gain is either $e = 2.72$ [Sne96, Chap. 2] or $\sqrt{e} = 1.65$ [Lee98, Chap. 8]. In the present circuit, we will consider only one preamplifier



(a) (b)

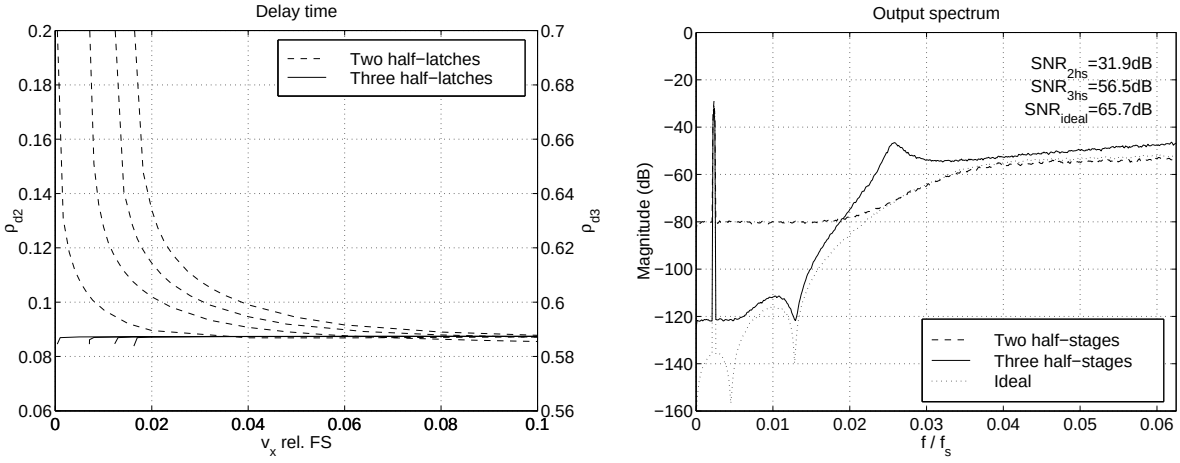
Figure 6.19: (a) Quantizer metastability curves and (b) modulator performance as a function of preamplifier gain.

stage and study how its gain affects metastability performance in the following example.

Example 6.9: Figure 6.19(a) shows metastability curves for a quantizer with a simple differential pair preamplifier as depicted in Figure 6.5. The gain was varied between 1 and 10 by changing the value of R_{pa}. Increasing the gain has the desirable effect of sharpening the corner of the metastability curves for constant quantizer inputs (see the solid lines in the figure), but for *slewing* inputs little sharpening can be seen as gain rises. Hysteresis increases slightly with gain, and in fact it has increased substantially over Figure 6.18(a) from about 10mV to about 30mV. This is not terribly detrimental to performance as we learned in Figure 6.12.

Figure 6.19(b) shows that a preamplifier does offer some SNR improvement (about 2dB) over parameter scaling, Figure 6.16(b), and regeneration time lowering, Figure 6.18(b). There is little point in using a gain above 4, it appears. □

Thus, preamplifying is somewhat beneficial for performance. An ancillary benefit of a preamplifier with an emitter follower buffer between it and the latch input is a reduction in clock feedthrough noise [Lee92].



(a) (b)

Figure 6.20: (a) Quantizer metastability curves and (b) output spectrum for quantizer with an additional latching stage.

6.4.4 Additional Latching Stages

A fourth thing we can try is using additional latching stages after the slave stage in Figure 6.5 [Jen95]. Clocking each stage on the opposite clock phase from the previous stage gives the previous stage a good deal of time to settle. The drawback is, each latching stage adds an additional half-sample delay in the feedback loop, and from Chapter 4 this delay is detrimental to stability and dynamic range. However, we can somewhat overcome these problems by tuning the k_r and k_h feedback parameters.

Example 6.10: Figure 6.20(a) shows quantizer metastability curves for our baseline latch which has only master and slave half-stages, and a latch that has a third half-stage following the slave which is clocked on the same phase as the master. We have added one half sample of extra delay as can be seen on the right y axis where ρ_{d3} is 0.5 more than ρ_{d2} on the left axis, but the variation of ρ_{d3} with v_x is drastically reduced. This results in a huge improvement—about 40dB—in the white noise floor of the output spectrum, Figure 6.20(b). From simulation, we find DPW variance has dropped nearly two orders of magnitude, from $5.9 \times 10^{-3} T_s$ to $1.4 \times 10^{-4} T_s$.

The fifth-order modulator was unstable with $\rho_d = 0.6$ and nominal k values, but

Table 6.1: Performance of LP modulators with two- and three-half latches against ideal.

Modulator	OSR	Ideal q., $\rho_d = 0.0$		Two half-latch		Ideal q., $\rho_d = 0.6$		Three half-latch	
		DR	Peak SNR	DR	Peak SNR	DR	Peak SNR	DR	Peak SNR
Double	32	64dB	56dB	45dB	50dB	52dB	46dB	52dB	46dB
integration	64	79dB	69dB	43dB	55dB	67dB	61dB	67dB	60dB
3rd order	32	74dB	68dB	49dB	52dB	66dB	61dB	66dB	61dB
Butter	64	95dB	89dB	51dB	55dB	88dB	83dB	84dB	81dB
4th order	32	78dB	74dB	48dB	51dB	68dB	65dB	67dB	65dB
Butter	64	105dB	99dB	50dB	54dB	95dB	91dB	85dB	85dB
5th order	32	83dB	80dB	47dB	50dB	73dB	69dB	72dB	69dB
Cheby	64	116dB	111dB	50dB	53dB	107dB	103dB	85dB	85dB

the ks were tuned so that the modulator was stable and the DR of a modulator with an ideal quantizer was maximized at $\rho_d = 0.6$. One artifact of the large ρ_d is the peak in the spectrum at $0.025 f_s$, something which is caused by the movement of the equivalent DT loop filter poles toward the unit circle as excess loop delay increases. □

We seem to have come across a solution to the metastability problem. How well does it work in general?

Example 6.11: Figure 6.21 shows DR plots for several LP $\Delta\Sigma$Ms for an ideal quantizer and the two quantizers with the metastability curves in Figure 6.20(a). With two half-latches, there is only about 10% excess delay, but the third half-latch pushes that up to 60%. A modulator with an ideal quantizer and 60% delay usually requires k tuning to remain stable, and even then, the DR is less than for the 10% delay case. However, when the ideal quantizer is replaced with a metastable one, the three half-latch quantizer is the clear DR winner.

Table 6.1 summarizes the results for four cases: an ideal quantizer, a quantizer with two half-latches, an ideal quantizer with 60% excess loop delay and tuned ks to maximize DR, and a quantizer with three half-latches and the same tuned ks. For

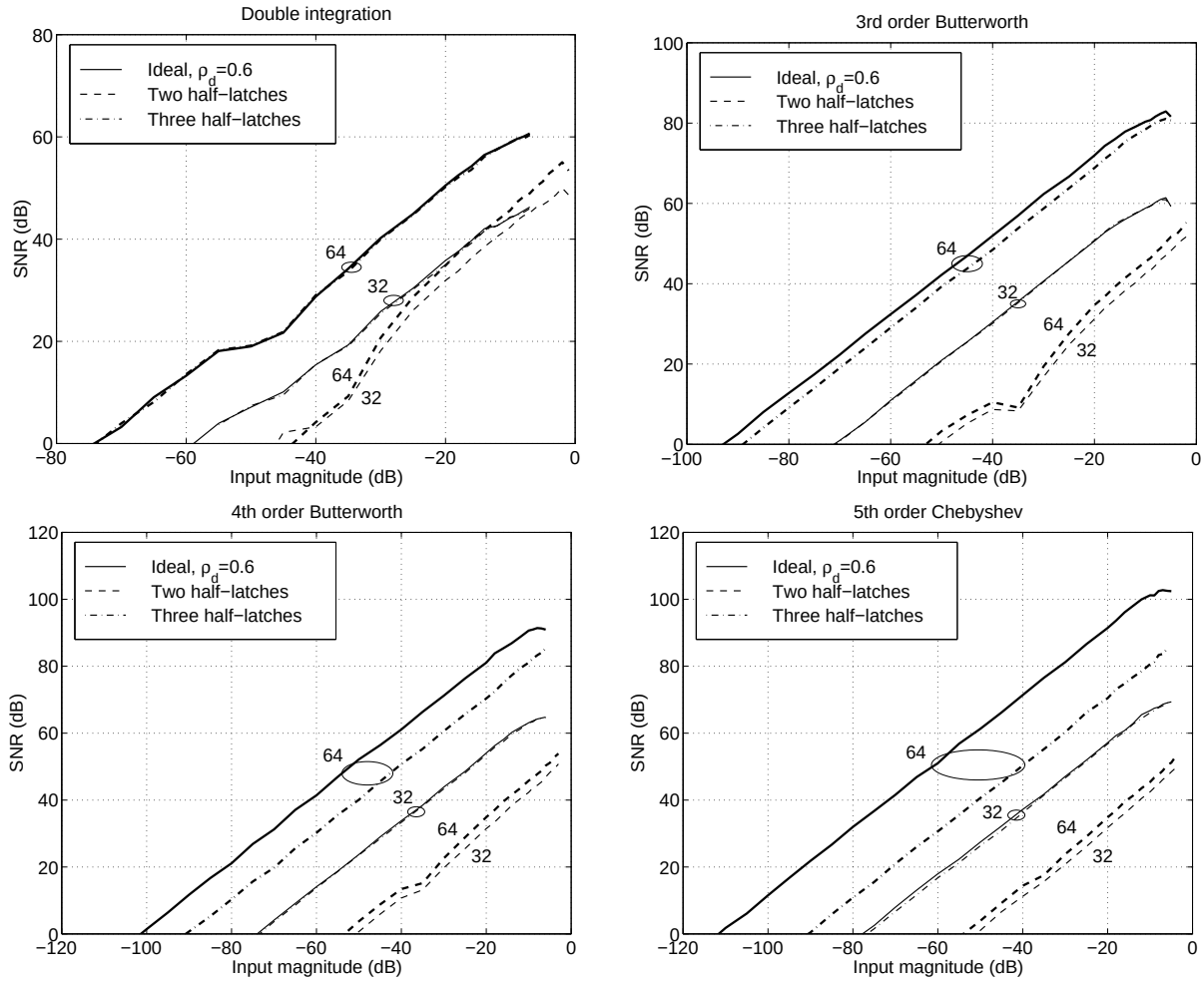


Figure 6.21: Dynamic range plots. Numbers on curves are OSR values.

high-order modulators with high OSR, the white noise resulting from metastability is what limits the achievable performance, though much less severely when with three rather than two half-latches. □

The idea of using a third latching stage "to provide additional regeneration" is mentioned in passing in [Jen95, p. 1123], though the claim that "the extra 1/2 delay does not have any impact on modulator performance" seems suspect given the first two rows of Table 6.1: we find a half-sample delay costs 12dB of DR in an ideal second-order CT $\Delta\Sigma$M. Adding a fourth latching stage will not usually be possible because stabilizing a CT $\Delta\Sigma$M with a full sample of delay probably cannot be accomplished through feedback tuning, but even the third stage is clearly highly advantageous for performance.

6.4.5 Other Modulator Architectures

The previous four subsections assumed LP $\Delta\Sigma$Ms with NRZ DACs, but we said in Chapter 4 and §5.2.2 that it is possible to build LP modulators with RZ DACs and BP modulators which use both RZ and HRZ DACs. An RZ DAC will be affected by metastability in much the same way as an NRZ DAC: the time when the rising edge begins will vary depending on v_x and v_{sl}. To make the latch output return to zero at $0.5T_s$ simply requires connecting the bases of the transistors in the dotted box in Figure 6.5 to the same node as their respective collectors; thus, the falling RZ edge is not affected by metastability. But given the same σ_{ms} in an NRZ vs. an RZ system, it will cause 3dB more noise in the RZ output spectrum because the same σ_{ms} appears twice as large relative to an RZ pulse (which is half the width of an NRZ pulse).

That being said, applying the ideas of the previous subsection is still worthwhile. In (5.15), we found the equivalent CT loop filter for a double integration modulator when the DAC has RZ pulses. We can do the same thing for a DAC with HRZ pulses, which results in

$$H(z) = \frac{-2z+1}{(z-1)^2} \leftrightarrow \begin{cases} \hat{H}(s) = \frac{-2.5s-2}{s^2}, & \text{RZ DAC} \\ \hat{H}(s) = \frac{-3.5s-2}{s^2}, & \text{HRZ DAC.} \end{cases} \tag{6.10}$$

We can build an HRZ DAC with an additional latching stage in Figure 6.5—and we learned in

§6.4.4 that adding such a stage greatly reduces DPW jitter caused by metastability. Thus, rather than building LP $\Delta\Sigma$Ms with RZ DACs, it behooves us to choose HRZ DACs.

BP modulators with a noise notch at $f_s/4$ have the property that there is a two-sample delay in the numerator of the loop filter $H(z)$, we learned in (4.33). If we choose the one digital delay BP architecture, then we need to insert a full sample of delay in the feedback path. This can be accomplished by using not one but *two* additional half-latches in Figure 6.5—and once again, the previous subsection showed adding half-latches provides immunity to metastability DPW jitter. Thus, any modulator with a two-sample delay in the numerator (which is the case for the BP $f_s/4$ modulators treated here) should be built with one digital delay in the feedback path. In *any* modulator with only a single sample of delay, HRZ-style DAC pulses are called for, as we noted in the previous paragraph for LP modulators.

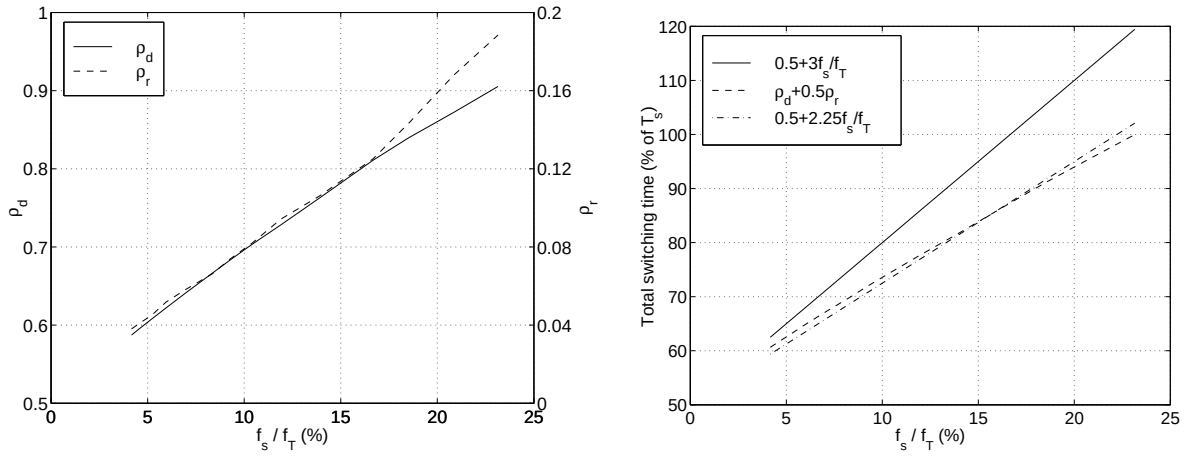
Using a multibit quantizer is intriguing because it appears to give a win: for an M-level quantizer, there are now $(M-1)$ regions around which metastability can occur but the distance between steps is smaller by a factor of $(M-1)$. DPW variance power is related to the square of this latter quantity, so it offsets the increase in number of metastability regions and appears to result in $10\log_{10}(M-1)$ dB smaller white noise power. This topic could benefit from future study.

6.5 Maximum Clocking Frequency

In our LP NRZ examples so far, we have been clocking at $f_s = 500$MHz in a $f_T = 12$GHz technology. A natural question arises: what is the maximum f_s at which it is safe to clock given a converter resolution specification?

As we increase f_s, two things together limit resolution. First, the transistor switching time starts to become a larger fraction of a clock period. This means the excess loop delay ρ_d and DAC pulse rise time ρ_r start to increase. There comes a point when excess loop delay makes the modulator completely unstable and impervious to stabilization through feedback coefficient tuning. Second, the metastability behavior of even the three half-latch comparator will start to degrade[2]. We study

[2]In §6.4.5 we suggested using half rather than full DAC pulses for LP modulators. While RZ LP $\Delta\Sigma$Ms remain



(a) (b)

Figure 6.22: (a) Effect of increasing f_s on ρ_d and ρ_r, (b) theoretical vs. measured switching time.

both of these issues in the following example.

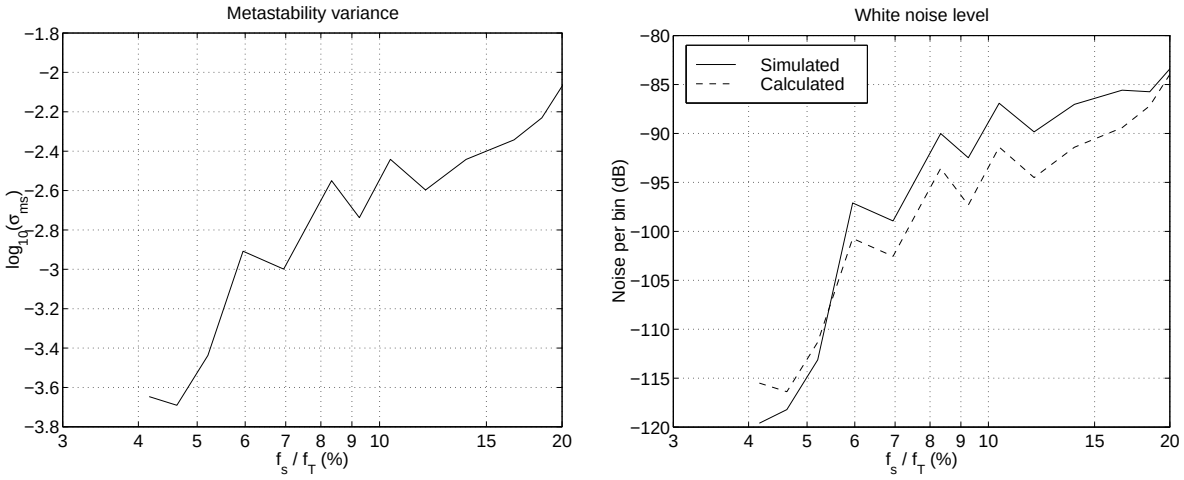
Example 6.12: Figure 6.22(a) shows how ρ_d and ρ_r change as we increase the clock speed of the three half-latch comparator from 500MHz to 2.5GHz. Returning to our crude formula for ρ_d in (4.12),

$$\rho_d \approx \frac{n_t f_s}{f_T}, \tag{6.11}$$

we see that it is somewhat pessimistic. First of all, ρ_d and ρ_r are both quite linear with f_s/f_T, as predicted by (6.11). Moreover, our circuit has $n_t = 3$ transistors in the feedback path (two followers and a differential pair), and so from (6.11) we expect them to have switched fully after

$$0.5 + \frac{n_t f_s}{f_T} = 0.5 + 3\frac{f_s}{f_T} \tag{6.12}$$

stable for more excess delay than NRZ LP $\Delta\Sigma$Ms, the worsening of performance due to metastability increases proportionally with f_s for both styles of modulator. As the following example shows, it is metastability that limits DR more than stability; thus, RZ $\Delta\Sigma$Ms have no performance advantage over NRZ $\Delta\Sigma$Ms at high clock speeds.



(a) (b)

Figure 6.23: Effect of increasing f_s on (a) σ_{ms}, (b) calculated and simulated noise level.

where the 0.5 is for the extra half-latch. In terms of ρ_d and ρ_r, full switching is accomplished after

$$\rho_d + 0.5\rho_r, \tag{6.13}$$

c.f. Figure 6.7. Figure 6.22(b) plots both (6.12) and (6.13); rather than using a factor of $n_t = 3$ in (6.12), a better fit is obtained with a factor of 2.25.

In any case, Figure 6.23(a) shows σ_{ms} as a function of f_s with both variables on a log scale. This was found from simulating the fifth-order LP NRZ modulator with feedbacks tuned for optimal DR at the given clock frequency over the range 500MHz to 2.5GHz, and finding the variance of the DPW histogram like the one in Figure 6.15(a). Using those same simulations with an OSR of 32 at clock frequencies from 500MHz to 2.5GHz yields the in-band white noise level per bin shown in Figure 6.23(b). This agrees to within 3dB with the calculated value from (5.13) where $N = 8192$, σ_β is found from (6.9), and $\sigma_{\delta y} \approx 1.1$ is found from simulation. The modulator goes unstable at $f_s = 2.5$GHz due to excess delay and no amount of feedback tuning seems to restore stability. □

We can use the data in Figure 6.23 to come up with an approximate rule of thumb for the

maximum performance achievable with a three-half latch quantizer assuming in-band noise is dominated by white noise due to metastability and $n_t = 3$ transistors in the feedback path. The calculation is shown in §A.2, and the results are equations (A.16) and (A.18):

$$\begin{aligned} \text{DR} &\geq 11.5 + 0.5\log_2 \text{OSR bits}, & f_s/f_T \leq 5\% \\ \text{DR} &\approx 8.5 + 0.5\log_2 \text{OSR} + \log_2 \tfrac{f_s/f_T}{5} \text{ bits}, & f_s/f_T \geq 6\%. \end{aligned} \tag{6.14}$$

This tells us that clocking slower than about 5% of f_T is recommended if we desire at least 14-bit performance with a reasonable OSR like 32 or 64; better performance can be achieved with a slower clock. Clocking faster than 5% or so of f_T means we are limited to 12-bit or worse performance at the same OSRs. We do not recommend clocking faster than $f_s = 0.2 f_T$ under any circumstances since stability will be questionable at best and nonexistent at worst at such high speeds.

In closing this section, we must comment further on (6.14). First, it gives an upper bound on DR: DR will be limited either by white noise due to metastability *or* quantization noise, depending on the OSR chosen. Second, it is not continuous: it has a jump between 5% and 6%. Third, the bound is not tight for $f_T/f_s < 5\%$: DR improves as we slow the clock down, though because of the semi-empirical nature of the calculations we can't easily extrapolate below this point. We estimate that metastability will have a negligible effect in most modulators when $f_T/f_s < 2\%$.

6.6 Summary

Quantizer metastability causes a variation in the width of the DAC pulses in a CT $\Delta\Sigma$M and degrades modulator performance by whitening the in-band noise in a very similar manner to clock jitter. A three half-latch quantizer design is recommended for reducing adverse metastability effects over a simple master/slave design. As was the case in Chapter 5, we have distilled our results into a pair of easy-to-apply equations (6.14). Using them tells us that metastability starts to become significant when clocking at more than about 5% of the maximum transistor switching speed, limiting modulator resolution to about 12 bits. Higher resolutions can be obtained by clocking more slowly.

Chapter 7

A 4GHz Fourth-Order Band Pass $\Delta\Sigma$M

Until this point, we have dealt with modulators on a fairly abstract and theoretical level. It would seem foolish not to supplement this work with some of the nitty-gritty practical issues in modulator design and testing. To this end, we present performance measurements on an actual fabricated fourth-order BP CT $\Delta\Sigma$M which clocks at $f_s = 4$GHz and has a center frequency of $f_0 = f_s/4 = 1$GHz. This will allow us to see how the work in the previous chapters applies to a real design *and* illustrate some additional practical considerations.

A block diagram of the circuit appears in Figure 7.1. The input voltage is fed through an input

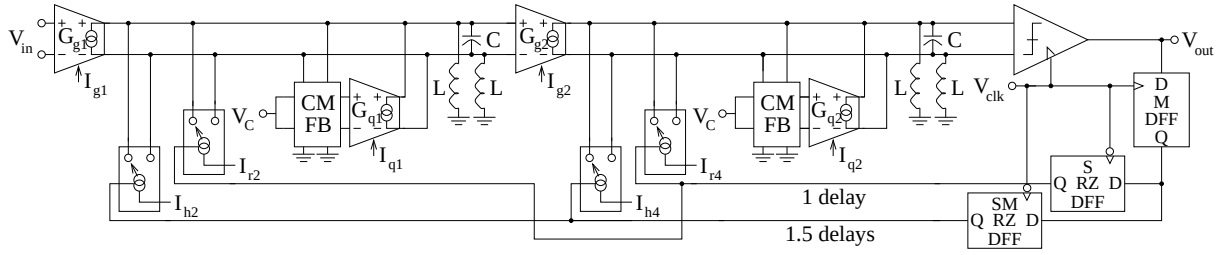


Figure 7.1: A 4GHz fourth-order BP CT $\Delta\Sigma$M.

transconductor G_g which produces a current $i_g = G_g v_i$ to drive an on-chip parallel LC tank. This gives the tank output voltage v_o a band pass shape:

$$V_o = I_G Z_{LC} = \frac{G_g V_i}{sC + 1/sL} = \frac{(G_g/C)s}{s^2 + 1/LC} V_i. \tag{7.1}$$

The resonator described by (7.1) is a second-order transfer function, so the series connection of two resonators yields a fourth-order modulator. The integrated inductor has a poor quality factor Q_L, so a Q-enhancement transconductor G_q is connected as a negative resistor to cancel the positive resistance of the inductor. Both the gain A_0 and the Q of the resonator Q_{res} are tunable. The quantizer and latches are such that this is a one digital delay multi-feedback architecture, and the DACs are simple tunable current switches where the feedback operates via KCL. All in all, the architecture is fairly reminiscent of Figure 4.1, only with resonators in place of integrators.

The intended application for this modulator is in a system like Figure 2.7: it is to be the IF filter in a 5GHz radio, where we convert the entire band to digital and sort out the components in the spectrum in software with DSP. It could, in theory, also be used as an RF converter in a 1GHz radio. This author wrote a paper on its performance and presented it at the 1998 Symposium on VLSI Circuits [Gao98a], but the circuit was designed by Weinan Gao. In this chapter, we give the circuit a much more detailed treatment than in that publication.

7.1 General Design Considerations

Before discussing this specific modulator, it is instructive to understand how we should go about choosing the parameters in a general $f_s/4$ BP design. We develop a procedure in this section which was not applied to the design of this modulator, but which could be applied to future designs.

A simplified single-ended model of the modulator appears in Figure 7.2[1]. The design problem may be stated roughly as follows: given that we desire a certain center frequency, OSR, and SNR, how do we choose the parameters L, C, R, G_g, G_q, k_2, and k_4? We must recognize immediately that it is more or less mandatory to operate an LC-style resonator at $f_0 \geq$ 1GHz since on-chip inductors tend to have Qs that are poor below this frequency. That being said, let us discuss the other constraints on the parameters.

[1]We have renamed some of the parameters (e.g., the feedback ks) so they are consistent with what was used in this design, but inconsistent with earlier naming. Moreover, there is a mild notational conflict in this section with the feedback ks and k for Boltzmann's constant. The author apologizes for both of these.

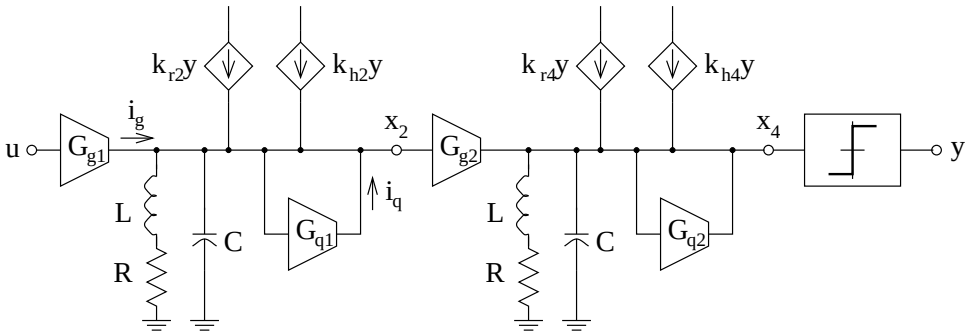


Figure 7.2: Approximate single-ended model for modulator.

7.1.1 Element Parameter Selection

In §3.1.5 we noted that the first stage of a modulator is usually the most important part to design well because nonlinearities and nonidealities here appear immediately at the input. It should come as no surprise, then, that the first circuit component which constrains the design of Figure 7.2 is the input transconductor G_{g1}. The minimum detectable input voltage u_{min} for the whole modulator is determined by the input-referred noise of G_{g1} while the maximum voltage u_{max} is constrained by its linearity. Let us derive approximate expressions for each to find which parameters are important.

We start with a series/parallel tank transformation as follows. The resistor $R_s = R$ on the left of Figure 7.3 represents the finite Q_L of the inductor,

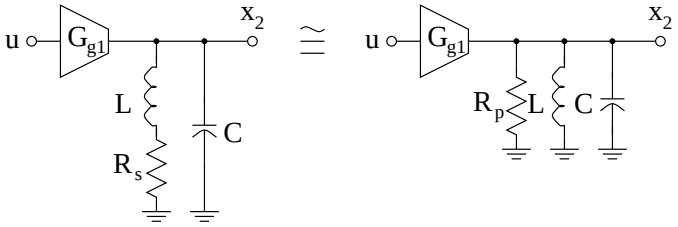


Figure 7.3: Series/parallel tank equivalence near resonance.

$$Q_L = \omega_0 L/R. \tag{7.2}$$

It can be shown [Lee98, §4.4] that over a suitably-restricted frequency range near resonance, the series LR circuit with a parallel C is approximately equivalent to a purely parallel RLC circuit as

on the right of Figure 7.3 when

$$R_p = R_s(Q_L^2 + 1),\ L_p = L_s\left(\frac{Q_L^2 + 1}{Q_L^2}\right). \tag{7.3}$$

This is useful because at resonance, the impedances of L and C cancel in the parallel RLC circuit leaving only R_p. Next, we assume that G_{q1} is tuned such that it makes a resistance $-R_p$ to ground as depicted in Figure 7.4. This is desirable because once again, at resonance, the positive and

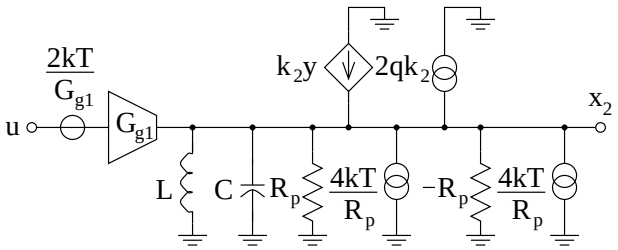


Figure 7.4: Input transconductor equivalent circuit for noise considerations.

negative R_ps cancel which means we will have an infinite resonator Q and hence an infinitely-deep notch in the quantization noise. It now becomes possible to write expressions for the noise currents of each resistor and the feedback DAC as depicted in the figure. The resistors have noise current densities $4kT/R_p$ A^2/Hz, and assuming the DAC is a bipolar transistor with collector current $I_c = k_2$, its noise current density will be of the form $2qk_2$ A^2/Hz [Gra93, Chap. 11]. All these currents drive x_2 from ground, and therefore they may be referred to the input by dividing them by G_{g1}^2, whence they become noise *voltage* densities. Lastly, the input transconductor itself has a certain input-referred noise voltage density, and if we assume once again that it is a bipolar-based circuit we may write its noise voltage density as $2kT/G_{g1}$ V^2/Hz. Finally, then, all the noise voltages at the input are uncorrelated, so we add them to get a total input noise voltage density of

$$\overline{v_{ng1}^2} = \frac{2kT}{G_{g1}} + \frac{2qk_2}{G_{g1}^2} + \frac{8kT\omega_0 C}{G_{g1}^2 Q_L}\ \text{V}^2/\text{Hz} \tag{7.4}$$

where we have used the fact that $R_p \equiv Q_L/(\omega_0 C)$. This noise density is a mild function of frequency because transistor noise currents are frequency-dependent; we treat it as white in the (narrow) signal band. The total in-band noise voltage is, by definition, the minimum detectable

signal

$$u_{min} \equiv \sqrt{\overline{v_{ng1}^2}} \times \frac{f_s}{2 \cdot \text{OSR}}. \tag{7.5}$$

Immediately we see from (7.4) that in order to be able to detect small signals, we wish for G_{g1} to be *large*. Our first design constraint, therefore, is to make G_{g1} "large enough" to have small in-band noise. In general, transconductance is related to current; in a bipolar design, large G_{g1} means large current i_{g1} supplied to G_{g1} and hence high power dissipation. As usual, low noise (and thus high DR) can be achieved at the expense of power.

How large is large enough? That is determined by the required SNR, which in turn fixes the needed linearity of G_{g1}. Clearly, the maximum signal that must be handled with acceptable linearity is

$$u_{max} = u_{min} \times 10^{\text{SNR}/20}. \tag{7.6}$$

To quantify this, let us assume the linearity of G_{g1} has been characterized by a standard measure such as input-referred third-order intercept point IIP_3. Let us further assume that it is a differential circuit with a weak cubic nonlinearity described by

$$i_{g1} = G_{g1}u - \epsilon_{g1}u^3, \tag{7.7}$$

quite a reasonable assumption for an integrated transcondcutor. (7.7) can be solved to yield

$$\text{IIP}_3 \text{ for } G_{g1} \equiv \sqrt{\frac{G_{g1}}{\epsilon_{g1}}}. \tag{7.8}$$

The linearity requirement for G_{g1} is then straightforward to state: at u_{max}, we require harmonics to be at least SNR dB below the fundamental. A simple geometrical argument says that we require

$$\text{IIP}_3 \text{ for } G_{g1} = 20 \log_{10} u_{max} + \text{SNR}/2 \text{ dB} \tag{7.9}$$

because the third harmonic has a slope 3dB/dB with u while the linear term has a slope 1dB/dB.

So far, our first consideration is the design of the input transconductor. It must have sufficient dynamic range (i.e., sufficiently low noise and sufficiently high linearity) to meet our SNR requirements. Higher dynamic range usually requires greater power dissipation.

Continuing in this vein, it is illustrative to write an expression for SNR using the following fact: in order to keep the modulator stable, the feedback current must be at least as large as the maximum input current. Recalling that the DAC current is $k_2 \equiv k_{r2} + k_{r4}$, we may write

$$k_2 \geq u_{max} G_{g1}. \tag{7.10}$$

Put another way, we require

$$u_{max} \leq \frac{k_2}{G_{g1}} \tag{7.11}$$

where u_{max} is the full-scale input voltage. Assuming we choose k_2 no larger than necessary, the inequality in (7.10) and (7.11) becomes an equality, and therefore the signal power is $(k_2/G_{g1})^2$. We wrote an expression for the integrated noise power in (7.5); combining this with (7.11) and simplifying leads to

$$\text{SNR}_{\text{max}} = \frac{k_2^2}{kTG_{g1}f_N(1 + \frac{k_2}{i_{g1}} + \frac{4}{Q_L}\frac{\omega_0 C}{G_{g1}})} \tag{7.12}$$

where f_N is the Nyquist bandwidth and we have used the fact that small-signal $g_m \equiv I_c/V_T$ and hence $G_{g1} = i_{g1}/(kT/q)$ for a bipolar transistor. This expression shows that the noise is made up of the sum of three components; the one that dominates will depend on the actual design. One of the interesting insights this equation offers us is that even if G_{g1} and the DAC were noiseless, SNR would still be limited by finite Q_L. If Q_L is poor, then we need either high G_{g1} or low C to ensure that the third denominator term does not dominate; thus, poor inductor Q either increases our power dissipation or constrains our choice of capacitor size.

To understand how to pick tank component values and the G_qs, we write an expression for x_2 in Figure 7.2. Assuming the G_{q1} transconductor draws negligible current (reasonable for a bipolar design), we may write an equation for the first resonator output X_2

$$\begin{aligned} X_2 &= [I_g + I_q + k_2 Y] Z_{eq} \\ &= [G_{g1}U + G_{q1}X_2 + k_2 Y] \frac{1}{\frac{1}{sL+R} + sC}. \end{aligned} \tag{7.13}$$

Solving for X_2 gives

$$X_2 = [G_{g1}U + k_2 Y] \frac{\frac{1}{C}s + \frac{R}{LC}}{s^2 + (\frac{R}{L} - \frac{G_{q1}}{C})s + \frac{1}{LC}(1 - RG_{q1})}. \tag{7.14}$$

A similar equation could be written for x_4 in terms of x_2 and the second resonator parameters. Recalling that the center frequency of a band pass transfer function is determined by the coefficient of the s^0 term in the denominator and assuming for the moment that RG_{q1} is small, we arrive at the design constraint

$$\omega_0 \approx \frac{1}{\sqrt{LC}}. \tag{7.15}$$

Choosing one of L or C then fixes the other according to (7.15). Usually, the inductor series resistance R is given once L is known because one has little control over integrated inductor Q. A deep noise-shaping notch requires a high-Q resonator; the rule of thumb we gave in §3.1.1 was that

$$Q_{res} \approx \text{OSR}. \tag{7.16}$$

Integrated inductor Qs typically range from 5 to 10, hence we require Q-enhancement of some kind which as we have said is provided by the G_{q1} transconductor. From (7.14), a high-Q resonator has a denominator s^1 coefficient of near 0; thus, we need

$$\frac{R}{L} - \frac{G_{q1}}{C} \approx 0. \tag{7.17}$$

G_{q1} may now be found because it is the only unknown in (7.17), and G_{q2} may be found in a similar manner. What are some of the considerations for how we should choose L and/or C? (7.12) shows that small C is good for noise. But smaller C means larger L, which for an integrated inductor means larger die area. As well, we can only reduce C so much before parasitics start to become significant. If Q_L is a function of L, then instead of choosing C it may be more sensible to choose L so that Q_L is maximized.

Thus far, we have chosen all the parameters except the feedback DAC currents and G_{g2}. Our choices of these depend on two things: achieving the correct noise-shaping transfer function and the linearity of the the transconductors other than G_{g1}.

Addressing the first issue, recall the CT/DT equivalence in Chapter 4 and 5: in this section we are discussing building a one digital delay $f_s/4$ fourth-order BP modulator which has

$$H_{BP}(z) = z^{-1}\frac{2z^{-1} + z^{-3}}{(1 + z^{-2})^2} \tag{7.18}$$

from (4.33). Using the parameter names in this section, the values of the feedback DAC levels in the CT circuit to give the correct equivalent $H_{BP}(z)$ can be shown to be

$$(\bar{k}_{r2}, \bar{k}_{r4}, \bar{k}_{h2}, \bar{k}_{h4}) = (-1.1107\frac{C}{G_{g2}T_s}\frac{C}{T_s}, -0.9957\frac{C}{T_s}, +2.6815\frac{C}{G_{g2}T_s}\frac{C}{T_s}, +4.6927\frac{C}{T_s}) \quad (7.19)$$

(the reason for the bars over the names will be explained shortly). C and T_s have already been determined, so $\bar{k}_{r4}$ and $\bar{k}_{h4}$ are now known. Moreover, the sum $\bar{k}_2 \equiv \bar{k}_{r2} + \bar{k}_{h2}$ is known from (7.10). The only remaining unknown is thus G_{g2}, which is found to be

$$G_{g2} = \frac{\pi/2}{\bar{k}_2}\frac{C^2}{T_s^2}. \quad (7.20)$$

It appears that the design is now complete, except there is one remaining detail: the second issue above, i.e., the linearity of the other transconductors. Let us consider it now.

When the modulator is operating, the voltages at x_2 and x_4 are stochastic in nature with standard deviations σ_{x_2} and σ_{x_4}. It is not difficult to see that these values are directly proportional to the feedback current levels: driving more DAC current into x_2 and x_4 produces proportionally more voltage across the (fixed) tank impedance. The $\bar{k}$s above are nominal currents; let us make the actual currents be scaled by γ_k, so that

$$(k_{r2}, k_{r4}, k_{h2}, k_{h4}) = (\gamma_k\bar{k}_{r2}, \gamma_k\bar{k}_{r4}, \gamma_k\bar{k}_{h2}, \gamma_k\bar{k}_{h4}). \quad (7.21)$$

With this scaling applied, it is found from simulation that with no input signal,

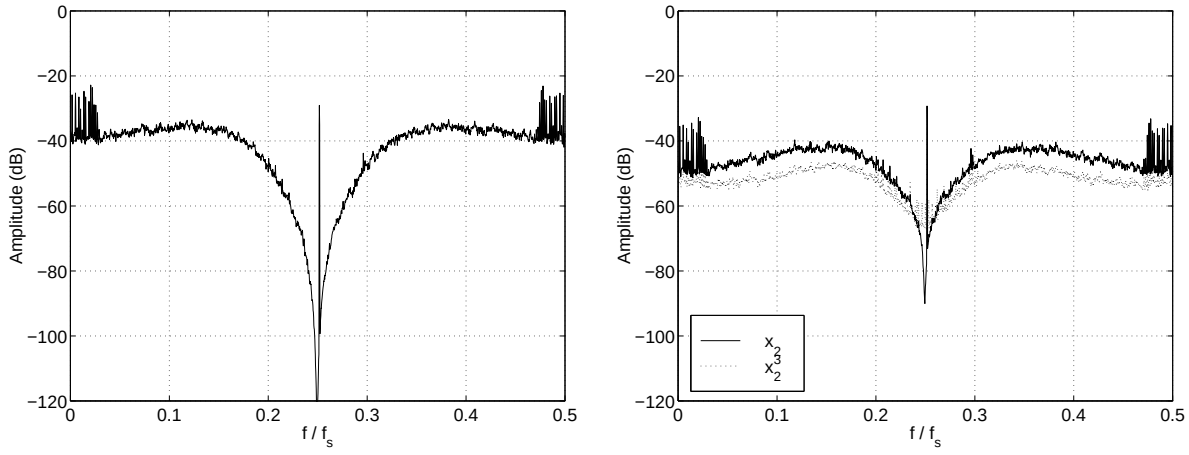
$$(\sigma_{x_2}, \sigma_{x_4}) \approx (\frac{1}{\sqrt{2}}\frac{C}{G_{g2}T_s}\gamma_k, 1.157\gamma_k) \quad (7.22)$$

which are values in volts. The proper scaling for G_{g2} is

$$G_{g2} = \frac{\pi/2}{k_2}\frac{C^2}{T_s^2}\gamma_k \quad (7.23)$$

where k_2 is from (7.10). x_2 drives G_{q1} and G_{g2} while x_4 drives G_{q2}, so it stands to reason that there must be a way to relate the linearity requirements of G_{q1} and G_{g2} to the typical level of x_2, i.e., σ_{x_2}, and to relate the linearity of G_{q2} to σ_{x_4}.

As before, suppose these three transconductors have known IIP_3 with a form similar to (7.8). It is not immediately apparent how to treat them because they are driven by stochastic wideband



(a) (b)

Figure 7.5: Spectrum of (a) output bits, (b) x_2 and x_2^3.

signals rather than sinusoids. To make matters more confusing, G_{q1} and G_{q2} have the same output and input node. But one way to grasp what nonlinearity does is to write out the time-domain differential equations for the states. For simplicity, assume G_{q1} is the only nonlinear transconductor and that $R = 0$. The coupled first-order equations for x_2 can be written as

$$\frac{dx_1}{dt} = \frac{1}{LC}x_2, \ \frac{dx_2}{dt} = -x_1 + \frac{1}{C}\left[G_{g1}u + \epsilon_{q1}x_2^3 + k_2 y\right] \tag{7.24}$$

If $\epsilon_{q1} = 0$, the term inside square brackets describes normal modulator operation: the input u is combined with the fed-back output bit y and the amplitude of u in the spectrum of y is determined from k_2/G_{g1}. Viewed in this light, for $u = 0$, we have the fed-back output y combining with x_2^3. By analogy to the $\epsilon_{q1} = 0$ case, we can think of x_2 as though it is acting like an input. Therefore, by analogy, we expect the spectrum of x_2^3 to appear in the spectrum of y with a ratio involving k_2/ϵ_{q1}. Figure 7.5(a) shows a typical output spectrum, whereas Figure 7.5(b) shows the spectra of the voltage at x_2 and x_2^3 for the same input conditions. From simple theory, the spectrum of x_2^3 is the spectrum of x_2 convolved with itself twice. This means some of the out-of-band noise will fold in-band, but how much?

The best way to characterize it turns out to be with *normalization*. If we plot the DR and

SNR_{max} from simulation as a function of normalized ϵ_{q1},

$$\bar{\epsilon}_{q1} \equiv \frac{\epsilon_{q1}\sigma_{x_2}^3}{k_{r2}+k_{h2}}, \tag{7.25}$$

the graphs appear as in Figure 7.6(a) and look the same for a given OSR. The form of $\bar{\epsilon}_{q1}$ is logical given (7.24). Similar normalizations can be found for the other two nonlinear parameters:

$$\bar{\epsilon}_{g2} \equiv \frac{\epsilon_{g2}\sigma_{x_2}^2}{G_{g2}}, \tag{7.26}$$

$$\bar{\epsilon}_{q2} \equiv \frac{\epsilon_{q2}\sigma_{x_4}^3}{k_{r4}+k_{h4}}. \tag{7.27}$$

Graphs of DR and SNR_{max} are plotted in Figures 7.6(b) and (c). From these graphs, we may derive the following rules of thumb for the restrictions on the $\bar{\epsilon}$s that will not affect DR significantly:

$$\bar{\epsilon}_{q1} < 10^{-3},\ \bar{\epsilon}_{g2} < 10^{-2},\ 10\log_{10}\bar{\epsilon}_{q2} < -5 - \log_2 \text{OSR}. \tag{7.28}$$

The final portion of the design procedure can now be described. The nominal feedbacks $\bar{k}$s and signal levels σ_xs are found from the other known parameters by using (7.23) for G_{g2} followed by (7.21) and (7.22), where to start we assume $\gamma_k = 1$. The IIP_3 for the transconductors other than G_{g1} are characterized, and the normalized $\bar{\epsilon}$s are calculated and compared with (7.28). If they are large enough that linearity is a problem, then γ_k can be lowered and the calculation redone. We should also keep in mind that we can also alter the signal levels σ_{x_2} and σ_{x_4} by altering the tank impedance if changing γ_k is found to be unsatisfactory. Lowering γ_k also lowers power consumption.

7.1.2 Design Procedure

We summarize the salient points of our design method here. Take as given center the frequency f_0 ($f_0 = \omega_0/2\pi = f_s/4$), SNR (assumed equal to DR), and conversion bandwidth $f_N/2 = f_s/(2 \cdot \text{OSR})$.

For the input transconductor:

$\rightarrow$ Design the circuit and find the achieved G_{g1} and ϵ_{g1} in (7.7)

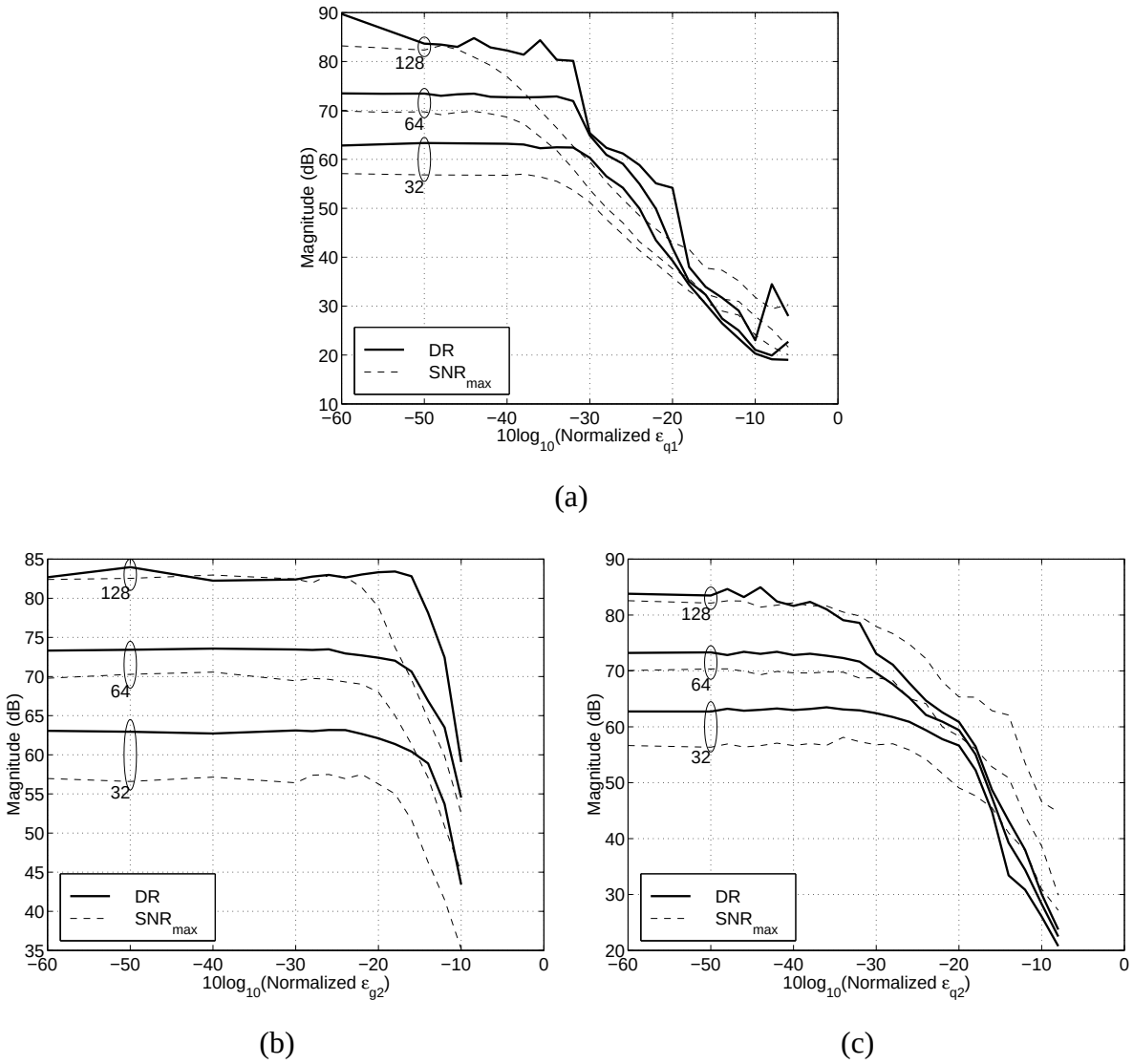


Figure 7.6: DR and SNR_{max} for (a) $\bar{\epsilon}_{q1}$, (b) $\bar{\epsilon}_{g2}$, (c) $\bar{\epsilon}_{q2}$. Numbers on curves are OSR values.

→ Use SPICE to find the total input-referred noise voltage over the Nyquist band

→ Calculate u_{min} from (7.5), u_{max} from (7.6)

→ Ensure IIP_3 satisfies (7.9)

For the tank parameters:

→ Calculate first feedback current k_2 from (7.10)

→ Calculate L and C product from (7.15)

→ Determine inductor series resistance

→ Calculate required G_{q1} and G_{q2} from (7.17)

→ With DAC and G_{q1} circuits present, resimulate input-referred noise in SPICE and ensure input transconductor still has necessary dynamic range

For the feedback DAC levels and other transconductors:

→ Calculate required G_{g2} from (7.23)

→ Calculate nominal $\bar{k}$s and σ_xs from (7.21) and (7.22) using $\gamma_k = 1$

→ Design the other transconductors to meet G_q and G_{g2} specs and find the achieved ϵ_q and ϵ_{g2}

→ Calculate normalized $\bar{\epsilon}$s from (7.25)–(7.27)

→ Check if performance loss is significant with (7.28) and adjust γ_k and/or tank impedances appropriately

Of course, application of this procedure will involve a good deal of iteration. Note that we recommend SPICE or some other full-circuit simulator for noise measurements; our estimates in (7.4) and (7.12) are only very approximate.

7.1.3 Parameters for This Design

The circuit we present in the rest of this chapter was designed long before this procedure was formalized. Before we describe the circuit, it is interesting to see how its parameters look. They

Table 7.1: Parameters for the fourth-order design in this chapter.

Tank element values		$L = 3.5$nH
		$C = 6.1$pF
		$R = 2.45\Omega$
G_g	Range	$2 \rightarrow 8$ mA/V
ϵ_g	Typical	$9{\times}10^{-3}$ mA/V^3
G_q	Range	$2 \rightarrow 9$ mA/V
	For $Q = \infty$, calc	4.3mA/V
	For $Q = \infty$, meas	8.9mA/V
ϵ_q	Typical	$5{\times}10^{-4}$ mA/V^3
k_r, k_h	Range	$0 \rightarrow 500$ μA
σ_{x_2}, σ_{x_4}	Range	$4 \rightarrow 12$ mV
$\overline{v_{ng1}}$	Calc (typical)	3.5nV/$\sqrt{\text{Hz}}$
	Sim (typical)	20nV/$\sqrt{\text{Hz}}$
u_{min}	Typical	90μV
G_{g1} IIP$_3$	Sim	-2.3dBV
$\bar{\epsilon}_{q1}$	Maximum	$2.3 \times 10^{-6} = -56.4$dB
$\bar{\epsilon}_{g2}$	Maximum	$1.8 \times 10^{-4} = -38.5$dB
$\bar{\epsilon}_{q2}$	Maximum	$2.6 \times 10^{-6} = -55.8$dB
SNR limit	u_{min}, IIP$_3$	52dB

are presented in Table 7.1 for a bandwidth of 20MHz, which corresponds to OSR $= 100$, and typical biasing conditions. Their derivations will follow in later sections. There are several things worth noting about them.

1. The inductors have a Q of about 8 according to SPICE, so the G_q value required to achieve $Q = \infty$ is 4.3mA/V when calculated from (7.17). In measurements, from Figures 7.34(b) and B.2(b), the value comes out closer to 9mA/V. We discuss possible reasons for this in §7.4.3.

2. SPICE measures typical in-band noise voltage densities of 20nV/$\sqrt{\text{Hz}}$ while our simple

formula (7.4) predicts 3.5nV/$\sqrt{\text{Hz}}$. However, test indicate both SPICE and our formula predict the same dominant term: the noise seems to come mostly from the DAC, the middle term in (7.4).

3. The swing at the resonator outputs σ_{x_2} and σ_{x_4} can be made only as high as about 12mV because the DAC currents were chosen very small in this design. As a result, when we find the normalized $\bar{\epsilon}$ values and compare them to (7.28), it happens that none of them are large enough to affect DR appreciably at OSR $= 100$.

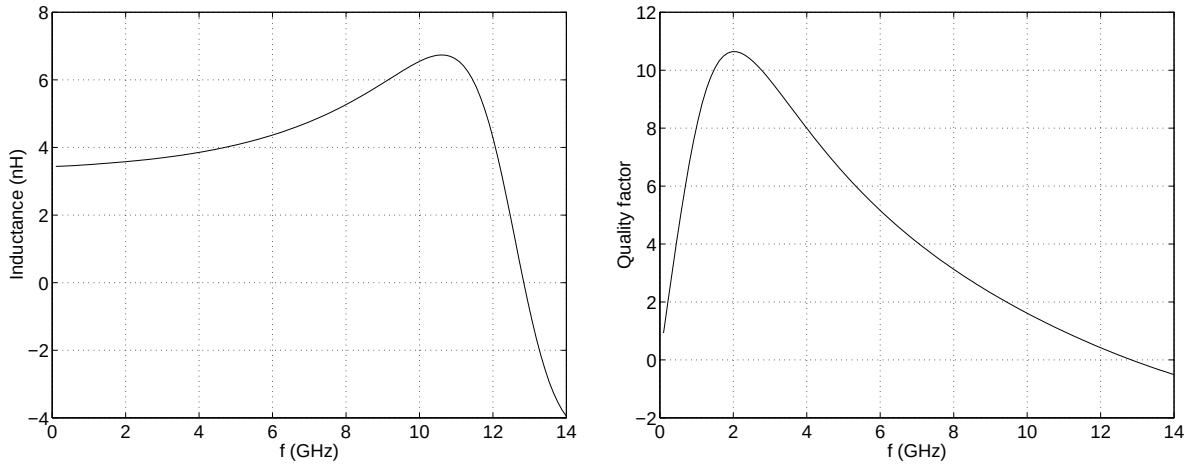
4. The input-referred noise for G_{g1} is quite large, typically 20nV/$\sqrt{\text{Hz}}$, which in a 20MHz bandwidth gives a minimum-detectable input signal of $u_{min} = 90\mu$V. The linearity of that transconductor is such that IIP$_3 = -2$dBV or so, and calculation with (7.6) and (7.8) gives a maximum SNR of 52dB.

At the outset, our simple formulae predict we will not do better than SNR $= 52$dB which means this is just over an 8-bit ADC. Let us study the circuit more closely, however.

7.2 Circuit Blocks

The circuit is built in a 0.5μm SiGe BiCMOS process, though it is an all-bipolar design and so only uses the HBTs of the process. These are rated at speeds of approximately $f_T = 40$GHz and $f_{max} = 60$GHz. It should be stressed once again that the author did not design this circuit—there were no notes to be found on it, so everything written in this chapter is based largely on inference and a scant few conversations with the designer. The circuit *does* function, so it is useful to study. Let us describe each circuit block at the transistor level[2].

[2]Until now we have specified input levels in dB, which as we noted in Chapter 2 is dB relative to full scale. In this chapter, because this is a real circuit with an input voltage, we talk about input levels both in V and (because the circuit is intended for a radio receiver) dBm assuming a 50Ω impedance. The one place we refer to dB, Figure 7.44, still uses dB relative to full scale, and we calculate the full-scale input level in §7.3.1.



(a) (b)

Figure 7.7: SPICE ac analysis of inductor: (a) L, (b) Q.

7.2.1 Resonator

Before proceeding to the final resonator circuit, it is useful to break it down into separate components.

Single-ended block diagram

The model in Figure 7.2 approximates the resonator quite well. A lumped-element equivalent circuit for each on-chip inductor half-circuit can be derived from the physical inductor layout which includes metal resistance, inter-turn capacitance, capacitance through the dielectric to the substrate, etc. A SPICE ac analysis of the lumped equivalent produces the characteristics in Figure 7.7. The inductor's nominal value at $f_s/4 = 1$GHz is $L = 3.5$nH with a Q of about 8.1, and its self-resonant frequency is about 12.8GHz. This means the series resistance is about $R = 2.45\Omega$; it mildly frequency-dependent, but in simulation the dependence is weak enough that we may consider R to be constant. C is actually two 1.525pF capacitors in parallel with each other with both ends connected to either collector of a differential pair. Thus, the equivalent capacitance to ac ground is $C = 6.1$pF, four times this value.

Transconductor

Both input and Q-enhancement transconductors are so-called *multi-tanh* circuits [Gil98] whose operation can be understood starting with the simple differential pair in Figure 7.8. A differential

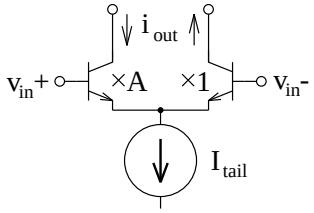
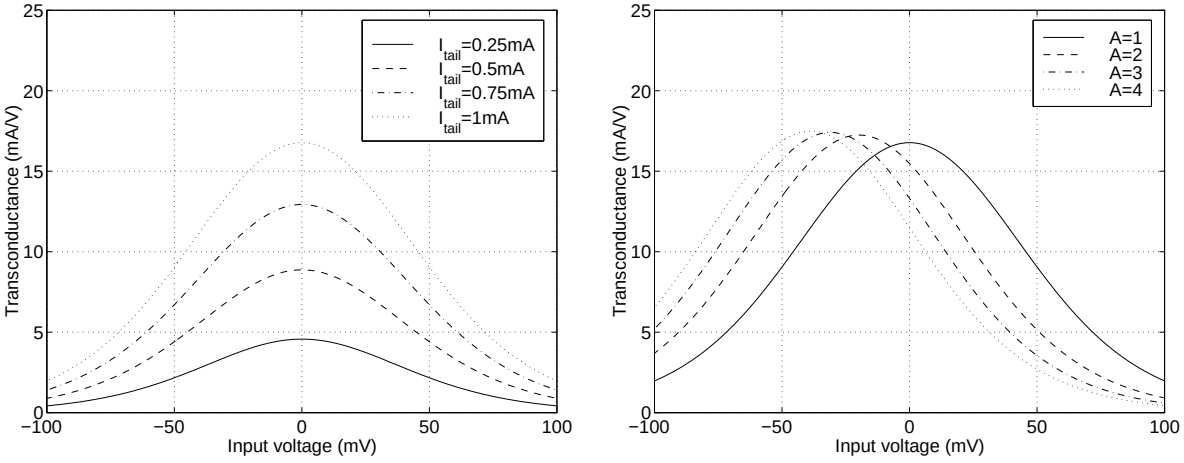


Figure 7.8: Differential pair transconductor.

input voltage v_{in} becomes a differential output current i_{out} with a hyperbolic tangent characteristic [Gra93, Chap. 3]; the transconductance $G_m \equiv di_{out}/dv_{in}$ thus has a sech^2 shape. Figure 7.9(a) shows how the G_m vs. v_{in} curve varies as a function of tail current I_{tail} for $A = 1$: we can increase the peak G_m by increasing I_{tail}. The input range over which the circuit is linear can be improved by first unbalancing the differential pair, where A transistors are connected in parallel on one side (effectively creating a transistor whose emitter is A times larger). This has the effect of shifting the peak of the G_m vs. v_{in} curves as illustrated in Figure 7.9(b). Next, unbalanced pairs have their outputs cross-coupled, Figure 7.10, which results in the overall G_m characteristic having a double-hump shape, Figure 7.11(a). The horizontal shift of the G_m curves is altered by changing A, and we also have the option of adding small emitter resistors R_e to further change the shape of the individual pairs' G_m curves, Figure 7.11(b). By correctly choosing A and R_e, we can get a flat top on the final G_m vs. v_{in} curve. This is what gives us the desired increase in linear range.

The main advantage of using a multi-tanh circuit for linearity over a differential pair with emitter degeneration is that the latter has a fixed transconductance, while in the former G_m is tunable with I_{tail} while retaining good linearity. Furthermore, the increase in noise suffered by using two pairs of transistors and two tail current generators (instead of one of each in a simple diff pair) is more than made up for by the increase in 1dB compression point—multi-tanh circuits have higher DR than degenerated differential pairs when both noise and linearity are taken into account.



(a) (b)

Figure 7.9: Transconductance of differential pair as a function of (a) tail current, (b) number of transistors.

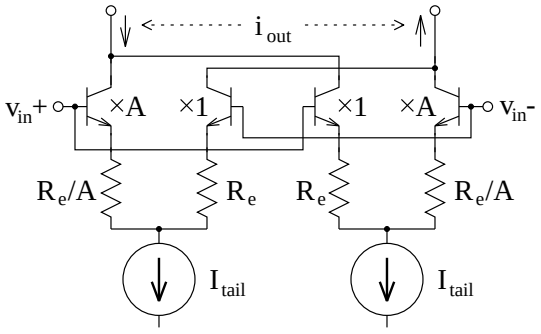
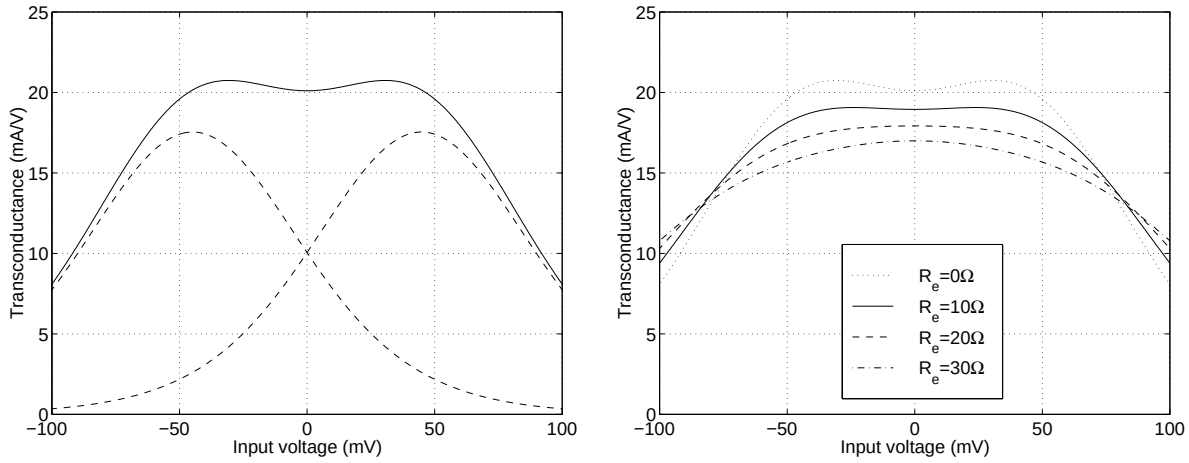


Figure 7.10: Multi-tanh circuit.



(a) (b)

Figure 7.11: (a) Multi-tanh G_m characteristic, (b) effect of varying R_e.

Input transconductor

The actual multi-tanh topology used in this architecture is depicted in Figure 7.12. In place of

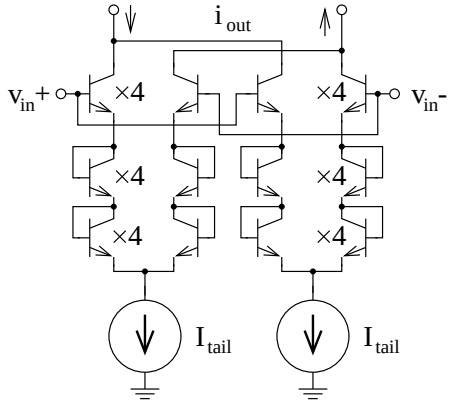
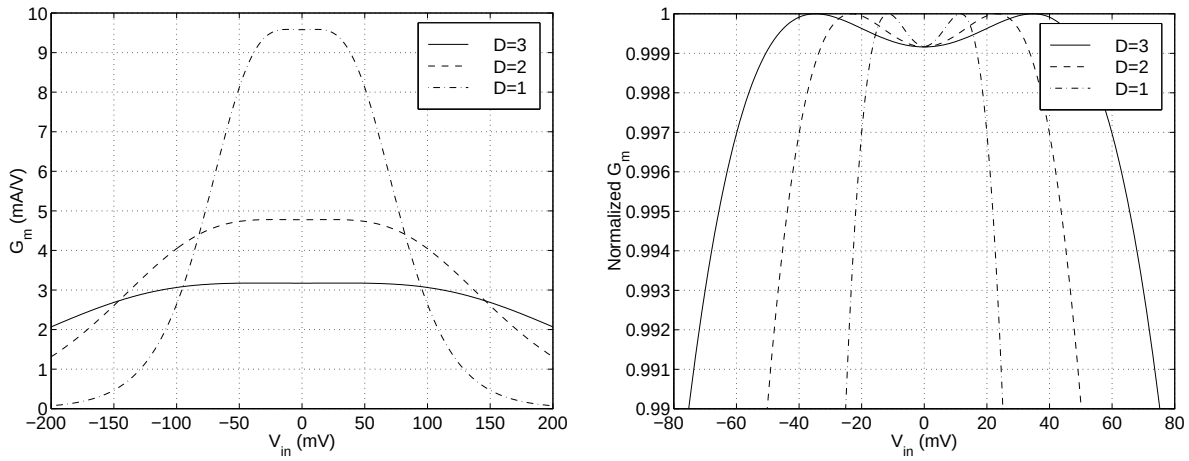


Figure 7.12: Actual transconductance topology used.

resistors, diode-connected transistors are used. Between the input and ac ground, we have $D = 3$ diodes formed by base-emitter junctions; what are the ramifications of employing this configuration over $D = 1$ as in the original multi-tanh design in Figure 7.10 or $D = 2$?

Example 7.1: Let us study the circuit in Figure 7.12 with 500Ω load resistors



(a) (b)

Figure 7.13: Transconductance as a function of number of diodes: (a) absolute, (b) normalized to peak G_g.

on the collectors of the input transistors going to $V_{CC} = 5$V. We will use an input common-mode (CM) level of 3.4V, which is about what the actual level in the final modulator is.

For $I_{tail} = 0.4$mA, Figure 7.13(a) plots G_g vs. V_{in} from a SPICE dc analysis for $D = 1$, 2, and 3 base-emitter diodes. G_g falls from 9.40mA/V to 4.70mA/V and 3.68mA/V: it is inversely proportional to D. At the same time, the linear range in Figure 7.13(b) increases proportionally to D: a 1% drop in G_g happens at $V_{in} = 25$mV, 50mV, and 75mV. This behavior is easily understood by considering the series connection of D identical diodes with the same current I and voltage V across their terminals, Figure 7.14. The current through each diode is the same and is given by

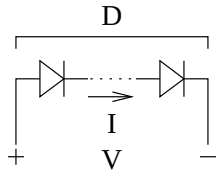
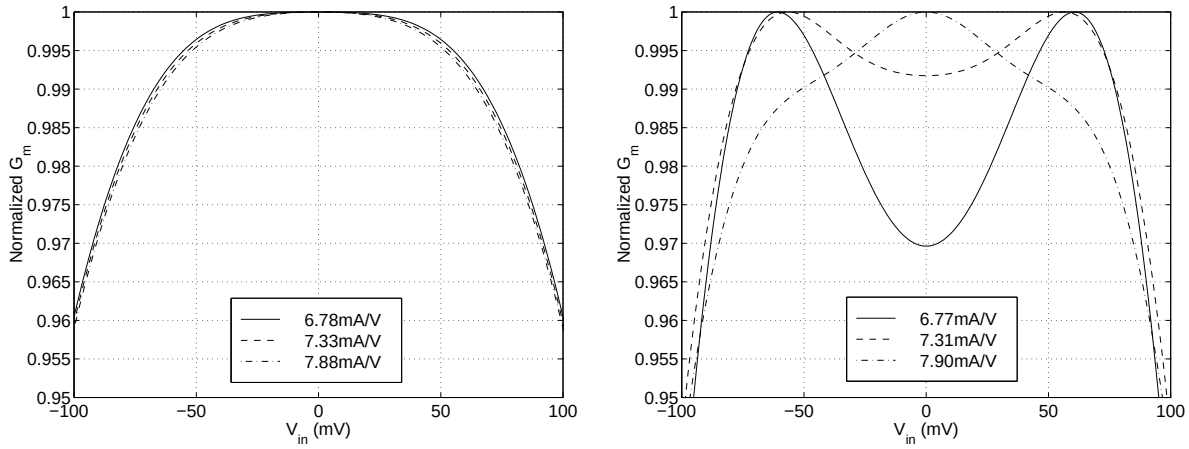


Figure 7.14: Series-connected diodes.



(a) (b)

Figure 7.15: Linearity for emitter diodes vs. emitter resistors: (a) $A = 4$, $D = 3$, (b) $A = 8$, $R_e = 100\Omega$.

$$I = I_s \exp\left(\frac{V/D}{kT/q}\right) \tag{7.29}$$

because the voltage across each diode is V/D. The small-signal transconductance is found from

$$g_m = \frac{dI}{dV} = \frac{I_s}{D(kT/Q)} \exp\left(\frac{V/D}{kT/q}\right) = \frac{1}{D}\frac{I}{kT/q}. \tag{7.30}$$

The transconductance G_g above falls because of the $1/D$ factor in front of (7.30), and the linear range increase arises because of the V/D inside the exponential.

The advantage of using diodes rather than passive resistors should be clear: the g_m for a diode is proportional to I_{tail}, but for a passive resistor g_m is fixed. This explains why in Figure 7.15, which contrasts the two cases for similar G_g and I_{tail}, the linearity is retained as G_g is varied in the diode case but not in the resistor case.

A fair comparison of the D choices includes several parameters: the realizable range of G_g values, I_{tail} per G_g (which gives a measure of power dissipation), and the dynamic range, which is a combination of the noise figure and the linearity. We will use an input frequency of 1GHz, since that is approximately the frequency at which the circuit must operate in the ΔΣM. The parameters for this cell are presented in

Table 7.2. A discussion of the results is in order.

Table 7.2: Comparison of multi-tanh architectures.

Parameter		$D = 1$	$D = 2$	$D = 3$
Realizable G_g range (mA/V)		2–22	2–11	2–8
ΔI_{tail} (μA per mA/V)		45	90	135
NF_{opt} (dB), R_{Sopt} (Ω)	$I_{tail} = 400\mu$A	5.67, 600	7.51, 900	9.11, 1100
	$I_{tail} = 1$mA	4.73, 400	5.83, 550	6.86, 700
Linearity	1dB compression (dBm)	-11.5	-5.5	-1.9
	Estimated IIP_3 (dBm)	-1.9	$+4.1$	$+7.7$
Approximate ΔDR (dB)		0	5	7

- The realizable G_g range is unlimited in theory as long as we are willing to supply the current I_{tail}. What limits us in this design is headroom, in particular the design of the biasing circuit that supplies I_{tail}. For $D = 3$, excessive I_{tail} pushes the transistor supplying I_{tail} into saturation which degrades linearity. This could be remedied with increased supply voltage V_{CC}, though this would increase V_{CE} on all the transistors and possibly introduce problems with BV_{CEO}.
- As expected, power dissipation is proportional to D for a given G_g. Again, high G_g can be obtained no matter what D is as long as we are prepared to dissipate more power.
- Noise figures were measured in SPICE at 1GHz using ac analysis; the source resistance was swept until the optimum NF was found, and both values are listed. NF falls as I_{tail} increases; the NF_{opt} increases between 1 and 1.5dB with D depending on I_{tail}. As well, larger D requires higher R_{Sopt} for optimum NF. That being said, NF and R_{Sopt} are roughly constant for the same G_g.
- Linearity was measured with transient simulation in SPICE. The 1dB compression point is fairly easy to measure by sweeping the input voltage, plotting the

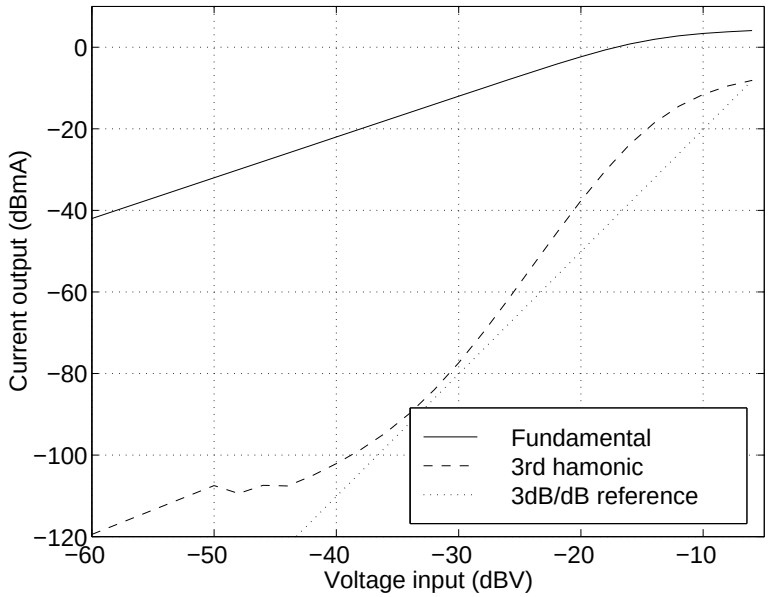


Figure 7.16: Linearity plot for a multi-tanh circuit.

output current, and using straight-line extrapolation to find where it deviates from linear by 1dB. Figure 7.16 shows the results of a two-tone test in SPICE where the input tones are at 980MHz and 1GHz, and the third harmonic at 1.02GHz is plotted. Unfortunately, the third harmonic does not behave in a Taylor-series manner: the slope of its magnitude doesn't increase by 3dB per dB of input voltage, as the dashed and dotted lines show. This is an inherent property of multi-tanh circuits [Gil98]; because of it, defining IIP_3 is difficult. The definition we adopt (simply so we have a method of discussing it) is that it is 9.6dB higher than the 1dB compression point, which derives from the assumption of a weak Taylor-type cubic nonlinearity in (7.7) and (7.8). In any case, linearity improves roughly as $20 \log_{10} D$.

- Combining the previous two facts—the small increase in NF with the larger increase in 1dB compression point—leads to the final table row which shows DR improvement resulting from increasing D.

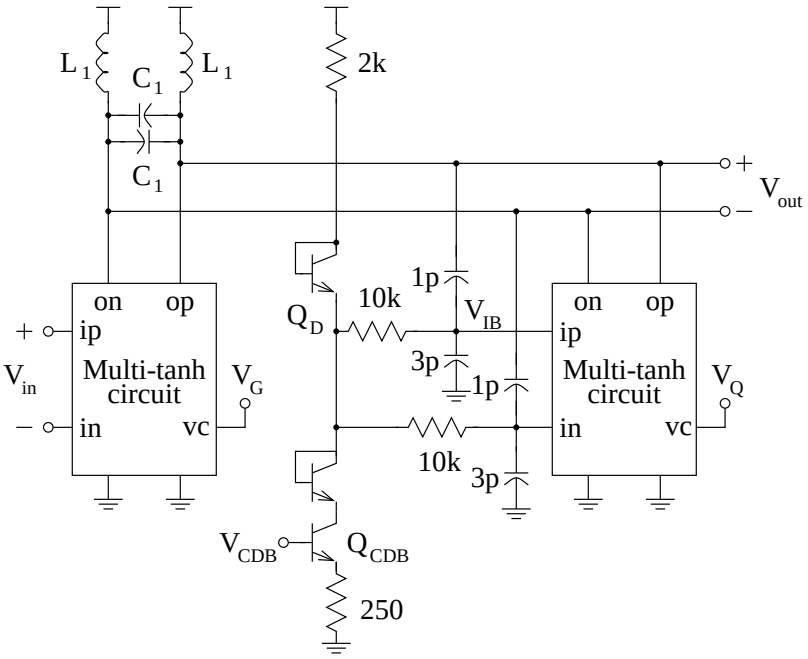


Figure 7.17: Band pass resonator block.

In conclusion, there is a clear DR advantage of using $D = 2$ instead of $D = 1$, and a slight further advantage in using $D = 3$ over $D = 2$. In a $V_{CC} = 5$V design such as this one, $D = 3$ is about the maximum we can get away with while retaining acceptable headroom. □

Q-enhancement transconductor

The band pass resonator block appears in Figure 7.17. The input voltage is applied through emitter followers (not shown) to the input multi-tanh block whose load is the LC tank. The Q-enhancement transconductor is a second multi-tanh circuit whose input is derived from the output voltage sampled by a capacitive divider. The dc level at the inputs to the Q-enhancement multi-tanh would not be well-defined without the control voltage V_{CDB} and the circuitry associated with it.

Examination of the dc operating point of the circuit makes it clear that care must be taken when choosing where to set various voltages when the power supply is 5V. The bias circuit has to be turned off in practice because the base currents of the Q multi-tanh input transistors alone drop

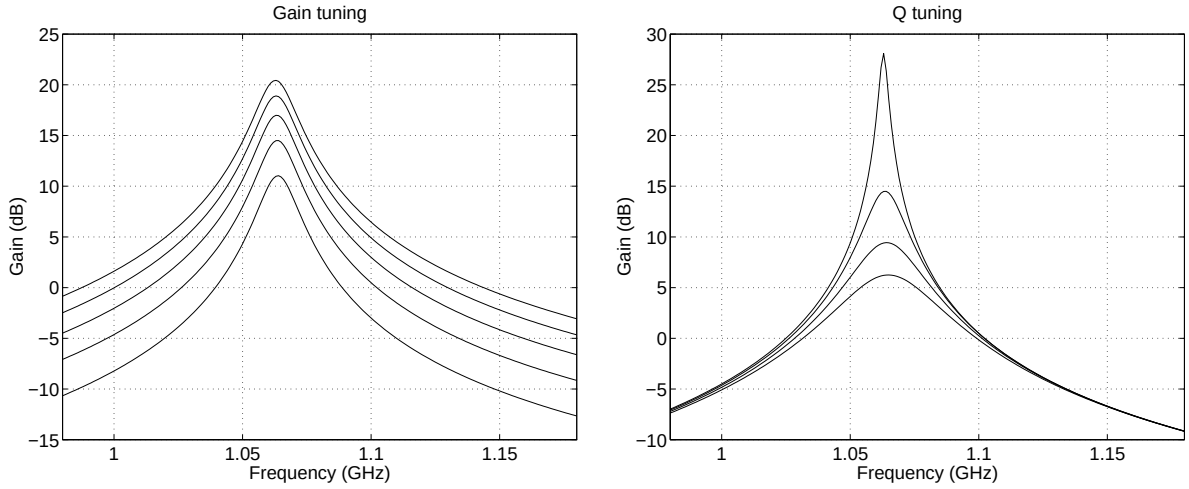
enough voltage across the $2\text{k}\Omega$ and $10\text{k}\Omega$ resistors to push the input common-mode voltage V_{IB} to 3.5V, which, as was also true with the input transconductor, strains the ability of the transistors supplying I_{tail} to stay out of the saturation region. Raising V_{CDB} to a voltage which turns Q_{CDB} on pulls V_{IB} down further resulting in worse IIP_3 for the G_q transconductor. Therefore, $V_{CDB} = 0\text{V}$ is required in normal circuit operation.

The G_q transconductor's ac input voltage derives from V_{out} through the 1pF/3pF capacitive voltage divider. We expect a voltage division of 0.25 (i.e., the input signal at V_{IB} smaller than V_{out} by a factor of four), though SPICE simulations indicate a value of closer to 0.20 for a signal between 1GHz and 4GHz. The transistors in the G_q multi-tanh circuit are, however, four times larger than those in the G_g circuit, so they are capable of supplying about four times the current at the same V_{BE}. The net result is, the achievable transconductance range obtainable for the G_q transconductor is not markedly different from that for the G_g transconductor. The linearity is better, however: G_q achieves $\text{IIP}_3 = +20\text{dBm}$ or so vs. $+8\text{dBm}$ for G_g, though this is expected because of the voltage division.

Resonator characteristics

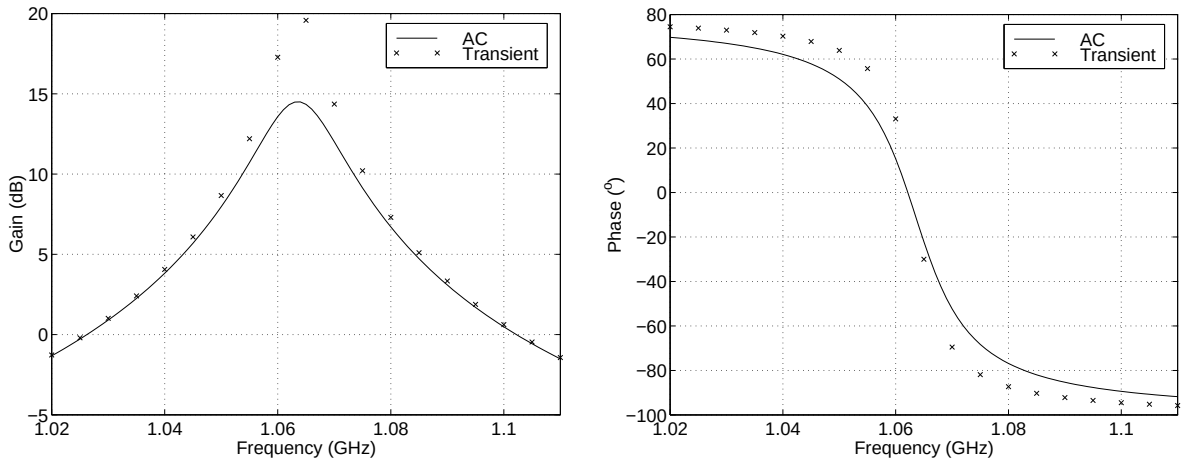
We illustrate gain and Q tuning for the overall resonator in a SPICE ac analysis in Figure 7.18. Figure 7.18(a) shows V_G tuning with fixed V_Q, where these two voltages control the tail currents in each multi-tanh block. The peak gain varies over about 9.5dB, with Q_{res} remaining almost constant at about 73; the peak gain is proportional to the G_g in the gain multi-tanh circuit. Figure 7.18(b) is with V_G fixed and V_Q tuned, and the Q_{res} varies from 28 for $V_Q = 2.4\text{V}$ to about 360 for $V_Q = 2.7\text{V}$. These results are useful because they let us estimate actual voltage levels which result in a certain gain and Q during testing.

We also do a comparison of ac analysis to transient analysis. Figure 7.19 contrasts the analysis results for $V_G = 2.2\text{V}$ and $V_Q = 2.6\text{V}$, gain in Figure 7.19(a) and phase in Figure 7.19(b). It takes the output amplitude about 400 cycles to settle, so each simulation takes quite a bit of time. Agreement is good except near the peak gain where it becomes merely acceptable: ac analysis predicts $Q = 74$ while the transient analysis shows $Q \approx 150$. SPICE ac analysis is linearized



(a) (b)

Figure 7.18: Filter gain characteristic: (a) fixed $V_Q = 2.6$V, stepping V_G by 0.2V from 2.0V to 2.8V, (b) fixed $V_G = 2.2$V, stepping V_Q by 0.1V vrom 2.4V to 2.7V.



(a) (b)

Figure 7.19: Transient analysis for $V_G = 2.2$V and $V_Q = 2.6$V: (a) gain, (b) phase.

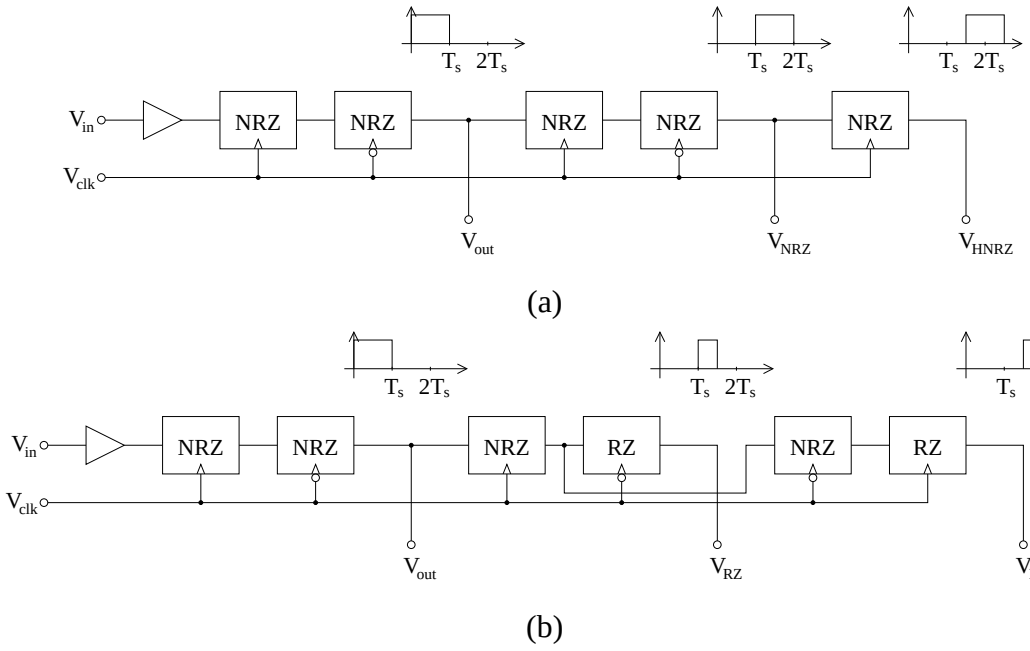


Figure 7.20: Overall latching scheme and waveforms: (a) NRZ modulator, (b) RZ modulator.

while transient analysis preserves nonlinearities, hence the two disagree here [Che94, Che98c].

We can find the input-referred noise (and hence the minimum-detectable input signal u_{min}) from a SPICE ac simulation. A value for typical control voltage settings is $\overline{v_{ng1}} = 20\text{nV}/\sqrt{\text{Hz}}$, though this can vary by a factor of two either way depending on the exact biasing. In a 20MHz band, the total noise comes out to about $u_{min} = 90\mu\text{V}$ which is therefore the smallest modulator input voltage which can be sensed. Both these values were listed in Table 7.1.

7.2.2 Latch

Two different modulators were designed: the "NRZ modulator", which has NRZ and half-delayed NRZ (HNRZ) feedbacks, and the "RZ modulator" with RZ and HRZ feedbacks. Block diagrams of the latching schemes in each are shown in Figures 7.20(a) and (b). The NRZ and RZ blocks are half-latches with outputs that either don't or do return to zero after a half cycle (c.f. the dashed and dotted lines in Figure 4.15). The one-bit quantizer in both designs is a preamplifier with an ECL master/slave latch, exactly as was depicted in Figures 4.15 and 6.5. As mentioned at the start

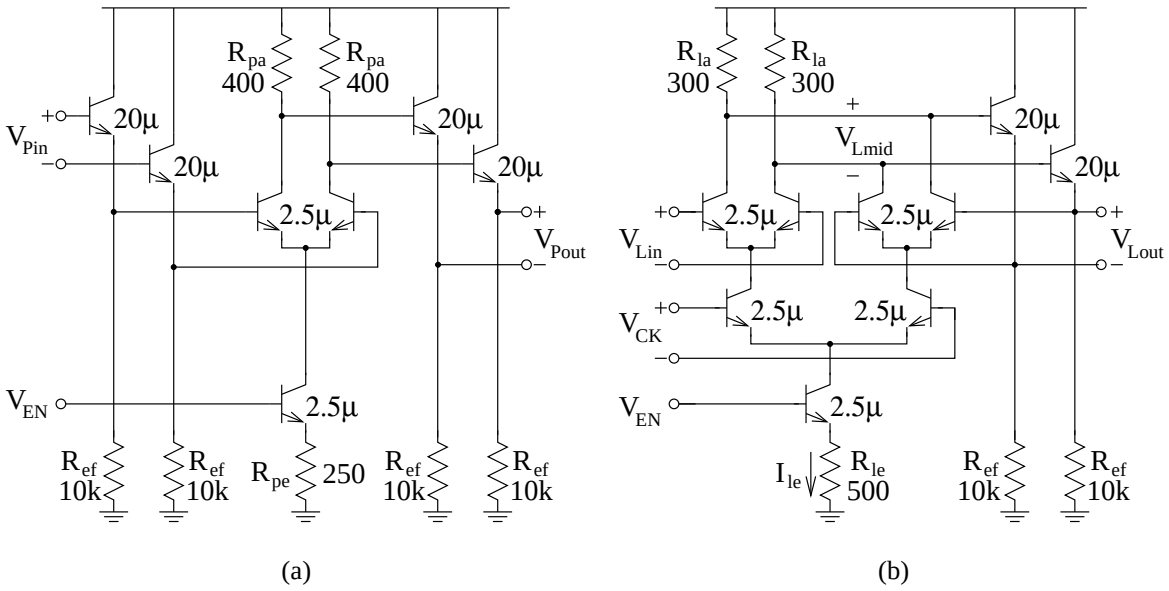


Figure 7.21: Schematics for (a) preamplifier, (b) half-latch.

of this chapter, there is a full sample of delay prior to each DAC, and these are implemented with appropriate further half stages as shown.

The preamplifier circuit, Figure 7.21(a), is a simple differential pair with input and output buffers. As we noted in §6.4.3, it has been shown [Lee92] that emitter followers before and after a preamplifier are good for eliminating coupling of the clock signal between the main latch and the preamp. But the followers in this circuit are apparently sized and biased incorrectly for optimum speed, a rather serious oversight for a high-speed circuit. We will worry about correcting them in §7.4.2; for now, we provide gain and phase curves of SPICE ac analysis (supplemented with transient analysis for verification) for the input follower in Figure 7.22(a). Followers are fairly forgiving circuits, so the gain and phase shifts are not huge, but they can be improved a good deal. One result of the rolloff exhibited in the input follower gain curve is that the overall preamp has an ac analysis given in Figure 7.22(b): the -3dB frequency is quite low at 4.59GHz. The dc gain is 18.7dB, and the phase shift at $f_{-3\text{dB}}$ is $-61.6°$.

A half-latch in this design appears in Figure 7.21(b). The output swing is typically 270mV and the regeneration time constant for the latch as designed is $\tau_{rg} = 17.4$ps, which again can be improved with proper follower design. We leave this for §7.4.2.

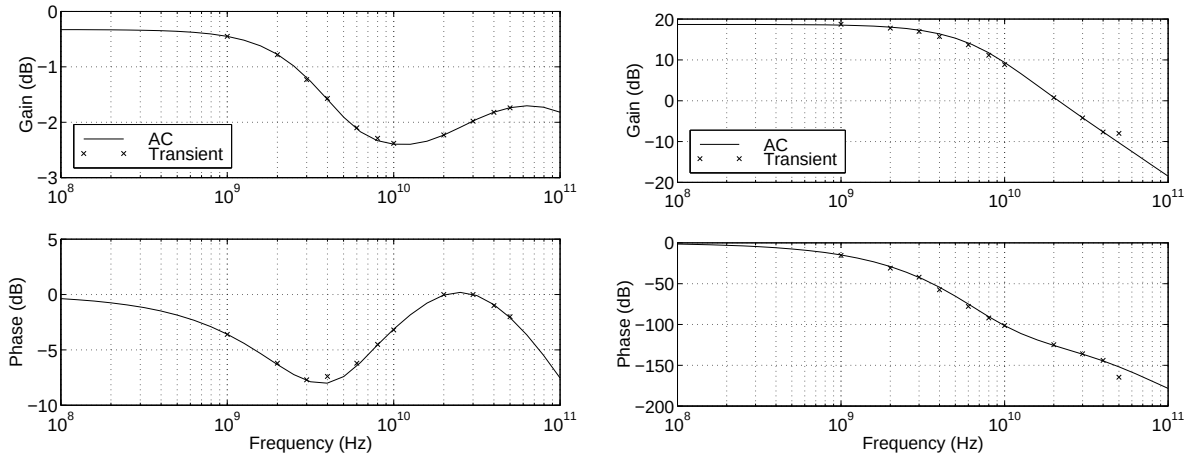


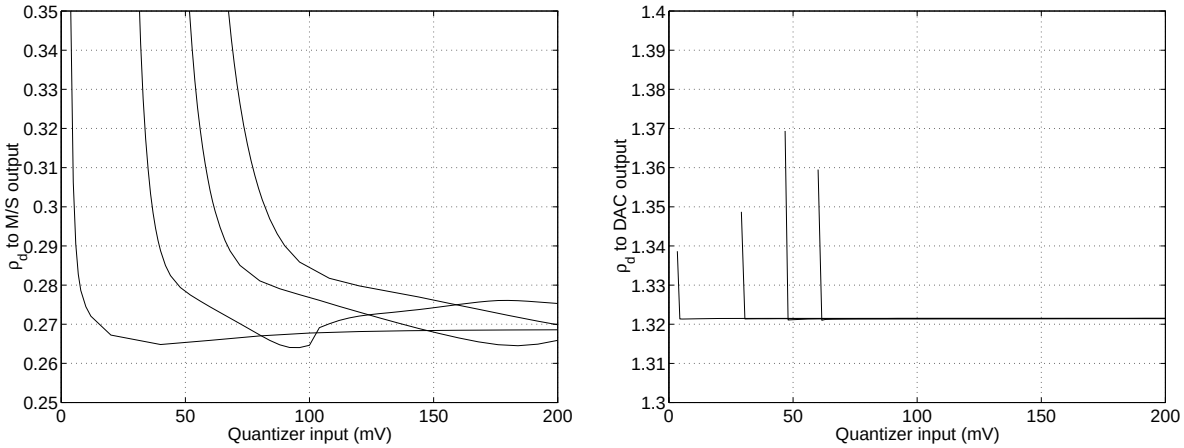
Figure 7.22: Original preamp ac analyses: (a) input follower, (b) entire circuit.

Typical ZCT characteristics for the M/S latch output and one-sample delayed latch output are illustrated in Figures 7.23(a) and (b), respectively. Clocking at $f_s = 4$GHz in an $f_T = 40$GHz process is aggressive, to be sure, if the guideline of 4–5% in §6.6 is to be believed. That guideline was for a three half-latch design, and this one contains four, so the regeneration at the final latch output is adequate, as is clear by the sharpness of the corners in Figure 7.23. However, it is the hysteresis in combination with small quantizer input swing which will turn out to be a major problem in this design: we barely use 5% of the full-scale input range. Our redesign will address this.

7.2.3 Output Buffer

The output is obtained from the slave stage of the M/S latch driving a differential pair with 50Ω load resistors, Figure 7.24, for matching to an off-chip 50Ω measuring device. The bias current, and hence the output swing, is controlled with a voltage V_{BUF} applied directly to the base of a current-source transistor. A typical desirable swing for us is 200mV, which requires a current of 4mA; this can be achieved by using $V_{BUF} = 3$V.

In Figure 7.25(a), we show a typical output waveform from the M/S latch, and Figure 7.25(b)



(a) (b)

Figure 7.23: ZCT characteristics for (a) M/S latch output, (b) one-sample delayed output.

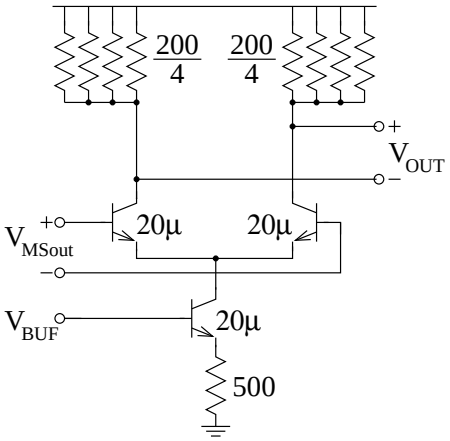
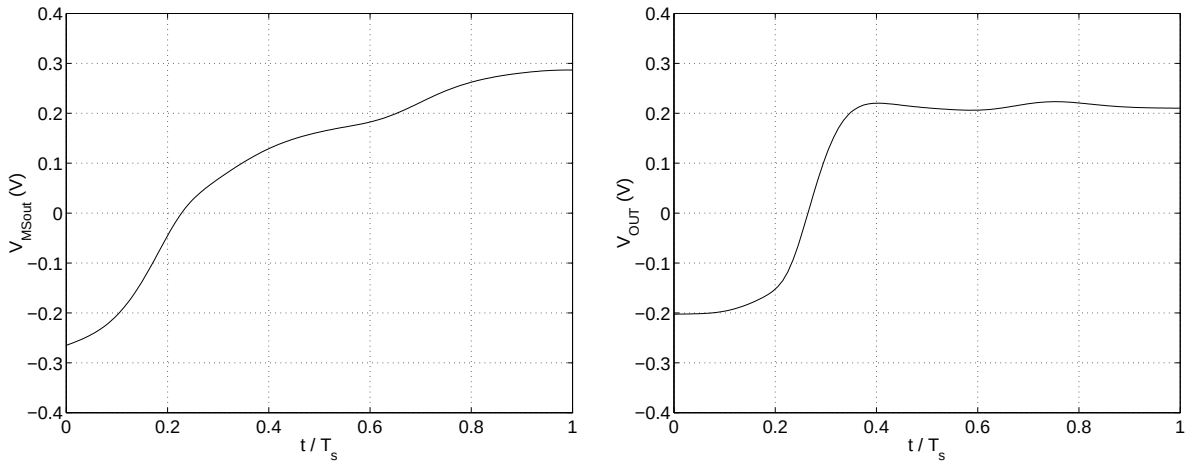


Figure 7.24: Modulator output buffer.



(a) (b)

Figure 7.25: Output waveforms: (a) M/S latch, (b) output buffer.

depicts the output buffer waveform. The latch output seems not to rise very sharply, but the edge of the output buffer waveform is much better-defined.

7.2.4 DAC

There are a total of four DACs on the chip, two for each of the V_{NRZ} and V_{HNRZ} (or V_{RZ} and V_{HRZ}) signals; for each signal, one DAC connects to the first resonator output and one to the second. The DACs are relatively simple current-steering circuits, Figure 7.26, with follower inputs and current outputs derived from the sum of cross-coupled diff pairs. A typical output voltage waveform vs. normalized time appears in Figure 7.27. The M/S latch output switches just after $t/T_s = 0$, then there is a full sample of delay before the DAC switches. The ZCT is $\rho_d = 1.322$ and the rise time is $\rho_r = 0.146$. Ideally, this waveform would switch instantaneously at $t/T_s = 1$.

7.2.5 Complete Circuit

Finally, complete transistor-level schematics for both modulators are shown in Figures 7.28 and 7.29. The boldface words are the names of the external signals. A die photomicrograph of the

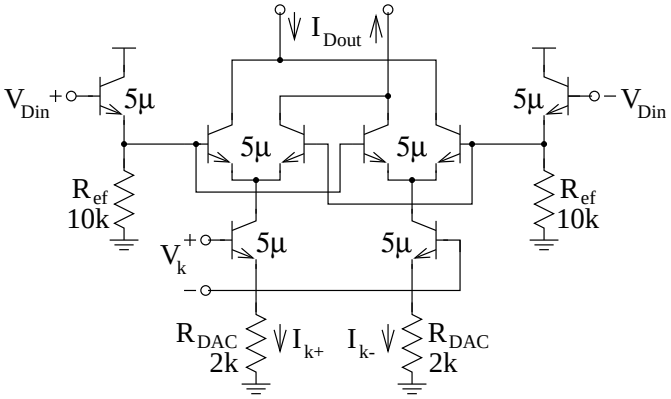


Figure 7.26: Current-steering DAC schematic.

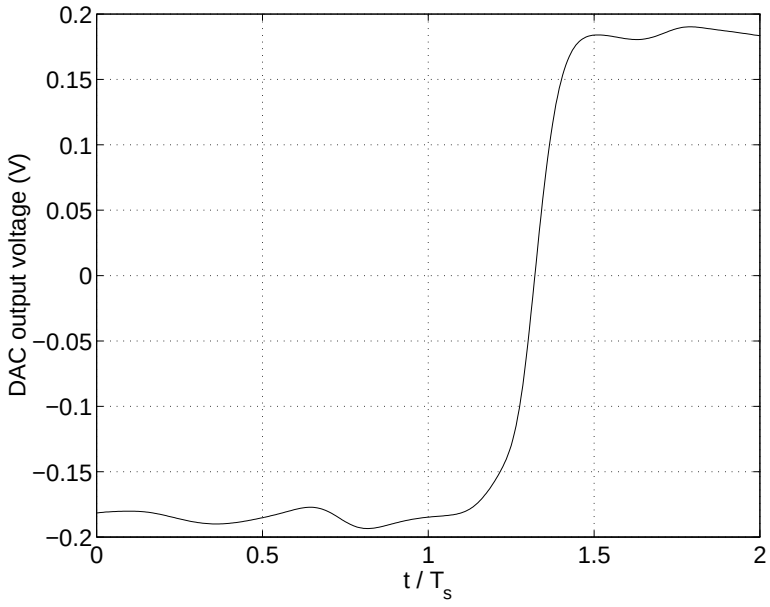


Figure 7.27: Dynamic DAC output voltage.

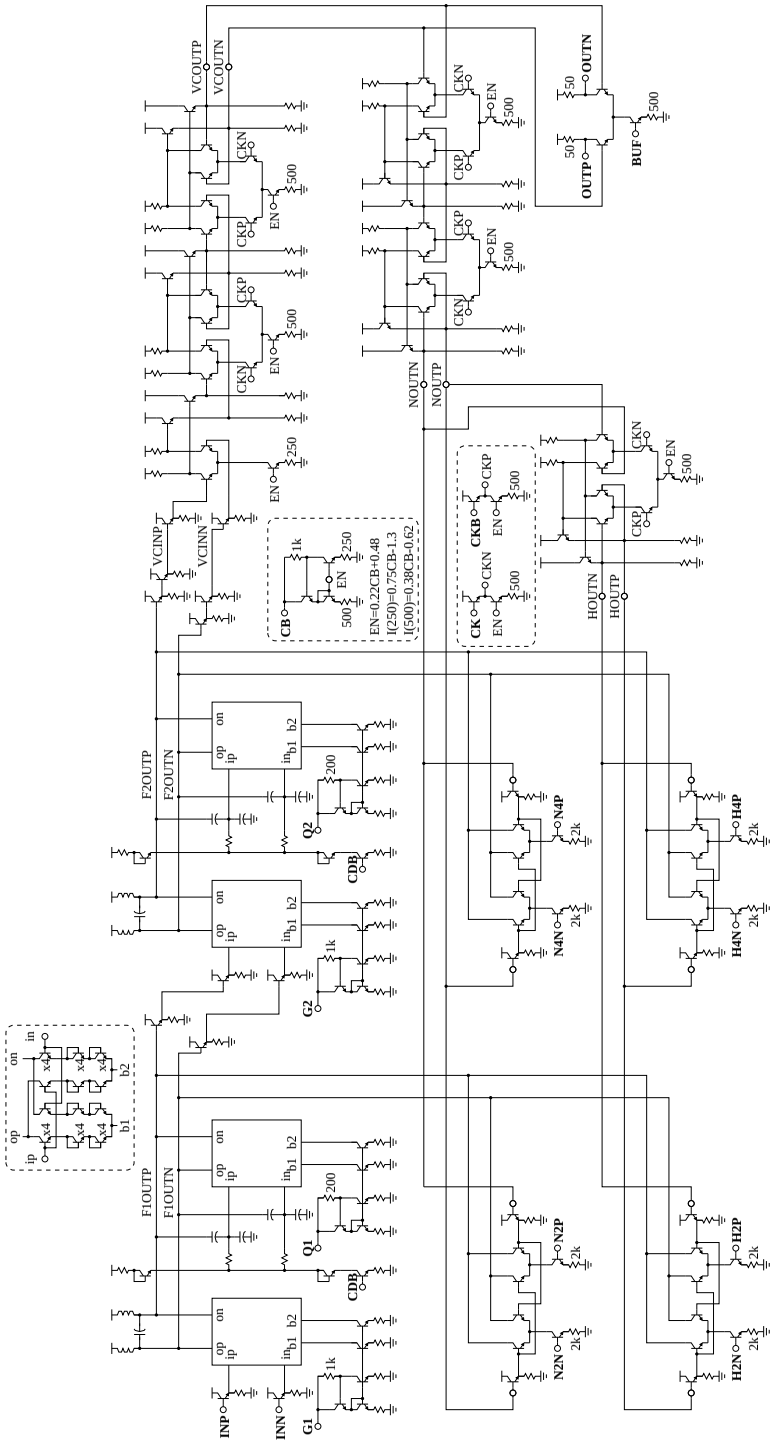


Figure 7.28: Complete NRZ ΔΣM schematic.

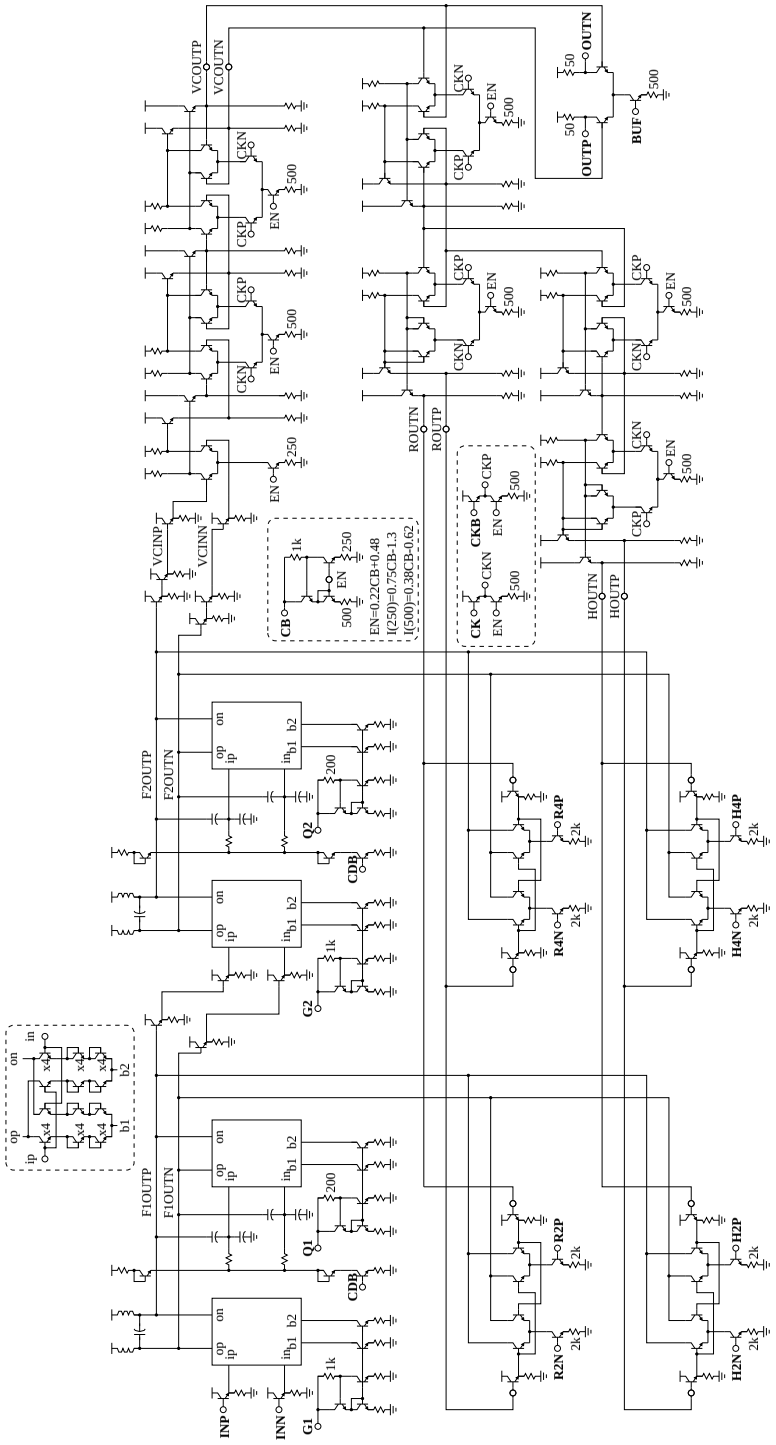


Figure 7.29: Complete RZ ΔΣM schematic.

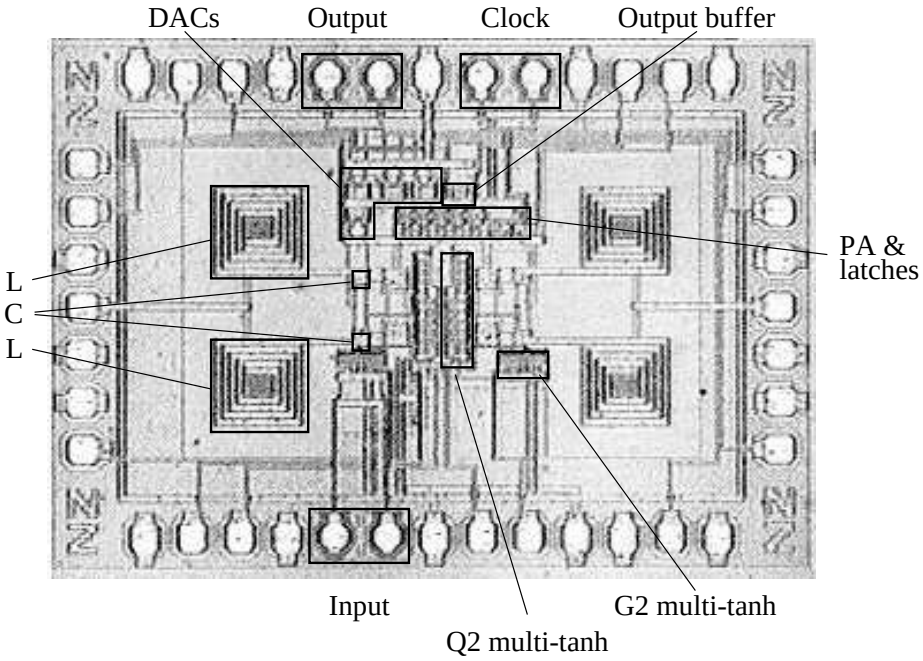


Figure 7.30: Die photomicrograph of NRZ modulator.

fabricated NRZ modulator appears in Figure 7.30. The die measures 2.4×1.6mm^2 with the pads and 1.6×0.85mm^2 without. There are a total of 40 pads: 6 input (two each for differential input, clock, and output), 2 V_{CC}, 15 dc bias (V_{CB}, V_{BUF}, two each of V_G and V_Q, V_{CDB}, and four each of V_{k+} and V_{k-} for the DACs), and 17 ground. As is evident from the schematics, the input signal common-mode (CM) levels are not set on-chip and so must be provided through bias tees.

7.3 Measurement Results

Given the number of dc biases that must be controlled in this design, standard high-speed probe configurations for wafer-level tests are all but impossible to come by. It is possible to have a "membrane probe card" specially constructed, but several factors (not least the financial expense of US$17,000) ruled out this possibility. Thus, diced wafers were packaged and mounted on a four-layer test board. There are no individual circuit block breakouts, so we must devise methods to check circuit behavior based only on the overall modulator output bit stream, either in the time

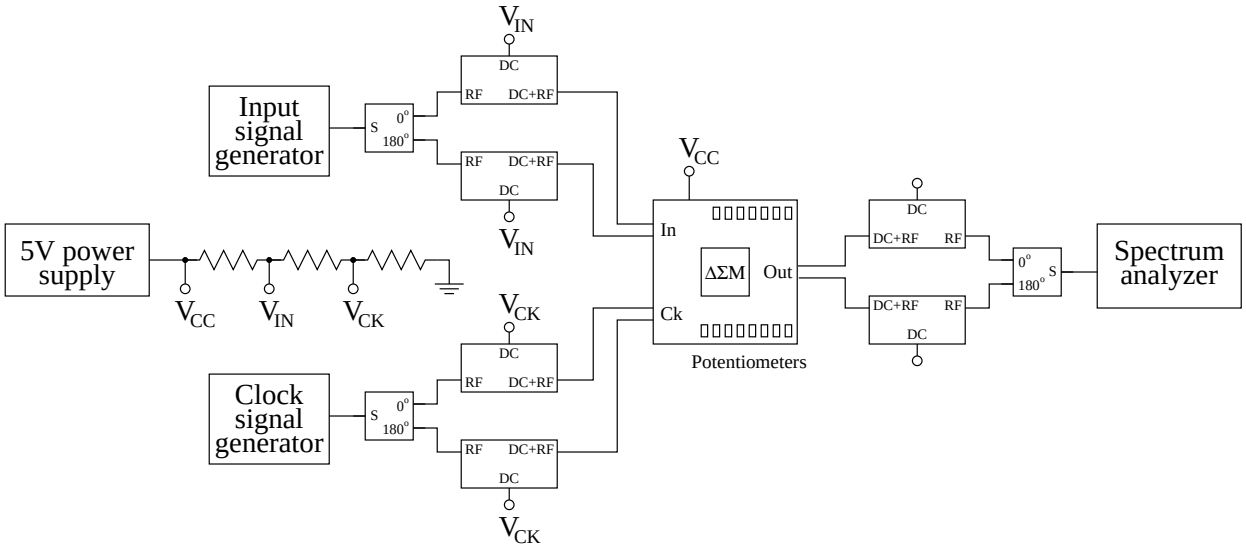


Figure 7.31: Measurement test setup.

domain or the frequency domain.

The input and clock signals were provided from signal generators, driven differentially onto the board through 180° power splitters, each with two bias tees for providing CM voltages. At first, V_{CC} and the two CM voltages were all provided with separate power supplies, which resulted in the destruction of several packaged parts by applying inappropriate voltages across certain junctions of the input buffer transistors; eventually, a single supply for V_{CC} was used, with the CM levels being drawn from a tunable resistive divider circuit. SMA connector-terminated cables of equal lengths rated to 40GHz were connected to the board. The remaining dc biases were set with $10\text{k}\Omega$ potentiometers connected between V_{CC} and ground. Each required hand tuning with a screwdriver and voltmeter to set a desired voltage level. The output came differentially from two similar cables connected to the "DC+RF" input of bias tees; the RF outputs have no remaining dc component, and they were connected to a spectrum analyzer through a combiner. A diagram of the test setup appears in Figure 7.31.

A typical spectrum analyzer display for the NRZ modulator output bit stream appears in Figure 7.32. The conditions with which this plot was made were

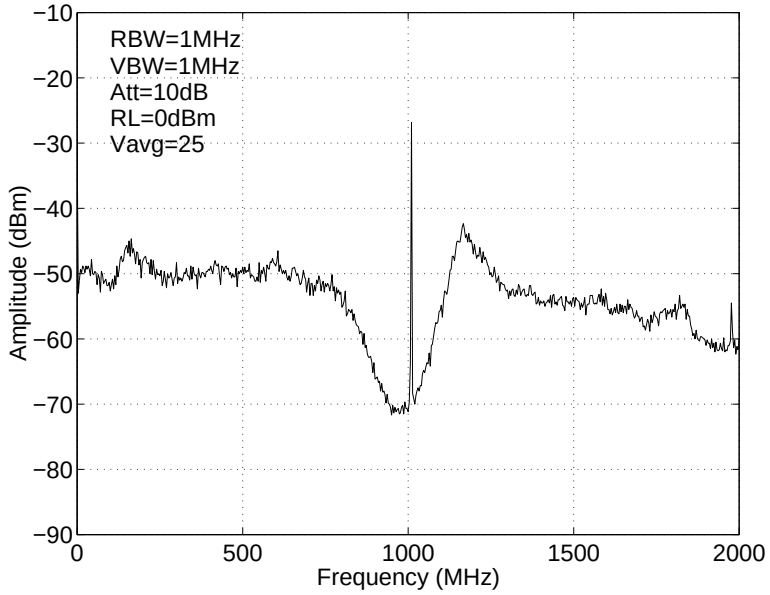


Figure 7.32: NRZ modulator output spectrum.

- Input 4.2V CM, -26dBm, 1.010GHz
- Clock 3.0V CM, -10dBm, 4.000GHz
- Power supply 5.03V, 75mA
- $V_{G1} = V_{G2} = 2.6$V, $V_{Q1} = V_{Q2} = 2.8$V, $V_{CDB} = 0$V
- $V_{BUF} = 3$V, $V_{CB} = 4$V
- DAC CM 1.2V, $V_{n2} = 0.4V$, $V_{n4} = 0.2$V, $V_{h2} = V_{h4} = 0$V

The noise-shaping behavior is evident: the quantization noise has a dip of 20dB or so at about $f_s/4 = 1$GHz. Thus, the circuit appears to be functioning correctly.

7.3.1 Resonator

For the resonator, there are three voltages which should have a noticeable effect: V_G, V_Q, and V_{CDB}. Let us examine each in turn.

Varying V_G

For simplicity, we test the NRZ modulator with the half-delayed feedback pulses disabled, i.e., $V_{h2} = V_{h4} = 0$V. This allows us to specify the level of a full-scale input easily. From (7.14) and Figure 7.2 (recall also Example 2.7), the maximum input is one where the current due to the input transconductor $G_{g1}u$ has the same magnitude as the feedback current $k_{n2}y$. Thus, the output magnitude relative to full scale of an input signal u in V is

$$\frac{G_{g1}}{k_{n2}}u, \tag{7.31}$$

where G_{g1} is in mA/V and k_{n2} in mA. Let us relate all these quantities to the signals we actually use.

- G_{g1} is related to V_{G1} through Figure B.2(a). An approximate formula is

  $$G_g = 5.43V_G - 8.73, \tag{7.32}$$

  where G_g is in mA/V and V_G in V.

- For k_{n2}, define $k_{n2} \equiv I_{k+} - I_{k-}$ and $V_{n2} \equiv V_{k+} - V_{k-}$ in Figure 7.26. From Figure B.4,

  $$I_k = 0.48V_k - 0.38 \tag{7.33}$$

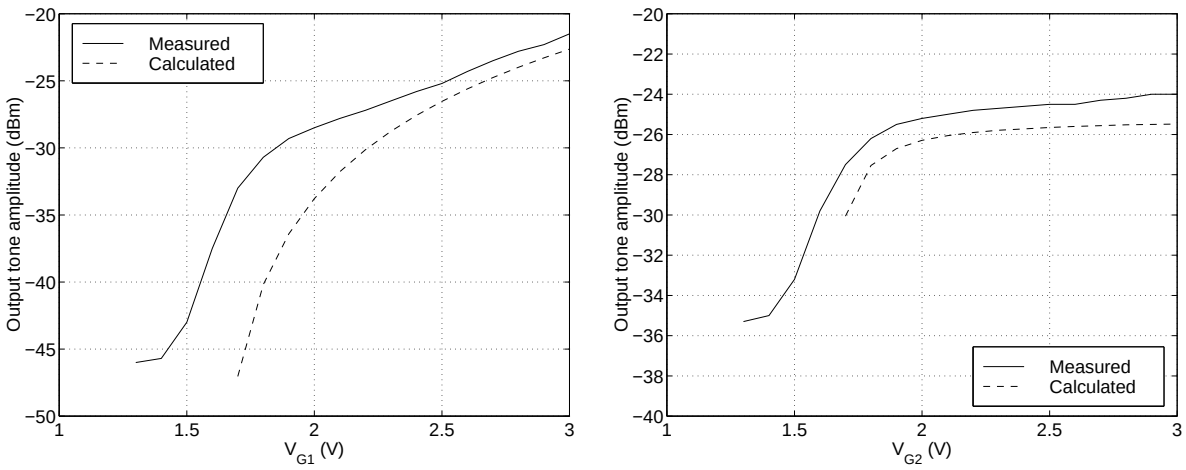
  for I_k in mA and V_k in V. Substituting our definitions in (7.33), we arrive at

  $$k_{n2} = 0.48V_{n2} \tag{7.34}$$

  for k_{n2} in mA and V_{n2} in V.

- The input voltage V_{in} from the signal generator is calibrated in dBm assuming a 50Ω load. The modulator input, however, was not designed to have a 50Ω input impedance: the signal generator drives the pin capacitance, a bond wire inductor, and then an emitter follower. In §7.4.2, we estimate that the signal at the base of the emitter follower will be about 4dB smaller than the dBm reading on the generator. Taking this into account, we may write

  $$u = 10^{(V_{in}-14)/20} \tag{7.35}$$



(a) (b)

Figure 7.33: Tone magnitude in output spectrum against (a) V_{G1}, (b) V_{G2}.

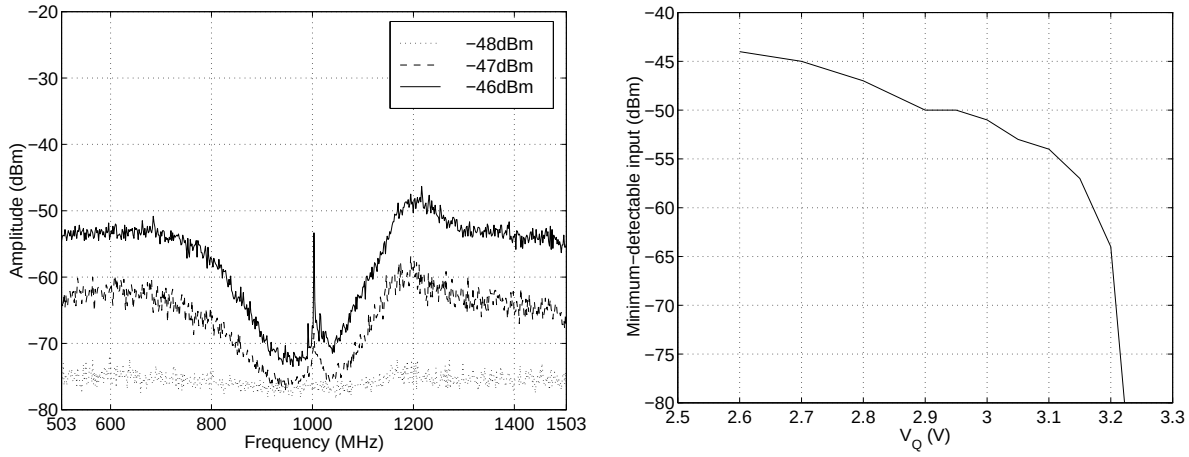
for u in peak V (as opposed to rms) and V_{in} being the nominal output from the generator in dBm.

- We shall see that the time-domain output voltage has a swing of about 120mV peak-to-peak, or 60mV peak. An 0dB input tone thus requires a peak magnitude of 60mV, which is

$$20 \log_{10} 0.06 + 10 = -14.5\text{dBm}. \tag{7.36}$$

For a 1.003GHz -26dBm input, the magnitude of the 1.003GHz tone in the output spectrum as a function of V_{G1} appears as the solid line in Figure 7.33(a). The result calculated from equations (7.31)–(7.36) is plotted as the dashed line. The curves agree reasonably well. According to our approximate formula (7.32), the transconductor turns off at $V_{G1} = 1.6$V, at which point no output tone should be visible; in reality, the output tone remains with an amplitude is about -47dBm even with $V_{G1} = 0$V, likely because of coupling across C_μ from input to output of G_{g1}.

Simulation of the modulator using the RK4 program and a model like Figure 7.2 shows that the output amplitude depends slightly on V_{G2} as well, though in a manner that is more difficult to calculate. Figure 7.33(b) shows measured and simulated output tone magnitude against V_{G2}



(a) (b)

Figure 7.34: (a) Loss of noise shaping for small input and low Q, (b) minimum-detectable input amplitude against V_Q.

for fixed $V_{G1} = 2.6$V, and once again, even with $V_{G2} = 0$V, there is still an output tone of about -35dBm. Generally, the output tone magnitude behaves as expected when either V_G is varied.

Varying V_Q

Ideally, a modulator is tuned so that it has infinite Q. This means (in theory) an infinitely-deep notch in the quantization noise and optimal SNR. Practically, there are two cases of interest which we demonstrate here. If Q is tuned too low, then the modulator will not exhibit noise shaping for very small input levels [Fee91]. Figure 7.34(a) depicts output spectra for $V_{Q1} = V_{Q2} = V_Q = 2.8$V and the input amplitude increasing slowly. At -48dBm, no noise shaping is seen; the modulator is sensitive only to inputs of -47dBm. Figure 7.34(b) plots the minimum-detectable input amplitude versus V_Q: at $V_Q = 3.25$V, the input can be disabled without the loss of noise shaping at the output.

On the other hand, if Q is too high, then instead of a resonator we will have an oscillator. Figure 7.35(a) is the output spectrum for $V_Q = 3.31$V and no input, which turns out to be just on the edge of stability—if we make $V_Q = 3.33$V, the spectrum looks like Figure 7.35(b), which has the tonal behavior characteristic of a modulator with an oscillator in the forward path[3]. The V_Q

[3]It is actually possible to have a pole slightly outside the unit circle and still have a stable modulator: this yields

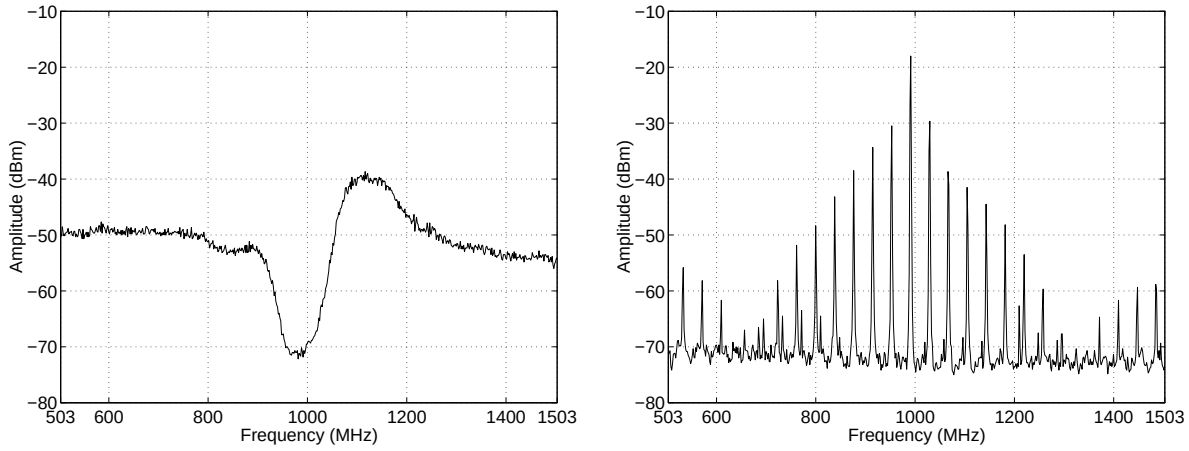


Figure 7.35: Oscillation in output spectrum: (a) $V_Q = 3.31$V, (b) $V_Q = 3.33$V.

which causes oscillation in practice is higher than that predicted by (7.14): from Figure B.2(b), we may write

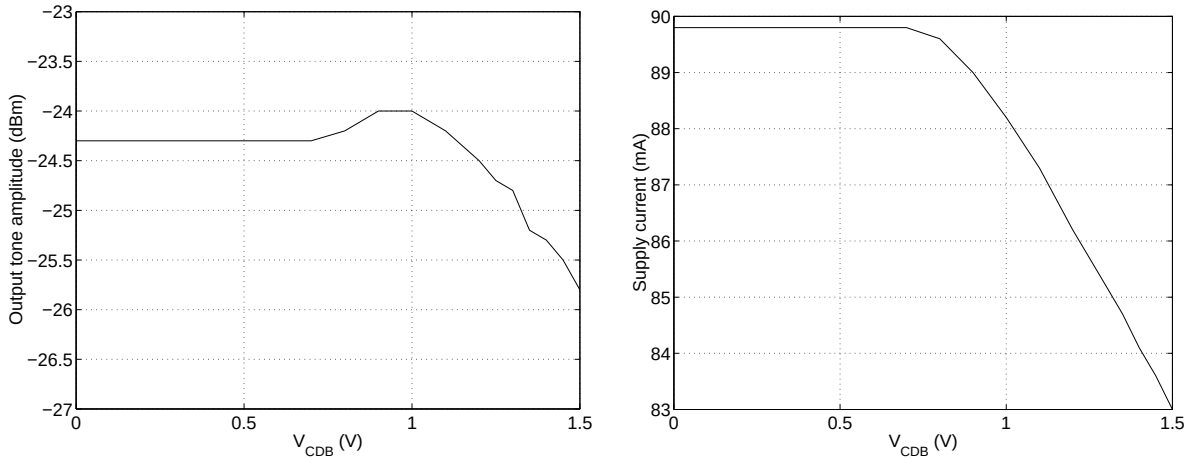
$$G_q = 3.63V_Q - 6.01 \tag{7.37}$$

for G_q in mA/V and V_Q in V, and for the parameters in Table 7.1, we expect $V_Q = 2.83$V or so. The spacing of the tones in Figure 7.35(b) is curious: they seem to occur every 38MHz or so, which suggests we have entered an output limit cycle whose period is $4\text{GHz}/38\text{MHz} \approx 105$. No explanation for this value is obvious, though it might reasonably be some kind of beating between the oscillation frequency and $f_s/4$. Naturally, the modulator is not intended to be operated in this regime.

Varying V_{CDB}

We stated in §7.2.1 that setting V_{CDB} too high would give linearity problems due to saturating the current-source transistors in the Q-enhancement multi-tanh block. The best way to verify this in

a so-called chaotic modulator [Ris94, Chap. 3]. Pushing the pole too far outside the unit circle results in instability like that shown in Figure 7.35(b). From Figure 7.34(b), $Q = \infty$ seems to be achieved at $V_Q = 3.22$V, so the plot in Figure 7.35(a) for $V_Q = 3.31$V is very likely one where the modulator is chaotic.



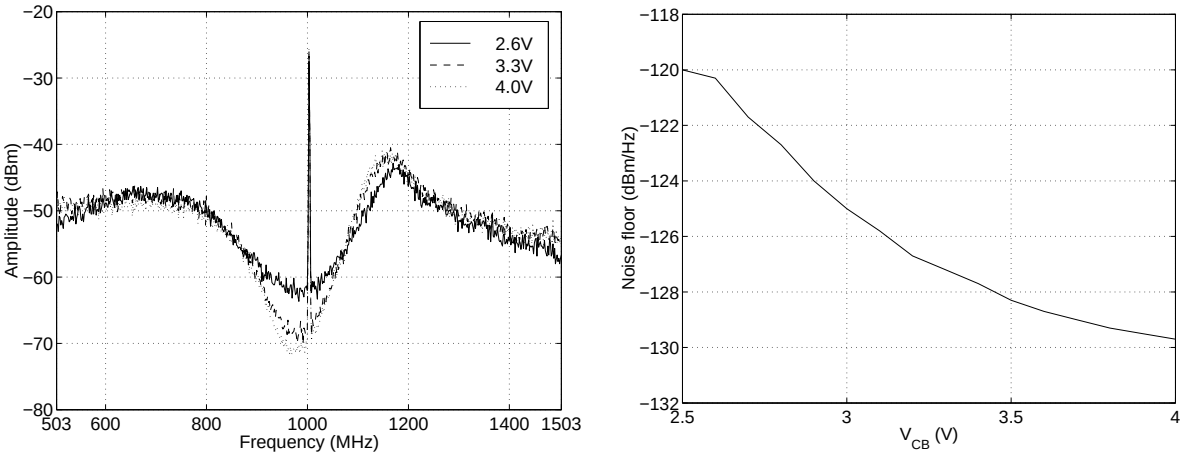
(a) (b)

Figure 7.36: Effect of V_{CDB} on (a) linearity, (b) supply current.

practice would be with a two-tone test, but our setup is too cumbersome to allow this to be done easily. However, with a fixed-amplitude -26dBm tone, we can observe the amplitude of the output tone varying as V_{CDB} increases, Figure 7.36(a). The gain to the output is constant for small V_{CDB}, but as soon as Q_{CDB} in Figure 7.17 turns on, we start to see distortion, first gain expansion, then gain compression. The transistors supplying I_{tail} in Figure 7.12 are being driven into saturation almost immediately when Q_{CDB} starts to conduct: Figure 7.36(b) shows that the current drawn from the supply begins to drop as V_{CE} is driven towards 0, which is the expected behavior from Figure B.1(b).

7.3.2 Latch

The control voltage V_{CB} affects the behavior of the latch in a quantifiable way: it changes the current I_{le} through R_{le} in Figure 7.21(b), and hence the regeneration time τ_{rg}. Increasing I_{le} leads to a closer bunching of the ZCT curves in Figure 7.23(a), in turn leading to smaller σ_{DPW}. Examination of the output spectrum near $f_s/4$ shows that the spectrum is white; if it is limited by noise due to DPW modulation from metastability, then the noise floor should become lower as σ_{DPW} falls. Figure 7.37(a) demonstrates that the noise floor near the resonator center frequency



(a) (b)

Figure 7.37: Changing V_{CB}: (a) overall spectrum, (b) in-band noise.

does indeed fall as V_{CB} is increased from 2.6V to 3.3V and 4.0V. Figure B.3(b) is the in-band noise measured with the spectrum analyzer set to display a 10MHz band near the approximate notch center frequency of 980MHz; as V_{CB} increases, the in-band noise falls.

The author also had a brief opportunity to take some time-domain measurements on a 50Gs/s sampling oscilloscope. Figure 7.38 shows an eye diagram of the 4Gb/s bit stream on a 50ps/div horizontal time scale. The eyes have a not-inconsiderable number of dots inside them, the cause of which is the location at which the output bits are taken: the M/S latch output. The dots correspond to instances where the latch output is delayed and the oscilloscope happens to sample at a point on that delayed waveform. The eyes would be more open if the output bits were taken from the one-sample delayed latch, where from Figure 7.23(b) there is less ZCT variance. This is of consequence when the modulator output spectrum is examined on a spectrum analyzer, as opposed to found from the FFT of a sequence of output bits. Even though much of the digital output edge jitter due to quantizer metastability is removed in the *feedback path* by the two extra half-latches, none of this jitter is removed at the modulator output because this output is taken *prior* to the extra regeneration stages. To a spectrum analyzer, the analog properties of the output waveform are significant. Thus, closed eyes due to metastability will degrade the spectrum measured on a

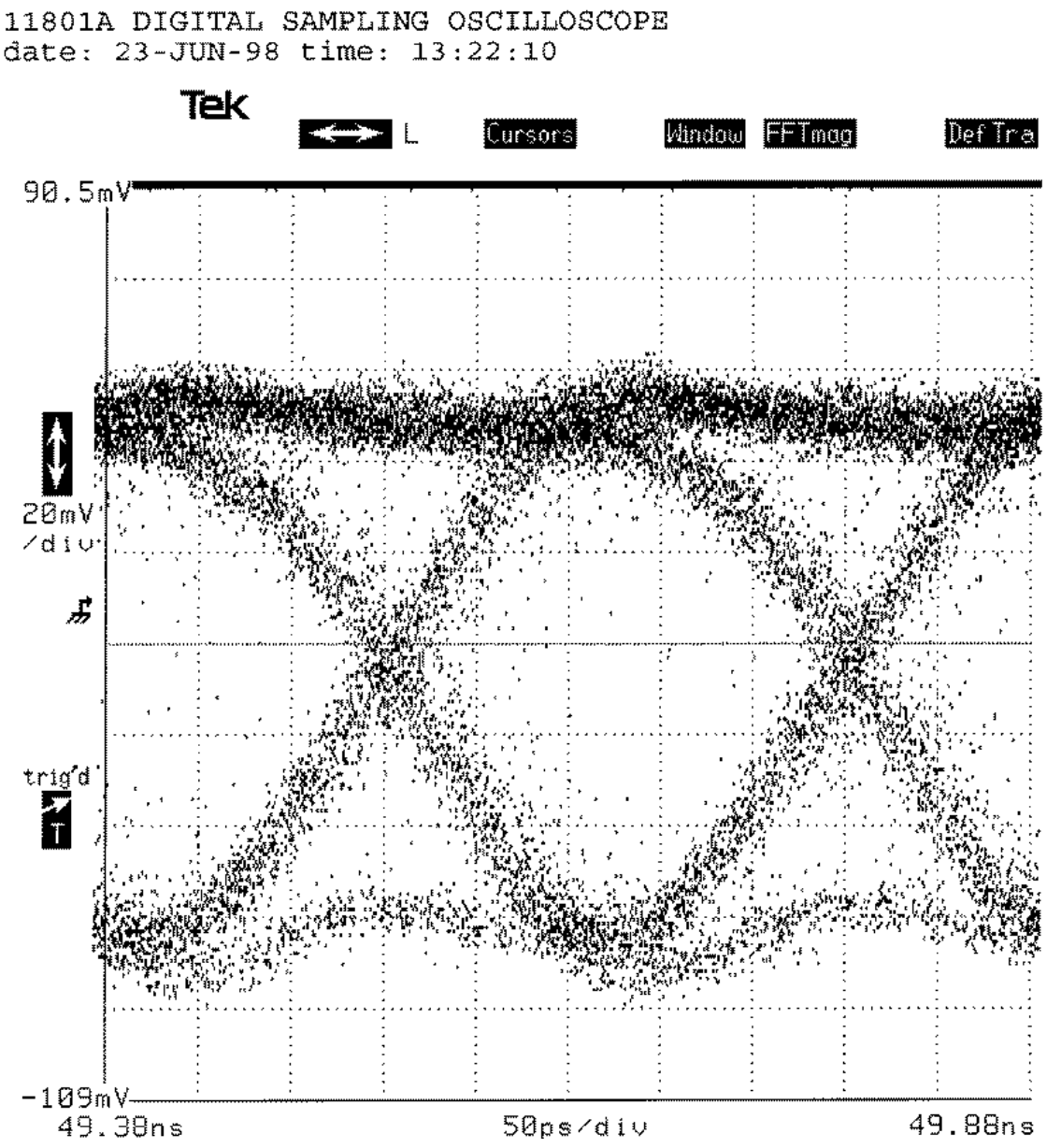


Figure 7.38: Output bit stream eye diagram.

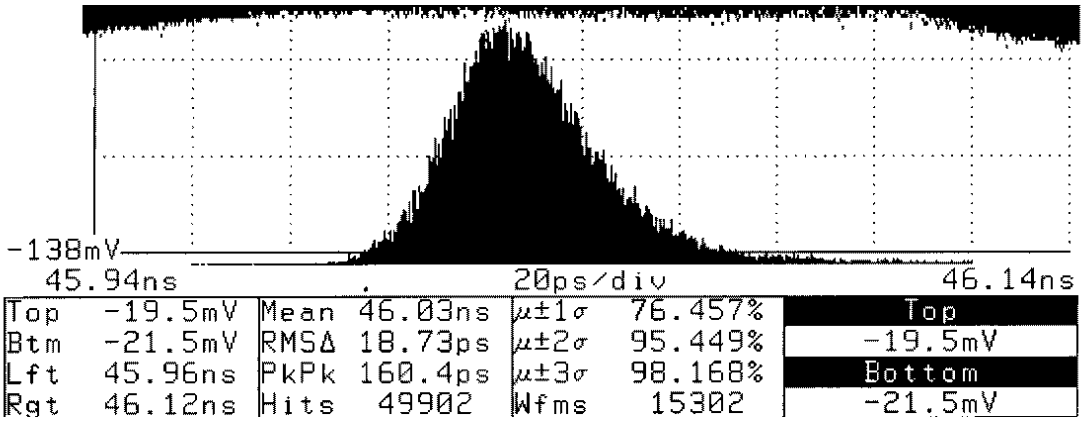


Figure 7.39: Histogram of time-domain output bit zero crossings.

spectrum analyzer by whitening it in-band. We *did* find that increasing V_{CB} resulted in improved eye openings, as one would expect.

More evidence of the effects of metastability can be seen in Figure 7.39, which is a histogram of the zero crossings of the time-domain output bit stream. At these rapid speeds, the sampling jitter of the oscilloscope itself is significant. When we used a common frequency reference for both a signal generator and the scope, and applied a 4GHz sine wave from the generator to the scope, we found a normally-distributed time jitter (the "RMSΔ" field in the figure) in the sine wave zero crossings of about 7ps. For the ΔΣM output, the rms jitter is 18.7ps, and there it is clear that the tail of the distribution descends more gradually to the right than the left as expected for a metastable quantizer. The same measurement was taken five times, and rms jitters of $\{18.2, 18.3, 18.7, 19.2, 21.2\}$ps were measured, so it is hard to specify an exact value.

In theory, the effect of metastability could be removed if we captured a bit stream and found its spectrum. Again, the author had brief access to an 8Gs/s oscilloscope which could sample and hold 128k data points. The scope thus sampled the 4Gs/s bit stream twice per bit, and then the odd or even 64k samples could be downloaded to a computer and a spectrum taken. For a 1GHz -15dBm input, Figure 7.40 shows the 16 averaged 4096-point Hann-windowed periodograms of the bit stream. Annoyingly, this data was captured before the author fully understood the ΔΣM, hence the biases were set incorrectly: we used $V_Q = 2.6$, which is nowhere near high enough for a deep noise notch. As a result, this spectrum has a similar noise floor to that observed on the

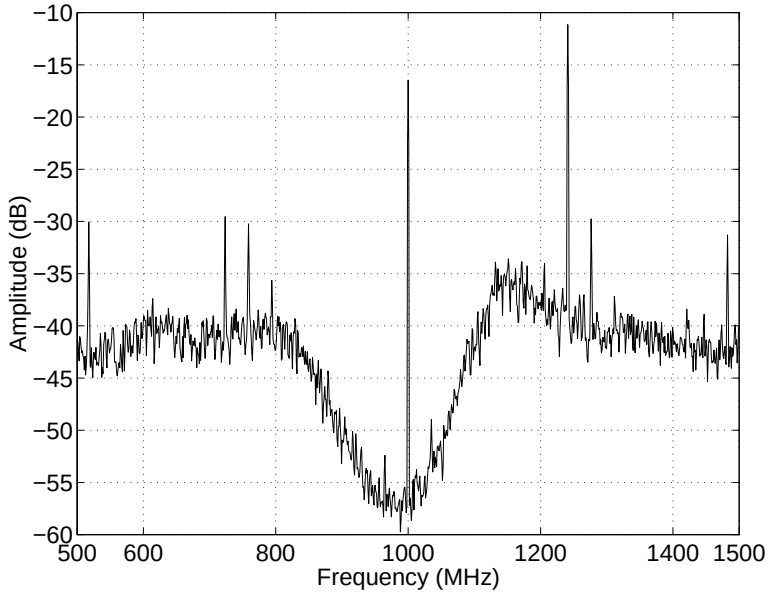


Figure 7.40: Output spectrum of captured bit stream.

spectrum analyzer and many spurious tones.

7.3.3 Output Buffer

There is not much to test on the output buffer itself. Figure 7.41 are output spectra for $V_{BUF} = 2.0$V and 3.0V. From Figure 7.24, such a change should result in a supply-current increase from about 2mA to about 4mA, and we measure it to go from 87.8mA to 90.0mA. Furthermore, doubling the switching current should mean double the output voltage swing and hence 6dBm more spectral power total; the measured increase is about 5dBm.

7.3.4 DAC

Changing V_{n2} in the NRZ modulator should affect the amplitude of the input tone as it appears in the output spectrum according to (7.31). Figure 7.42(a) is the output magnitude of a 1.003GHz -36dBm input tone as V_{n2} varies, both measured and calculated. Once again the shapes of the curves agree quite well. The supply current rises approximately 400μA over the range $V_{n2} = 0.2$V

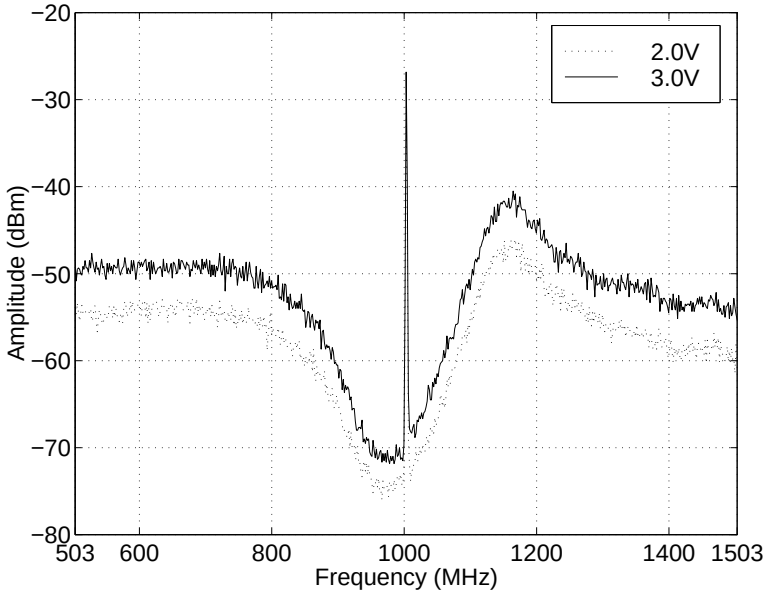
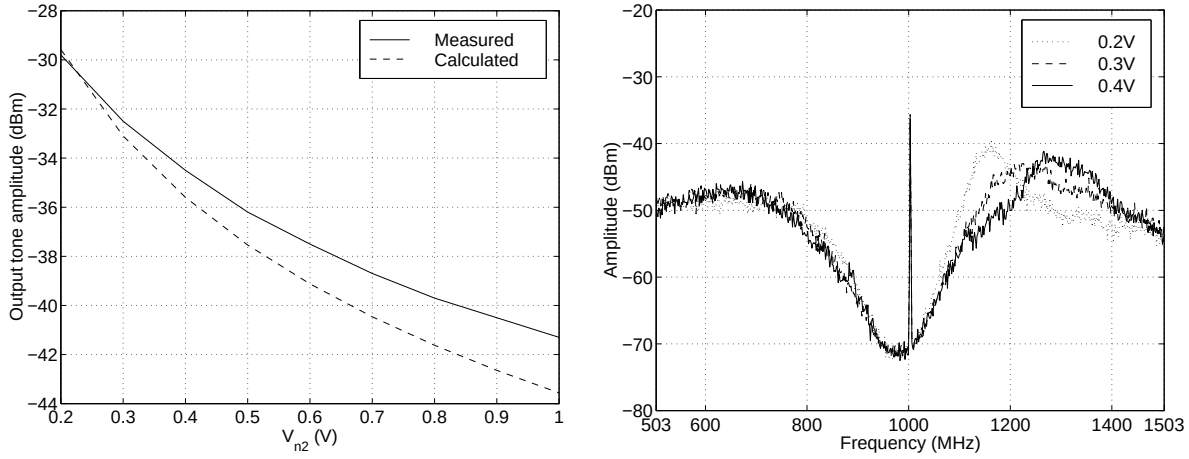
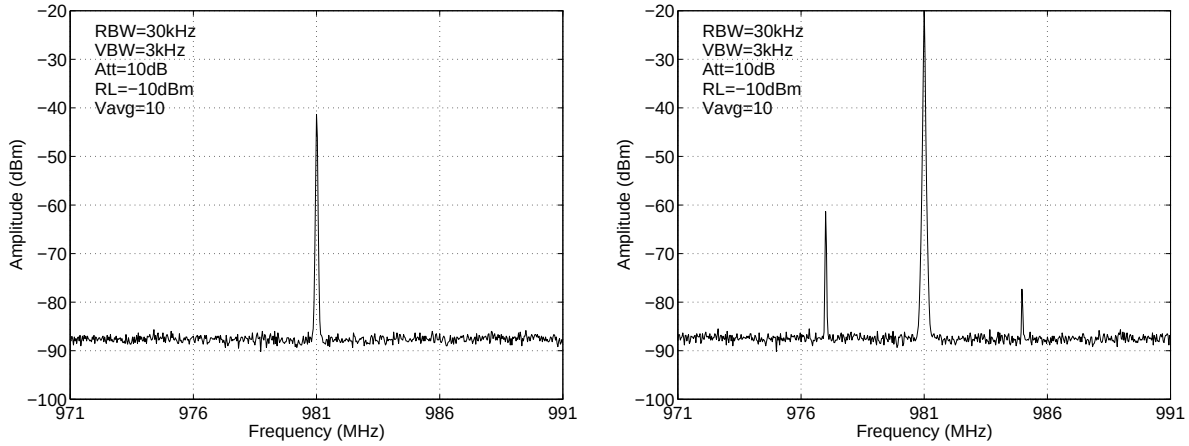


Figure 7.41: Varying V_{BUF}.



(a) (b)

Figure 7.42: Changing V_{n2}: (a) tone magnitude at output, (b) overall spectrum.



(a) (b)

Figure 7.43: Measured modulator spectra: (a) $V_{in} = -40$dBm, (b) $V_{in} = -20$dBm.

to 1.0V, which concurs with Figure B.4.

Otherwise, changing DAC voltages should affect the loop filter zero locations and hence the noise shaping. Figure 7.42(b) shows that an NTF pole moves up in frequency and further towards the middle of the z plane as V_{n2} is increased; a similar movement of this pole is observed in simulation in the RK4 program. Many other such examples could be demonstrated, but this one gives the general idea.

7.3.5 Dynamic Range

It is clear from the spectra presented in this section that the actual noise notch center frequency is approximately 980MHz. Thus, for a DR plot, we set $f_s = 3920$MHz, four times this value, and apply an input tone at 981MHz. We choose to consider a bandwidth of 20MHz (i.e., OSR $= 100$), which is what we assumed in Table 7.1. Typical in-band spectra appear in Figure 7.43; the noise floor is white with a level of about -130dBm/Hz. In a 20MHz bandwidth, the total noise power is thus -57dBm, and in Figure 7.43(a), the signal power is -42dBm, which gives SNR $= 15$dB. An input 20dBm larger shows much output harmonic distortion, as seen in Figure 7.43(b). From (7.31) and the circuit voltages, the full-scale input for these conditions is about -14dBm.

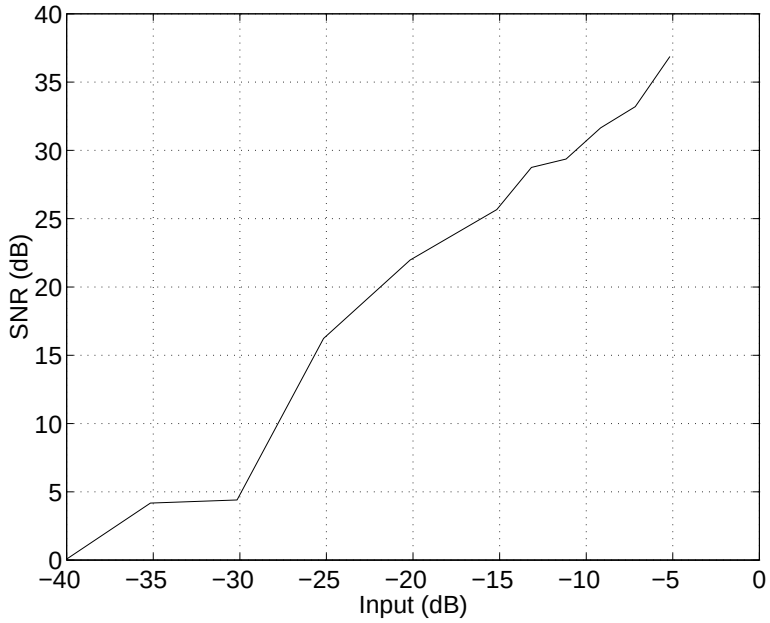


Figure 7.44: Dynamic range plot for NRZ modulator in 20MHz bandwidth.

Figure 7.44 shows the DR plot for the NRZ modulator, where spectra with 20MHz bandwidth were captured and the SNR calculated in Matlab. This SNR stays positive for inputs up to 0dB, but it is difficult to know how to calculate it fairly for large inputs because of strong harmonic content and distortion of the input signal. In any event, the peak SNR is 37dB and the DR is about 40dB, which makes this a 6.3-bit converter. The SNR value agrees well with our prediction in Table 7.1. The modulator consumes about 450mW from a single 5V supply. With a -5dB input, the harmonic at 977MHz dominates, and the SFDR is found to be approximately 48dB. In a narrower bandwidth, SNR performance would be better, improving at 3dB per octave of oversampling, though spurs can exist even in very narrow bands and thus SNR performance might still be limited.

7.4 Result Commentary

The performance of the modulator is disappointing, certainly, though a good deal was learned in the process of simulating and testing it.

7.4.1 Design for Testability

In *all* circuit designs, it is important to think about how the circuit will eventually be tested, and if possible, to design so that testing is facilitated. This becomes more necessary, indeed crucial, as the speed at which the design must operate increases. Though they may seem obvious, a number of points came up in the testing of this ΔΣM which deserve to be mentioned.

Individual block breakouts

It is a major boon if the individual circuit blocks are broken out of the whole circuit for separate testing, particularly in a relatively new manufacturing process (as was the case at the time this ΔΣM was made). Each block usually has fewer settable parameters than the entire circuit, which offers two advantages: it can likely be tested on-wafer with a standard probe arrangement, and the parameter space for a block can be rapidly explored. Furthermore, if one block operates differently than expected, this can be found by testing the block by itself rather than observing its effect on the output of the full circuit. The main disadvantages of breakouts are the increased amount of die area consumed and that special input and output buffers might need to be designed to test a block by itself. Experienced designers building a familiar circuit in a well-characterized process might have less need to heed this advice, but following it would have been beneficial here.

Tunability

How to choose the number of tunable parameters in a design is not always obvious. On the one hand, one would like to be able to control as much as possible when the process is unfamiliar or new. On the other hand, using a large number of parameters can lead to a testing nightmare—how can one be sure the design is tuned to give optimal performance when the parameter space is huge? For a first cut, tunability is probably a good idea, though for an actual product, over temperature and process variations, parameters must stabilized either by design or through stabilizing circuitry. At times during testing, this author found the amount of tunability in this design frustrating, but in the end it was probably prudent.

Data capture

A designer must anticipate how the circuit output(s) will be observed. For GHz-speed ΔΣM this is particularly relevant: how does one plan to capture the high-speed bit stream? For measurements directly in the frequency domain, one must remember that spectrum analyzers have a certain noise floor and that they are sensitive to analog imperfections in the waveform. Likewise, for time domain measurements, fast sampling scopes cannot necessarily sample very *deep*; getting enough bits for a reasonable spectrum (like 16k or more) might be nontrivial. Worth considering is an on-chip demux, for example 1:16 in the 4GHz design in [Rag97], which groups the bits into 16-bit 250MHz quantities which can be brought off-chip to a fast logic analyzer.

Packaging and board design

These are two more important factors in high-speed test. If the circuit can be tested on-wafer, so much the better, but if packaged testing is required, the board design and packaging can have a major impact on the measured performance. The test board for this circuit seemed well-designed to the author, but the package left a good deal to be desired: the footprint was $7 \times 7\text{mm}^2$ for a $2.5 \times 2\text{mm}^2$ die, which meant very long bond wires between the package pins and the die surface. We explore the effect of bond wire inductance in the following section.

7.4.2 Known Circuit Problems

This design was a first cut. The author is fairly certain that it was thrown together in a very short space of time for a tight deadline; that it works at all is a testament to the design skill of Mr. Gao. Even so, there are many areas in which, upon further examination, things could have been done better, a list of which follows.

Improper architecture choice

A modulator with half-delayed NRZ (HNRZ) feedback is a bad idea because it produces a different pulse shape when there are two of the same output bit in a row. To illustrate, suppose the

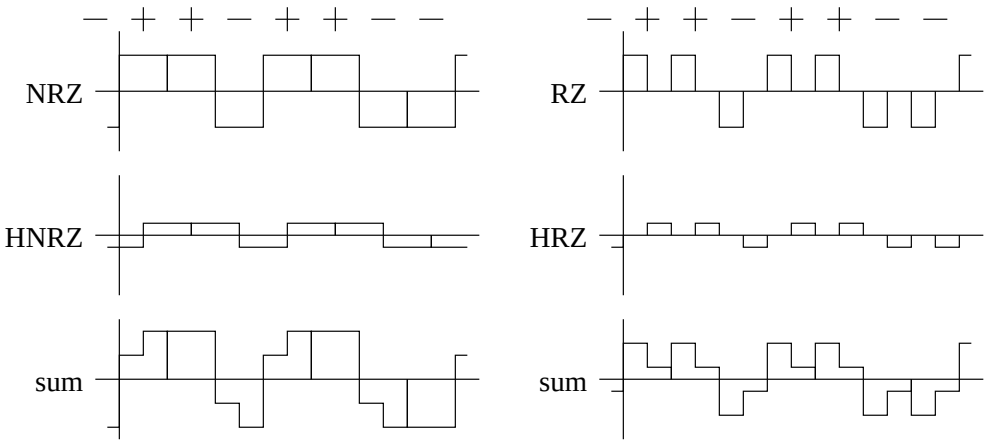


Figure 7.45: Illustration of nonuniform feedback caused by a half-delayed NRZ DAC.

modulator output goes $\{- + + - + + - -\}$, where $-$ is a -1 and $+$ is a $+1$. In Figure 7.45, the DAC pulses that would result from such a sequence are depicted for NRZ/HNRZ and RZ/HRZ modulators. At the feedback, the pulses are summed which results in the feedback waveforms in the bottom graphs. It is apparent that for two or more of the same output bits in a row, the waveform sum for the first bit looks different than for all the remaining bits in the NRZ/HNRZ case; by contrast, the waveform sum in the RZ/HRZ case looks identical for every $+$ and $-$ no matter how many of the same bit occurs sequentially. This nonuniform feedback sum means a modulator employing HNRZ feedback cannot implement mth-order noise-shaping in a BP ΔΣM of order m; it introduces additional numerator terms in the equivalent $H(z)$ which would require additional feedbacks to compensate.

One might ask, therefore, why all the test results in §7.3 were done on the NRZ modulator rather than the RZ modulator. There are three reasons. First, the HNRZ feedbacks were set to zero so that they did not affect modulator performance. Second, it is easier to calculate the full-scale amplitude for the NRZ modulator than the RZ modulator. Third, a modulator employing HNRZ feedback is nonideal only if the performance is limited by quantization noise alone; in our circuit, white noise filled in the noise notch. The performance of the RZ modulator was no better than the NRZ modulator, so it did not matter which we measured.

Output bit taken from wrong point in feedback

As we said in §7.3.2, the output bit V_{out} for the modulator comes from the M/S latch output. Instead, it should be taken from the one-delayed latch outputs to reduce edge jitter. This would matter less if there were an easy way to capture the bit stream, but when using a spectrum analyzer to measure performance, it matters more.

No input or clock matching networks

If this modulator were to be used in a radio receiver, matching between the driving circuit (perhaps a mixer) output and modulator input is important because the mixer would be sensitive to reflections due to mismatch. Moreover, the impedance level seen by the driver matters because it determines the actual signal amplitude at the modulator input. No apparent attempt was made to match the input to a source, 50Ω or otherwise.

An approximate model for what the source actually sees appears in Figure 7.46 [Szi98], where

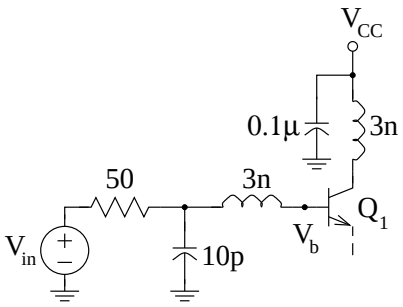


Figure 7.46: Model of actual circuit input.

the inductors represent the bond wires (1mm of bond wire has about 1nH of inductance), the 0.1μF capacitor is a power supply decoupling capacitor on the circuit board, and the 10pF capacitor is the package pin capacitance. A more accurate model would include the SMA connector model, the 50Ω transmission line on the circuit board, and the pad capacitance, but this will do for our purposes. Transient analysis in SPICE for the input transistor shows that a 1GHz signal at V_{in} gets reduced by 10.5dB at V_b; for the clock transistor and a 4GHz input, the attenuation is close to 20dB. It was this knowledge that allowed us to write (7.35), the actual input amplitude seen at V_b

relative to the reading on the signal generator.

Clock jitter due to circuit noise

The input-referred noise voltage at the base of the clock input buffer causes a deviation in the zero-crossing of the clock voltage, i.e., clock jitter. In Figure 7.47, near a zero crossing of the clock

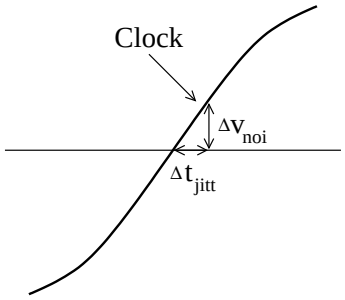


Figure 7.47: Clock jitter caused by circuit noise.

waveform, circuit noise Δv_{noi} causes a time jitter Δt_{jitt}. For a clock given by

$$V_{clk} = A_{clk} \sin 2\pi f_s t, \tag{7.38}$$

Figure 7.47 allows us to write

$$\frac{\Delta v_{noi}}{\Delta t_{jitt}} \approx \left. \frac{dV_{clk}}{dt} \right|_{max} \tag{7.39}$$

because the clock zero crossings are at the point of maximum slope of the clock waveform. Solving for Δt_{jitt} gives

$$\Delta t_{jitt} = \frac{\Delta v_{noi}}{2\pi A_{clk} f_s}; \tag{7.40}$$

writing $\Delta v_{noi} \equiv \sqrt{\overline{v_{nc}^2} f_s}$ and solving yields

$$\sigma_\beta \equiv \Delta t_{jitt} = \frac{\sqrt{\overline{v_{nc}^2} f_s}}{2\pi A_{clk}} T_s. \tag{7.41}$$

SPICE ac analysis tells us that the input-referred noise voltage at $f_s = 4$GHz for the clock transistor is $\overline{v_{nc}} = 3.56\text{nV}/\sqrt{\text{Hz}}$, so for $A_{clk} = -4\text{dBm} = 0.2\text{V}$,

$$\sigma_\beta = 1.8 \times 10^{-4} T_s. \tag{7.42}$$

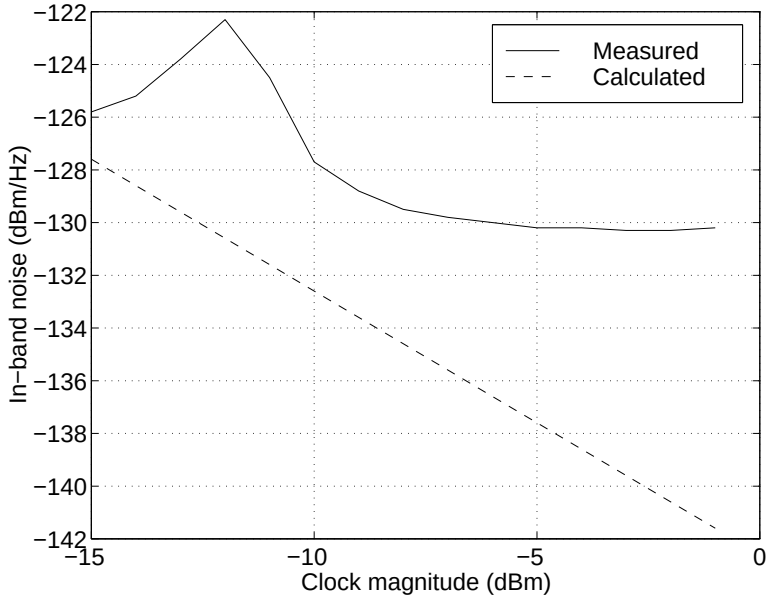


Figure 7.48: Measured in-band noise as a function of clock magnitude.

The measured in-band noise as a function of the dBm reading on the clock signal generator appears in Figure 7.48. There should be some way to relate this to (5.13), (5.19), (7.36), Figure 7.47 for the actual clock level on chip, and (7.41), which is plotted with the dashed line in the figure. The calculation can only be *very* approximate because of the uncertainty of many of the parameters, and the reality seems to bear little resemblance to the calculation. The author has found that clock amplitude has some bearing on τ_{rg}, the latch regeneration time, which in turn affects the metastability behavior of the latch; this is a complicated effect to model, and it might be responsible for the observed behavior. At this time, there is too little information to tell.

Misdesigned emitter followers

Emitter followers appear frequently in ECL designs, typically as interstage buffers, drivers, and/or level shifters. There are two important design parameters for followers: the bias current and the transistor size. Bias current is chosen to be large enough to drive the load of the following stage, but not so large as to waste power. Transistor size is determined by, among other things, bias current,

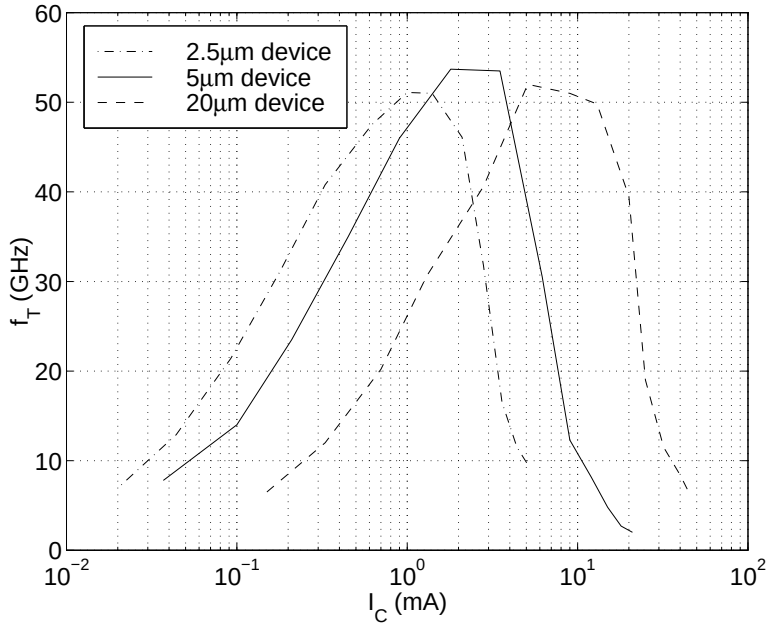


Figure 7.49: Measured f_T vs. I_C curves for SiGe BJTs.

where usually one chooses a transistor that operates at its peak f_T given I_C; loading, because C_μ in output buffers connects to analog ground and hence appears as an amplifier load; and noise, where if input-referred noise is important, a larger device should be used because its extrinsic base resistance is lower.

The majority of the followers in this design are devices with 20μm emitter widths and $10\text{k}\Omega$ emitter resistances. Figure 7.49 shows f_T against collector current for fabricated 2.5μm, 5μm, and 20μm devices. The typical voltage level at the emitters of these followers ranges between 2.5V and 4V, which means the bias current level is between $I_C = 250\mu$A and 400μA. From the figure, the 20μm device has an f_T from 10GHz to 13GHz; clearly, this is nowhere near the device's peak f_T. Fortunately, followers can be forgiving: Figures 7.50(a) and (b) show the input and output voltages of the resonator output buffers in Figure 7.28, and we see that the voltages are being reproduced faithfully despite the low bias current. The place where we get into trouble is in the preamplifier and half-latch, as we now detail.

Consider once again the preamplifier in Figure 7.21(a). The common-mode level at V_{Pin} is typ-

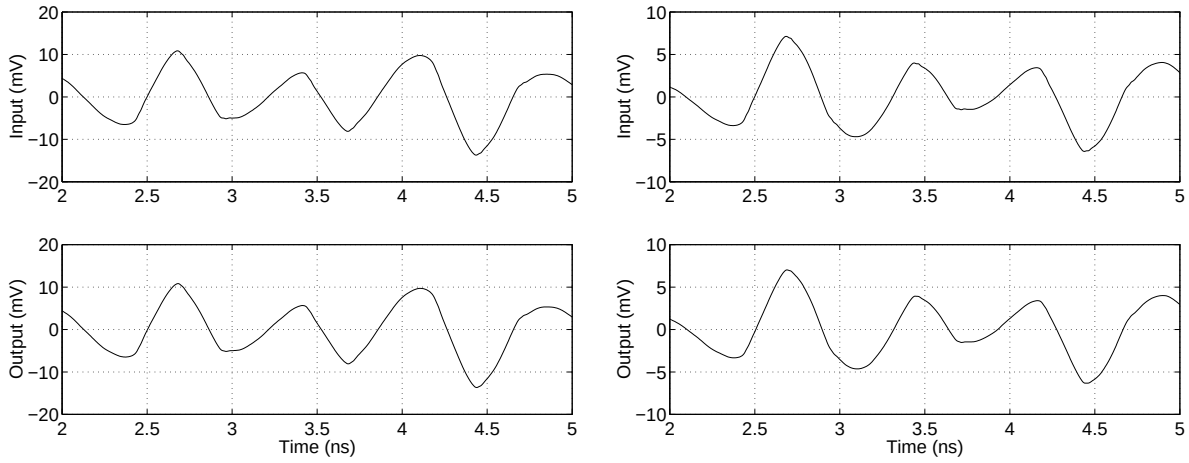
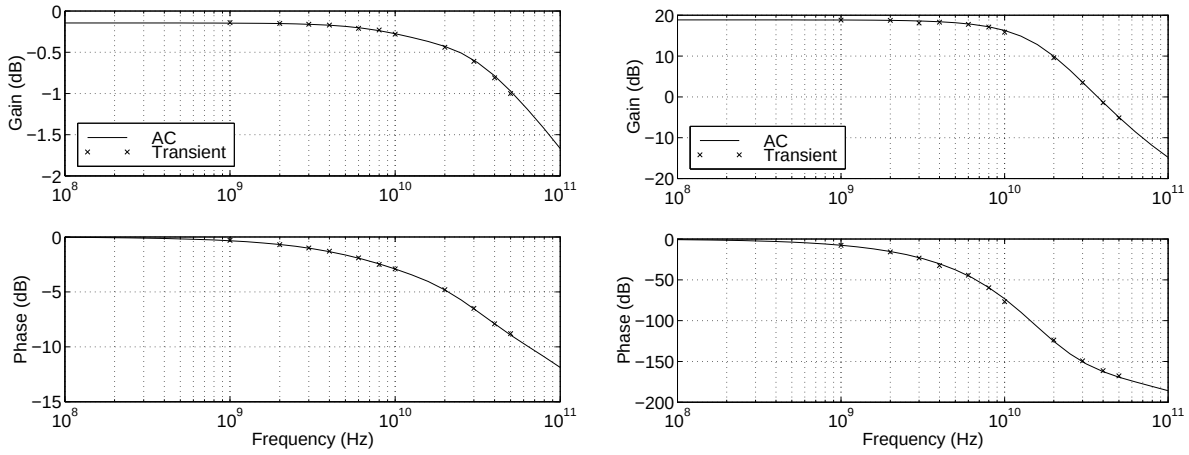


Figure 7.50: (a) First and (b) second resonator output buffer waveforms.

ically about 3.4V, which means 2.6V at the emitters of the input followers; with a $10\text{k}\Omega$ resistance, we can calculate $I_C \approx 250\mu\text{A}$. This is not nearly enough to drive the C_μ of the diff pair which is magnified by the Miller effect. The output followers are large devices whose C_μ together with the diff pair load R_{pa} create a largish RC time constant. These two factors, insufficient input drive and large output loading, resulted in the rolloff at 4.6GHz in Figure 7.22(b). Resizing the devices and changing R_{ef} appropriately results in the improved performance in Figure 7.51. The input followers are still 20μm, but $R_{ef} = 400\Omega$ instead of $10\text{k}\Omega$, which gives them much higher drive ($I_C = 6$mA) and operates them closer to their peak f_T. Consequently, in Figure 7.51(a) we observe only 0.13dB of rolloff and $-2.9°$ phase shift at 10GHz. Shortening the output followers to 5μm reduces the loading on the amplifier output nodes, and $R_{ef} = 2\text{k}\Omega$ sets $I_C \approx 2$mA which according to Figure 7.49 operates the devices near their peak f_T. The overall preamp ac response appears as in Figure 7.51(b): the low-frequency gain is 18.9dB, the corner frequency is 10.8GHz, and the phase shift there is $-78.2°$. This is a substantial improvement in corner frequency compared to the 4.6GHz in the original preamp in §7.2.2

Similar problems exist in the half-latch, Figure 7.21(b). In §6.2.1 we noted that the regeneration time constant τ_{rg} of this style of latch is related to the GB product of the regenerative quad; in turn,

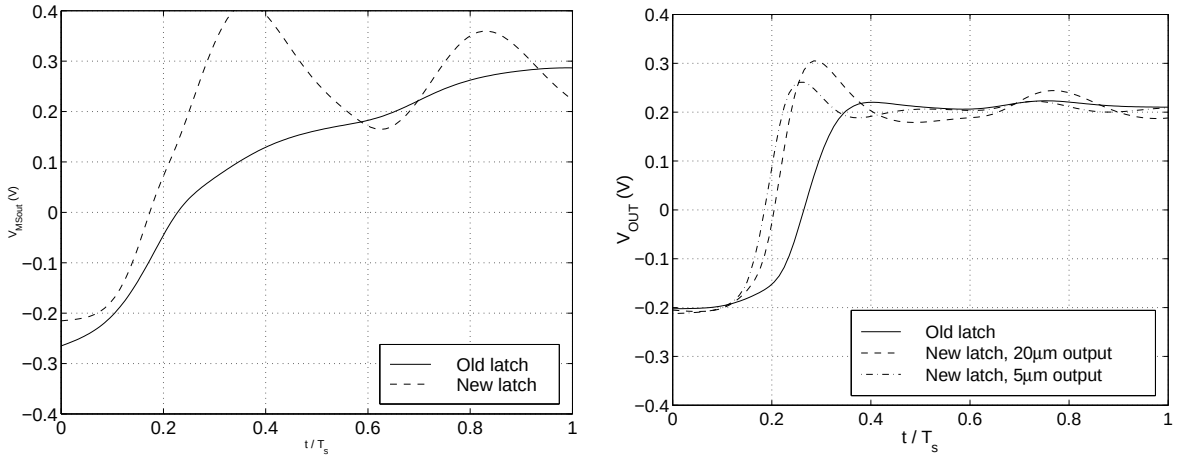


(a) (b)

Figure 7.51: Optimized preamp ac analyses: (a) input follower, (b) entire circuit.

this GB product is affected by V_{EN} (which controls the current I_{le} in the diff pair in the quad), the capacitance at both nodes V_{Lmid} and V_{Lout}, R_{la}, and the drive of the output follower. We stated in §6.4.2 that making the latch as fast as possible doesn't do much to improve the performance lost due to metastability; this was assuming the latch was at least *close* to optimized, which this one is not. With a 20μm output follower and $R_{ef} = 10\text{k}\Omega$, SPICE transient analysis gives $\tau_{rg} = 17.4$ps. This has the same two problems as before: large loading at V_{Lmid} due to C_μ of the follower and inadequate drive of the Miller capacitance of the next stage's amplifier. Sticking with a 20μm transistor and changing R_{ef} to 500Ω helps greatly with the drive aspect, lowering τ_{rg} to 12.3ps, but the loading is larger than necessary. This can be seen by using a 5μm transistor and $R_{ef} = 1.5\text{k}\Omega$, which gives $\tau_{rg} = 10.4$ps. Going to a smaller device like 2.5μm reduces loading still further, but such a device cannot drive as much current without itself slowing down; the optimal R_{ef} seems to be about $2\text{k}\Omega$ for such a device, in which case $\tau_{rg} = 10.9$ps. The best tradeoff between loading and drive in this design, therefore, seems to be 5μm and $R_{ef} = 1.5\text{k}\Omega$.

How much difference would a proper design make? Figure 7.52(a) contrasts the original M/S latch output waveform from Figure 7.25(a) (the solid line) with the output waveform resulting from a latch with redesigned followers. The new output buffer wave in Figure 7.52(b) crosses



(a) (b)

Figure 7.52: Output waveforms: (a) M/S latch, (b) output buffer.

zero earlier (i.e., the output buffer responds more quickly), but at the cost of a large overshoot in Figure 7.52(b). This is partly as a result of the ripple in the latch output, but also because there is a good deal of coupling from the bases of the output buffer diff pair through the Miller capacitor C_μ to the collectors. We can reduce the severity of the coupling by using smaller transistors; replacing the 20μm devices with 5μm devices yields the dash-dot output waveform in Figure 7.52(b). The overshoot has been cut approximately in half, and moreover we have achieved a slight speed increase (note that the zero crossing now occurs slightly earlier) because we have lowered the Miller capacitance which the latch output has to drive. Moreover, a 5μm device is still capable of operating quickly at $I_C = 4$mA (recall Figure 7.49). To be fair, however, the speed of the output buffer is not likely to be that important—as long as a recognizable bit comes out, we are not concerned overmuch with speed.

If we use the newly-optimized circuit components, we find $\rho_d = 1.255$ and $\rho_r = 0.113$ from the dotted line in Figure 7.53. Once again, the emitter followers in the DAC (which isolate the final latch output from the DAC switching transistors) appear to be biased at too low a current for optimum speed, in this case $I_C \approx 300\mu$A. If we choose $R_{ef} = 1.2$kΩ, the DAC output waveform is the dash-dot line in Figure 7.53, and now $(\rho_d, \rho_r) = (1.214, 0.894)$. However, the ringing out of

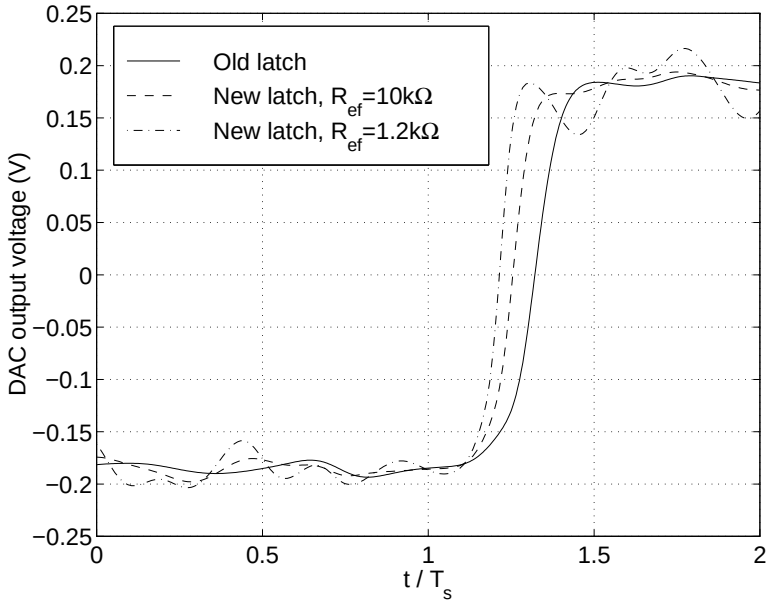
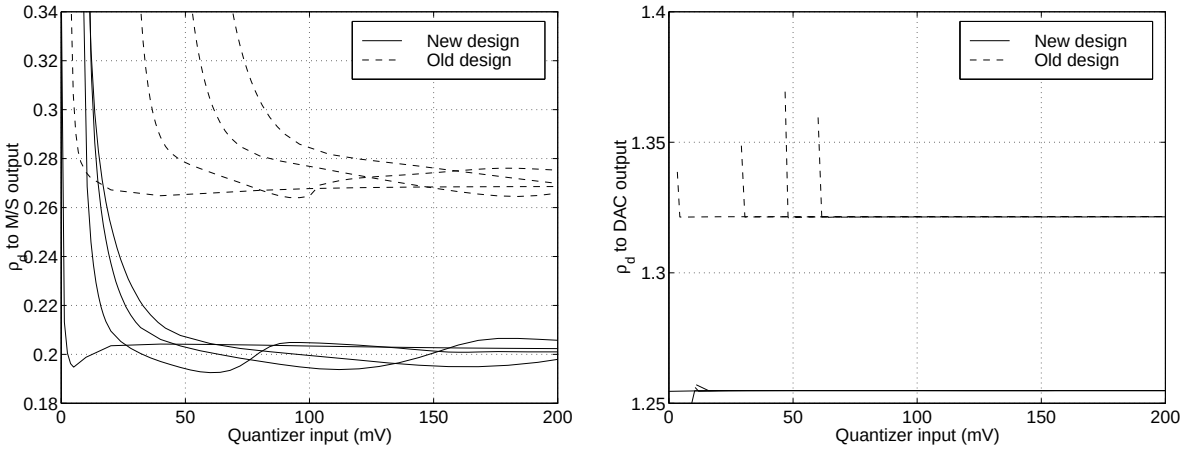


Figure 7.53: Dynamic DAC output voltage.

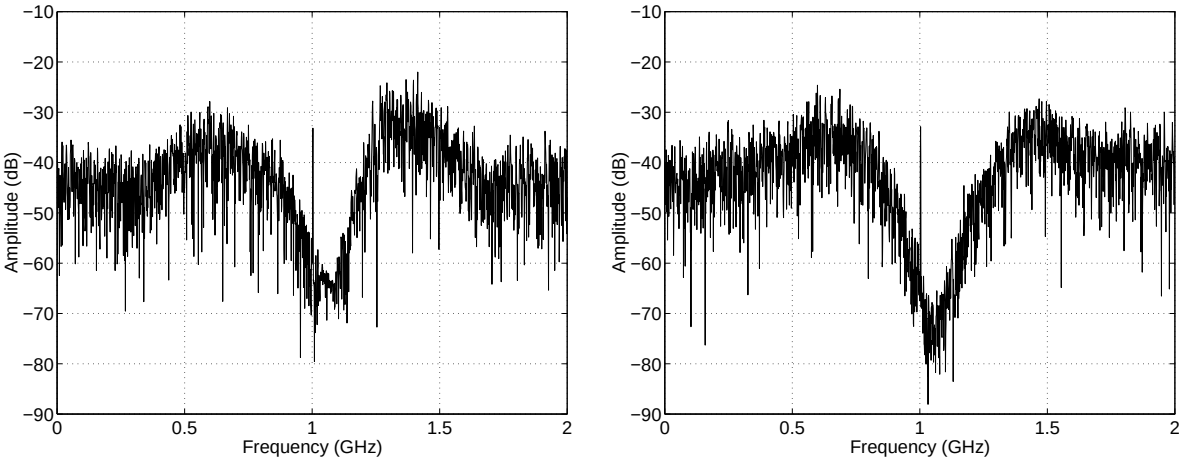
the final latch stage appears much more strongly at the DAC output, which might be undesirable. This could be reduced by adding cascode devices in the collectors of the DAC output transistors, or more simply by leaving $R_{ef} = 10\text{k}\Omega$ in the DAC followers—we only gain an additional 4% of excess delay, which could easily be compensated by appropriate V_k tuning. And, once again for fairness, the more important thing is that the amount of delay be relatively fixed—Chapter 6 taught us *variance* of σ_{DPW} is to be avoided for optimal performance.

The final proof, though, comes from (painfully slow) full-circuit SPICE simulation. Figure 7.54 illustrates the improved ZCT characteristics, which have much less hysteresis and also steeper slopes. Figure 7.55(a) is a 4096-point spectrum for the original modulator, and Figure 7.55(b) is for the modulator with the redesigned followers. The spectra are for $V_{Q1} = V_{Q2} = 3.15\text{V}$ in SPICE, which seems to be about the maximum value which keeps the modulator stable, and the output bits are taken from the one-delayed latch output. The in-band noise for $\omega_0 = 1.06\text{GHz}$ and OSR $= 100$ improves from -50.3dB to -57.3dB—over one full bit. Thus, maximizing the speed of the followers matters for performance. As usual, the price to be paid is increased power: in this



(a) (b)

Figure 7.54: New ZCT characteristics for (a) M/S latch output, (b) one-sample delayed output.



(a) (b)

Figure 7.55: SPICE output spectra for (a) original modulator, (b) optimized modulator.

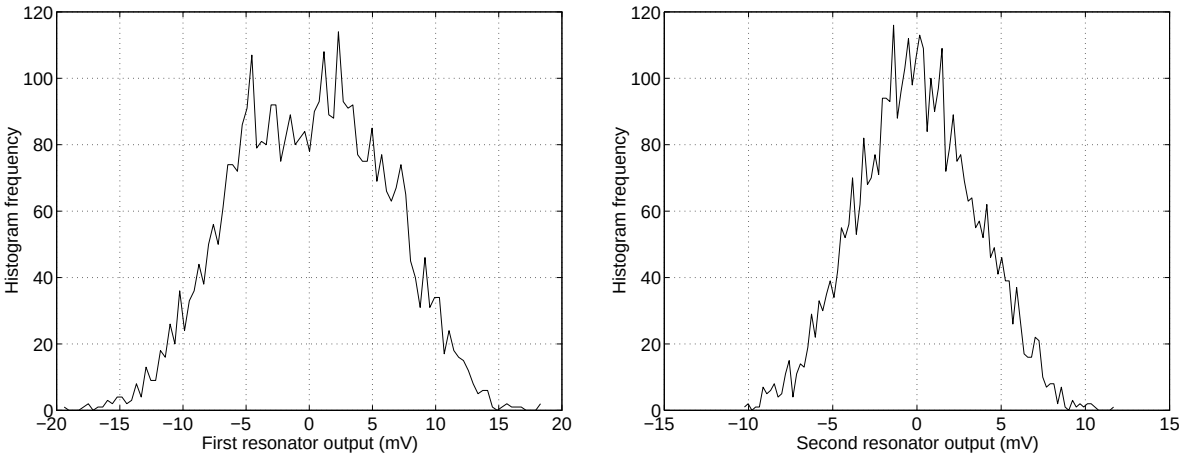


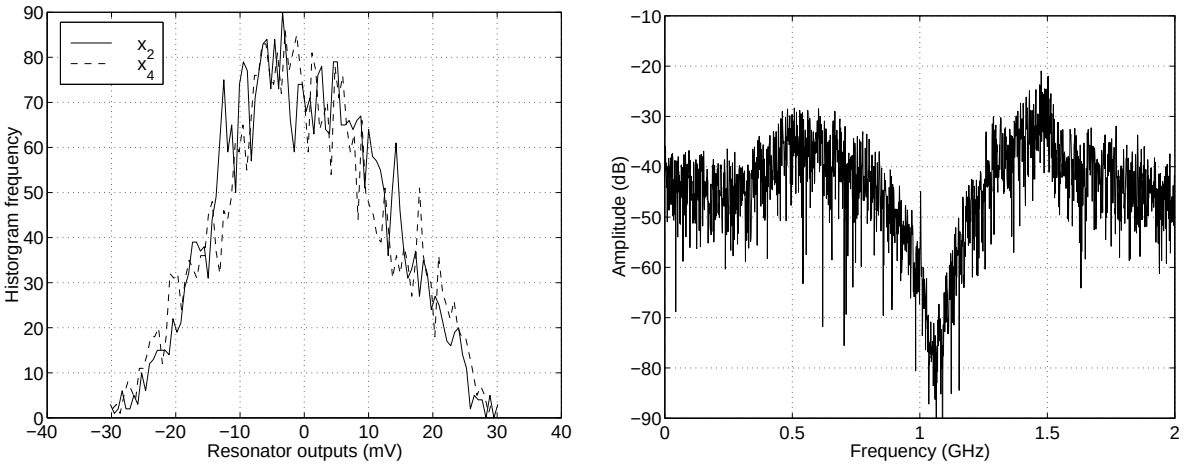
Figure 7.56: Resonator output voltage histograms from SPICE.

design, we estimate the suggested biasing would result in about 50% greater power consumption.

Resonator output signal scaling

The last problem comes out from closer examination of the voltages at the resonator outputs in SPICE. Figure 7.56 shows histograms of these voltages for the conditions at the start of §7.3: the first resonator ranges over about ± 20mV, the second over ± 10mV, and Matlab gives $\sigma_{x_2} = 6.0$mV and $\sigma_{x_4} = 3.5$mV. This latter value drives the quantizer, and we can see from the dashed lines in Figure 7.54 that it is too small for the quantizer to make a reliable decision—there will be a severe amount of hysteresis. As we noted in §7.2.2, the combination of quantizer hysteresis *and* small quantizer input signal is detrimental to this modulator. Even our redesigned quantizer has trouble with these signals at high speeds.

We find that we can raise the swings to $\sigma_{x_2} = 11.7$mV and $\sigma_{x_4} = 12.3$mV if we use $k_{n2} = k_{n4} = 500\mu$A instead of 200μA and 100μA, respectively; this makes sense because we know those swings to be proportional to k from §7.1.1. Figure 7.57(a) shows the new resonator output distributions, and Figure 7.57(b) plots the spectrum from SPICE. The in-band noise comes out to -63.3dB, over two bits better than the -50.3dB obtained with the smaller ks and original quantizer. If we desired to increase these swings still further, we could replace the R_{DAC} resistors in

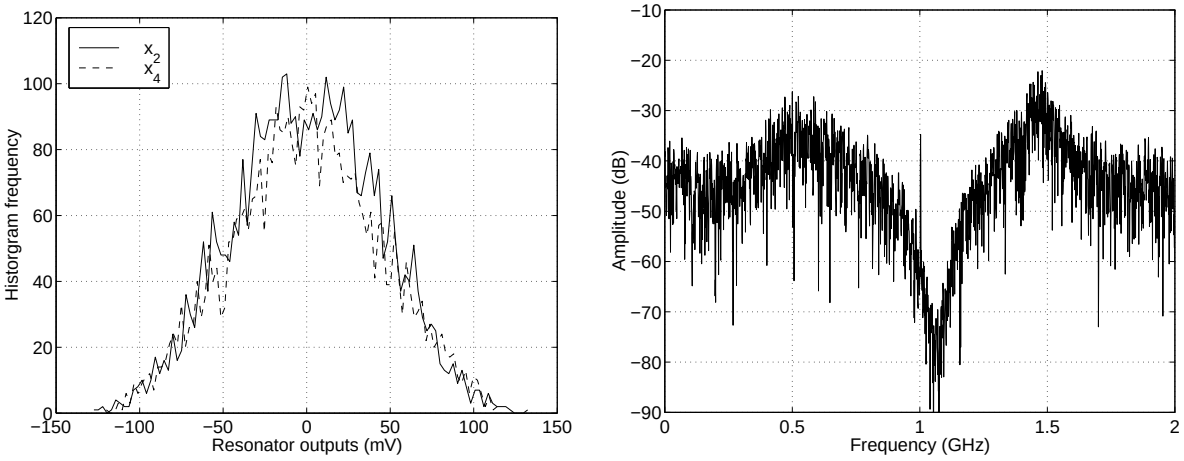


(a) (b)

Figure 7.57: Scaled DAC currents $k_{n2} = k_{n4} = 500\mu$A: (a) resonator output histograms, (b) output spectrum.

Figure 7.26 with something smaller; at present they are $2\text{k}\Omega$, and given that $V_k = 1.0$V maximum, the maximum current is fixed at $1/2\text{k} = 500\mu$A. Another SPICE simulation was carried out with $R_{DAC} = 560\Omega$, where the ks were 1.8mA, and the output distributions and spectrum are shown in Figure 7.58. We have now achieved $\sigma_{x_2} = 43.1$mV and $\sigma_{x_4} = 43.8$mV, though the in-band noise is no better than with 500μA of current, -61.7dB, while the power dissipation has increased. It might be that the actual modulator would perform a little better with these much larger swings; SPICE is too slow to run many simulations and average the periodograms to give us a more accurate idea of the in-band noise.

More importantly, though, we must recognize that this modulator's DR is not limited by quantization noise: we found in Table 7.1 that G_{g1}'s dynamic range is such that the maximum SNR we can expect is 52dB or so. This is based on the IIP_3 of G_{g1} and on the input-referred noise; what does SPICE say about this latter quantity at the three different currents? Table 7.3 shows simulations of the ac input-referred noise, which is the same as the minimum input signal u_{min}. At $k = 500\mu$A, we see the total noise drops a little, and this gives a G_{g1}-limited performance of about 55dB (IIP_3 for G_{g1} is still the same, -2.3dBV). As we raise the ks to 1.8mA, the input-referred noise increases again, and we are back to 52dB of performance. More significantly, as currents



(a) (b)

Figure 7.58: Scaled DAC currents $k_{n2} = k_{n4} = 1.8$mA: (a) resonator output histograms, (b) output spectrum.

increased, the normalized nonlinearity parameters of the *other* transconductors start to increase. In particular, G_{g2} is coming perilously close to the recommended -20dB maximum in (7.28).

In conclusion, then, scaling the DAC currents would result in a theoretical performance limit of about 55dB, or 9 bits, based on the noise and linearity of the first transconductor. This scaling is also beneficial for helping the latched comparator resolve the quantizer input voltage correctly.

7.4.3 Unaddressed Circuit Issues

We have taken into account a good number of factors that affect the performance of this ΔΣM, but there are a number that would need more thorough investigation in a final design.

Resonator center frequency and instability voltage

Simulations in SPICE seem to predict a resonator with a center frequency of about 1.06GHz, Figure 7.19 and Figure 7.55. The measured frequency appears closer to 980MHz, Figure 7.35. As well, in §7.4.2 SPICE predicts oscillation of the resonators in an operating modulator at $V_Q = 3.20$V, but the measured value was $V_Q = 3.32$V, Figure 7.35. Why the differences between the two?

Table 7.3: Comparison of modulators with different feedback currents.

k_{n2}	0.2mA	0.5mA	1.8mA
k_{n4}	0.1mA	0.5mA	1.8mA
σ_{x_2}	6.0mA	11.7mA	43.1mA
σ_{x_4}	3.5mA	12.2mA	43.8mA
IBN (SPICE)	-50.3dB	-63.3dB	-61.7dB
$u_{min} = \overline{v_{ng1}}$	90μV	60μV	90μV
SNR due to G_{g1}	52dB	55dB	52dB
$\bar{\epsilon}_{q1}$	-61.1dB	-56.4dB	-44.9dB
$\bar{\epsilon}_{g2}$	-44.7dB	-38.5dB	-27.6dB
$\bar{\epsilon}_{q2}$	-65.1dB	-55.8dB	-44.7dB

It is hard to say for certain. It might simply be due to process variations, but a reasonable conjecture about the center frequency involves the T-shaped strip of metal in Figure 7.30 connecting the inductors to the pads in the center of the die on the left- and right-hand sides. An $l\mu$m $\times$ $w\mu$m strip of this metal [Mar98] has a resistance of $15\text{m}\Omega/\square$ and an inductance of

$$L_{par} = 2 \times 10^{-4} l[\ln(\frac{2l}{w}) + 0.5] \text{ nH}. \tag{7.43}$$

The arms of the T are each 100μm $\times$ 20μm, which gives $L = 0.056$nH and $R = 0.075\Omega$, and the long strip of metal is 440μm $\times$ 20μm, which gives $L = 0.377$nH and $R = 0.33\Omega$. This long strip is equivalent to two strips in parallel, one for each inductor, giving a total additional inductance and resistance of $L_{par} = 0.81$nH and $R_{par} = 0.74\Omega$ in the LR branch in Figure 7.2. The center frequency changes from

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 1.089\text{GHz} \rightarrow \frac{1}{2\pi\sqrt{(L + L_{par})C}} = 981.6\text{MHz}, \tag{7.44}$$

which looks approximately correct. The instability voltage (which is determined by the coefficient of s^1 in the denominator of (7.14)) might also explained by these parasitics: $R/L = 0.70$, but $(R + R_{par})/(L + L_{par}) = 0.74$, which means a higher G_q in (7.37) would be needed to change the sign of the s^1 coefficient from positive to negative. However, to predict it exactly, we would need

to be sure that (7.37) was correct, and C in the s^1 coefficient likely includes some parasitics of its own.

Thermal noise and linearity

The smallest noise floor we observe on the spectrum analyzer had a power of about -130dBm/Hz. We have been assuming that this was caused by the analog properties of the output waveform, which is certainly reasonable, but it might also be affected by the input-referred thermal noise of the modulator being amplified to the modulator output, or indeed from the measurement noise floor of the spectrum analyzer itself. In a proper design, we would capture the bit stream and take its FFT, thus obviating the need to know the spectrum analyzer measurement limit, but we would still need to know the effect of circuit thermal noise. Our setup is not terribly suited to measuring, for example, input-referred thermal noise; the best we can do is estimate it from simulation as we have in §7.2.1.

We are also not well set-up to measure the third-order intercept point of the modulator. We estimated the 1dB compression point from simulation in §7.2.1, but in a real circuit we would need to have an easy way to do a two-tone test. Here, we did observe some gain expansion for large input amplitudes in Figure 7.44, but we did not make much attempt to quantify them.

Phase noise of sources

While there will be some circuit noise added to the clock input voltage as explained in §7.4.2, the phase noise of the signal generator itself will matter in a final design. The author was not able to observe significant skirts on the input tone in the output bit stream spectrum, perhaps because these skirts were below the white in-band noise floor. As noted, an FFT of the output bit stream would surely exhibit these skirts, so they should be accounted for.

7.5 Summary

Table 7.4 summarizes the performance achieved by this high-speed BP ΔΣM. In a redesign, the

Table 7.4: Modulator performance summary.

Process	0.5μm SiGe HBT
Die area with pads	2.4mm $\times$ 1.6mm
Die area without pads	1.6mm $\times$ 0.85mm
Supply voltage	5V
Sampling frequency	4GHz
Signal bandwidth	20MHz
Oversampling ratio	100
Dynamic range	40dB
Peak SNR	37dB
Peak SFDR	48dB
Power consumption	450mW

output bit should be taken from the delayed latch output, the emitter followers should be optimized for speed, and the resonator output voltages should be scaled up; we estimate these changes would improve dynamic range from 6.3 bits to about 9 bits in a 20MHz bandwidth. It is our feeling that with further careful design of the input transconductor for low noise and higher linearity, a resolution of 10 bits might be achievable. For reference, this agrees with the authors of [Jay97], who concluded that their $f_s/4$ BP modulator which clocked $f_s = 3.2$GHz could also achieve 10-bit performance in a 25MHz band. A second-cut of our design would also include a method of capturing the output bits for off-line FFTs.

Chapter 8

Conclusions

We have supplemented the theory in Chapters 4 through 6 with the practical test results in Chapter 7. We are now in a position to examine the usefulness of high-speed $\Delta\Sigma$Ms in general, and from this, propose work for the future.

8.1 Summary of Contributions and Results

We started with a discussion of the design choices in a $\Delta\Sigma$M and we explored some of the issues in performance measurement and simulation of both DT and CT $\Delta\Sigma$Ms. CT $\Delta\Sigma$Ms appear valuable because in theory their clock speed is not limited by settling time in the same manner as in a DT $\Delta\Sigma$M. Calculating modulator performance requires time-domain simulation, and many techniques from ideal equations (which are fast but unrealistic) to full-circuit simulation (which is realistic but slow) must be employed as the design progresses.

Next, we discussed nonidealities in DT $\Delta\Sigma$Ms, a subject that has been studied at length in the literature, and explained how they affect the performance of CT $\Delta\Sigma$Ms, something which had been studied less but which is newly summarized here. We presented a list of many of the important papers in CT $\Delta\Sigma$M and finished with a table showing the performance achieved by published high-speed CT $\Delta\Sigma$Ms, neither of which had been done before. Most published modulators are second-order, and most only succeed in shaping noise to an OSR of about 15—the rest of the band

is usually filled with unshaped white noise.

One possible explanation for why this might be is excess loop delay: high speed designs might have a delay between the quantizer clock and feedback output that is a significant fraction of a sampling clock period. This excess delay increases in-band quantization noise and lowers the maximum input amplitude for which a modulator remains stable. Its effects can be mitigated in many ways: a noise transfer function with a low out-of-band gain, a multibit quantizer, feedback coefficient tuning, return-to-zero-style feedback DACs, and additional feedbacks for extra controllability. Our study of loop delay summarized past work and advanced a number of new ideas, one of the more important ones being that the modified $\mathcal{Z}$-transform is not suitable for the study of excess delay in CT $\Delta\Sigma$Ms.

A second explanation for white in-band noise is quantizer clock jitter, which causes random modulations in the width of the feedback pulses and hence the folding of out-of-band noise into the signal band. We confirmed previous estimates of achievable SNR using an NRZ DAC, and showed that RZ modulators with the same amount of jitter have performance worse by about one bit. For the first time, we showed how to treat nonwhite jitter and estimated how much performance a GHz-speed modulator would lose with a typical integrated VCO. It turned out that we could describe maximum jitter-limited resolution with a single equation which depends only on the Nyquist bandwidth; we thus concluded that it is unlikely a typical VCO would be the limiting factor in the performance of an integrated $\Delta\Sigma$M.

A third explanation for white in-band noise is to be found in quantizer metastability. Quantizers built as latched comparators have finite regeneration gain so that small quantizer inputs take longer to resolve than large ones; because the quantizer input in a $\Delta\Sigma$M is a stochastic variable, at random times the input will be near zero and hence cause additional excess delay. The effect is the same as that of clock jitter: random modulations in the DAC pulse widths occur, which modulates out-of-band noise into the signal band. Our study was the first comprehensive one of its kind: we stumbled upon the importance of metastability with a new technique of z-domain extraction which we explained, and we also presented and validated a behavioral modeling technique which allows us to simulate a modulator with a metastable quantizer rapidly. We showed that many of the

usual things such as signal scaling, preamplification, and fast regeneration time are worth paying attention to in the design of a latched comparator for CT $\Delta\Sigma$M, but the most striking advantage arose from using a third half-latch in the feedback path for extra regeneration despite the extra half-delay it causes. Even using a third half-latch has its limits; as we illustrated, our new simple formula says clocking faster than 5% of the maximum transistor switching speed is likely to limit performance severely.

Finally, we presented test results on a fourth-order band pass CT $\Delta\Sigma$M with integrated LC resonators that clocks at 4GHz in a 40GHz process. We gave a concise procedure for how one would go about choosing the parameters in such a design, then we see how the actual design would perform had it been designed with that approach in mind. The circuit blocks were studied, with particular emphasis on the linearity and noise of the input transconductor (which is a very important component in the design), and detailed measurements of the modulator behavior were presented and explained. The major problems with the design were lack of matching to input and clock signal generators, the output bit taken from the wrong point in the feedback, emitter followers designed incorrectly for optimum speed, and signal scaling which resulted in poor quantizer response. The modulator achieved 6.3 bits of dynamic range in a 20MHz bandwidth centered at 1GHz while dissipating 450mW; in a redesign, part of which we do, we estimate this could be improved to 10 bits.

8.2 Practical $\Delta\Sigma$M Applications

In an ideal world, fast CT $\Delta\Sigma$Ms appear to be the solution to high-speed, high-resolution ADC needs. If we clock fast enough, the reasoning goes, we can oversample as much as we want and thus get whatever performance we want. This thesis has demonstrated that wide bandwidths and high-resolutions together are difficult to realize jointly with practical high-speed CT $\Delta\Sigma$Ms. Indeed, the advantage realized by oversampling has not been shown in practical modulators to extend past approximately OSR $= 15$ when f_s is any appreciable fraction of f_T, say over 1%. 20-bit resolutions have been achieved only with $f_s \ll f_T$, and hence only over narrow bands. The

design of the input stage for such extreme resolutions is a challenge for even low bandwidths—high bandwidths and high clock rates make it very difficult to achieve more than 10 to 12 bits of dynamic range in the first stage.

There are three areas in which this author feels optimistic about the future of CT $\Delta\Sigma$M. They are as follows:

1. Narrowband applications requiring high SFDR but with no constraints on power consumption. The authors of [Rag97] have a second-order modulator clocking at 4GHz with a tunable noise notch from 0 to 70MHz, and they achieve 92dB SFDR in a 370kHz band. Using such a fast $\Delta\Sigma$M with so much oversampling might seem like overkill to get 15 bits SFDR in a narrow band, but it *is* one option. We achieve high resolution through oversampling combined with the advantage of tunability, which could work to our favor in certain radio applications.

2. Hybrid mixer/modulator applications for radios. [Mor98] was mentioned in Chapter 3 as combining an analog mixer with the front end of two LP modulators for I and Q channel recovery, quite an elegant concept. This is a little different from the BP application envisioned for the modulator in Chapter 7, where the mixing is done digitally after the modulator. Although the performance that author achieved wasn't stellar (5.5 bits in 50MHz, 11.5 bits in 10kHz), it could well be attributed to the design of the latch, which apparently was only a two rather than three half-latch design. In his paper he says he feels he can improve the performance by at least three bits.

3. Hybrid wideband converters with $\Delta\Sigma$M front ends and Nyquist back ends. [Bro97] has a multibit $\Delta\Sigma$M front-end oversampled only eight times and clocked at 20MHz, whose output is fed to a pipeline stage. When the outputs of the stages are appropriately combined and decimated, the result is 16-bit performance with a 2.5MHz output rate (1.25MHz bandwidth). Again, the concept is elegant: use the $\Delta\Sigma$M where it is strong (high DR but limited bandwidth) and the pipeline where it is strong (high bandwidth but limited DR) to get the best of both worlds.

Thus, while it sometimes behooves us to think just of CT $\Delta\Sigma$M by itself as in the first example,

the latter two examples are excellent illustrations of how we can combine CT $\Delta\Sigma$M with other techniques to exploit the respective strengths of each. Standalone CT $\Delta\Sigma$M might not succeed at wideband ADC for BP applications, but it can do narrowband ADC or be combined with other things in novel ways.

As clock speeds increase significantly (20GHz and beyond, perhaps), surely other nonidealities will start to degrade performance: substrate noise coupling, transmission line effects, etc. Designing even simple circuits like multiplexers at these speeds poses a number challenges; CT $\Delta\Sigma$Ms are complicated circuits, which is a further argument in favor of pushing cleverness rather than clock speed.

8.3 Future Work

There are, of course, a number of areas in which the state-of-the-art for CT $\Delta\Sigma$Ms could well be advanced, thus improving their usefulness in a wider range of applications. The following problems remain to be studied and solved; they are listed in order of this author's opinion of most- to least-important.

Multibit DAC A working high-speed multibit design could be a significant breakthrough: as we said in §4.5, not only are multibit modulators higher resolution and more stable, but they improve clock jitter sensitivity too. Can fast DEM be made to work?

Calibration and tuning How does one tune a high-speed CT $\Delta\Sigma$M for maximum DR over process and temperature variations, either dynamically or off-line? For production parts, this is essential. Yet high-speed circuits are best when kept simple, and tuning will add complexity. This seems a tough problem to tackle.

System identification We attempted to give a method for rapid identification of nonidealities in a $\Delta\Sigma$M in §6.1. Can this be improved upon? That is, can we come up with a way to pinpoint modulator problem areas *rapidly* and *accurately*? Moreover, can we find a way to apply it to a real modulator in the lab, rather than just in simulation?

Power consumption Can power be reduced through non-bipolar circuits and/or lower supply voltages while maintaining speed?

Higher modulator order Is it worth going to a higher-order design for high-speed $\Delta\Sigma$M for the resolution gained? High-order audio converters often include reset circuitry that activates when modulator overload is sensed [dS90]; can such circuits be included in a GHz-speed design? Are they necessary?

There is still plenty of exciting work left to do in the field of high-speed CT $\Delta\Sigma$M.

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Appendix A

DR Derivations

A.1 VCO Clock Jitter

We derive the maximum-achievable DR for a CT $\Delta\Sigma$M clocked by a VCO with a phase noise given by (5.21). First, we start with (5.13) which is the in-band white noise level for a modulator with independent jitter and N bins:

$$10\log_{10}\left(\frac{2\sigma_{\delta y}^2\cdot 2\sigma_\beta^2}{NT_s^2}\right). \tag{A.1}$$

We have omitted the -7.27dB because that is needed only for the Hann-windowed periodogram. If the in-band noise was white over the entire band, whose width expressed in bins is

$$N/(2\cdot \text{OSR}), \tag{A.2}$$

then the total in-band noise would be the argument of $\log_{10}$ in (A.1) times (A.2),

$$10\log_{10}\left(\frac{\sigma_{\delta y}^2\cdot 2\sigma_\beta^2}{\text{OSR}\cdot T_s^2}\right). \tag{A.3}$$

The quantity $\sigma_{\delta y}$ in (A.3) is found in simulation to have a value between 1 and 2, so assume

$$\sigma_{\delta y}\approx 1.5 \tag{A.4}$$

on average. From (5.22), and also from the second column of Table 5.2, we can find that

$$\frac{2\sigma_\beta^2}{T_s^2} = 10^{-12} f_s, \;\; f_s \text{ in MHz.} \tag{A.5}$$

Substituting (A.4) and (A.5) in (A.3), and recalling from Figure 5.9 in §5.3.2 that accumulated jitter tends to give white noise levels 1–5dB (say 3dB on average) lower than independent jitter, yields

$$10\log_{10}\left(\frac{1.5^2}{\text{OSR}} \times f_s \times 10^{-12}\right) - 3 \approx -120 + 10\log_{10} f_s/\text{OSR} \tag{A.6}$$

as the total in-band noise. The DR is then the maximum allowable signal amplitude minus (A.6); the former is given by the MSA, which for typical modulators lies between -1dB and -5dB or so. Again, assume

$$\text{MSA} \approx -3\text{dB} \tag{A.7}$$

on average, and note that

$$f_N \equiv \frac{f_s}{\text{OSR}}. \tag{A.8}$$

Using (A.7) and (A.8) with (A.6) gives

$$\begin{aligned} \text{DR} &\approx -3 - (-120 + 10\log_{10} f_N) \\ &= 117 - 10\log_{10} f_N \text{ dB, } f_N \text{ in MHz,} \qquad (A.9) \\ &\approx 19 - 0.5\log_2 f_N \text{ bits, } f_N \text{ in MHz} \qquad (A.10) \end{aligned}$$

where we have made use of (2.10) in writing (A.10).

A.2 Three Half-Latch Quantizer

Here we find the maximum-achievable DR for a CT $\Delta\Sigma$M with a three half-latch single-bit quantizer as a function of f_s/f_T. Looking at Figure 6.23(b), there appear to be two distinct regions in the curve, one for $f_s/f_T < 5\%$ or so and one for $f_s/f_T > 5\%$. In the first case, the in-band noise per bin is -115dB or less in an 8192-point simulation; a single bin thus corresponds to OSR $= 4096$.

If the noise were completely white, then each doubling of the OSR would raise the total noise by 3dB. Extrapolating this in the opposite direction allows us to find the total in-band noise of

$$-79 - 3\log_2 \text{OSR} \tag{A.11}$$

when $f_s/f_T < 5\%$. For the opposite case, the noise starts at -97dB/bin when $f_s/f_T = 6\%$ and increases roughly at 6dB/oct with f_s/f_T. Assuming white in-band noise leads to a total noise of

$$-61 - 3\log_2 \text{OSR} + 6\log_2 \frac{f_s/f_T}{5}. \tag{A.12}$$

DR is given by MSA minus total noise. We can see in Figure 6.21 that a modulator with half a sample of feedback delay typically has an MSA between -10dB and -6dB; assume

$$\text{MSA} \approx -8\text{dB} \tag{A.13}$$

on average.

Combining (A.13) with (A.11) tells us that

$$\begin{aligned} \text{DR} &\geq -8 - (-79 - 3\log_2 \text{OSR}) && \text{(A.14)} \\ &= 71 + 3\log_2 \text{OSR dB}, f_s/f_T \leq 5\% && \text{(A.15)} \\ &= 11.5 + 0.5\log_2 \text{OSR bits} && \text{(A.16)} \end{aligned}$$

where (A.16) makes use of (2.10). The $\geq$ sign in (A.14) is because the noise in (A.11) is worst-case, for $f_s/f_T = 5\%$; at slower clock speeds, the in-band noise will be lower and DR higher. Using (A.13) and (A.12) gives

$$\begin{aligned} \text{DR} &\approx -8 - (-61 - 3\log_2 \text{OSR} + 6\log_2 \frac{f_s/f_T}{5}) \\ &= 53 + 3\log_2 \text{OSR} - 6\log_2 \frac{f_s/f_T}{5} \text{ dB}, f_s/f_T \geq 6\% && \text{(A.17)} \\ &= 8.5 + 0.5\log_2 \text{OSR} + \log_2 \frac{f_s/f_T}{5} \text{ bits}. && \text{(A.18)} \end{aligned}$$

Once again, (2.10) was used in writing (A.18).

Appendix B

BP $\triangle\Sigma$M Measurement Aids

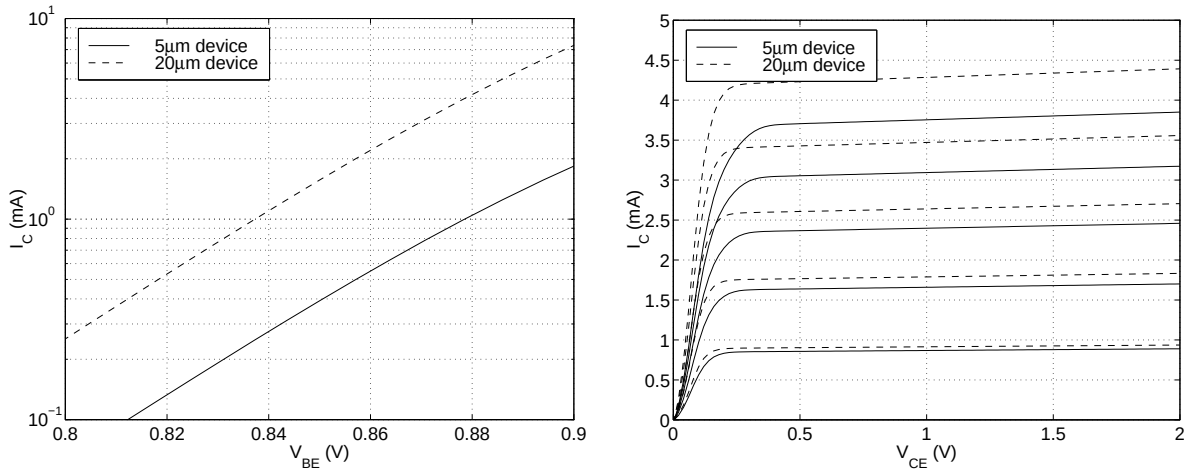
In this appendix we plot graphs from SPICE that allow us to estimate important parameters from the fabricated $f_s/4$ BP modulator in Chapter 7.

General transistor dc characteristics are plotted in Figure B.1. We show collector current against V_{BE} and V_{CE} for two commonly-used transistor sizes in this design, 5μm $\times$ 0.5μm and 20μm $\times$ 0.5μm.

Figure B.2 shows how varying the multi-tanh control voltages V_G and V_Q affects the transconductance G_g and G_q actually delivered.

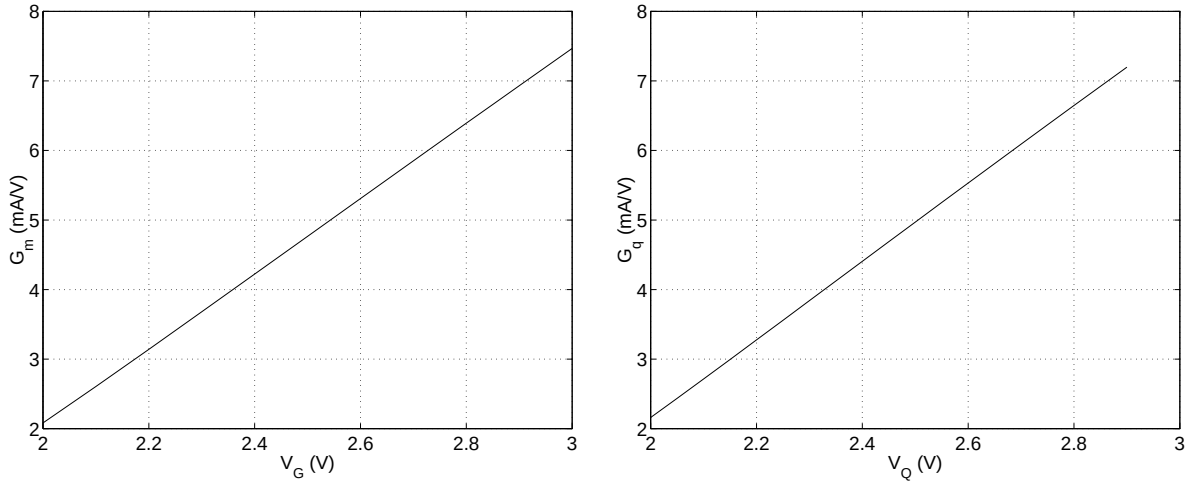
Figure B.3(a) contains the bias circuit for V_{EN} which sets the current in the latching stages, and Figure B.3(b) plots the current in the emitter resistors of that circuit.

Figure B.4 illustrates the current through one of the R_{DAC} resistors in Figure 7.26 as a function of the base voltage at the current-source transistor; the total amount of current switched is found by finding I_{k+} and I_{k-} for each of V_{k+} and V_{k-} separately from the graph, then subtracting the values.



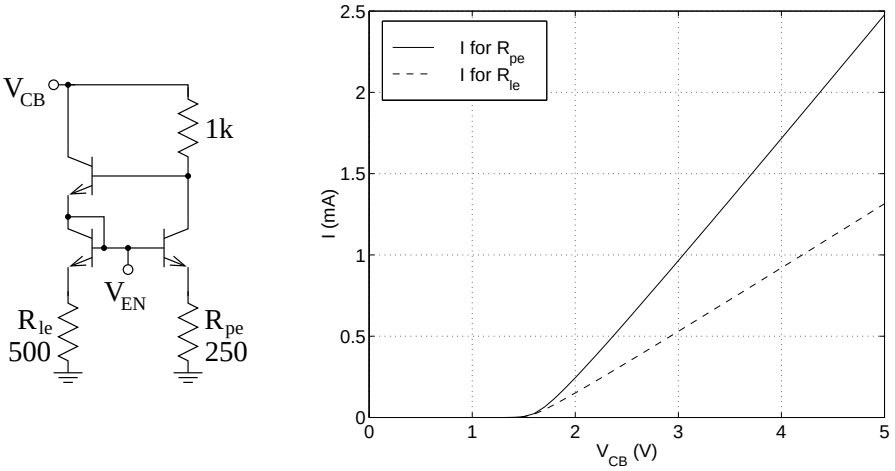
(a) (b)

Figure B.1: BJT characteristics: collector current vs. (a) V_{BE}, (b) V_{CE}.



(a) (b)

Figure B.2: (a) G_g against V_G, (b) G_q against V_Q.



(a) (b)

Figure B.3: (a) V_{EN} bias circuit, (b) current through bias transistor emitter resistors.

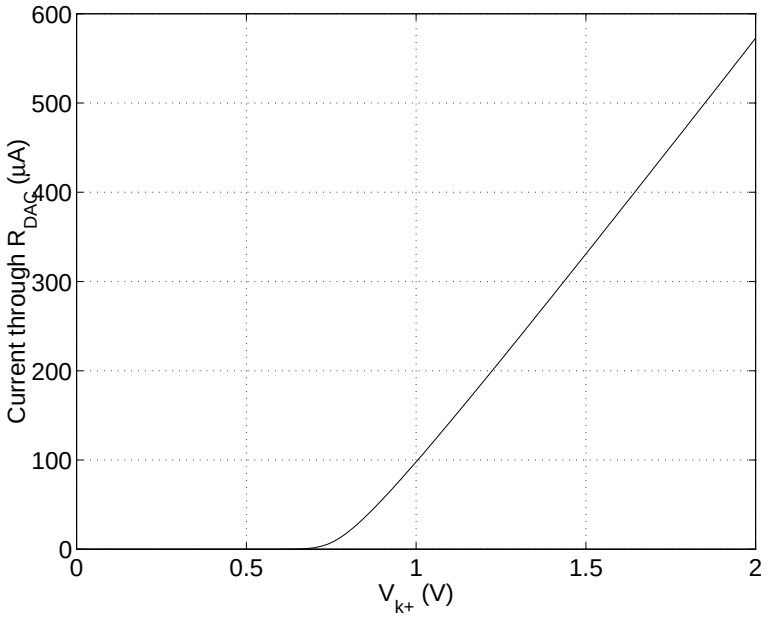


Figure B.4: DAC current vs. control voltage.