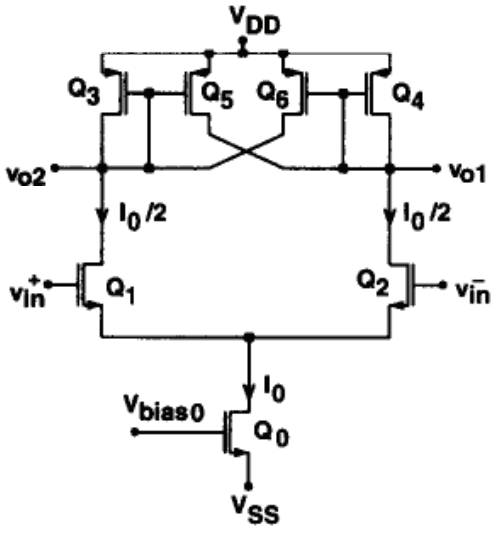


Figure 5.16. Source-coupled differential pair that uses positive feedback to provide increased gain.

dimensions. Higher-mobility NMOS transistors are used as input devices to achieve higher gain. To increase the gain further, the circuit of Fig. 5.15*b* can be used where the input transistor transconductance is increased by injecting currents I_1 and I_2 ($I_1 = I_2$) into them from the p-channel current source Q_5 and Q_6 [4,5]. The gain of the modified circuit is now given by

$$A_d = \sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_3(1 - 2I/I_0)}}. \tag{5.10}$$

A practical choice is $I = 0.9I_0/2$, which increases the gain by a factor of $\sqrt{10}$.

Another method that uses a controlled amount of positive feedback to effectively increase the driver devices transconductance and hence the overall gain is shown in Fig. 5.16 [1]. The gain of the positive feedback gain stage is given by

$$A_d = \sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_3}} \frac{1}{1 - \alpha}, \tag{5.11}$$

where $\alpha = (W/L)_5/(W/L)_3$ is the positive feedback factor that is responsible for increasing the gain. A reasonable value for α is 0.75, which increases the gain by a factor of 4. The value of α is determined by the ratio of the load device dimensions, and although it is a reasonably well controlled parameter, a practical maximum value for α is 0.9, because beyond that any mismatches due to process variations may cause the value of α to approach unity, and per Eq. (5.15), the gain will become infinity and the stage will operate as a cross-coupled latch.

The response times of the gain stages of Figs. 5.15 and 5.16 are limited by the parasitic capacitances of the load devices. The response time of the source coupled differential stage can improve significantly if the diode-connected loads are replaced

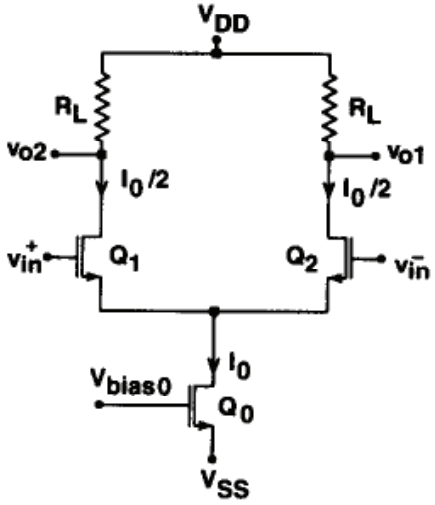


Figure 5.17. Resistive-load source-coupled differential pair.

with simple resistors, as shown in Fig. 5.17. The gain of the resistive load differential stage is given by

$$A_d = g_{mi}R_L, \tag{5.12}$$

where g_{mi} is the transconductance of the NMOS input devices and R_L is the load resistance. One drawback of this circuit is that the voltage drop across the load resistors can vary significantly due to variations in the resistance or the magnitude of the differential stage tail current. The variations of the output common-mode voltage makes it difficult to design multistage amplifiers and bias the circuit to operate under all process variations. One solution to this problem is to use a replica biasing scheme. A schematic of the resistive load differential stage with a simple V_{BE}-based bias generator is shown in Fig. 5.18. The bias current is given by

$$I_B = \frac{V_{BE}}{R_B}. \tag{5.13}$$

Assuming that $(W/L)_7 = (W/L)_6$, the voltage drop across the load resistors is given by

$$V_{RL} = \frac{(W/L)_{10}}{(W/L)_9}\frac{I_B}{2}R_L = \frac{(W/L)_{10}}{(W/L)_9}\frac{V_{BE}}{2}\frac{R_L}{R_B}. \tag{5.14}$$

This generates a very reproducible fraction of V_{BE} since it is determined by resistor and transistor ratios. In addition to providing known bias voltage, the maximum positive output swing of the differential stage is well controlled at a value of

$$\Delta V_o = 2\frac{I_o}{2}R_L = \frac{(W/L)_{10}}{(W/L)_9}V_{BE}\frac{R_L}{R_B}. \tag{5.15}$$

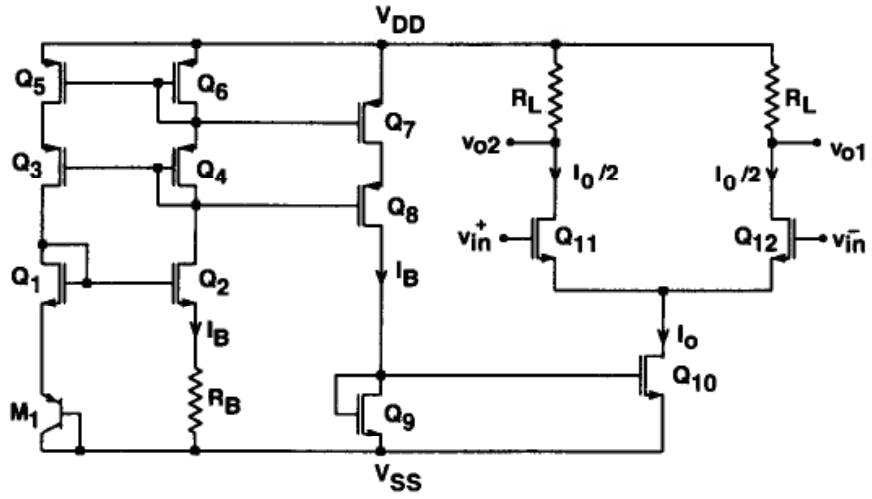


Figure 5.18. Resistive-load source-coupled differential stage with replica biasing.

Note that to first order the stage output voltage swing is independent of V_{DD}. As an example, if we assume that the bias resistance is $R_B = 3500\ \Omega$, the bias current is given by

$$I_B = \frac{0.7}{3500} = 200\ \mu\text{A}.$$

Using a value of $k'_n = 55\ \mu\text{A/V}^2$ for the NMOS transconductance factor and a threshold voltage of $V_{Tn} = 0.8$ V, then for $(W/L)_{10}/(W/L)_9 = 2$ and $(W/L)_{11}/(W/L)_{12} = 100$, the transconductance of the input devices will be

$$g_{mi} = 2\sqrt{k'_n\left(\frac{W}{L}\right)I} = 2.1 \times 10^{-3}\ \text{mhos}.$$

For $R_L = 5000\ \Omega$ the differential gain is given by

$$A_d = g_{mi}R_L = 2.1 \times 10^{-3} \times 5000 = 9.8$$

and the maximum output voltage swing is, from Eq. (5.15),

$$\Delta V_o = 2 \times 0.7 \times \frac{5000}{3500} = 2\ \text{V}.$$

A three-stage direct-coupled comparator circuit comprised of two cascaded resistive load and source-coupled differential stages followed by an op-amp comparator is

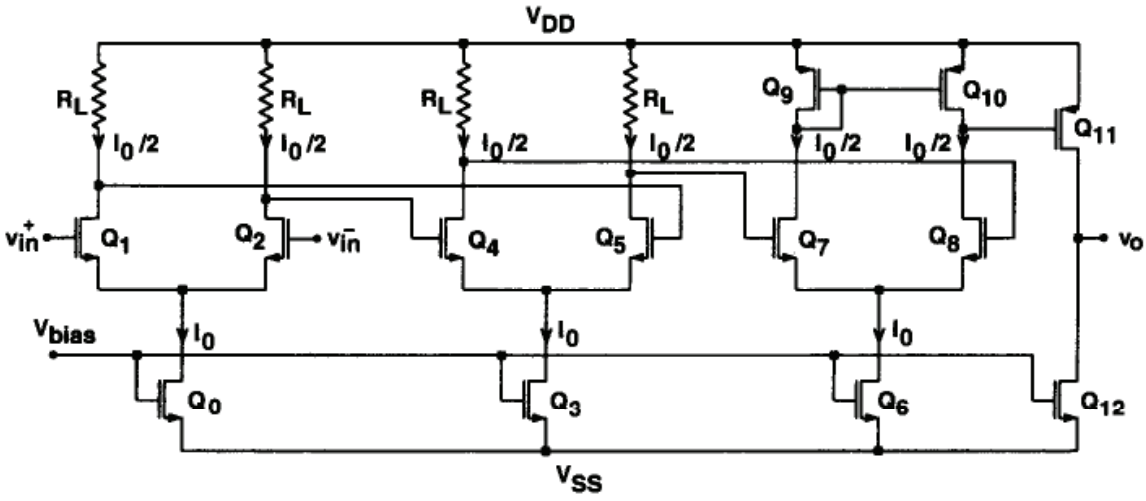


Figure 5.19. Direct-coupled three-stage comparator circuit.

shown in Fig. 5.19. The overall gain of the first two stages for identical sections is given by

$$A_d = (g_{mi}R_L)^2. \tag{5.16}$$

So if each stage has a gain of 10, the overall gain is $A_d = 100$, and a differential input of 100 μV appears as a 10-mV signal at the input of the final stage. This voltage is large enough to result in a fast response time in the last stage of the comparator. Since the stages are direct coupled, the offset is not canceled. If V_{off1}, V_{off2}, and V_{off3} represent the offset voltages of the first, second, and third stages, the input referred dc offset voltage is given by

$$V_{off} = V_{off1} + \frac{V_{off1}}{A} + \frac{V_{off2}}{A^2}. \tag{5.17}$$

Offset cancellation techniques for the multistage comparators will be introduced later.

5.4. REGENERATIVE COMPARATORS (SCHMITT TRIGGERS)

Often, comparators are used to convert a very slowly varying input signal into an output with abrupt edges, or they are used in a noisy environment to detect an input signal crossing a threshold level. If the response time of the comparator is much faster than the variation of the input signal around the threshold level, the output will chatter around the two stable levels as the input crosses the comparison voltage. Figure 5.20*a* shows the input signal and the resulting comparator output. In this situation, by employing positive (regenerative) feedback in the circuit, it will exhibit a phenomenon called *hysteresis,* which will eliminate the chattering effects. The

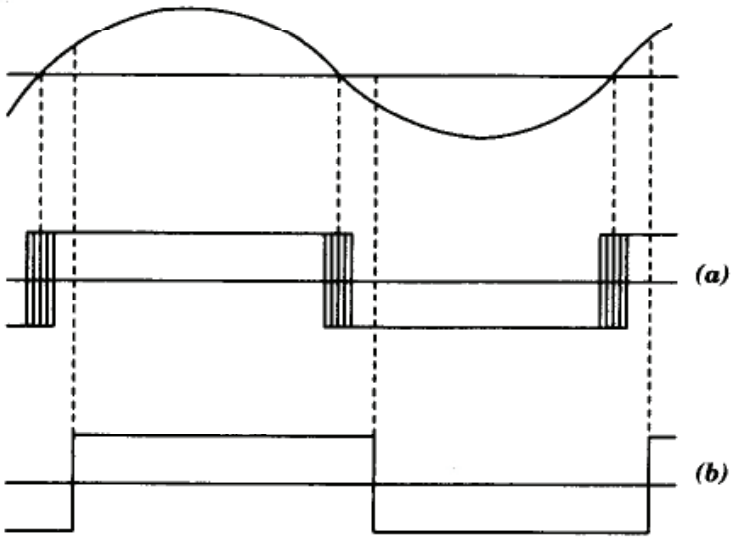


Figure 5.20. Response of a fast comparator to a slowly varying signal in a noisy environment: (*a*) without hysteresis; (*b*) with hysteresis.

regenerative comparator is commonly referred to as a *Schmitt trigger*. The response of the comparator with hysteresis to the input signal is shown in Fig. 5.20*b*.

A Schmitt trigger can be implemented by using positive feedback in a differential comparator, as shown in Fig. 5.21*a*. Assume that $v_i < v_1$, so that $v_o = V_o$; then v_1 is given by

$$v_1 = V_p = V_o \frac{R_2}{R_1 + R_2}. \tag{5.18}$$

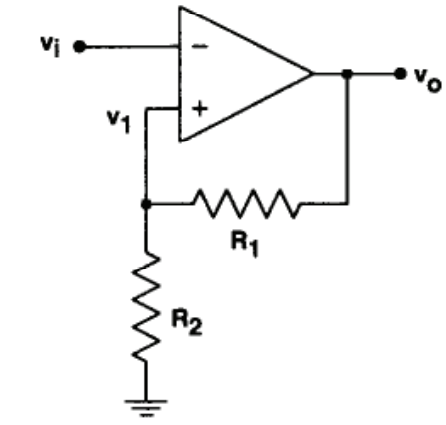
If v_i is now increased, v_o remains constant at V_o until $v_i = v_1$. At this triggering voltage, the output regeneratively switches to $v_o = -V_o$ and remains at this value as long as $v_i > v_1$. The voltage at the noninverting terminal of the comparator for $v_i > v_1$ is now given by

$$v_1 = V_n = \frac{-R_2}{R_1 + R_2} V_o. \tag{5.19}$$

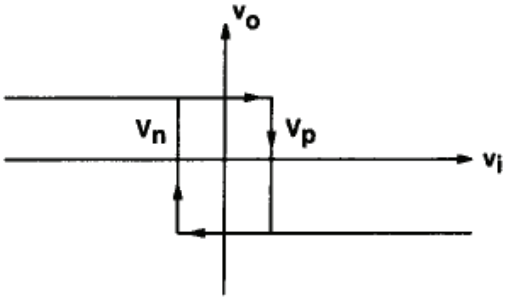
If we now decrease v_i, the output remains at $v_o = -V_o$ until $v_i = v_1$. At this voltage a regenerative transition takes place and the output returns to V_o almost instantaneously. The complete transfer function is indicated in Fig. 5.21*b*. Note that because of the hysteresis, the circuit triggers at a higher voltage for increasing than for decreasing signals. Note that $V_n < V_p$, and the difference between these two values is the hysteresis V_H given by

$$V_H = V_p - V_n = \frac{2R_2V_o}{R_1 + R_2}. \tag{5.20}$$

Another method to eliminate the chattering effect around the zero crossing of the input signal is to use the comparator with dynamic hysteresis shown in Fig. 5.22.



(a)

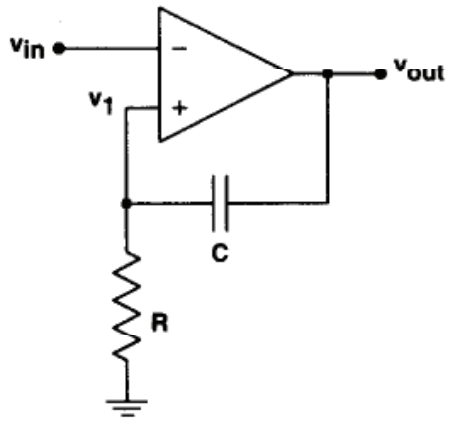


(b)

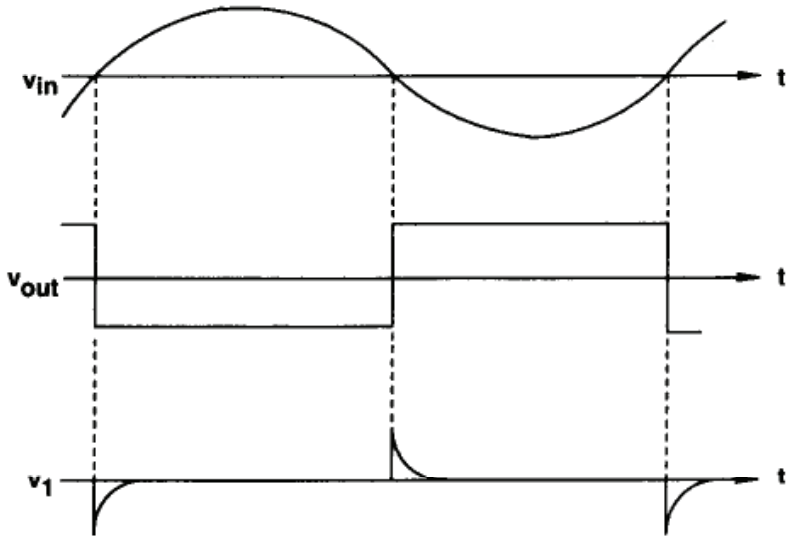
Figure 5.21. (*a*) Schmitt trigger; (*b*) composite input–output curve.

Assume that $v_{in} < v_1$, so that $v_o = +V_o$ and $v_1 = 0$. If v_{in} is now increased until $v_{in} > 0$, the output switches to $v_o = -V_o$. The negative transition of the output will capacitively be coupled to the positive input of the comparator, which also makes a negative transition. This will cause the differential input voltage between the negative and positive inputs of the comparator to become larger and speed up the output transition. Since the first transition at the output of the comparator regeneratively increases the magnitude of the differential input signal, the comparator responds to the first time the input crosses zero and ignores any subsequent zero crossings due to noise. The *RC* time constant determines the length of the time that the input signal will be ignored after its first zero crossing. If the time constant is made too large, it will limit the maximum frequency that the circuit can operate.

Many other ways are available to accomplish hysteresis in a comparator. All of them use some form of positive feedback. Earlier the source-coupled differential pair of Fig. 5.16 was introduced where positive feedback was employed to increase the gain [1]. The gain of the stage is given by Eq. (5.11), where $\alpha = (W/L)_5/(W/L)_3$ is the positive feedback factor. For $\alpha < 1$ $[(W/L)_5 < (W/L)_3]$, the circuit behaves as a gain stage. For $\alpha = 1$ the stage becomes a positive feedback latch. For $\alpha > 1$ the stage becomes a Schmitt trigger circuit with the amount of hysteresis determined by the value of α. Next, the trigger points and amount of hysteresis will be calculated for the case when $\alpha > 1$.



(a)



(b)

Figure 5.22. (*a*) Comparator with dynamic hysteresis; (*b*) input and output waveforms.

Consider the circuit of Fig. 5.23, where v_{in}^{+} is connected to ground (or any other reference potential) and the gate of Q_2 (v_{in}^{-}) is connected to a negative potential much less than zero. Thus Q_2 is off and Q_1 is on and all the tail current I_o flows through Q_1 and Q_3. The current through transistors Q_2, Q_4, Q_5, and Q_6 are zero and the node voltage v_{o1} is high while v_{o2} is low. Next assume that the input voltage v_{in}^{-} is gradually increased so that transistor Q_2 begins conducting and part of the tail current I_o starts flowing through it. This process continues until the current in transistor Q_2 equals the current in Q_5. Any increase of the input voltage beyond this point will cause the comparator to switch state so that Q_1 turns off and all the tail current flows through Q_2. At the switching

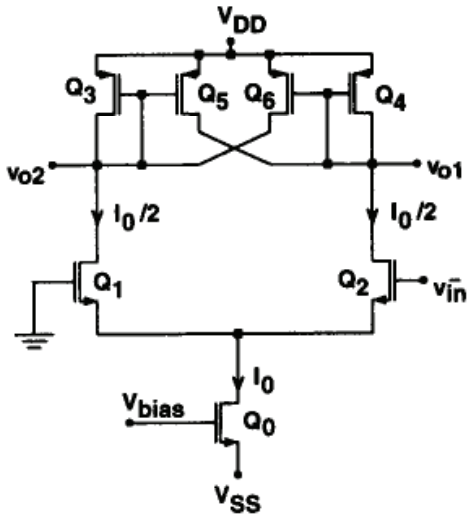


Figure 5.23. Source-coupled differential pair with positive feedback factor $\alpha > 1$ for hysteresis.

point assume that the current through transistors Q_1 and Q_2 are i_1 and i_2, respectively. Then we have

$$i_1 + i_2 = I_o \tag{5.21}$$

$$i_2 = i_5 = i_3 \frac{(W/L)_5}{(W/L)_3} = i_1 \frac{(W/L)_5}{(W/L)_3} \tag{5.22}$$

or

$$i_1 = \frac{I_o}{1 + \alpha} \tag{5.23}$$

$$i_2 = \frac{I_o \alpha}{1 + \alpha}. \tag{5.24}$$

Now the gate-to-source (v_{GS}) voltages of Q_1 and Q_2 can be calculated from their respective drain currents and are given by

$$v_{GS1} = V_{Tn} + \sqrt{\frac{i_1}{k'(W/L)_1}}, \tag{5.25}$$

$$v_{GS2} = V_{Tn} + \sqrt{\frac{i_2}{k'(W/L)_2}}. \tag{5.26}$$

In the equations above, $i_2 > i_1$, so $v_{GS2} > v_{GS1}$ and since the gate of Q_1 is tied to ground, the difference between v_{GS2} and v_{GS1} is the positive trigger level, equal to

$$V_{\text{trig}+} = \sqrt{\frac{i_2}{k'(W/L)_2}} - \sqrt{\frac{i_1}{k'(W/L)_1}}. \tag{5.27}$$

Using Eqs. (5.23) and (5.24) and since $(W/L)_1 = (W/L)_2$, Eq. (5.27) will be simplified to

$$V_{\text{trig}+} = \sqrt{\frac{I_o}{k'(W/L)_1}} \frac{\sqrt{\alpha} - 1}{\sqrt{1 + \alpha}}. \tag{5.28}$$

When the input voltage is increased beyond $V_{\text{trig}+}$, the comparator switches and v_{o1} turns low and v_{o2} goes high. Now transistor Q_2 is on and Q_1 is off, and all the tail current I_o flows through Q_2 and Q_4. The currents in transistors Q_1, Q_3, Q_5, and Q_6 are zero.

Next consider reducing the input voltage v_{in}^-, so that the current in Q_2 starts decreasing and Q_1 starts conducting. A similar argument can prove that the negative trigger point occurs when $i_1 = i_6$. It can be shown that the negative trigger point V_{trig}^- is given by

$$V_{\text{trig}-} = \sqrt{\frac{I_o}{k'(W/L)_1}} \frac{1 - \sqrt{\alpha}}{\sqrt{1 + \alpha}}. \tag{5.29}$$

The hysteresis can be calculated as

$$V_H = V_{\text{trig}+} - V_{\text{trig}-} = 2 \times \sqrt{\frac{I_o}{k'(W/L)_1}} \frac{\sqrt{\alpha} - 1}{\sqrt{1 + \alpha}}, \tag{5.30}$$

where $\alpha = [(W/L)_5/(W/L)_3] = [(W/L)_6/(W/L)_4]$.

The complete schematic of a comparator with hysteresis, which consists of a source-coupled differential pair with positive feedback, and a differential-to-single-ended converter is shown in Fig. 5.24. For this circuit the value of $\alpha = [(W/L)_5/(W/L)_3] = [(W/L)_6/(W/L)_4]$ is greater than 1 and the hysteresis is given by Eq. 5.30.

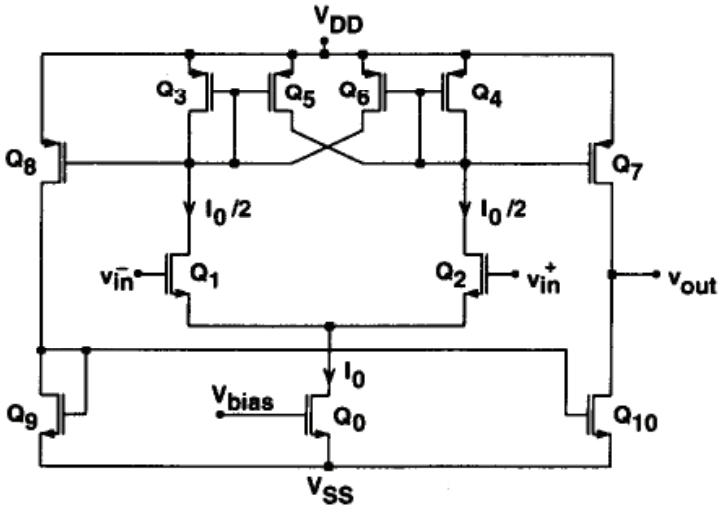


Figure 5.24. Complete schematic of a comparator with hysteresis.

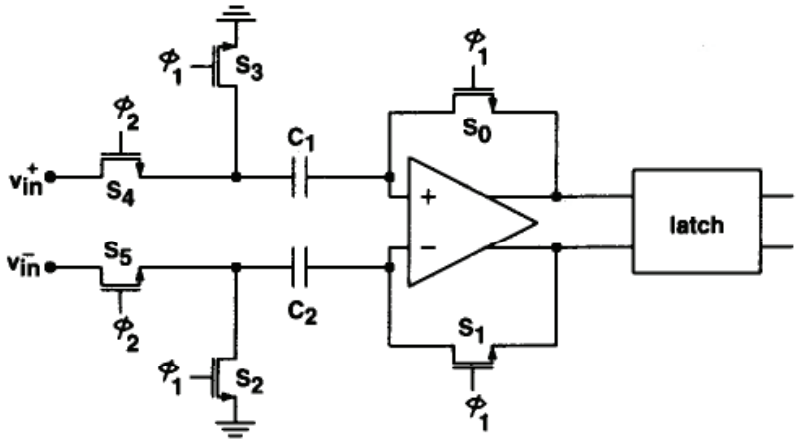


Figure 5.25. Fully differential input offset storage (IOS) comparator.

5.5. FULLY DIFFERENTIAL COMPARATORS

For high-accuracy applications an effective way for reducing the dc offset voltage due to the feedthrough charge is to use a fully differential scheme for the comparators. In such circuits, not only are clock-feedthrough effects reduced, but power supply noise and $1/f$ noise also tend to cancel. An offset-canceling fully differential comparator is shown in Fig. 5.25. In this scheme, during the offset cancellation mode, switches S_0 to S_3 are on while switches S_4 and S_5 are off. This will cause a unity-gain feedback loop to be established around the comparator and the two sampling capacitors to be charged between ground and the offset voltage of the comparator. During the tracking mode, switches S_0 to S_3 turn off, breaking the feedback loop of the comparator; S_4 and S_5 turn on and connect the capacitors to the input signal. The input differential voltage is amplified by the comparator and is sensed by the latch, which provides a logic level at its output, representing the polarity of the input differential voltage. If V_{offA} and V_{offL} represent the input offset voltages of the comparator and the latch, Q_0 and Q_1, represent the feedthrough charges of switches S_0 and S_1, the residual input referred offset voltage is given by

$$V_{off} = \frac{V_{offA}}{1 + A} + \frac{Q_0 - Q_1}{C} + \frac{V_{offL}}{A}. \tag{5.31}$$

From Eq. (5.31), if the charges injected by switches S_0 and S_1 match while the common-mode voltage will be slightly affected by an amount equal to $(Q_0 + Q_1)/2C$, the differential input voltage, $\Delta Q/C = (Q_0 - Q_1)/C$ will be zero. In practice, the charge injected by the two switches will never match, but the residual offset voltage due to the mismatches in the clock feedthrough will be an order of magnitude less than in the single-ended case. For this reason most advanced integrated comparators use fully differential design technique.

The offset compensation technique shown in Fig. 5.25 is known as the *input offset storage* (IOS) topology [4,5]. It is characterized by closing a unity-gain feed-