



Intel® 865G/865GV/865PE/865P Chipset Customer Reference Board Schematics

*For use with the Intel® 865G/865GV/865PE/865P Chipset Platform
Design Guide*

September 2003



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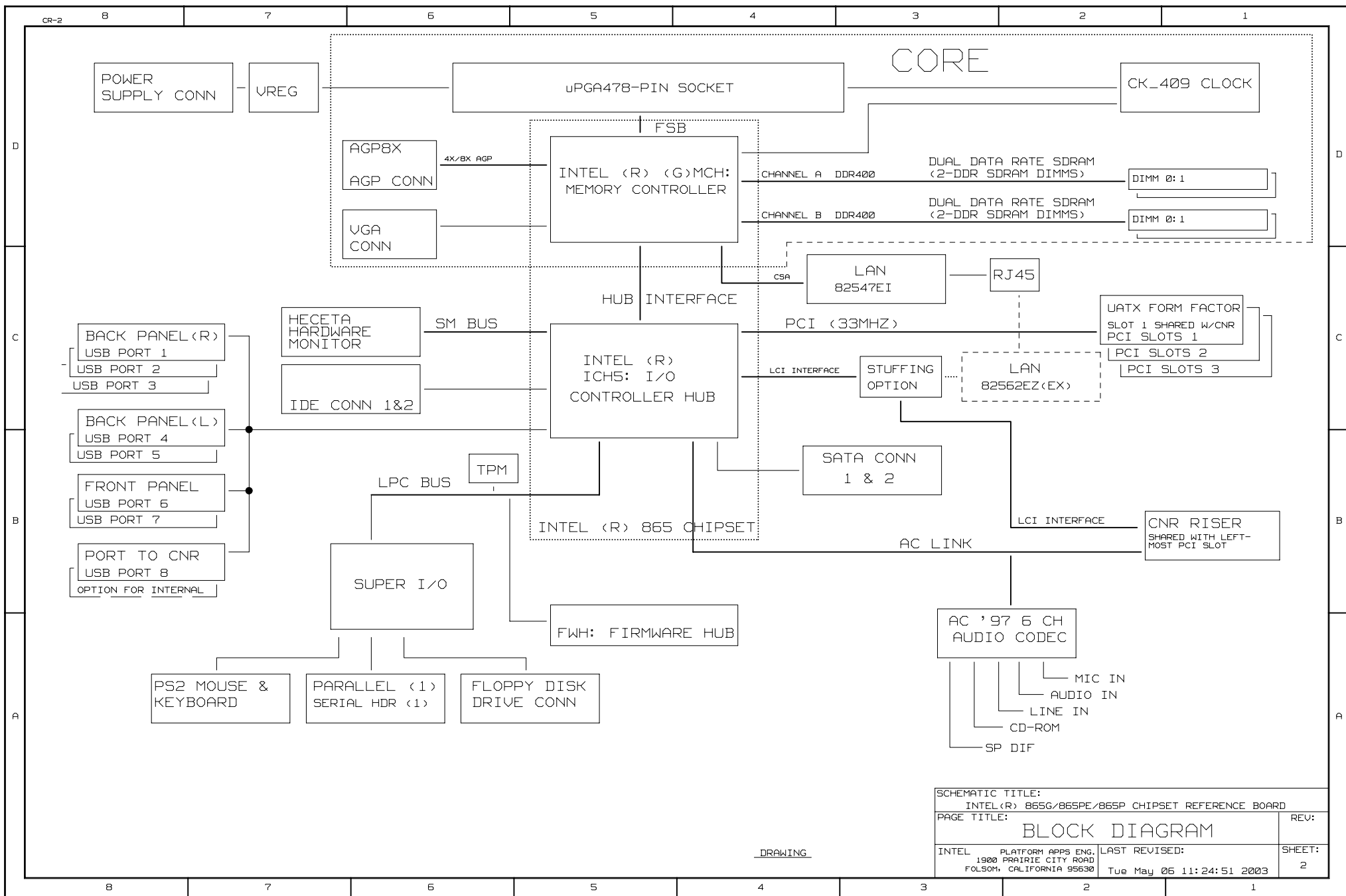
Revision History

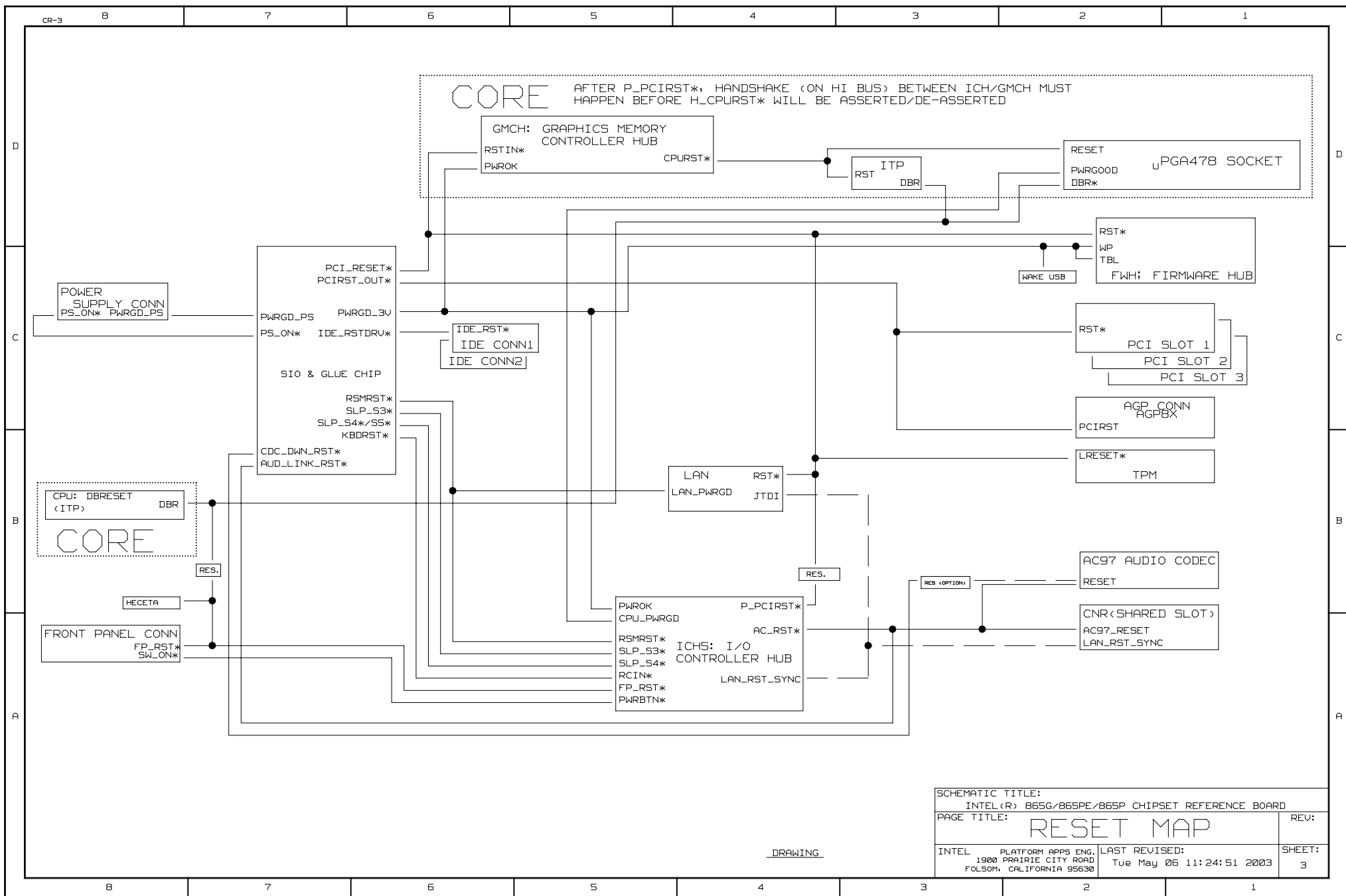
Rev. No.	Description	Rev. Date
-001	Initial Release.	May 2003
-002	Added 865GV to document title	September 2003

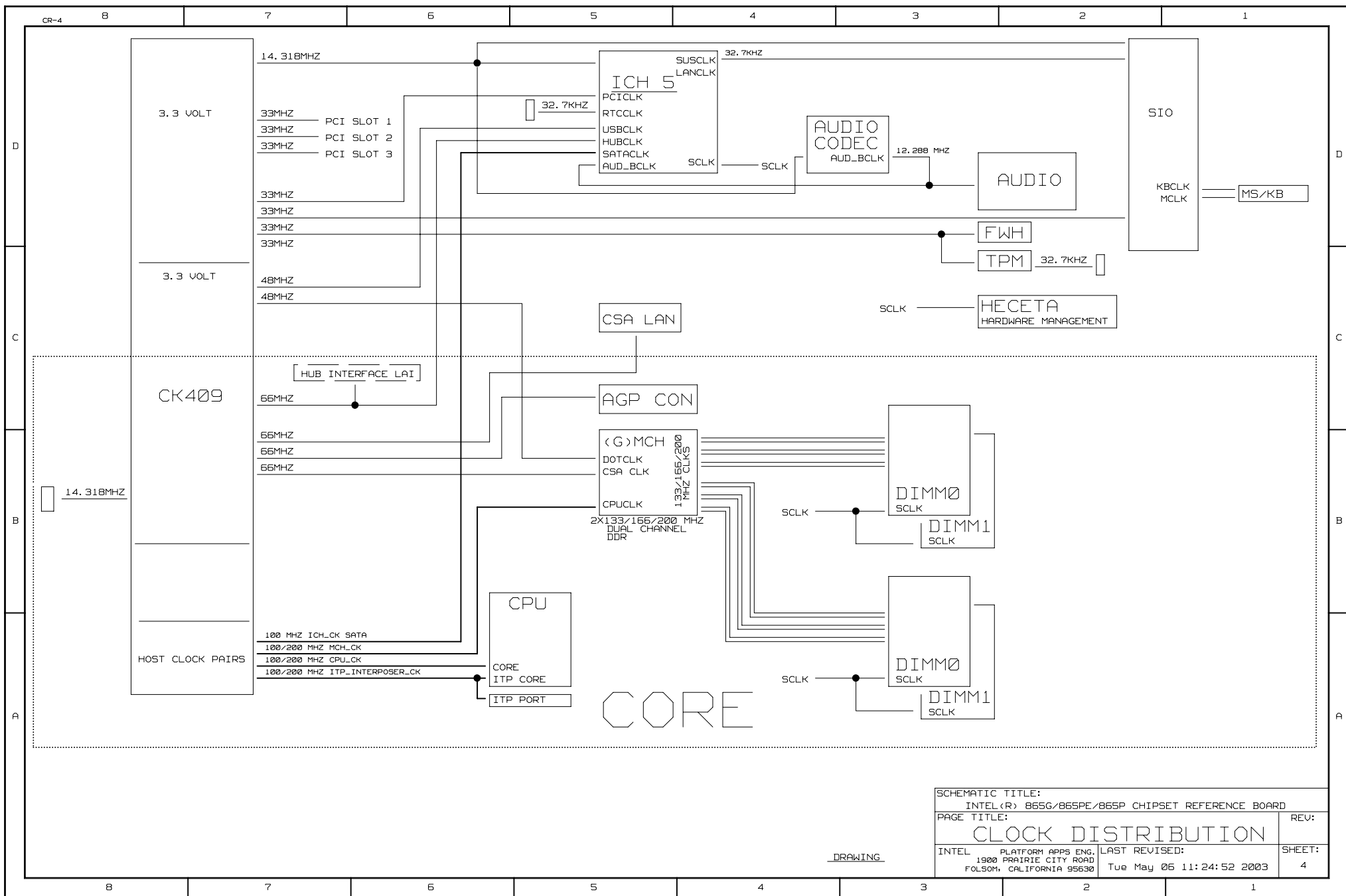
Document Contents

This document contains a set of Customer Board Reference (CRB) schematics for the 865G, 865GV, 865PE, and 865P chipsets. Note that the schematic diagrams for the AGP interface are only for the 865G, 865PE, and 865P chipsets.

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DRAWING									
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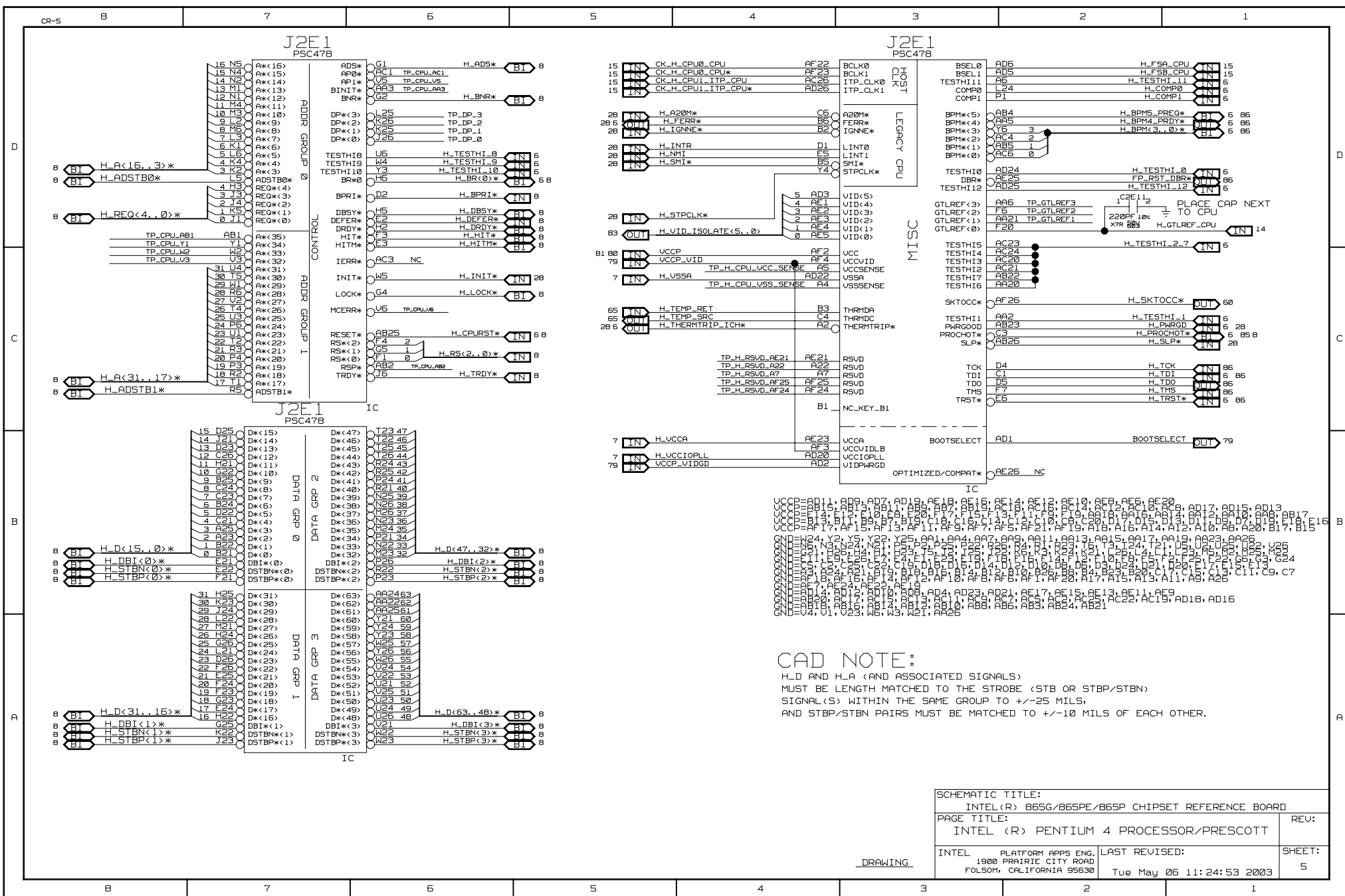


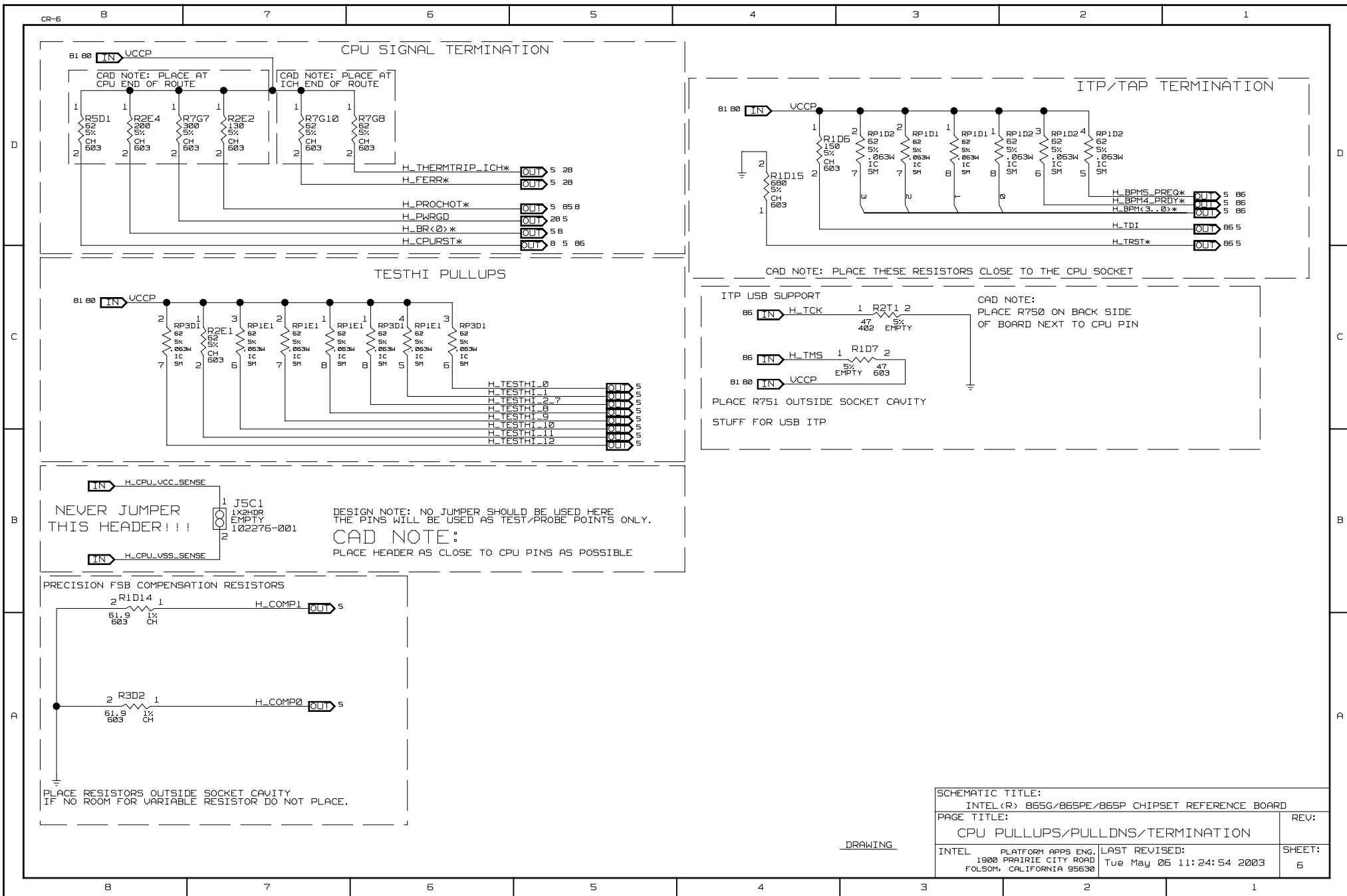




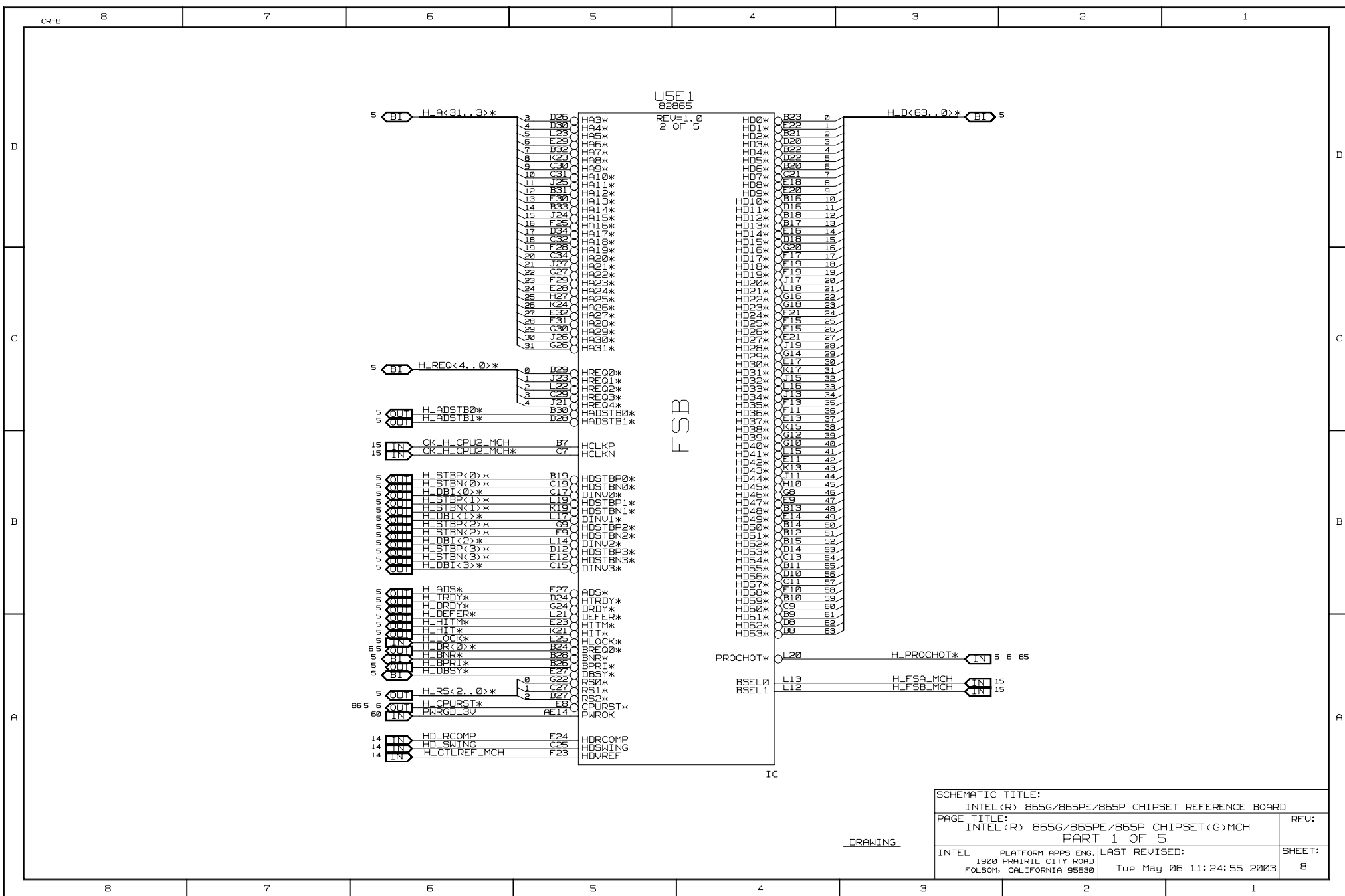
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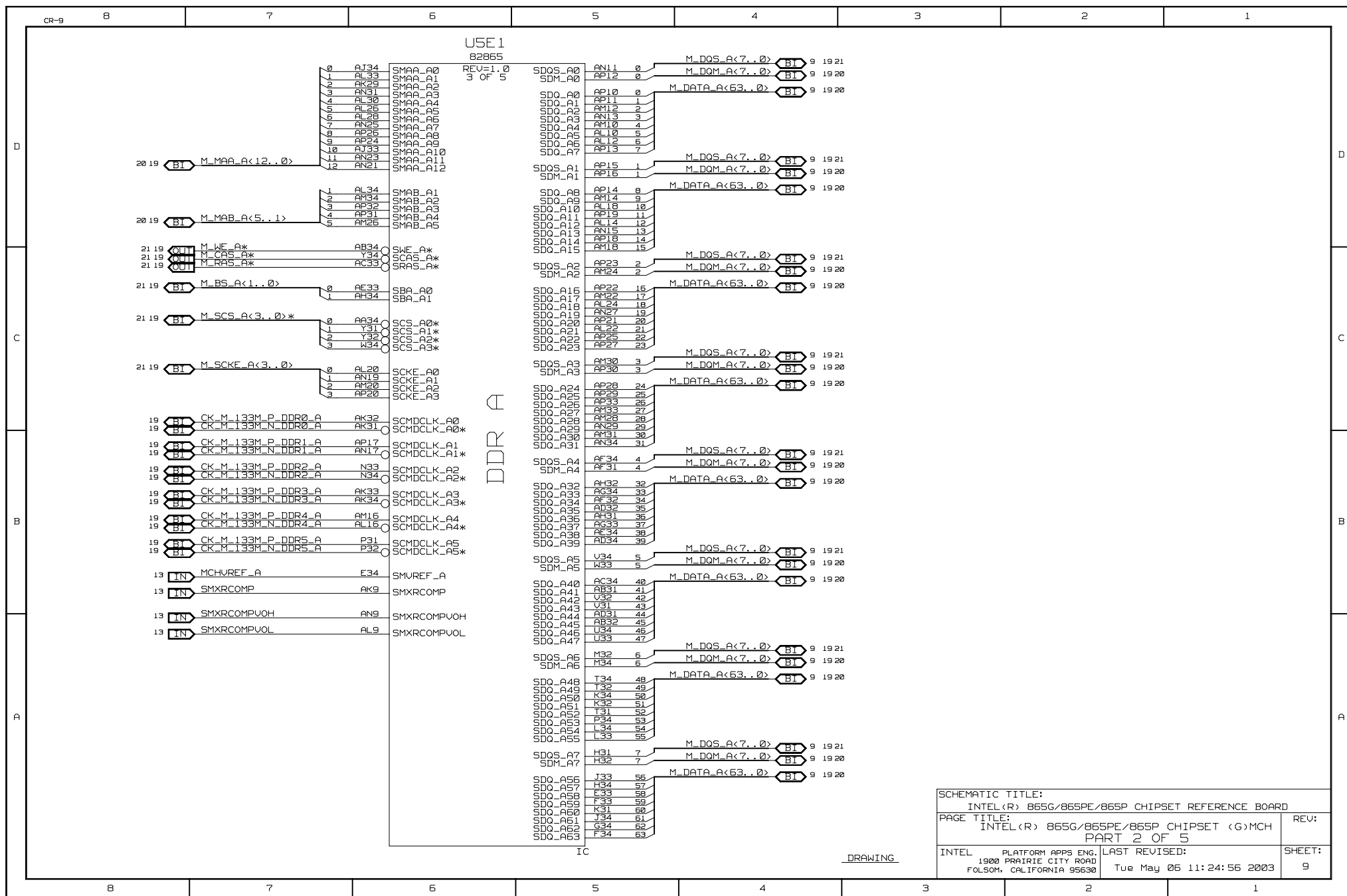
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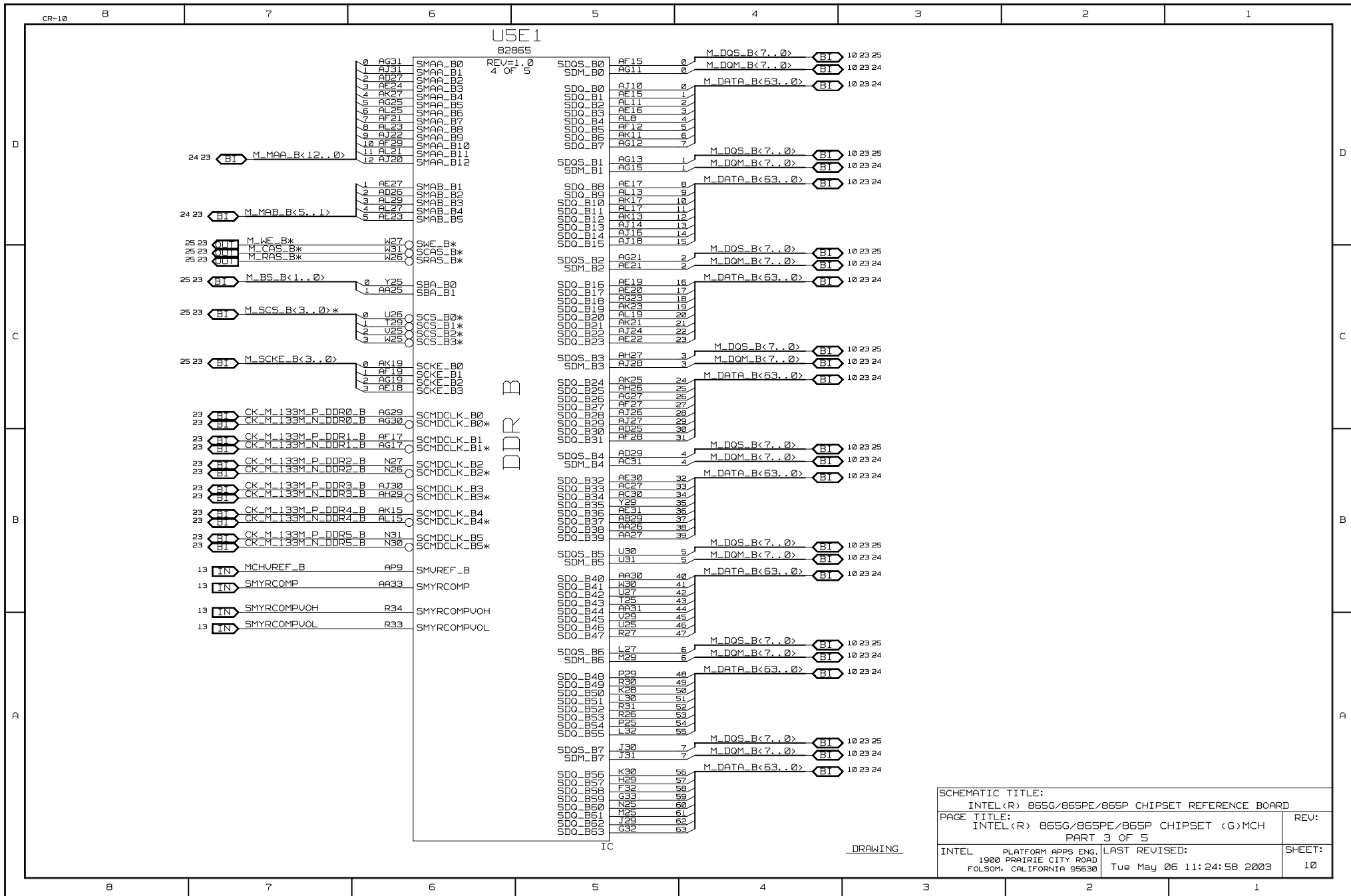


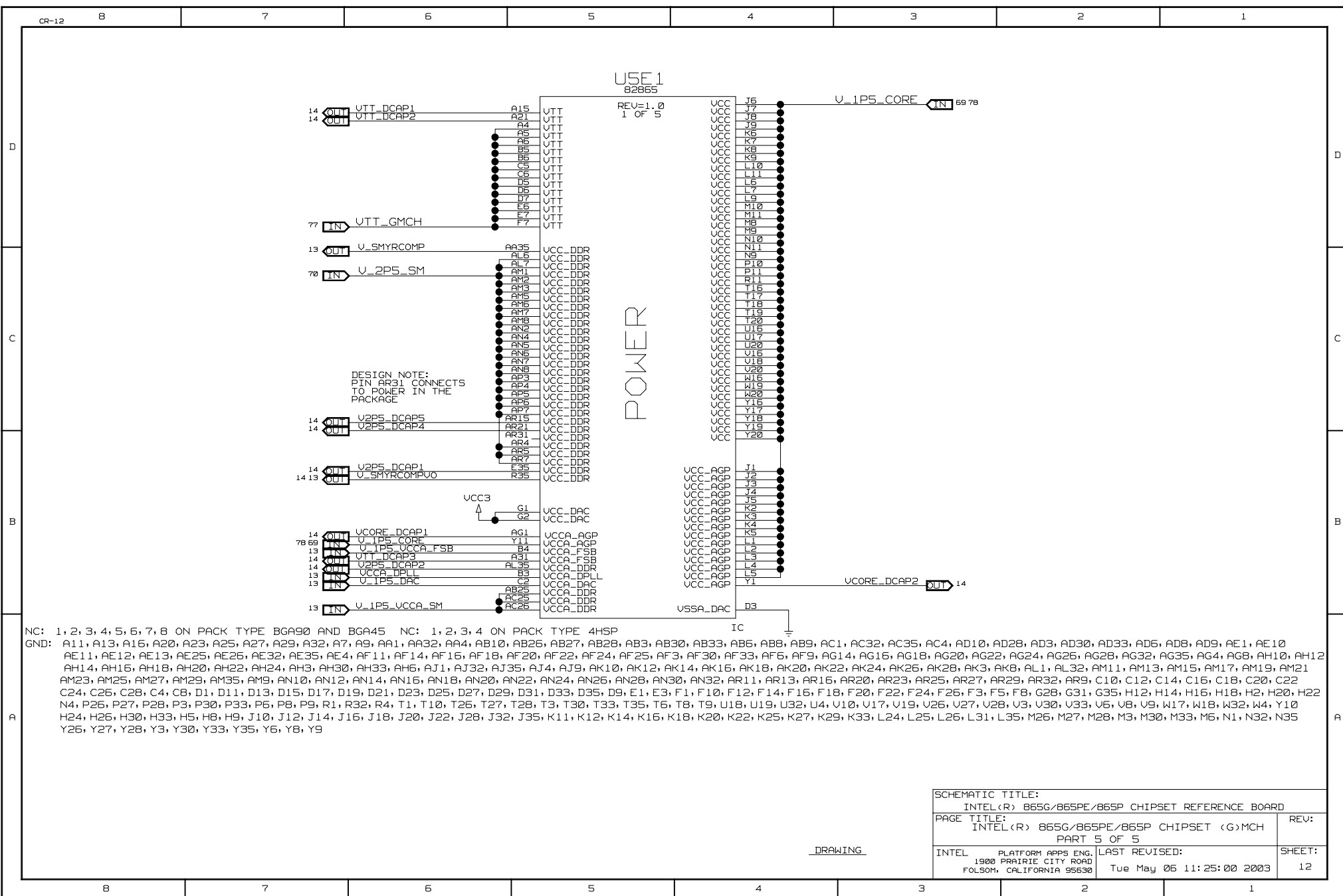


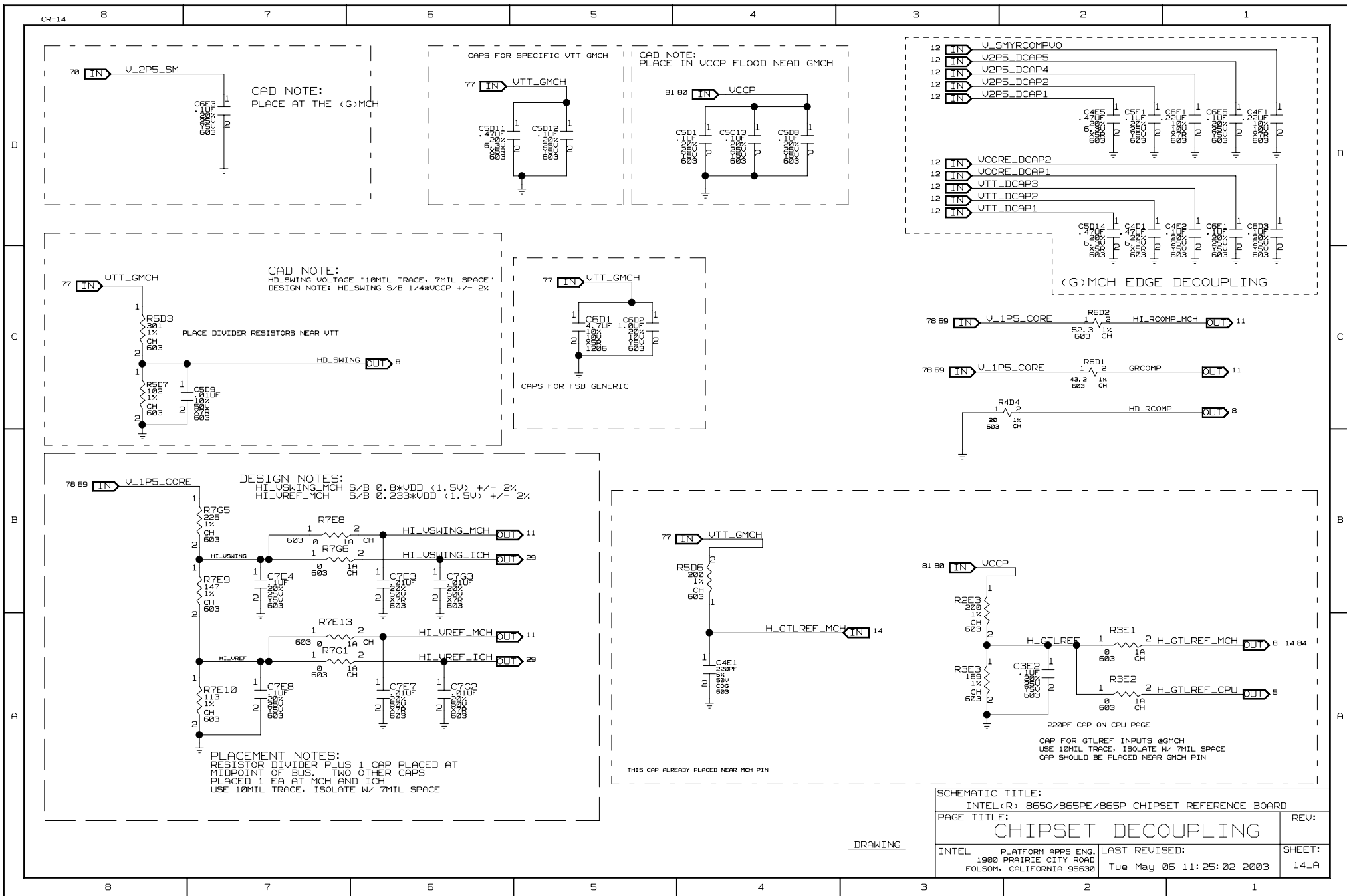
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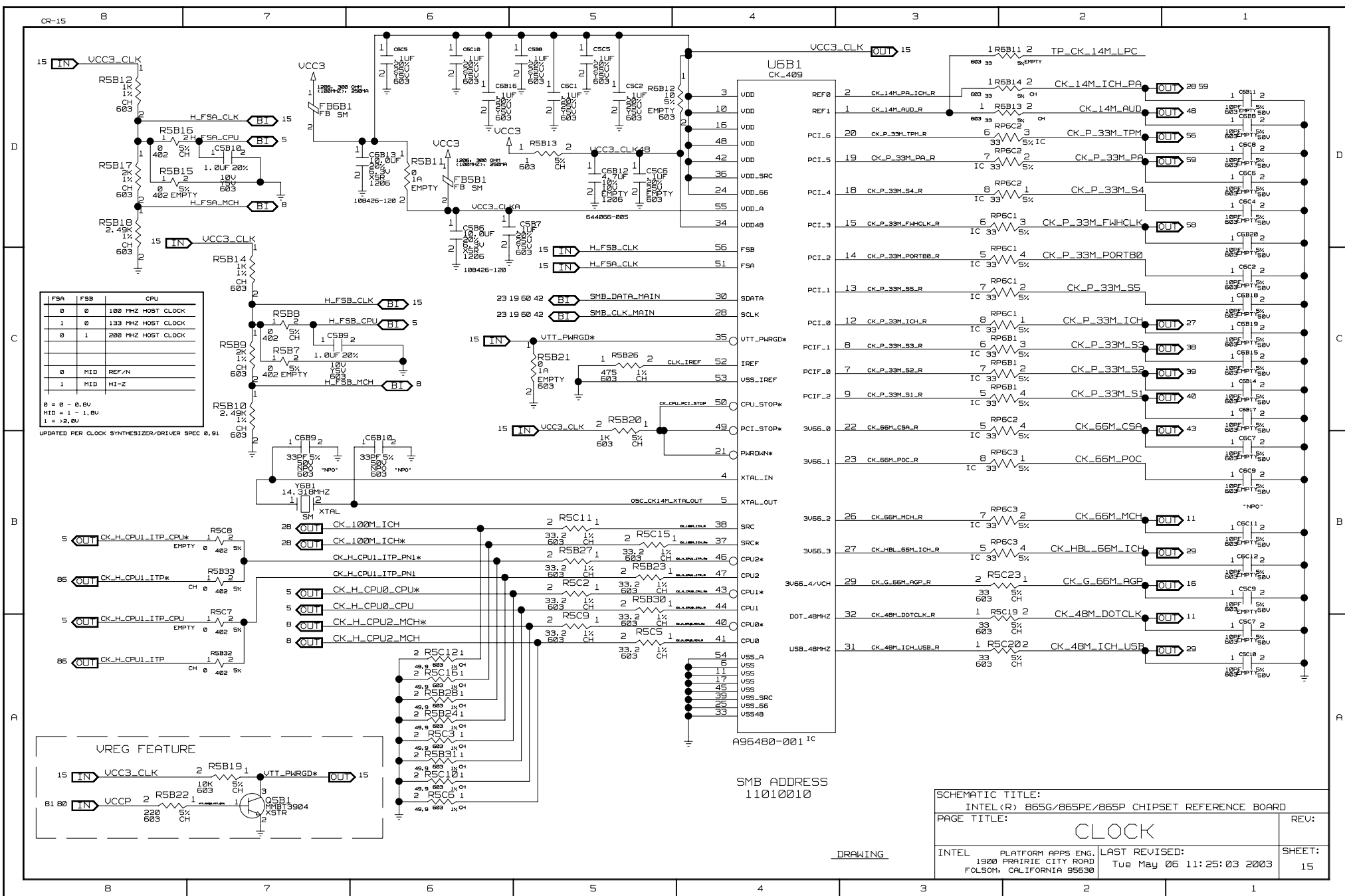


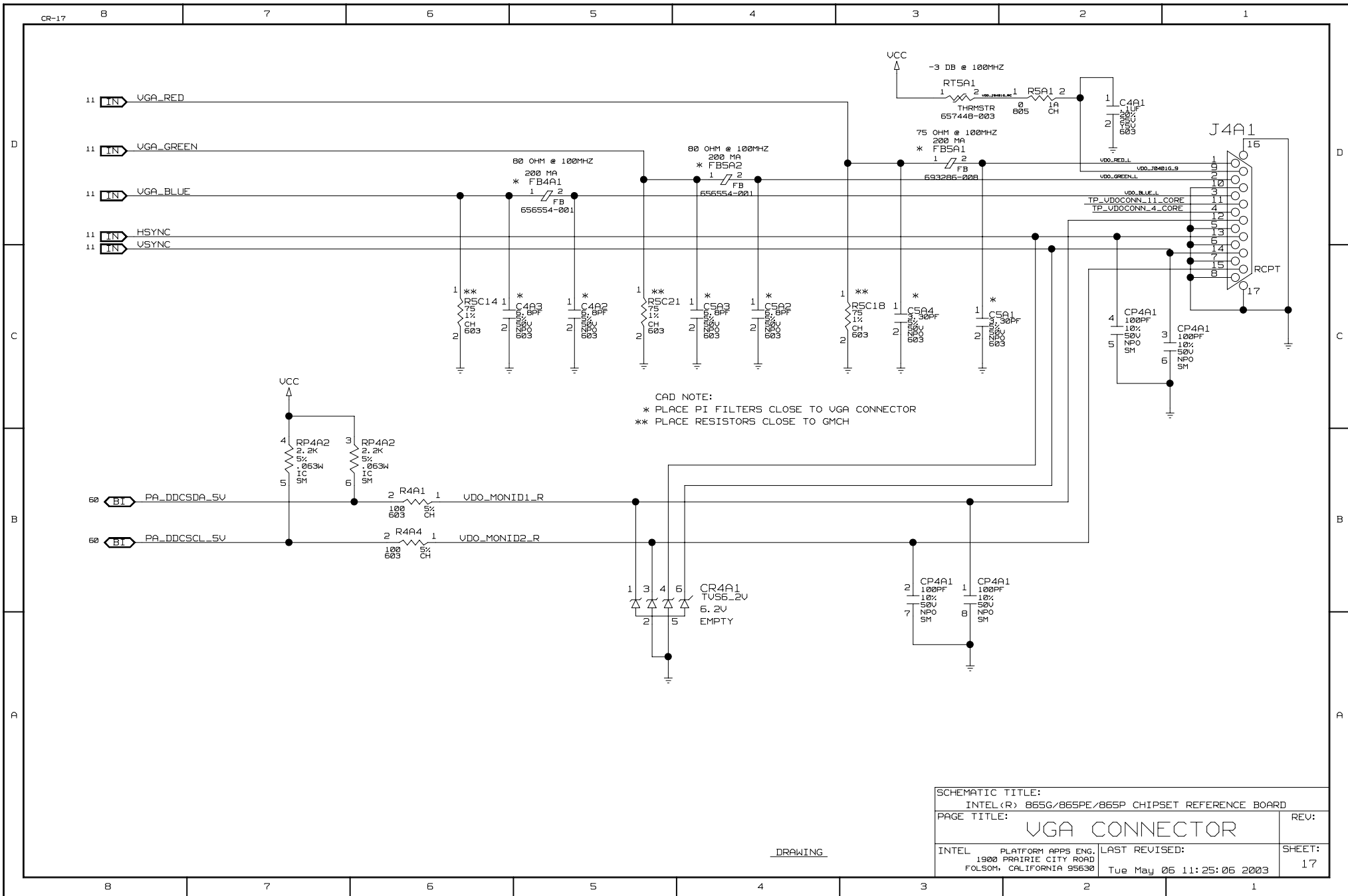


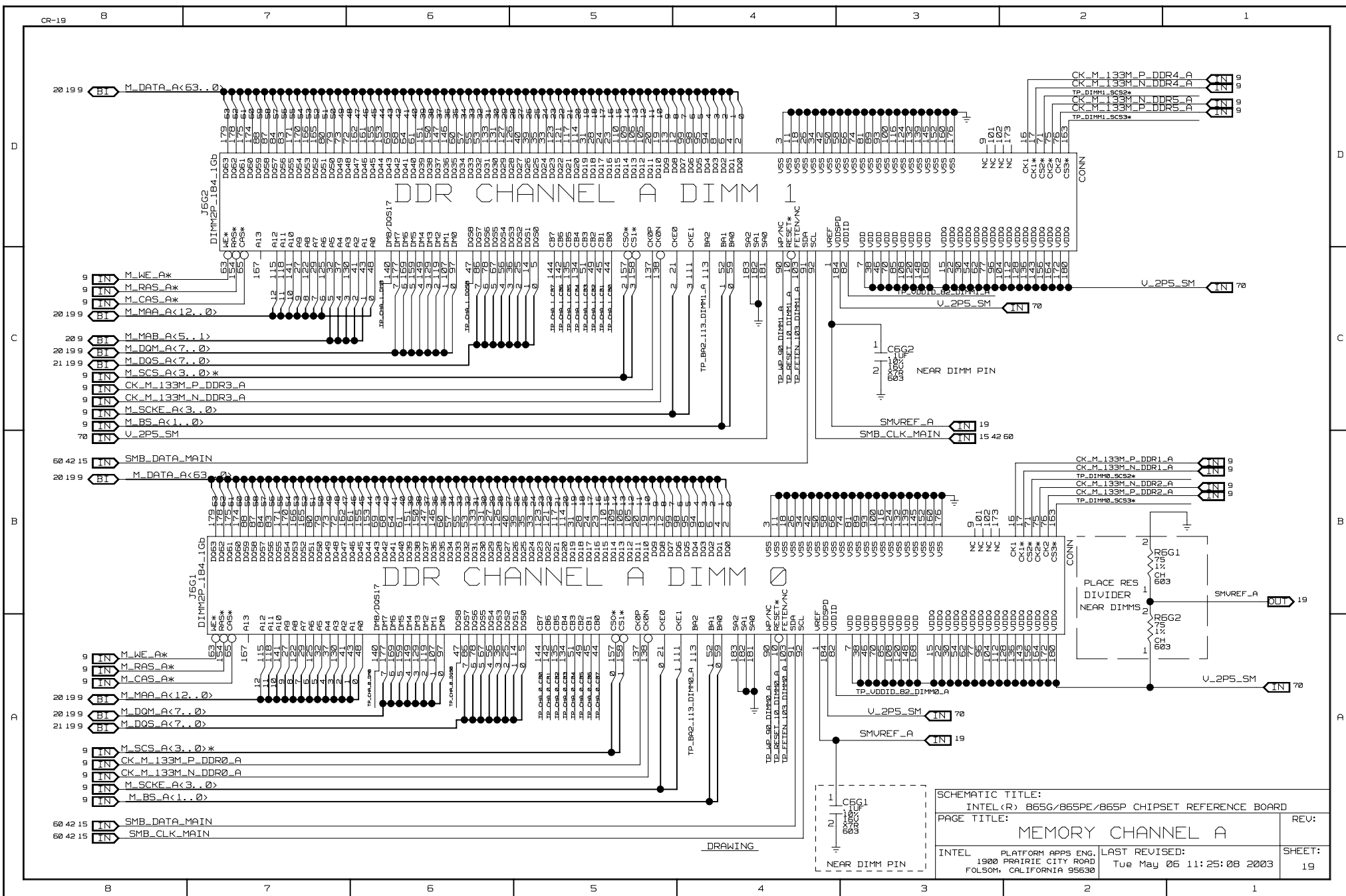












CR-20

8

7

6

5

4

3

2

1

DDR CHANNEL A

SPARE SECTIONS

70 IN V_1P25_MEMUIT

SPARE RPACKS

TP_RP20D2_1 4 5
RP3G1
47 SM 5% 063W ICTP_RP2105_1 4 5
RP3G5
56 SM 5% 063W IC

199 B1 M_MAB_A<5..1>

199 B1 M_DQM_A<7..0>

199 B1 M_DATA_A<63..0>

199 B1 M_MAA_A<12..0>

70 IN V_1P25_MEMUIT

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INTEL(R) B65G/B65PE/B65P CHIPSET REFERENCE BOARD

PAGE TITLE:

DDR RESISTOR TERMINATION

REV:

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630LAST REVISED:
Tue May 06 11:25:09 2003

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8

7

6

5

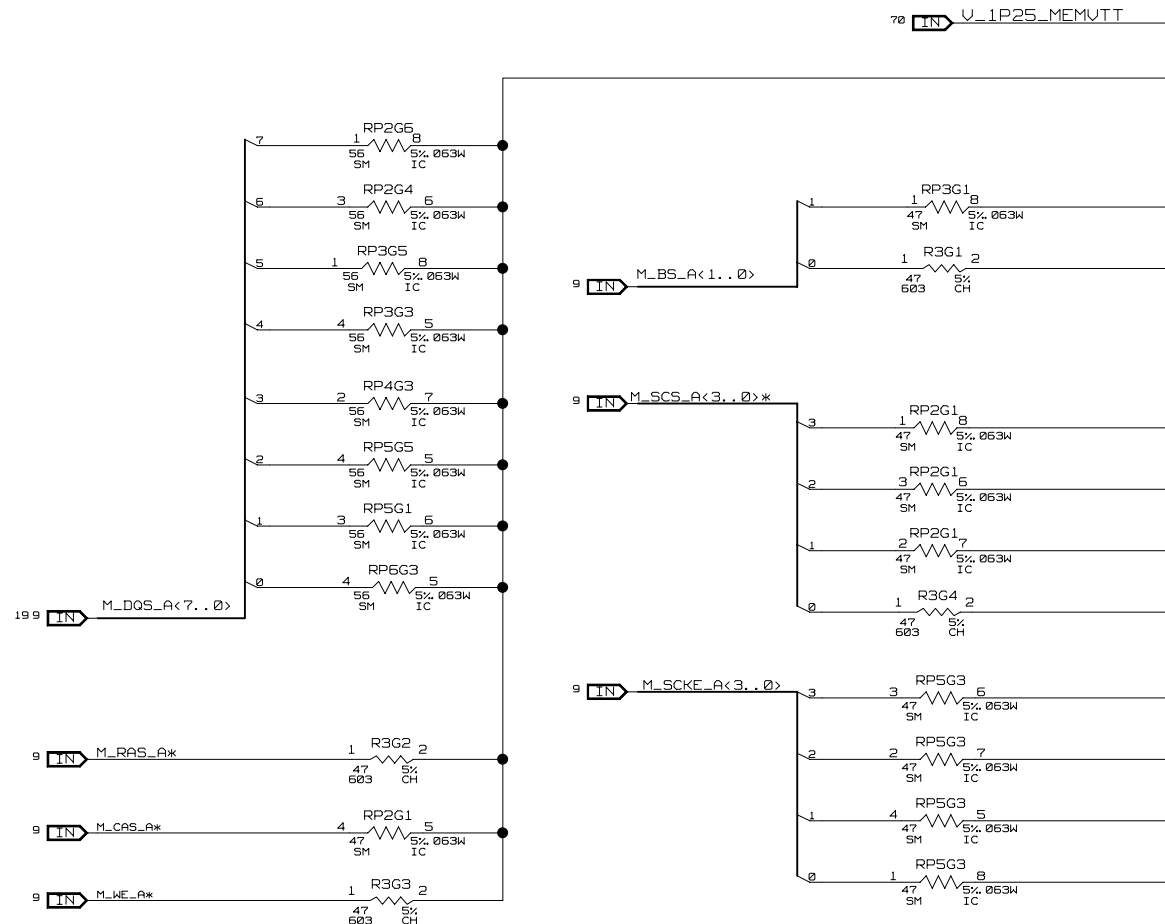
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3

2

1

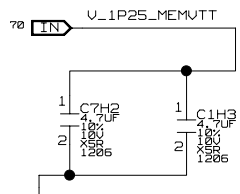
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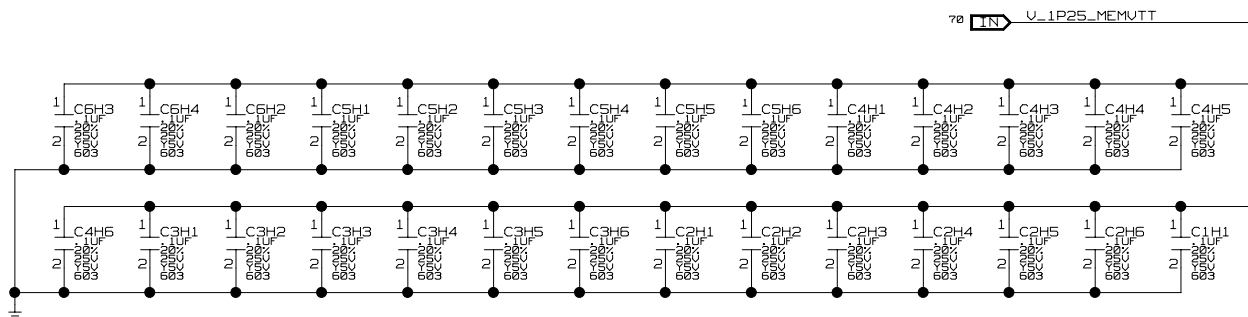
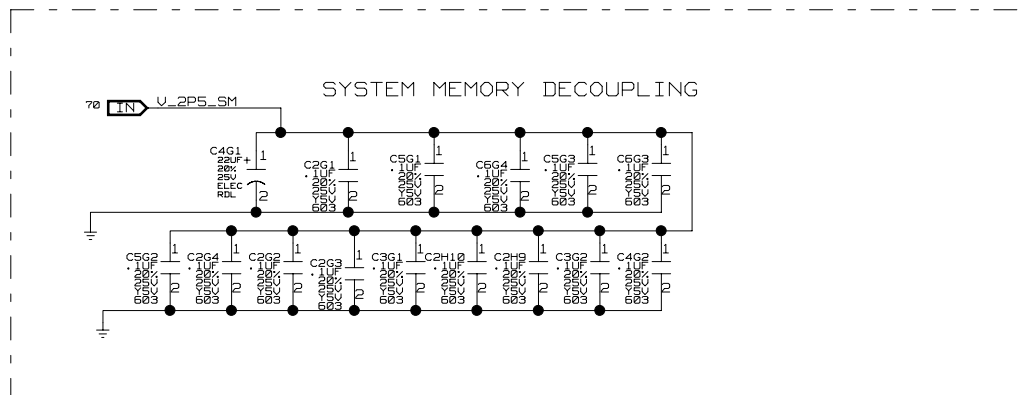
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DDR CHANNEL A



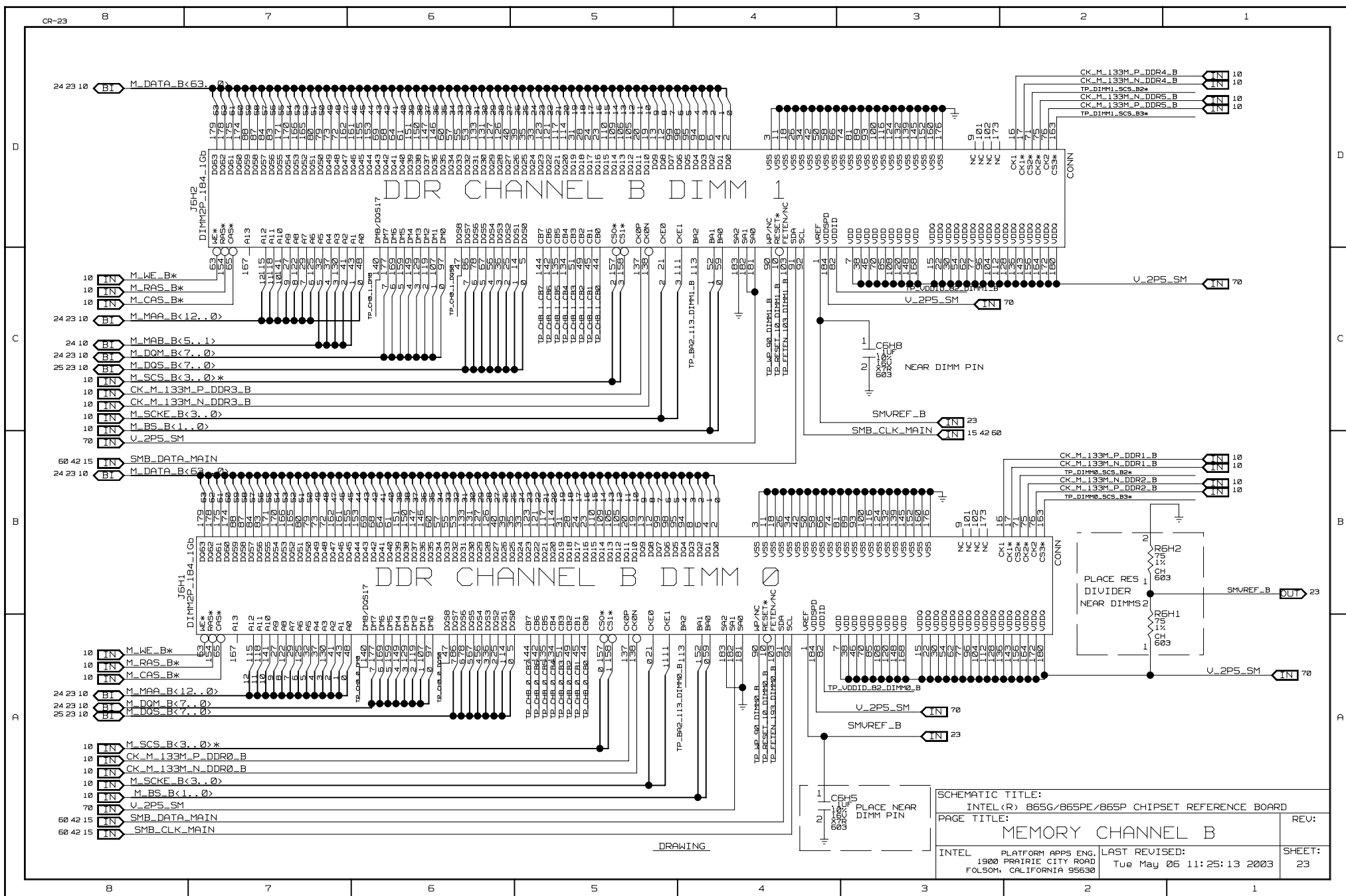
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DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

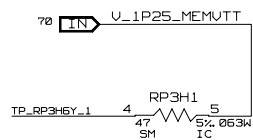
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DECOUPLING CAPACITORS	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 05 11:25:12 2003
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DDR CHANNEL B

SPARE SECTIONS

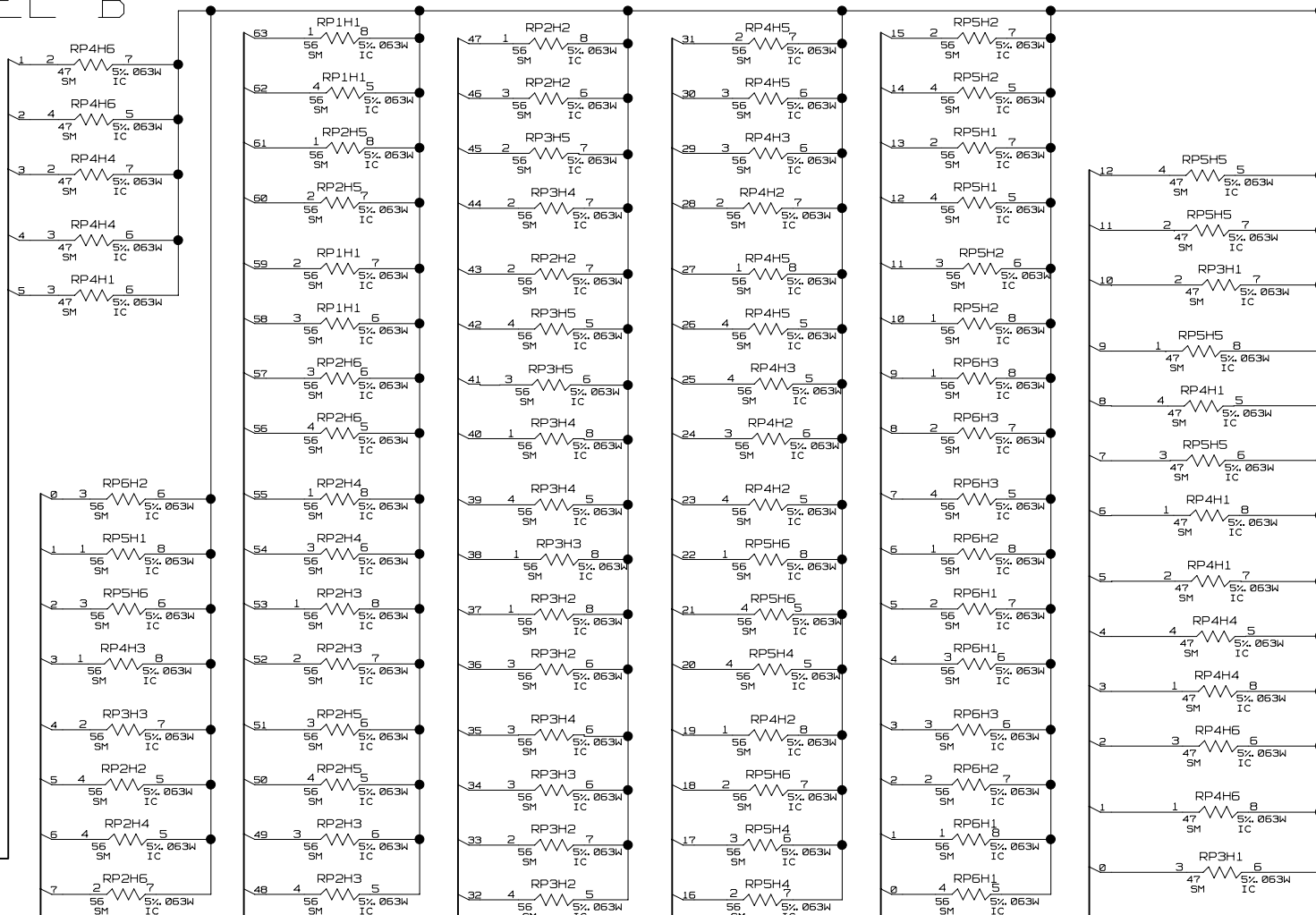
70 **IN** V_1P25_MEMVTT

23 10 **BI** M_MAB_B<5..1>

23 10 **BI** M_DQM_B<7..0>

23 10 **BI** M_DATA_B<63..0>

23 10 **BI** M_MAA_B<12..0>



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DDR RESISTOR TERMINATION

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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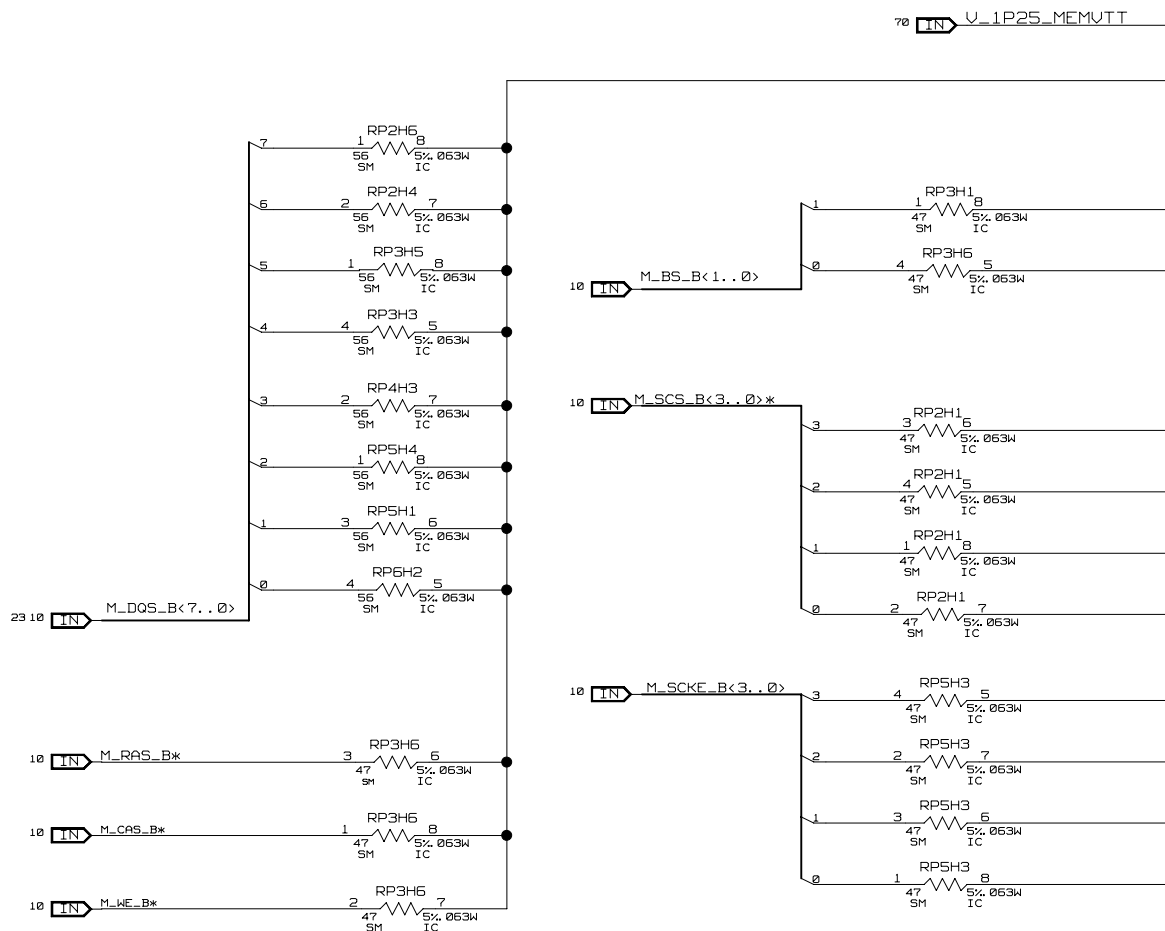
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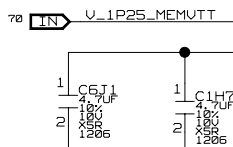
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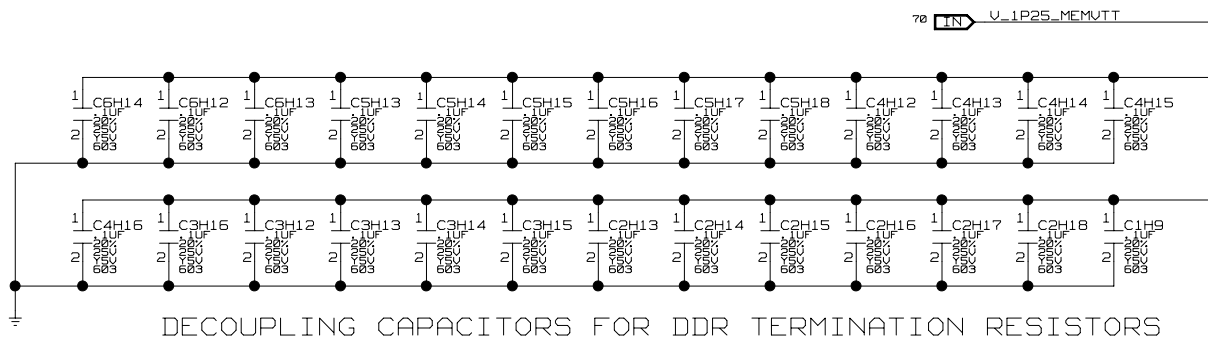
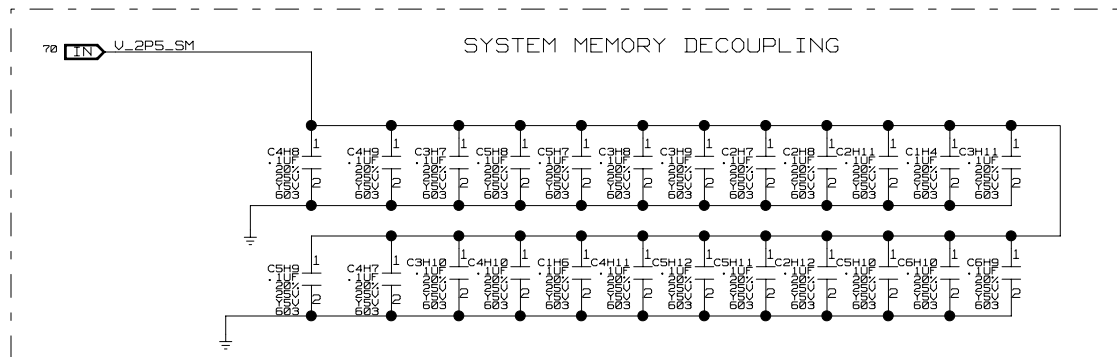
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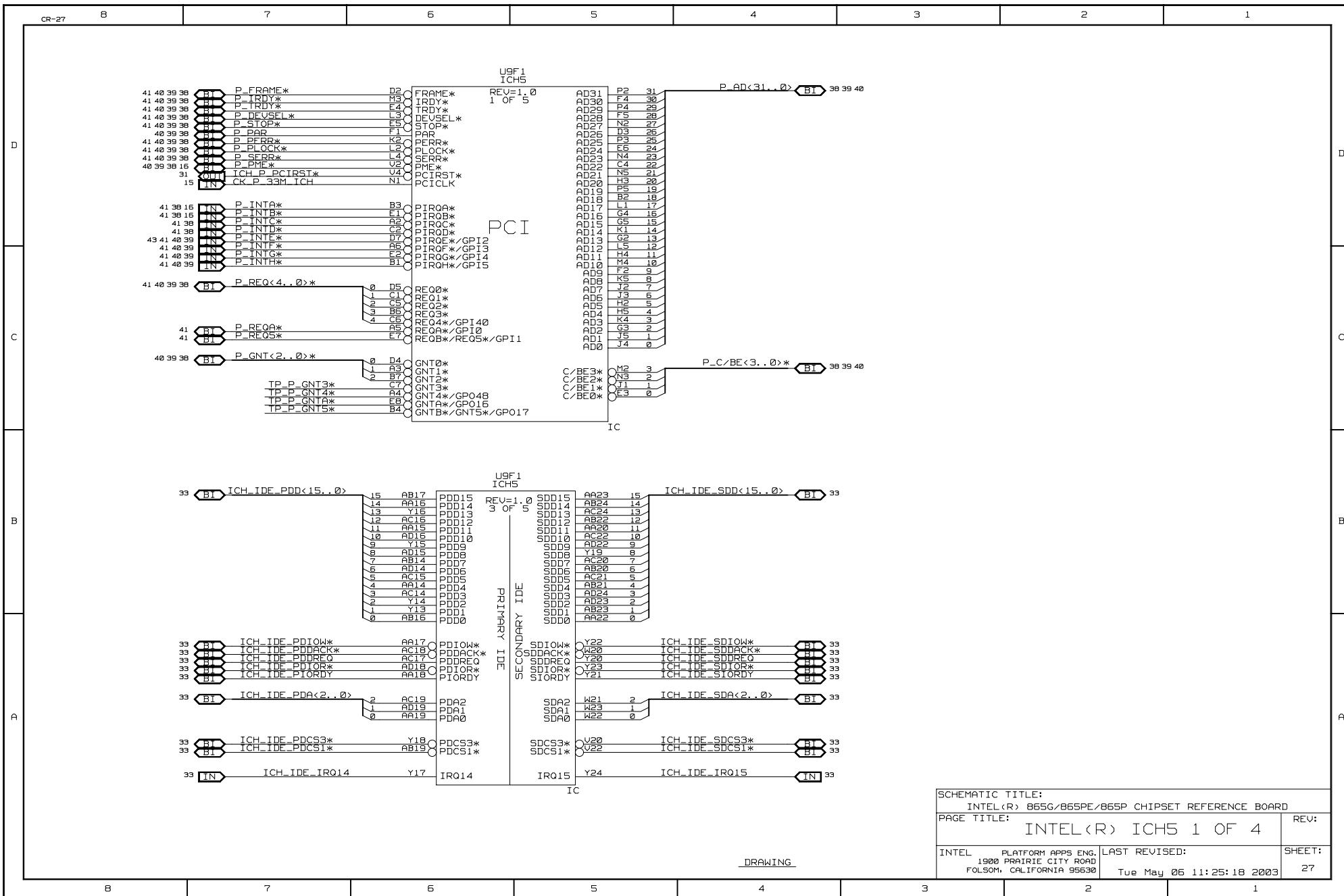


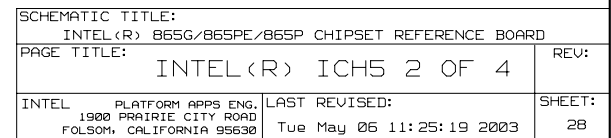
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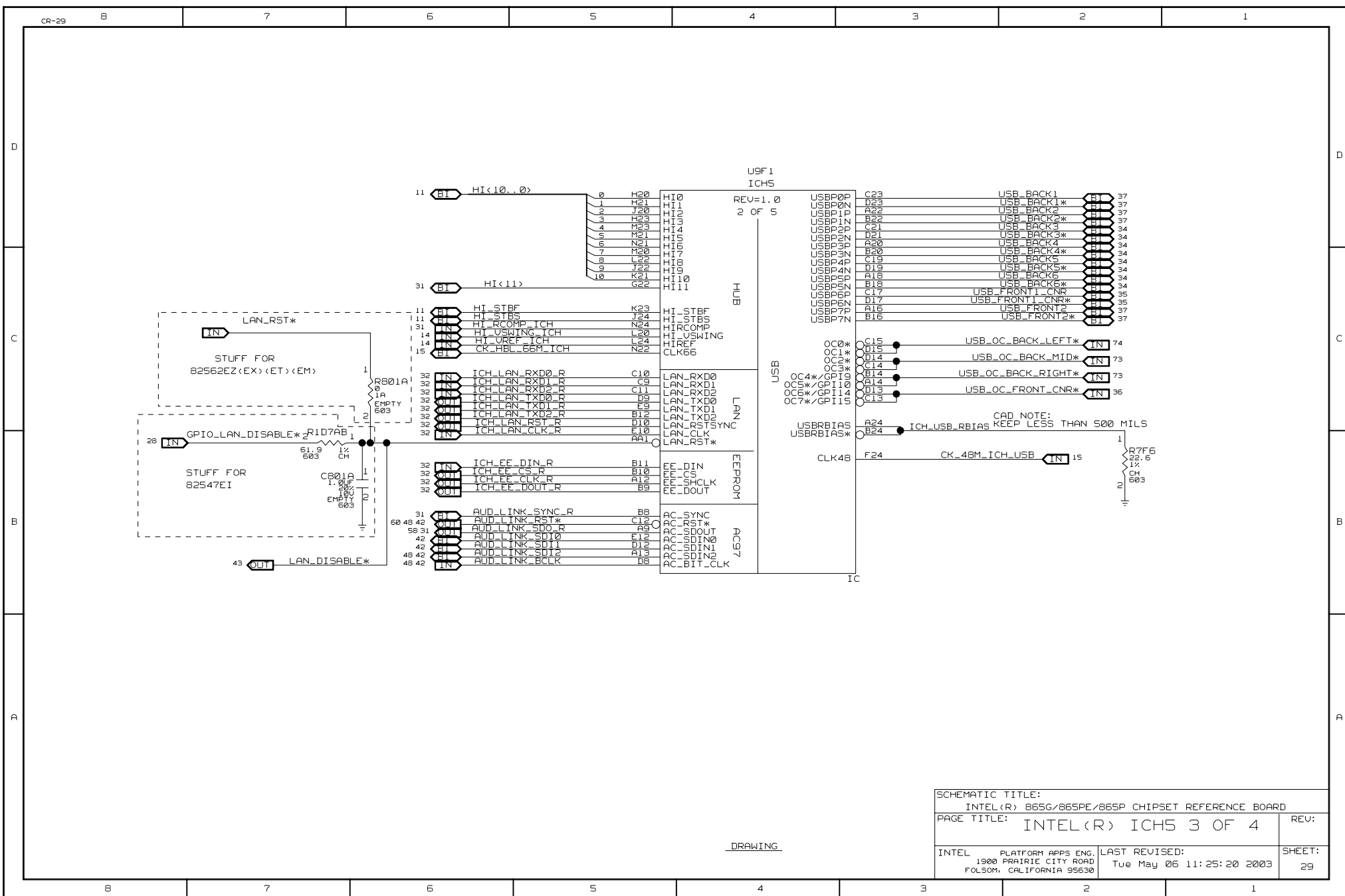


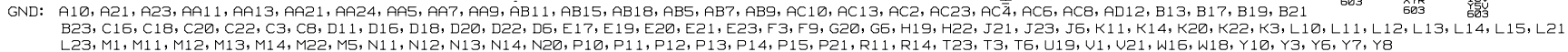
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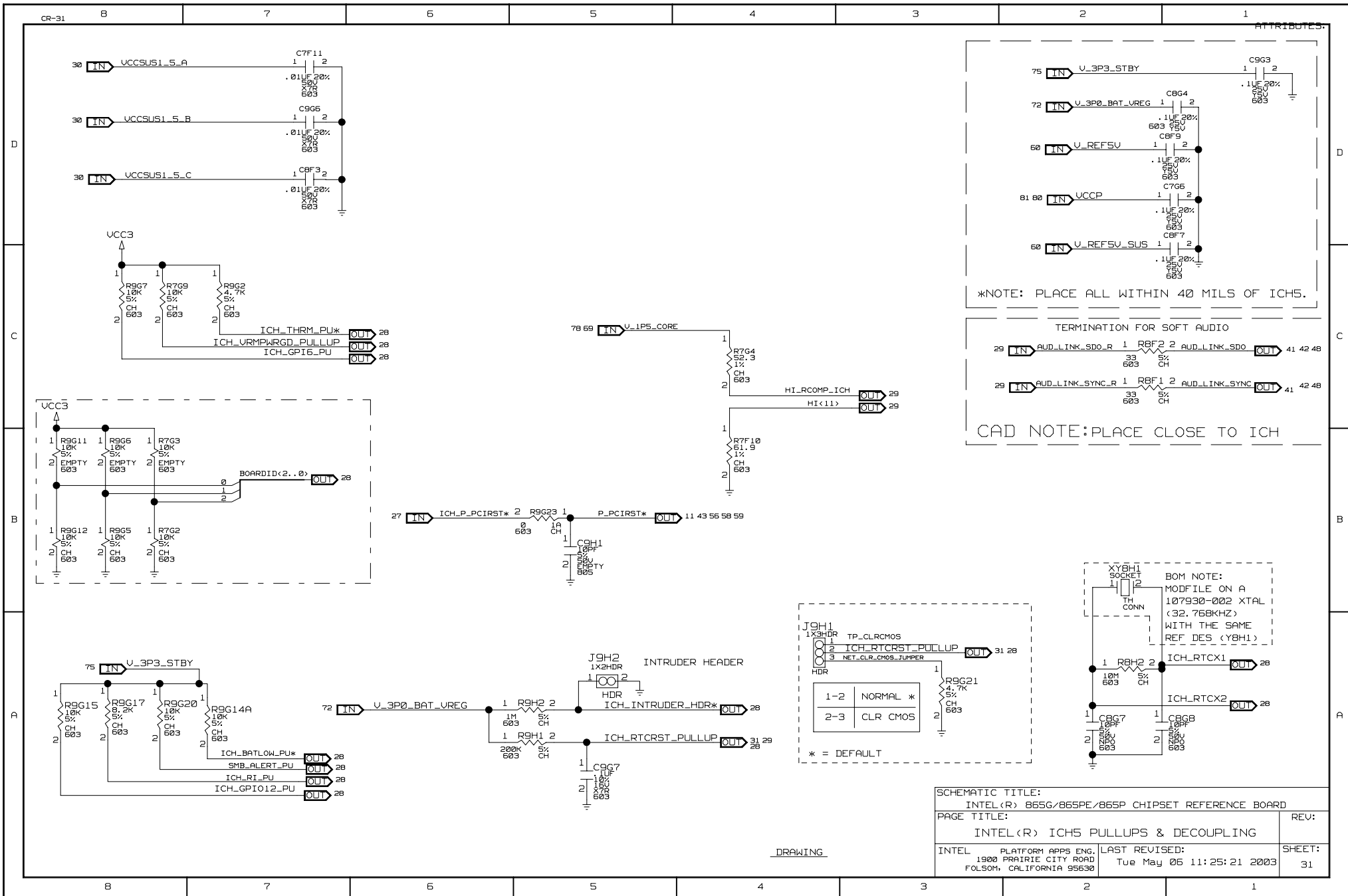


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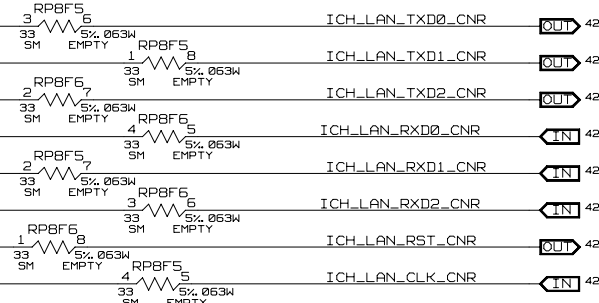


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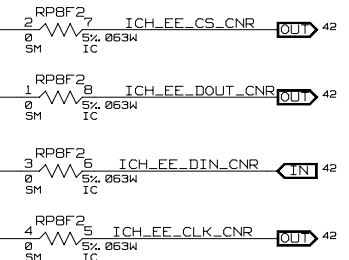


PROPERTIES FOR STUFFING OPTIONS: BOM= CNR_LINK_LAN
CNR STUFFING OPTION FOR LAN-UP SOLUTION

TO CNR



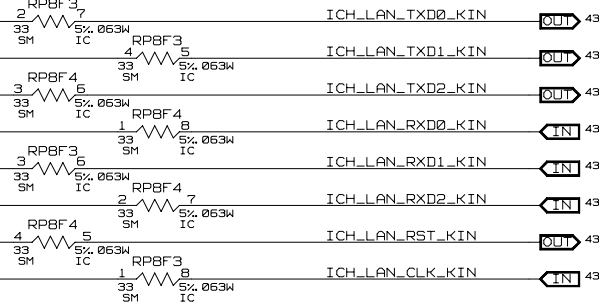
TO CNR



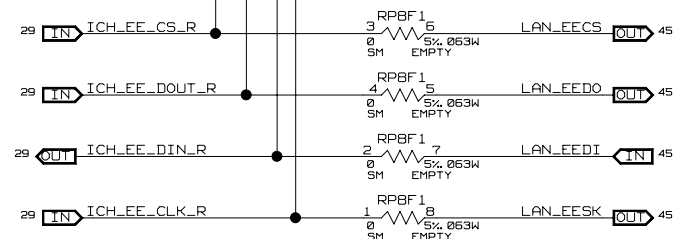
0-OHMS ARE PROVIDED
TO MINIMIZE STUBS
ON LAN INTERFACE

PROPERTIES FOR STUFFING OPTIONS: BOM= LAN_LINK_CNR

TO LAN (KINNERETH-R)



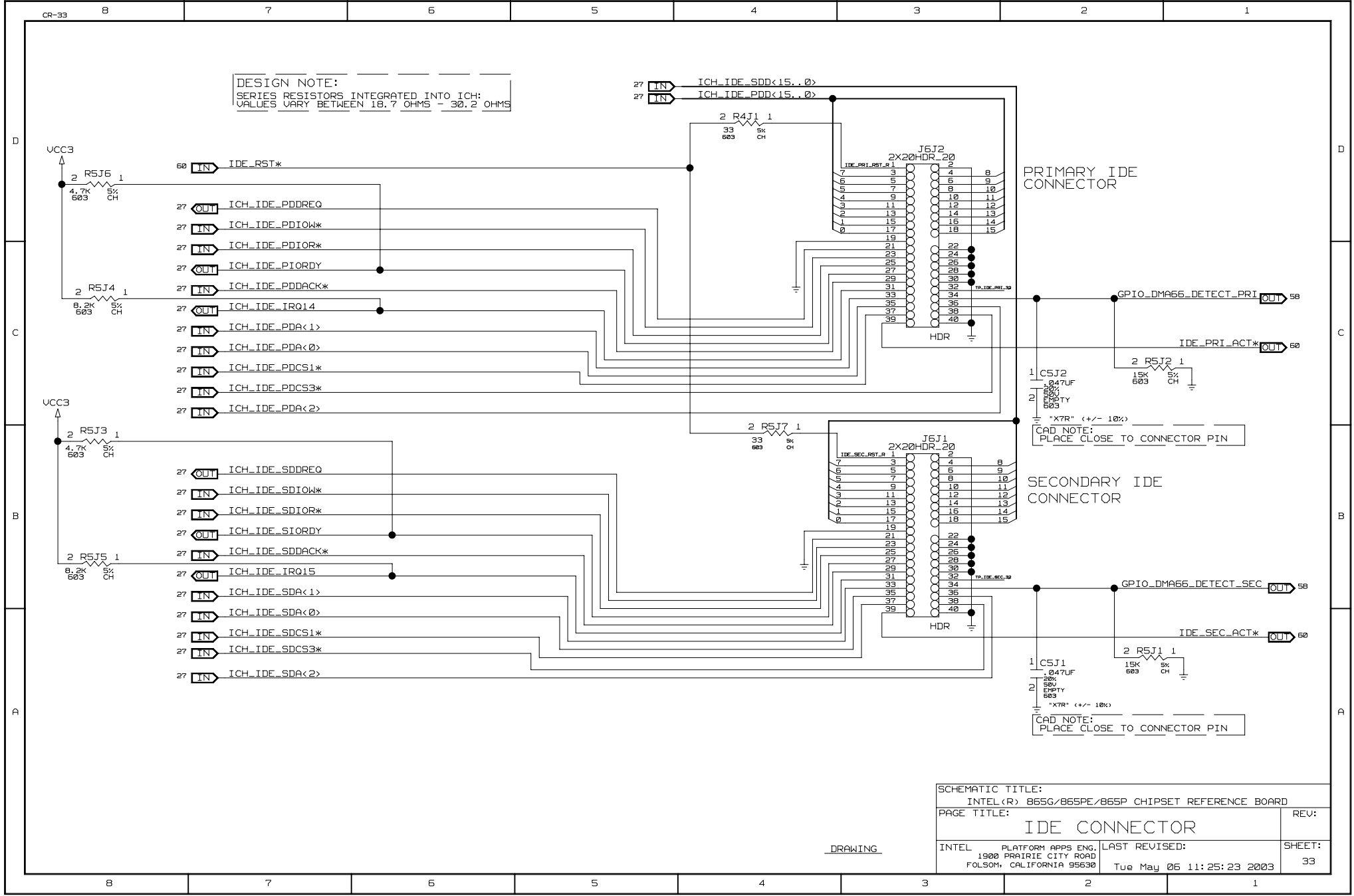
FROM ICH5

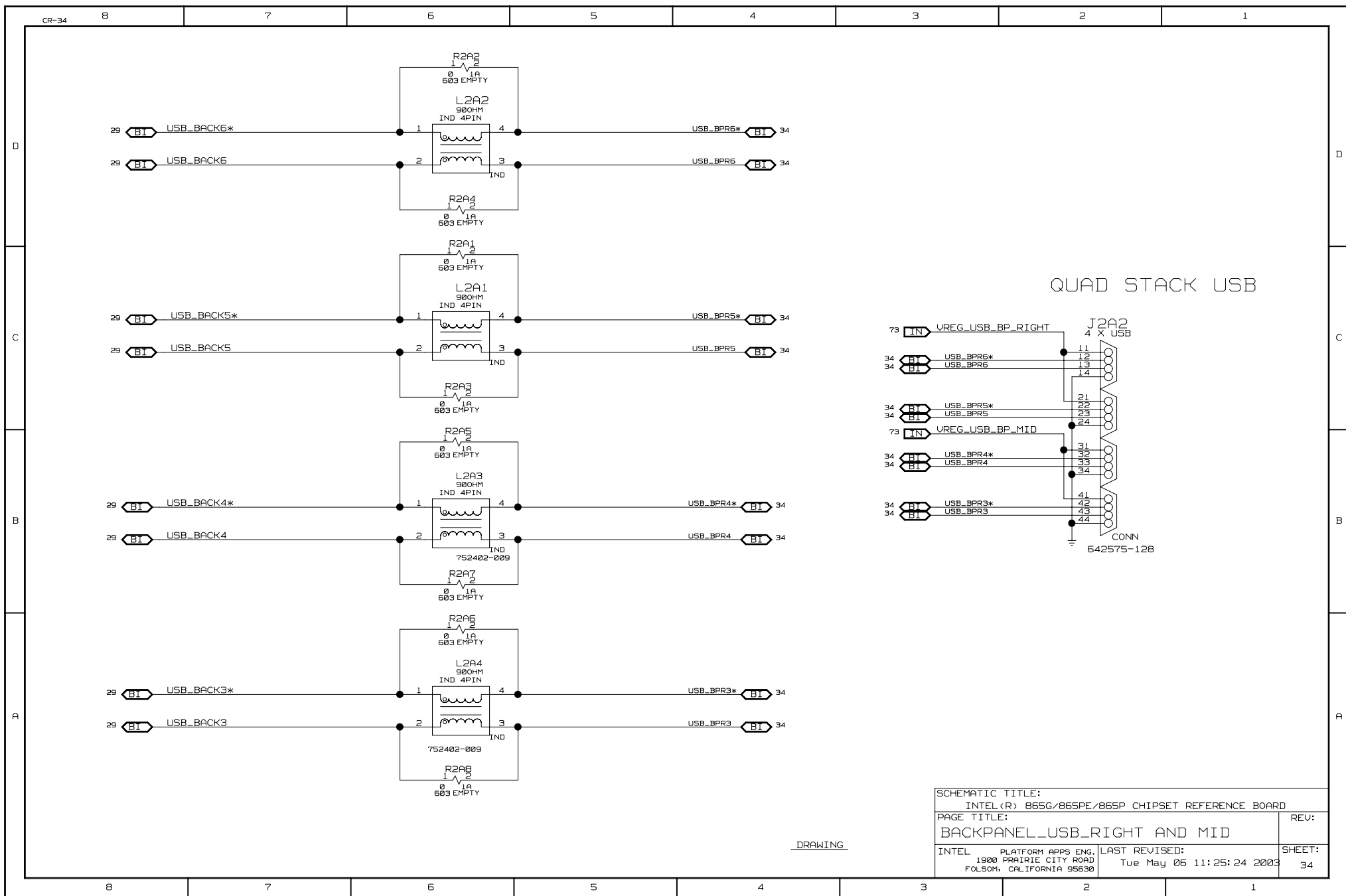


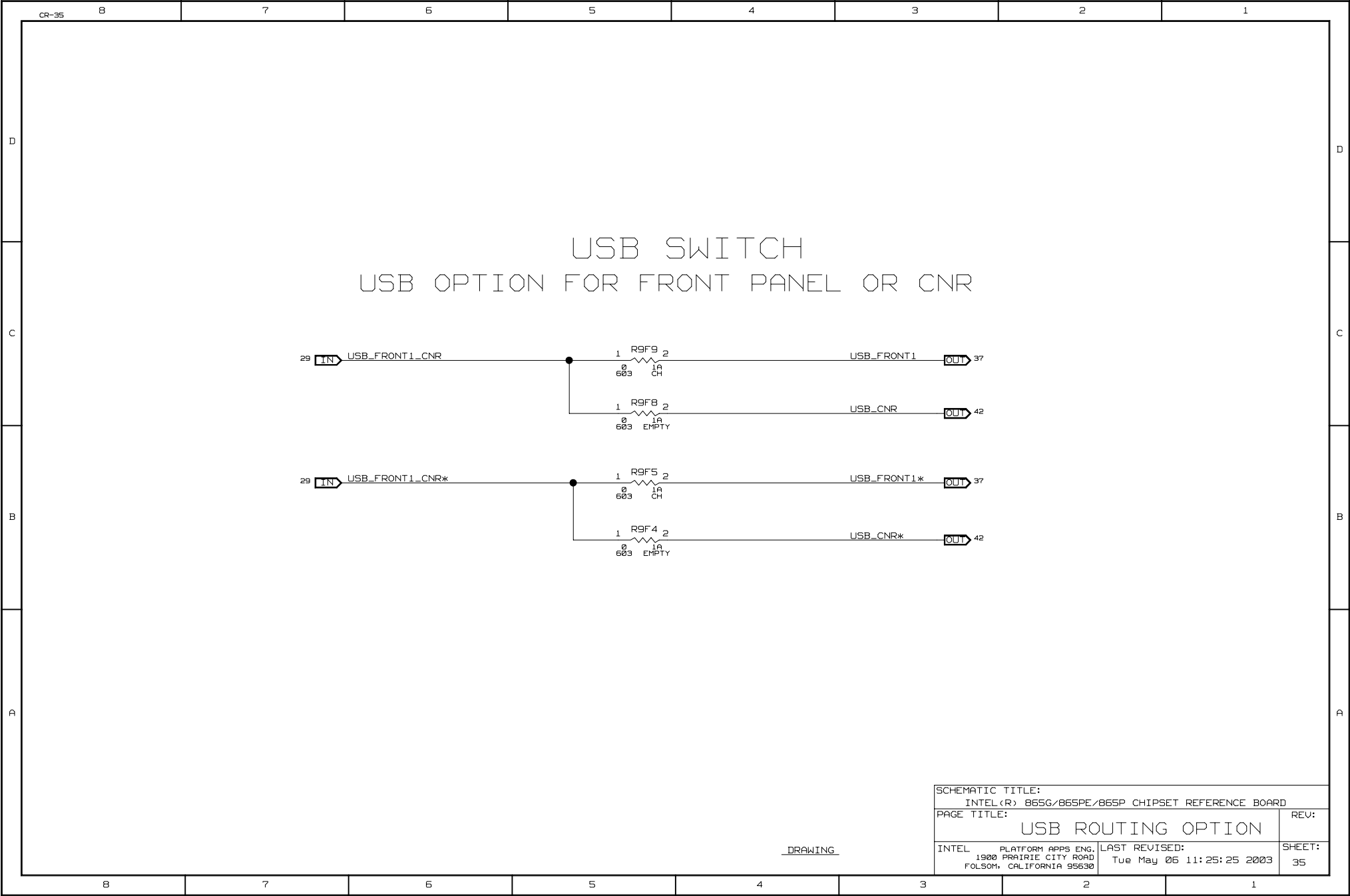
TO LAN EEPROMS

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LAST REVISED: Tue May 06 11:25:22 2003		

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SCHEMATIC TITLE:

INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD

PAGE TITLE:

USB ROUTING OPTION

REV:

INTEL

PLATFORM APPS ENG.

1900 PRAIRIE CITY ROAD

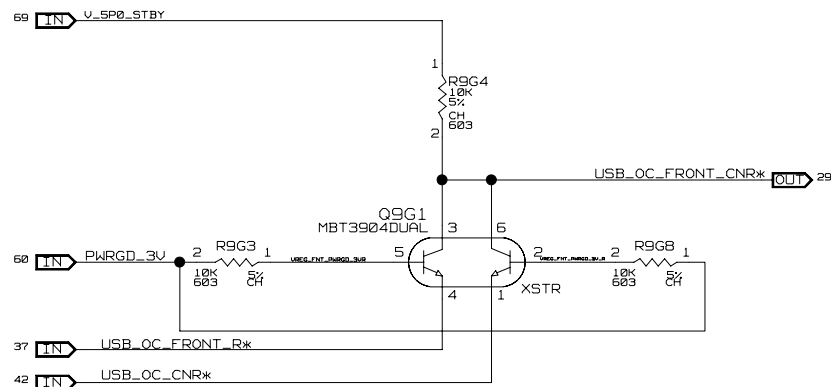
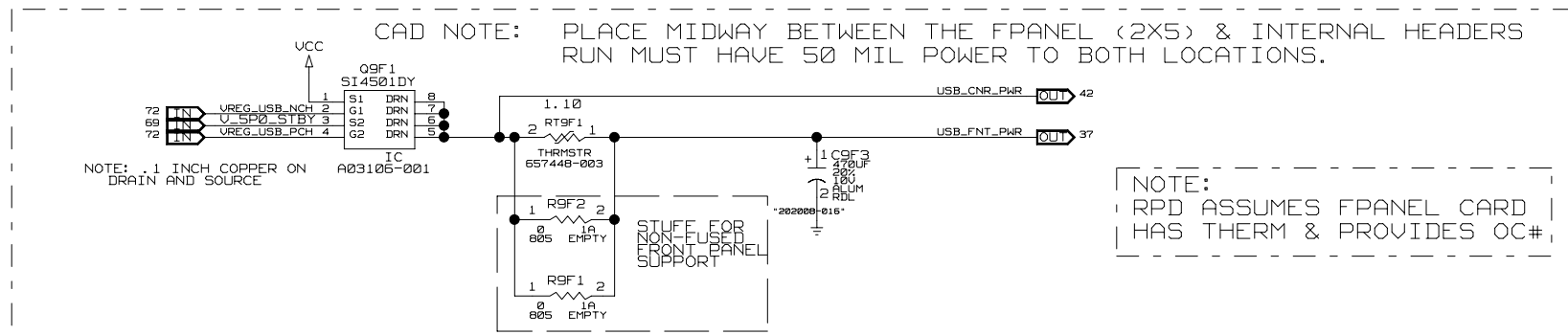
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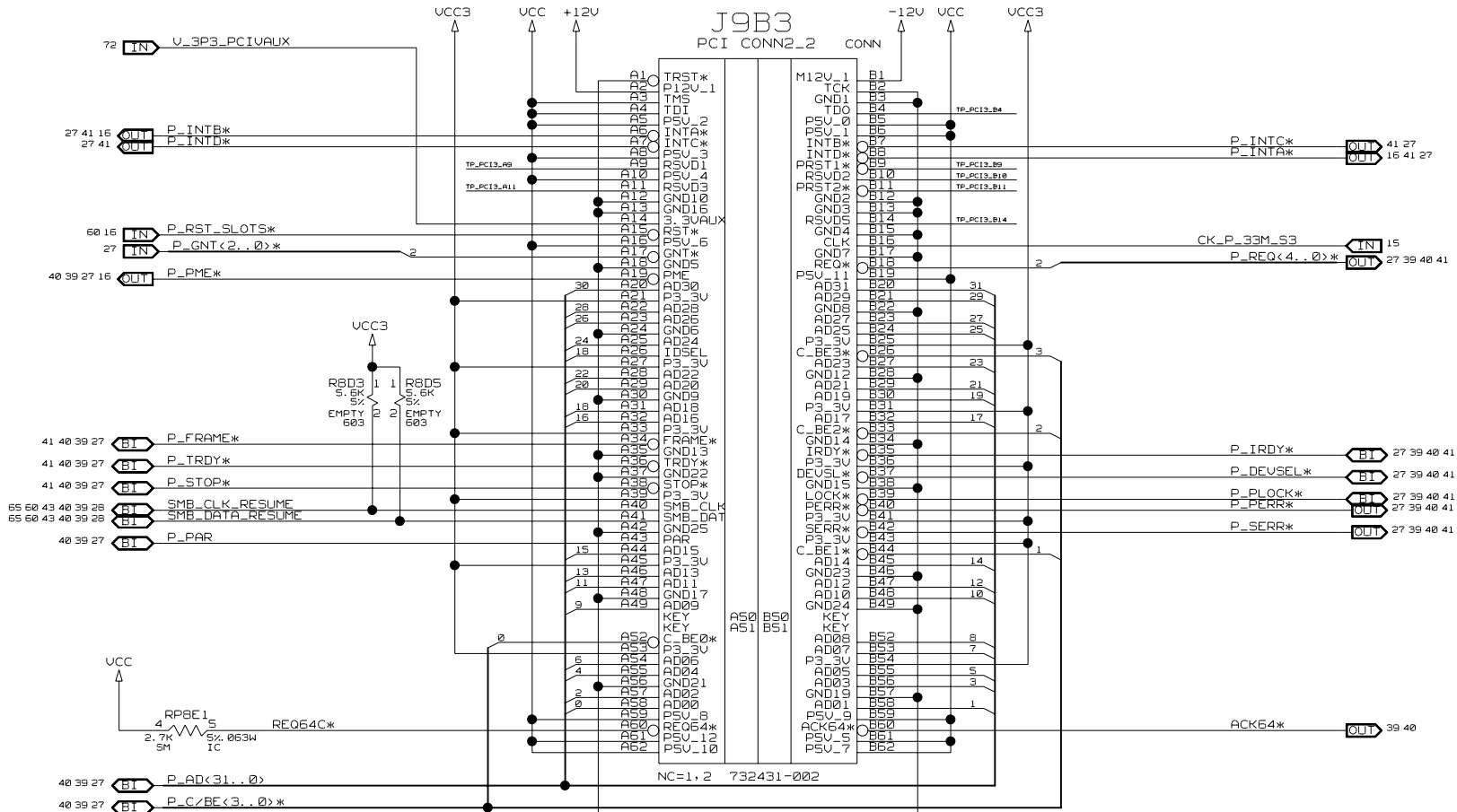
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INTEL	PLATFORM APPS ENG.	LAST REVISED:
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PCI SLOT 3

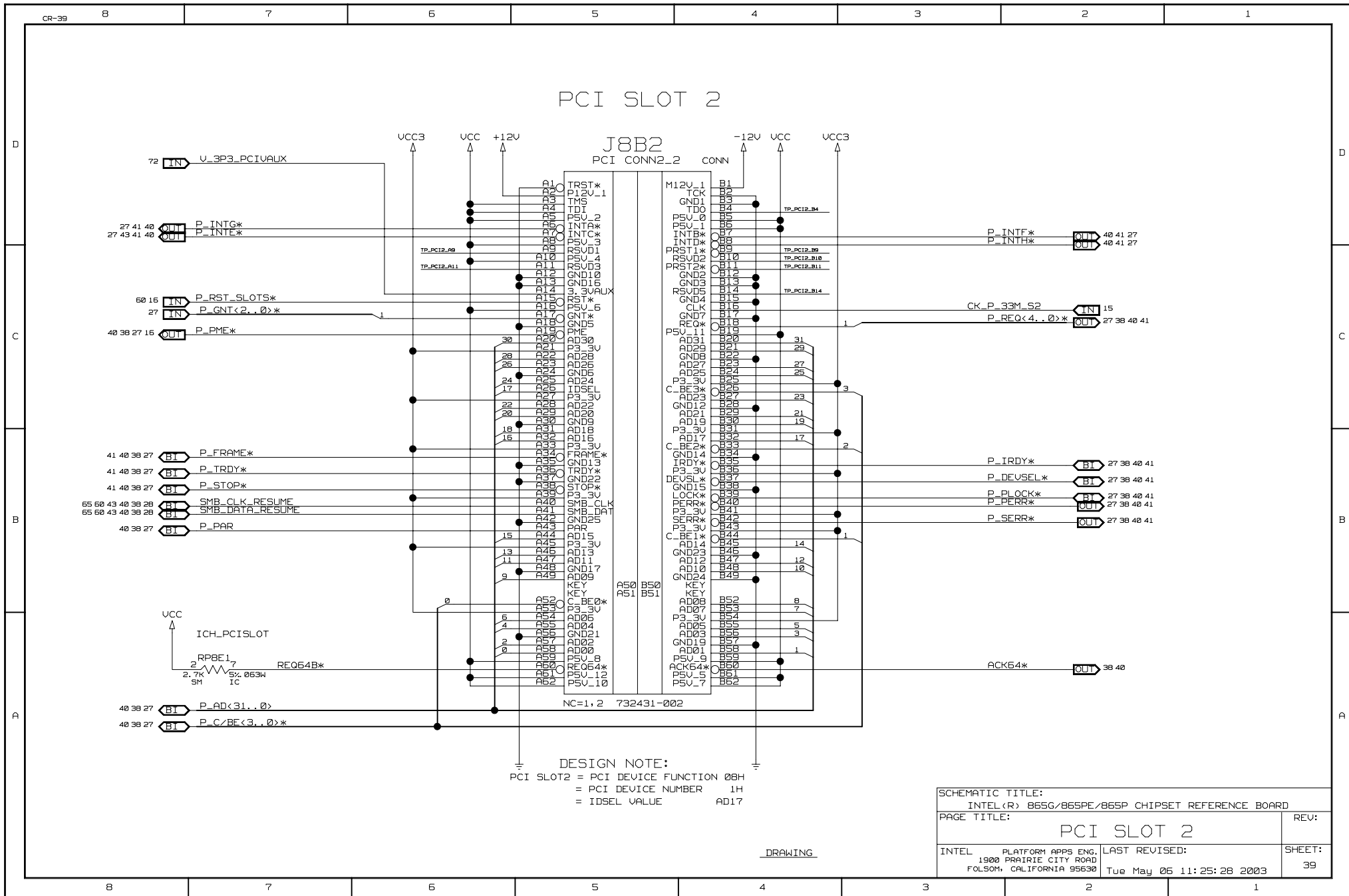


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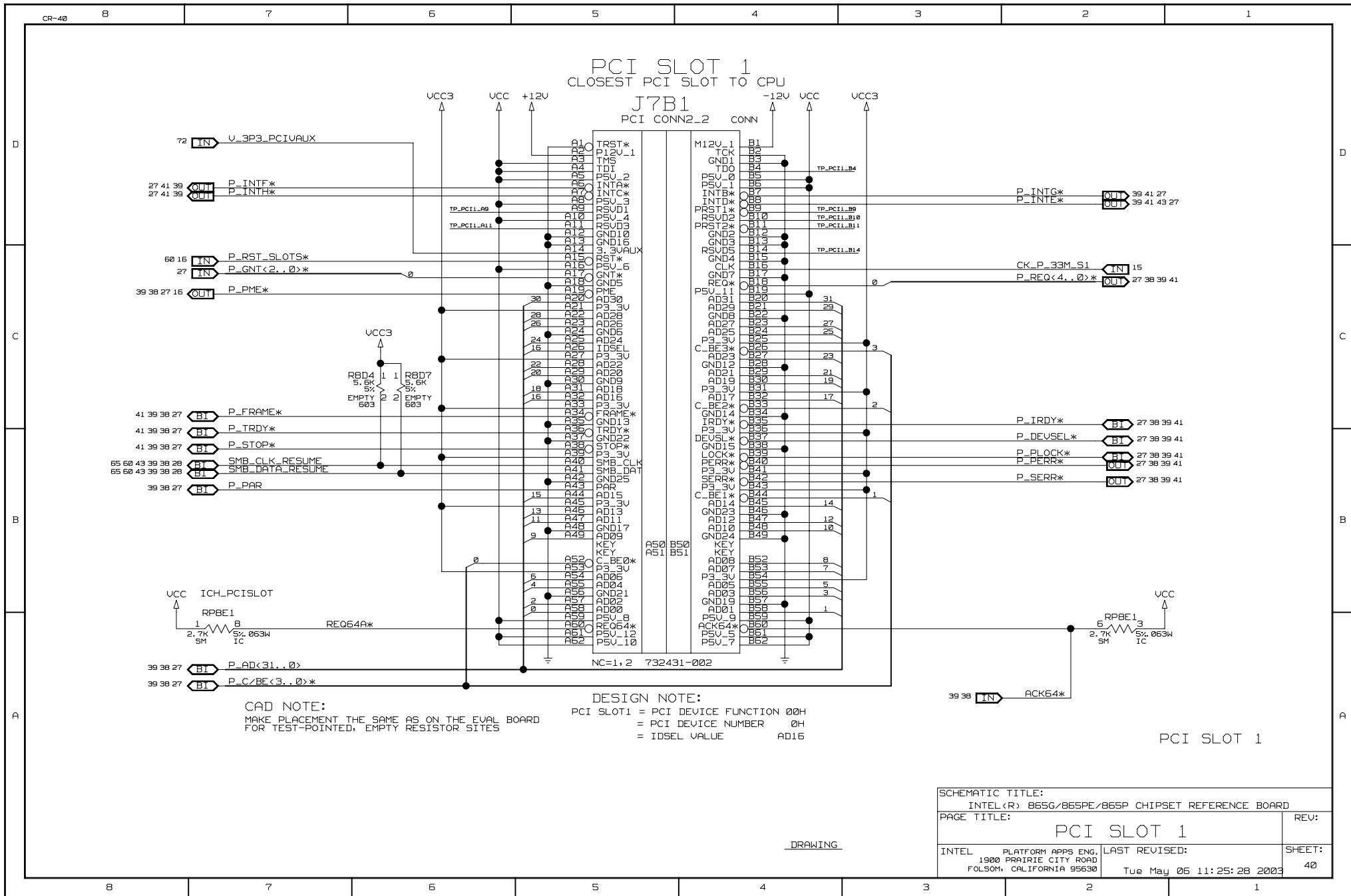
PCI SLOT3 = PCI DEVICE FUNCTION 10H
 = PCI DEVICE NUMBER 2H
 = IDSEL VALUE AD18

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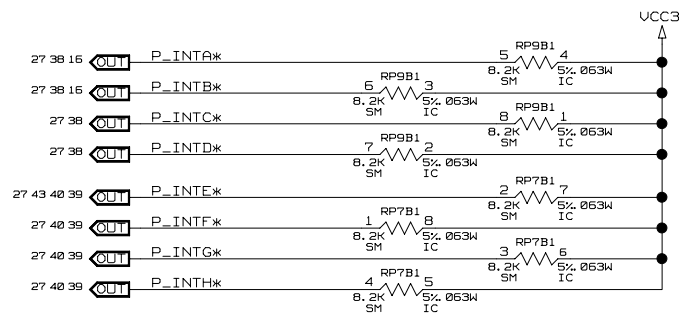
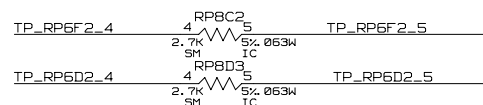
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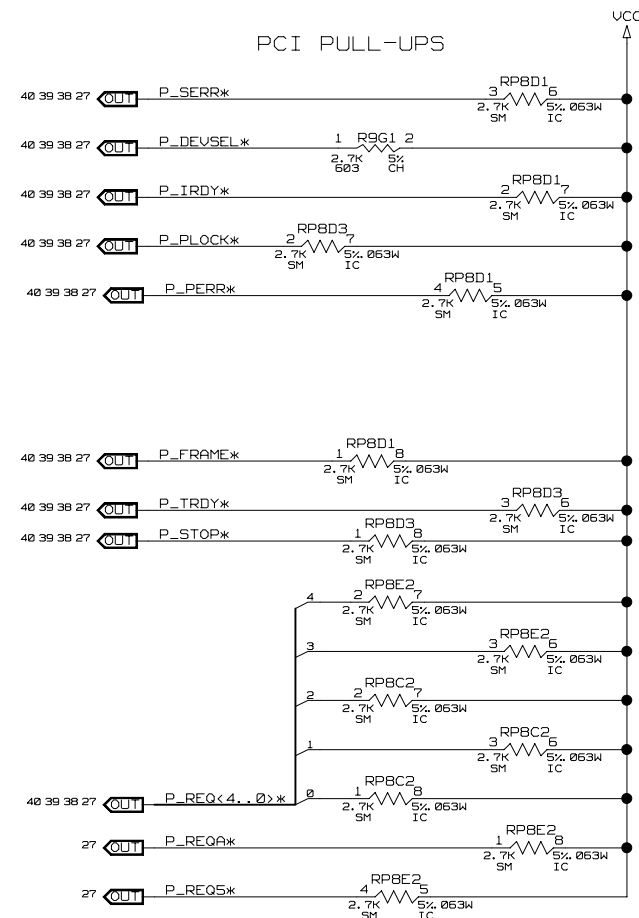
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PCI SLOT 2	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	SHEET: 39
LAST REVISED: Tue May 05 11:25:28 2003	



SPARE SECTIONS

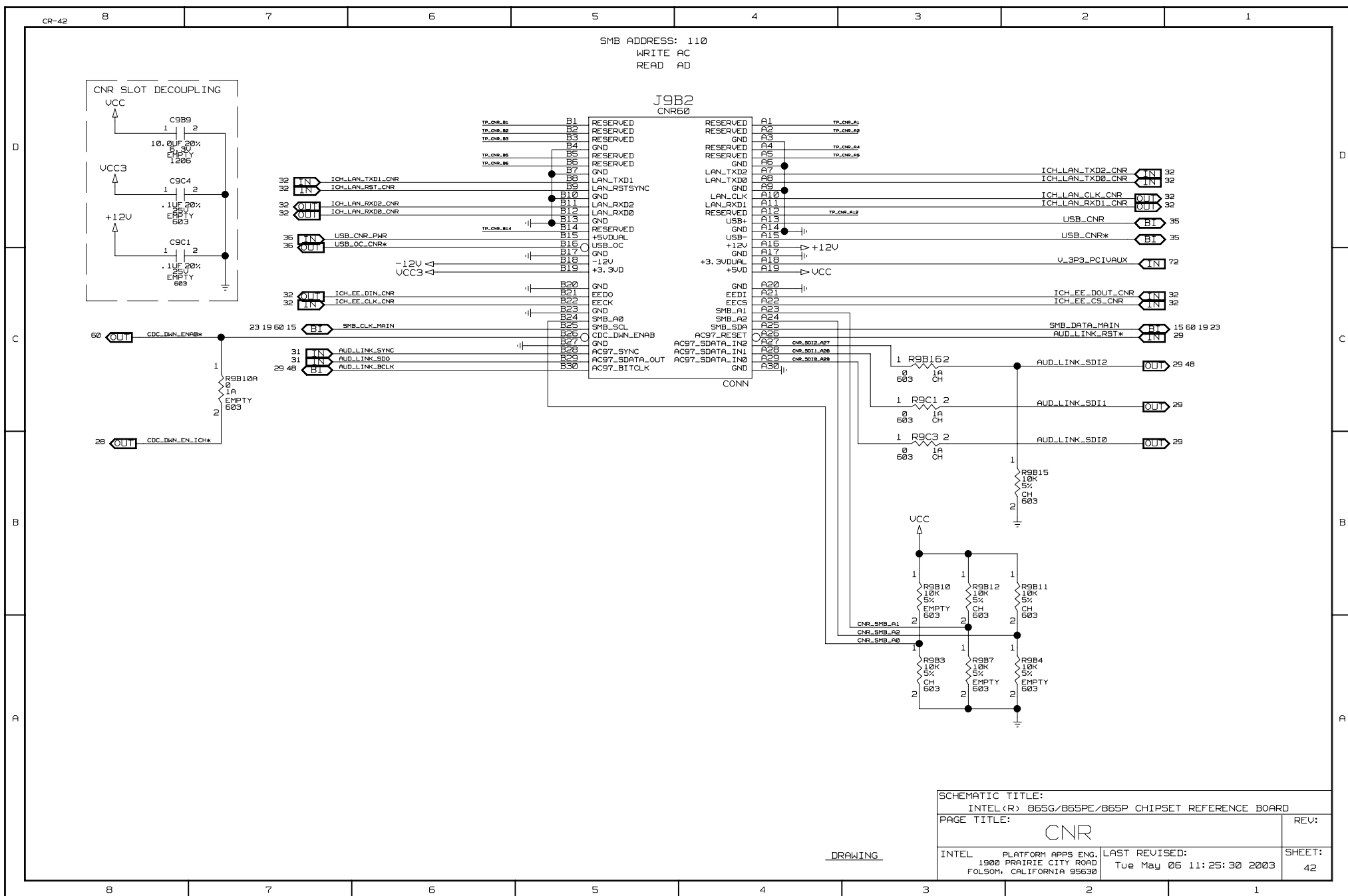


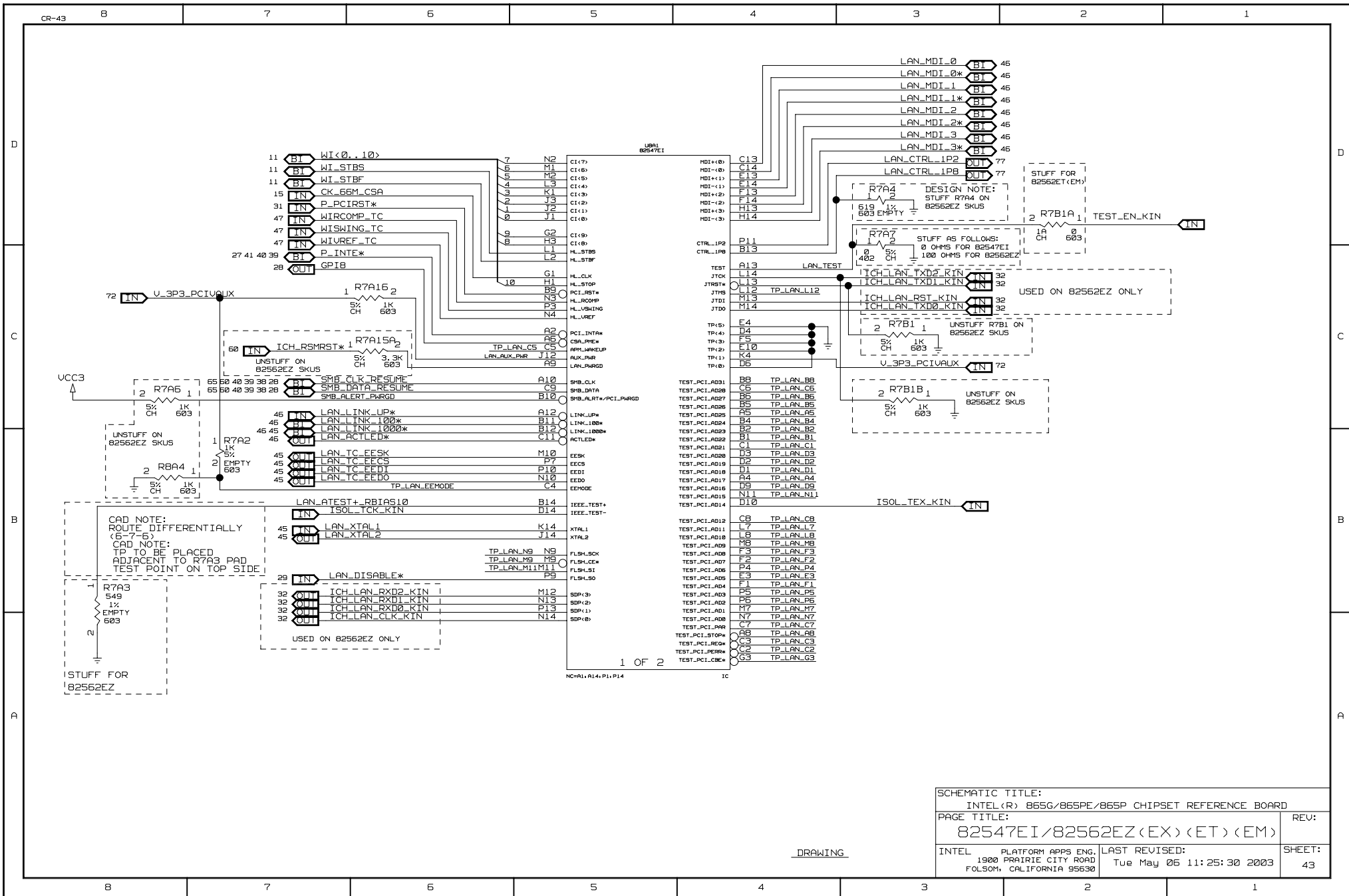
PCI PULL-UPS



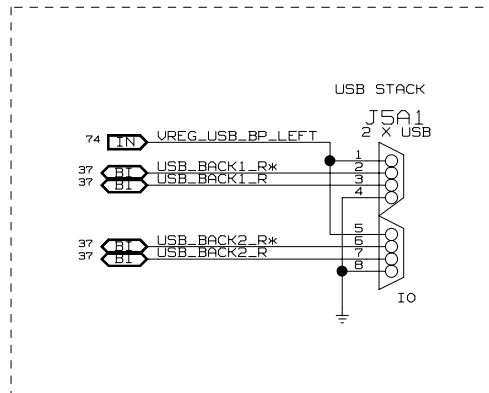
DRAWING

SCHEMATIC TITLE:		
INTEL(R) B65G/B65PE/B65P CHIPSET REFERENCE BOARD		
PAGE TITLE: PCI TERMINATION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		SHEET: 41
LAST REVISED: Tue May 06 11:25:29 2003		



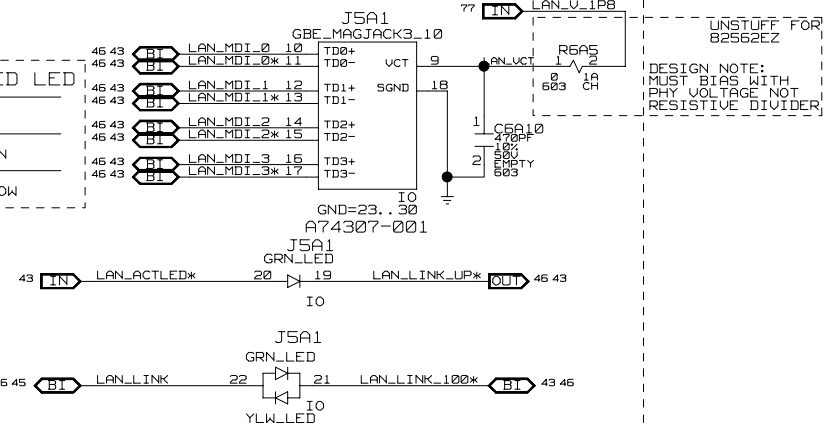


LAN CONNECTOR



BI-COLOR SPEED LED

10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW

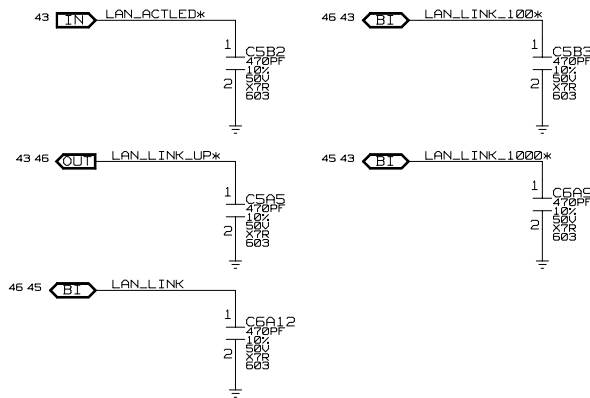


STUFF A74307-001 FOR 82547EI
STUFF A74314-002 FOR 82562EZ

LED DECOUPLING

CAD NOTE:

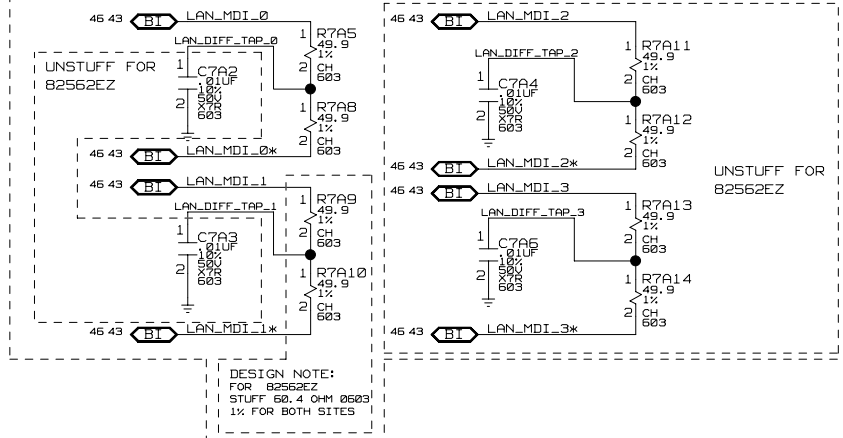
LED CAPS SHOULD BE PLACED NEXT TO CONNECTOR



DIFFERENTIAL PAIR TERMINATIONS

CAD NOTE:

PLACE NEXT TO CONTROLLER



SCHEMATIC TITLE:

INTEL(R) B65G/B65PE/B65P CHIPSET REFERENCE BOARD

PAGE TITLE:

LAN CONNECTOR/DECOUPLING

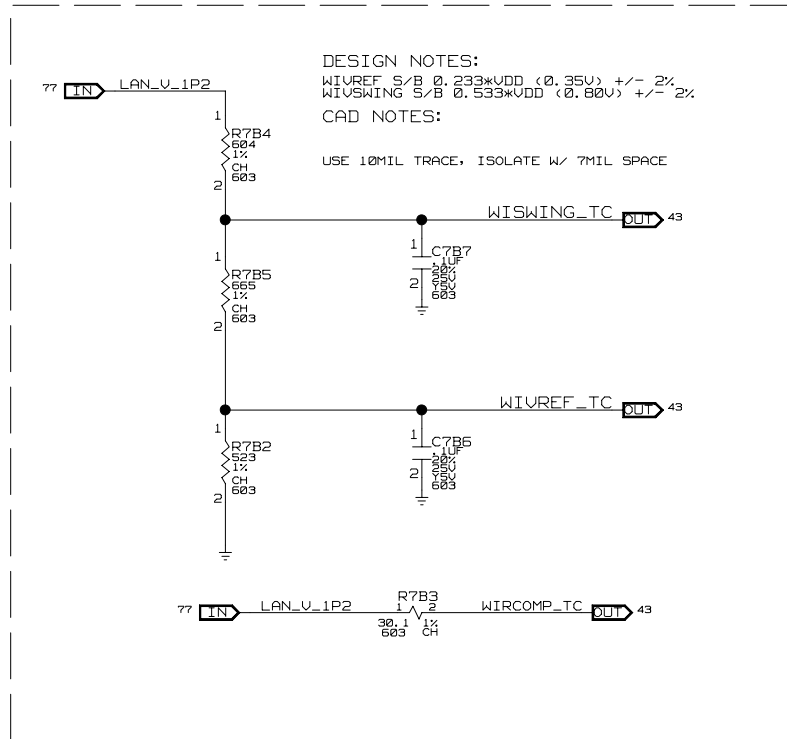
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue May 05 11:25:32 2003

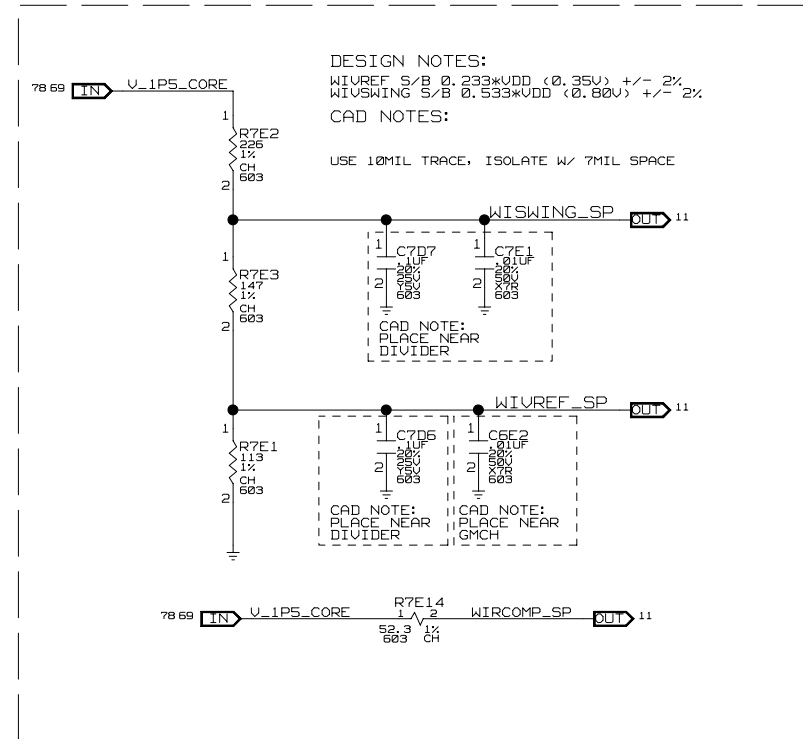
SHEET: 46

DRAWING

LAN CSA INTERFACE REFERENCE

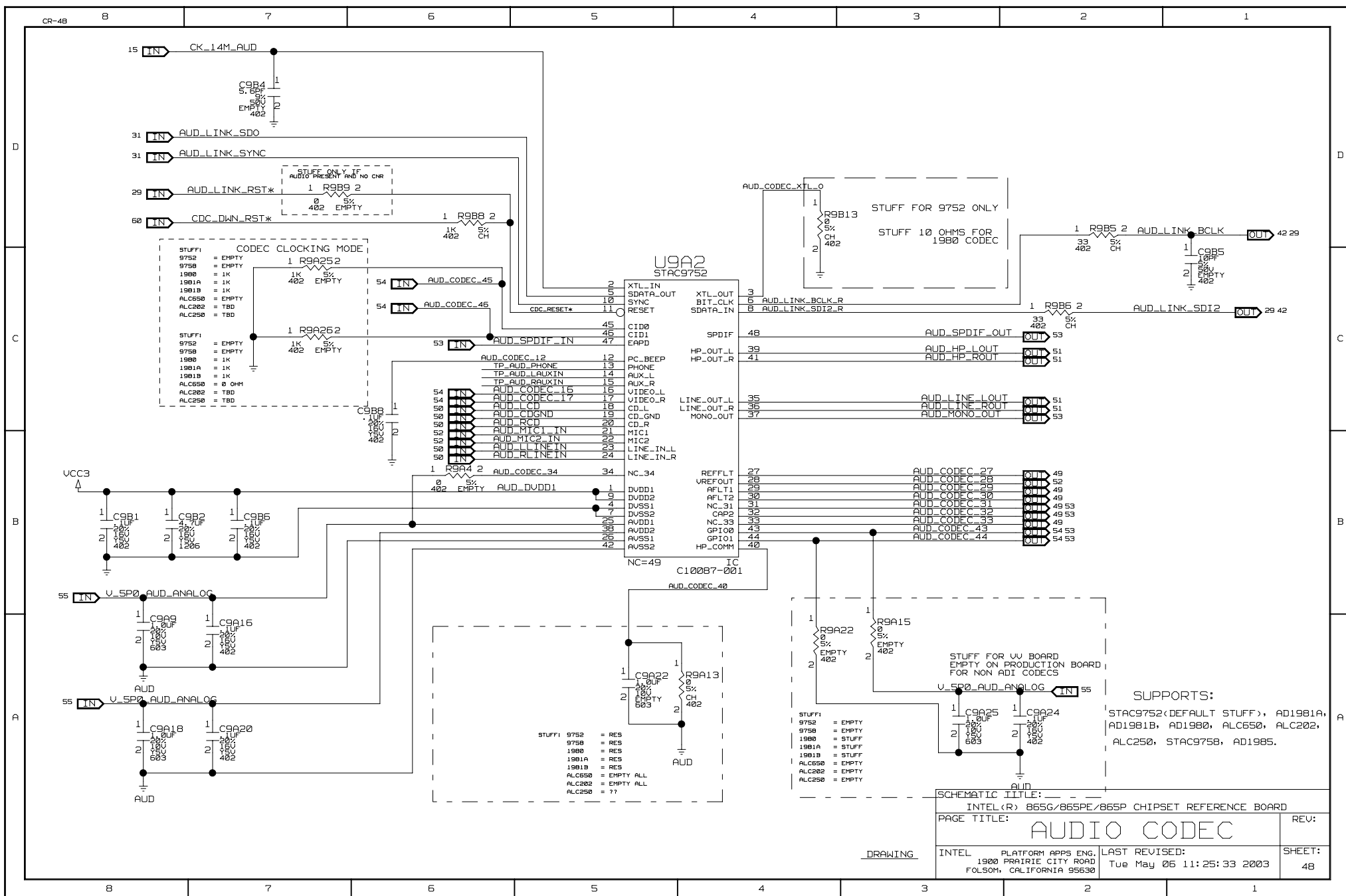


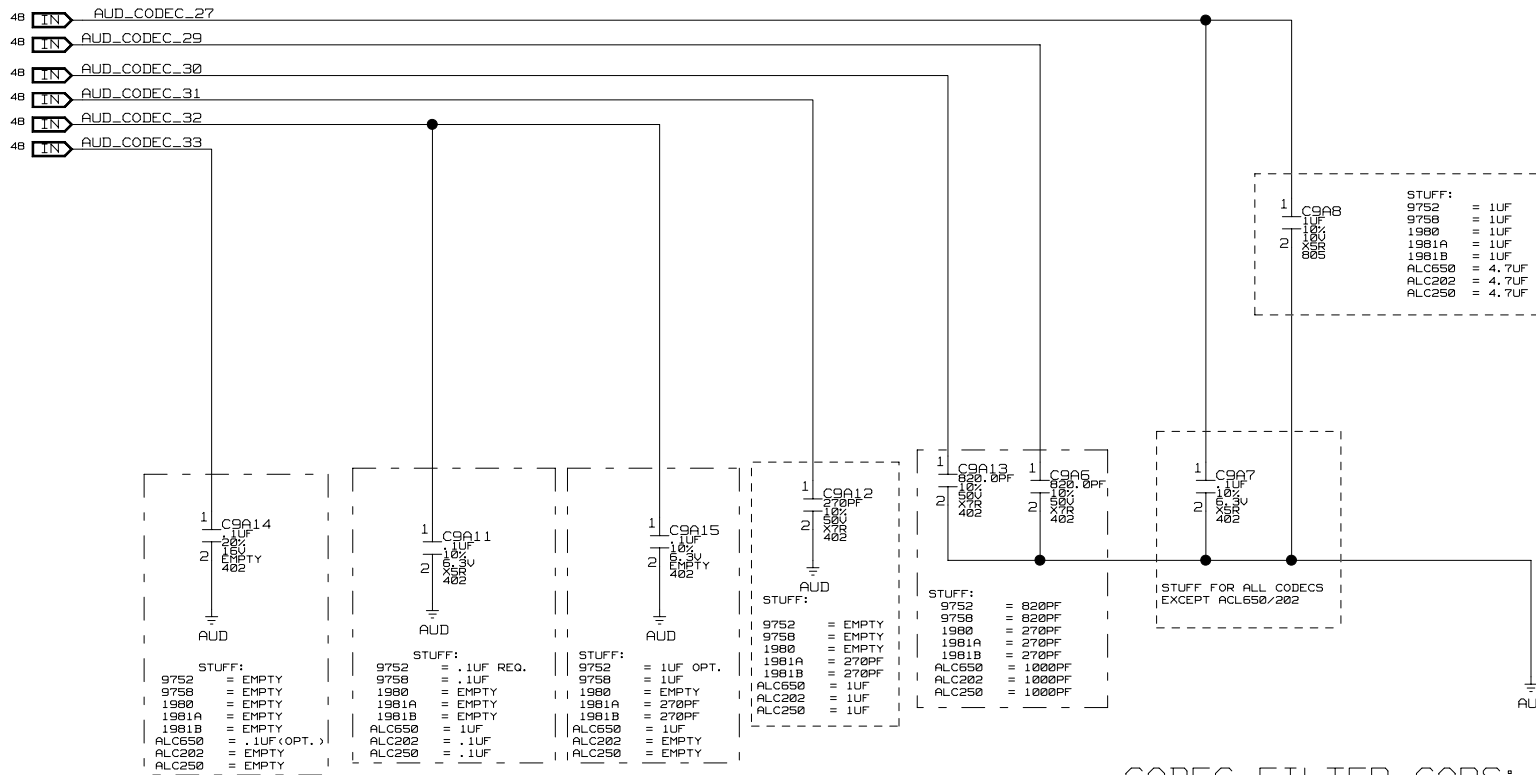
GMCH CSA INTERFACE REFERENCE



DRAWING

SCHEMATIC TITLE:	
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE:	REV:
CSA INTERFACE REFERENCE	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:33 2003
SHEET:	47



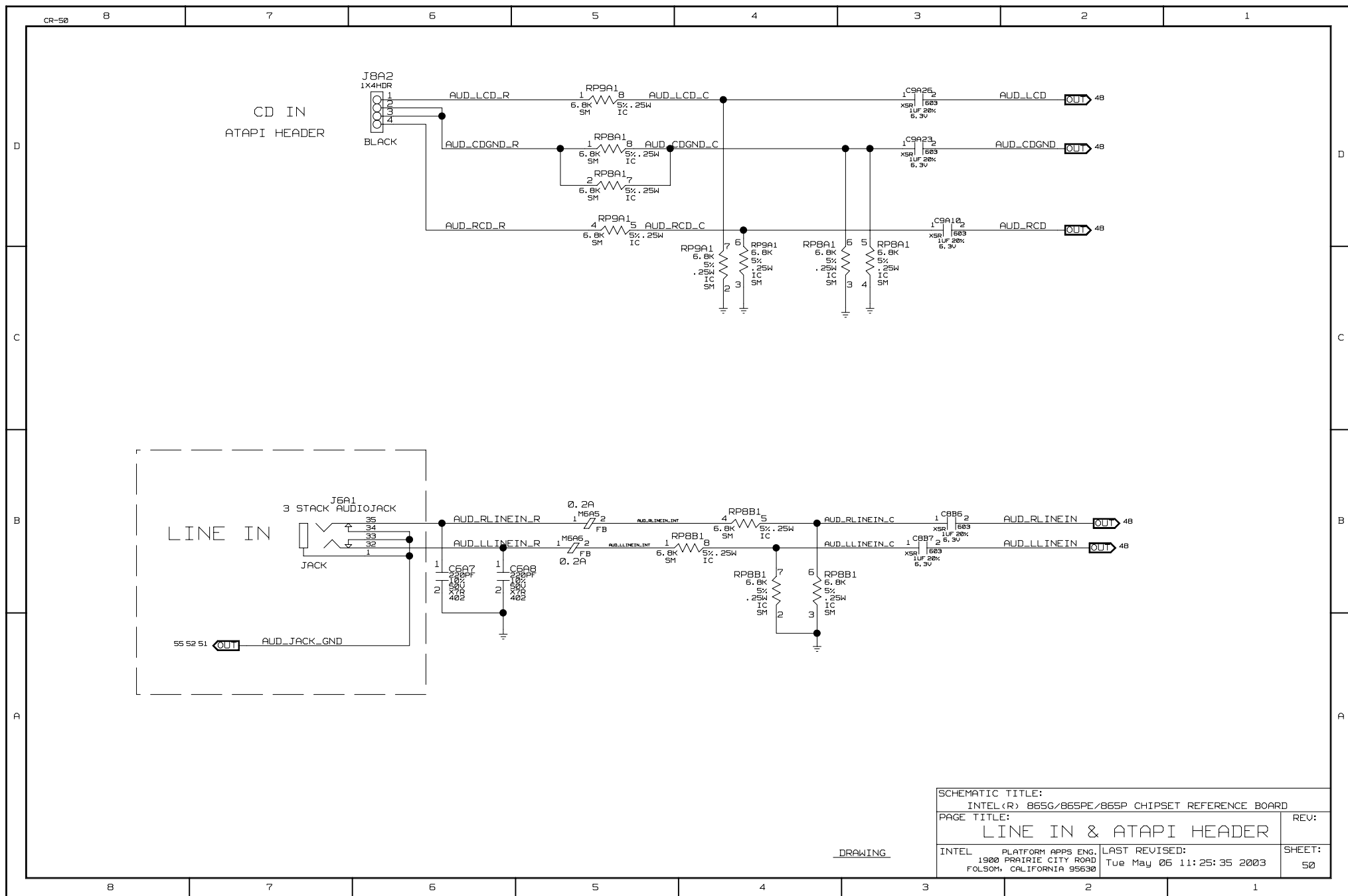


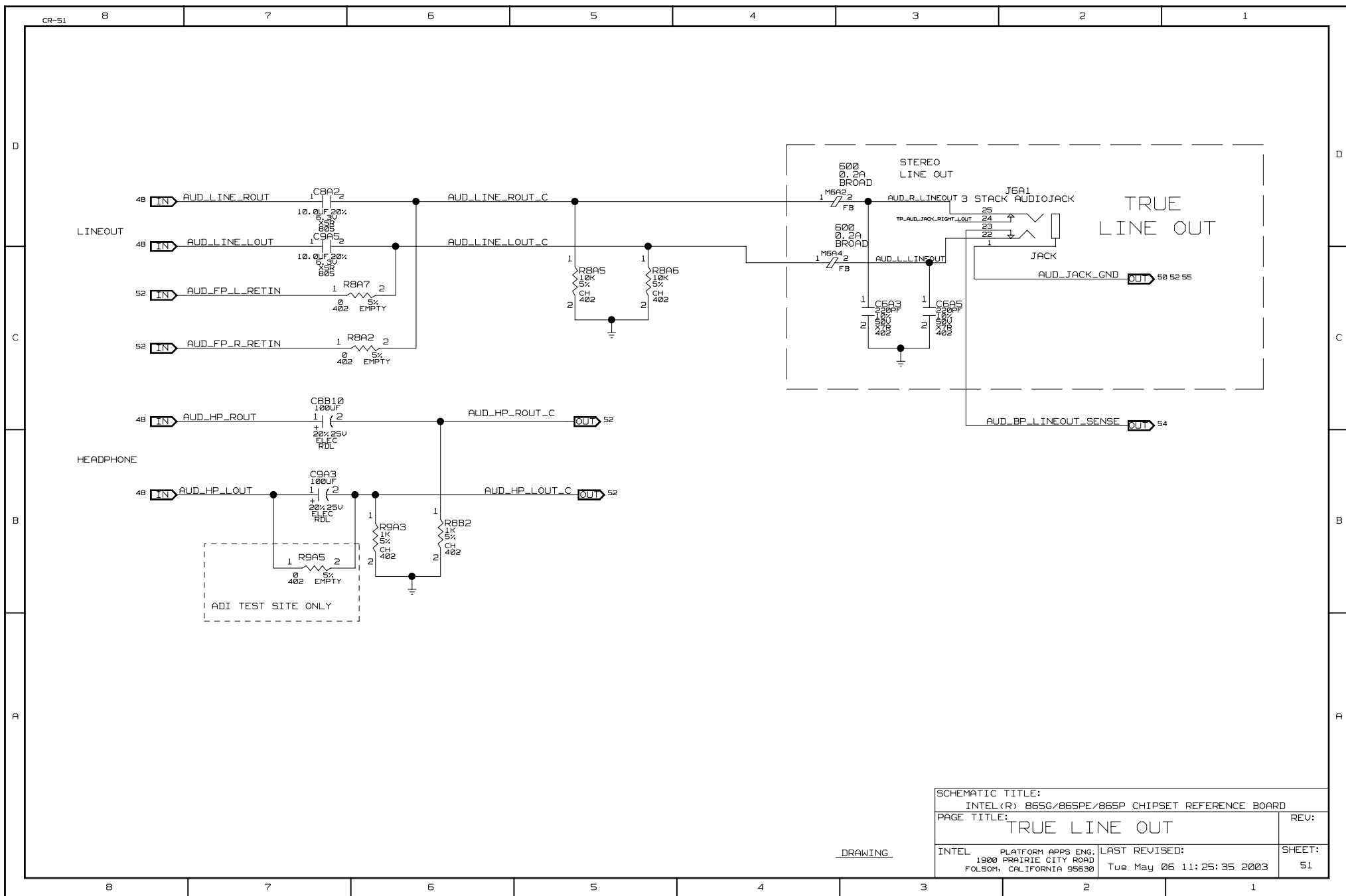
KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC

CODEC FILTER CAPS:
9752, 9758, 1980, 1981A, 1981B,
ALC650, ALC202, ALC250

SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:		REV:
CODEC FILTERING CAPS		
INTEL	PLATFORM APPS ENG.	LAST REVISED:
1900 PRAIRIE CITY ROAD	FOLSOM, CALIFORNIA 95630	Tue May 06 11:25:34 2003
SHEET:		49

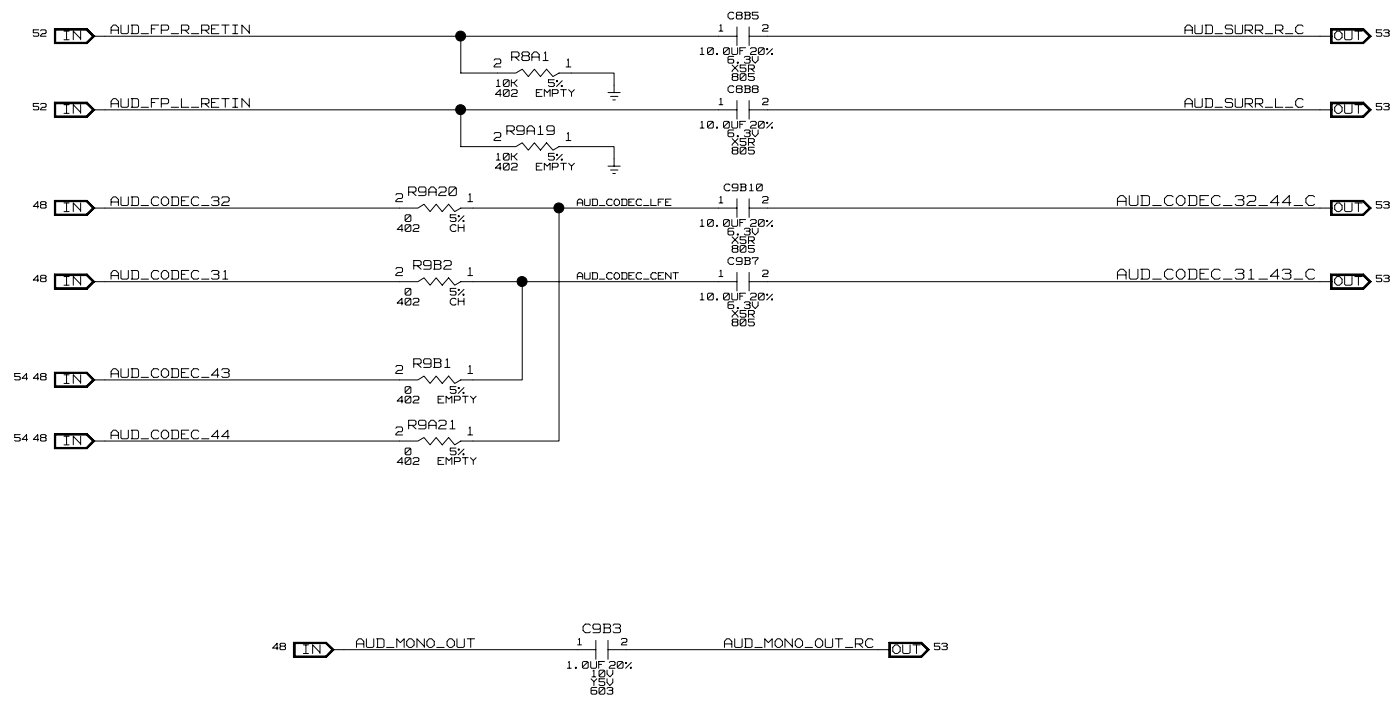
DRAWING



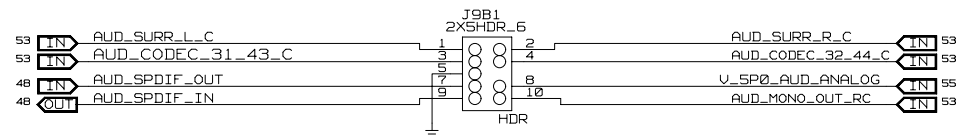


SCHEMATIC TITLE:	
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE:	REV:
TRUE LINE OUT	
INTEL	SHEET:
PLATFORM APPS ENG.	LAST REVISED:
1900 PRAIRIE CITY ROAD	Tue May 06 11:25:35 2003
FOLSOM, CALIFORNIA 95630	51

DRAWING



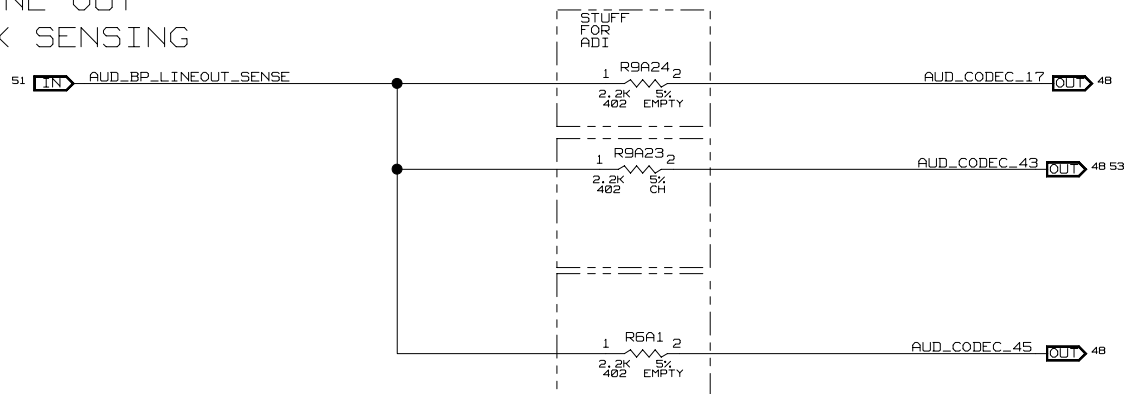
6 CHANNEL AUDIO HEADER



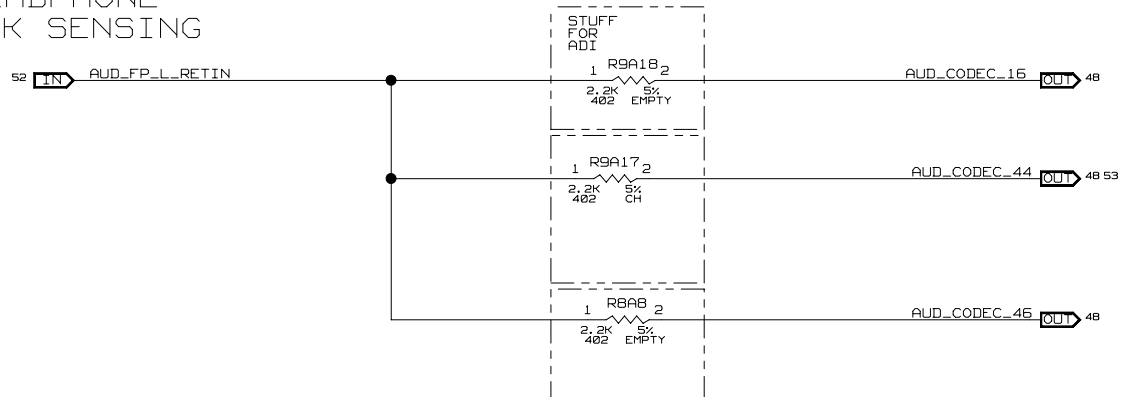
SCHEMATIC TITLE:	
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE:	REV:
AUDIO OUTPUTS/6 CHANNEL HEADER	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:37 2003
	SHEET: 53

DRAWING

LINE OUT JACK SENSING



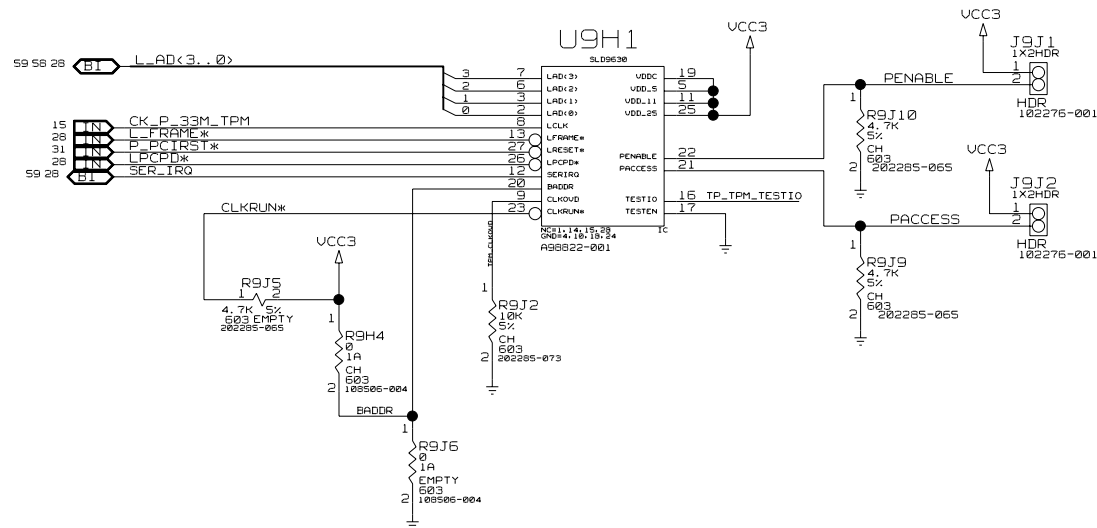
HEADPHONE JACK SENSING



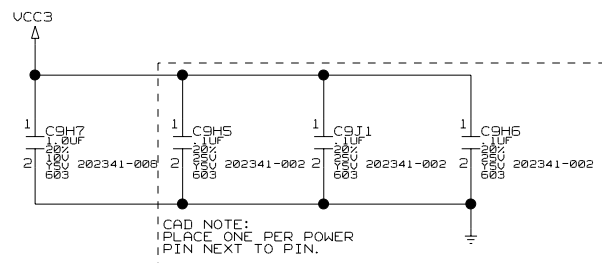
DRAWING

SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:		REV:
AUDIO JACK SENSING		
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:37 2003
		SHEET: 54

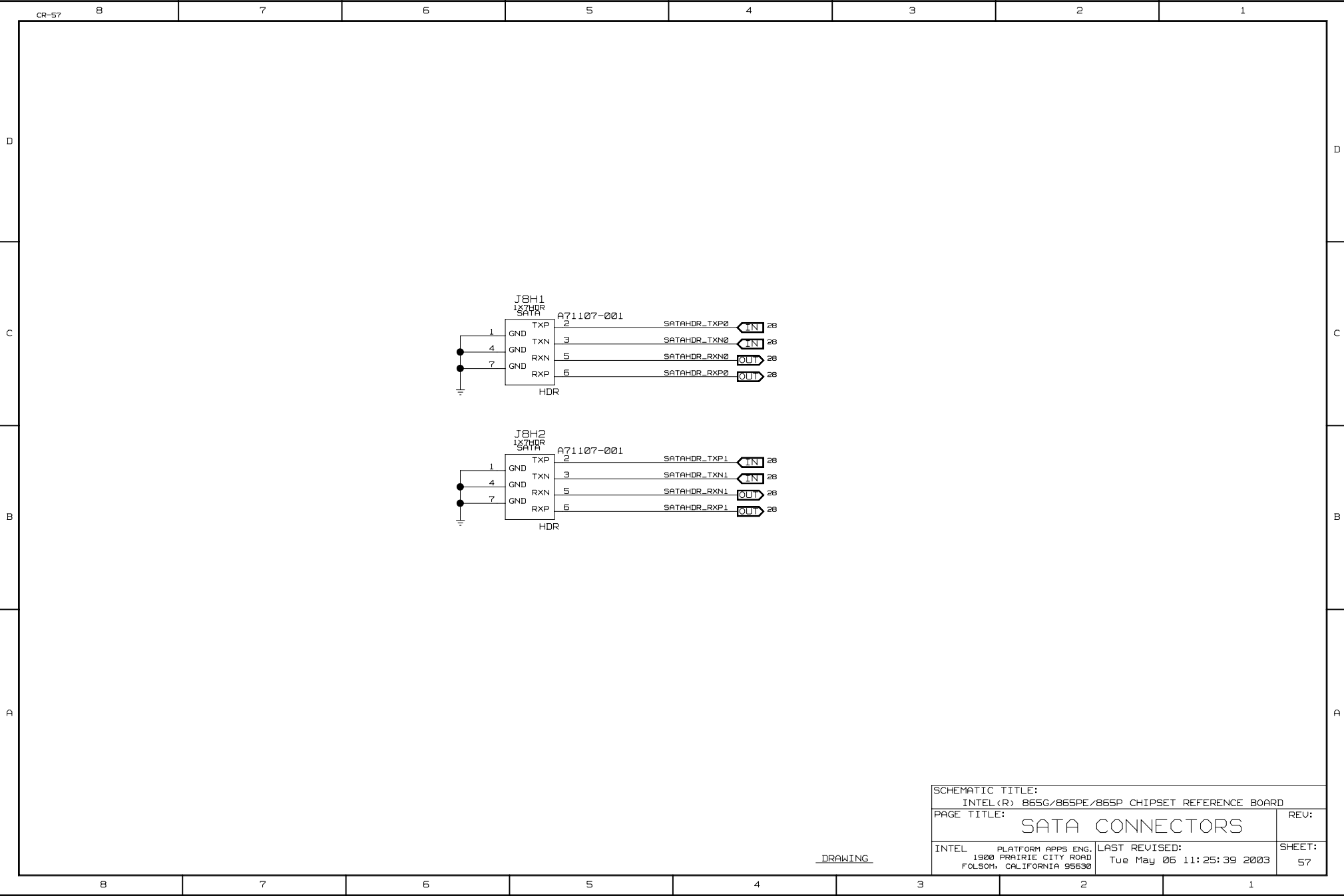
SECURITY: TPM (TRUSTED PLATFORM MODULE)

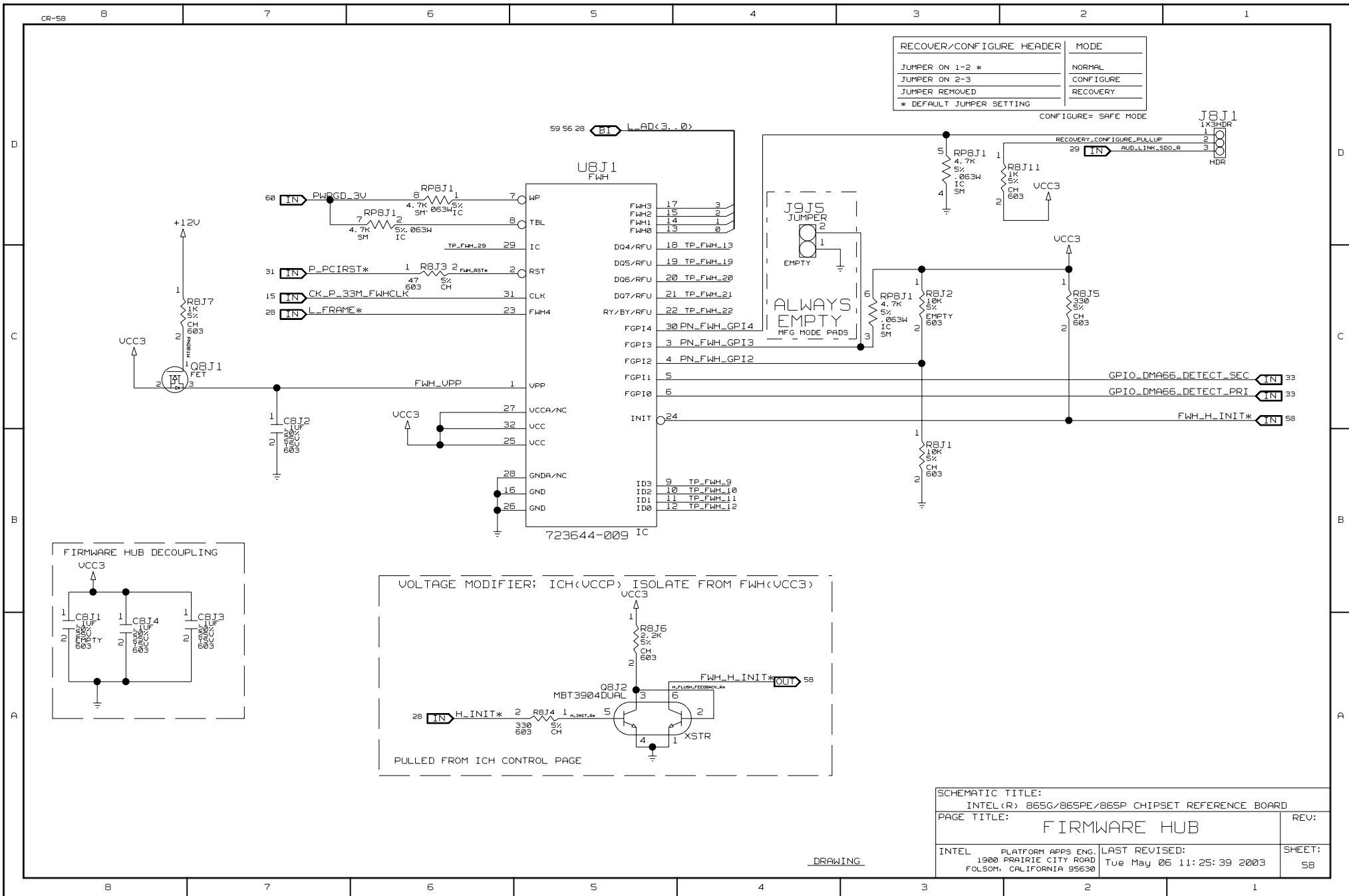


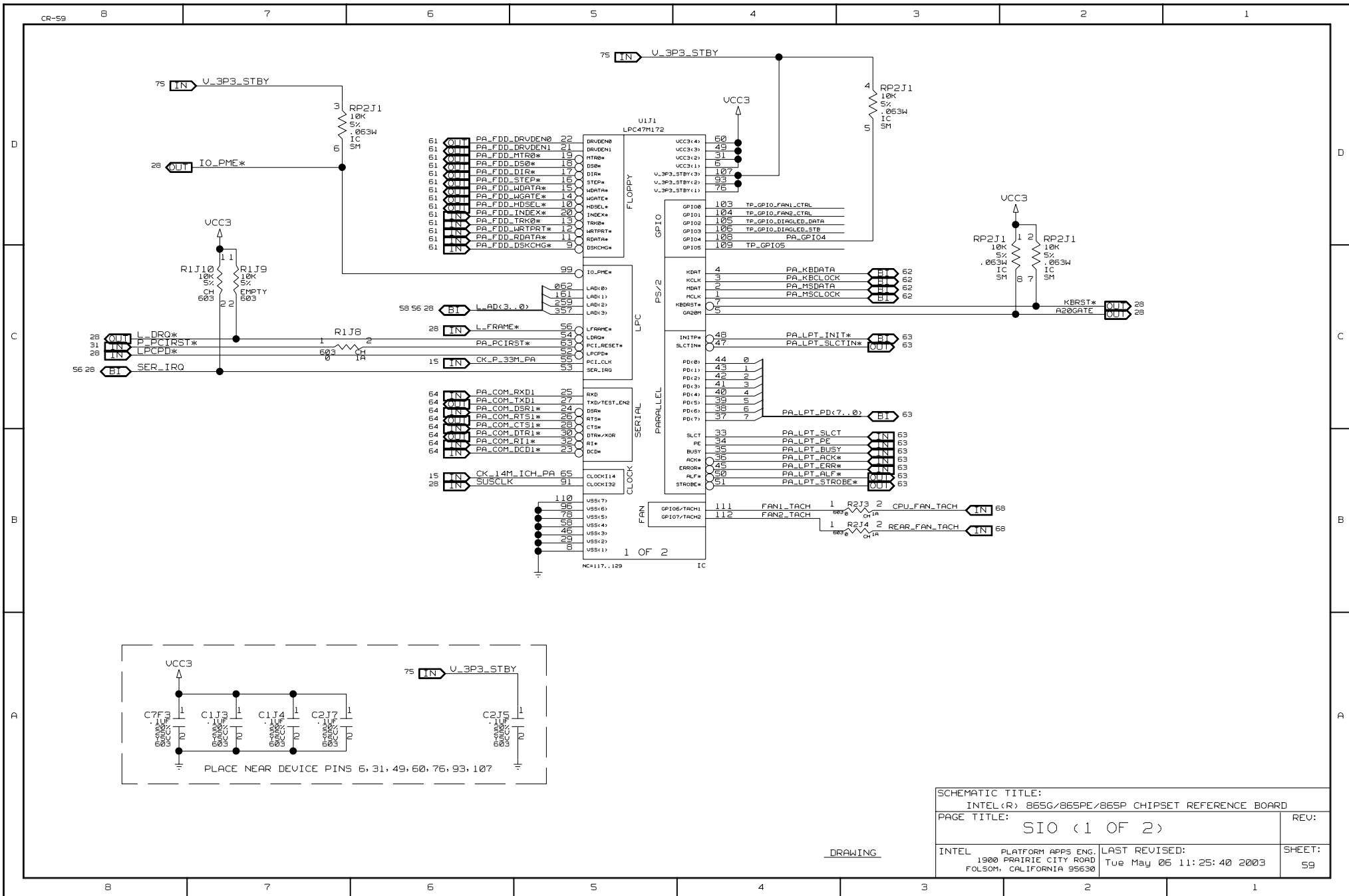
CAD NOTE:
CK_P_33M_TPM SHOULD
HAVE 20MIL SPACING
P_PCI_RST* SHOULD
HAVE 20 MIL SPACING
LAD(3..0) HAS 5 MIL
SPACING BETWEEN OTHER LAD
SIGNALS, BUT 10 MILS TO ALL
OTHER SIGNALS.

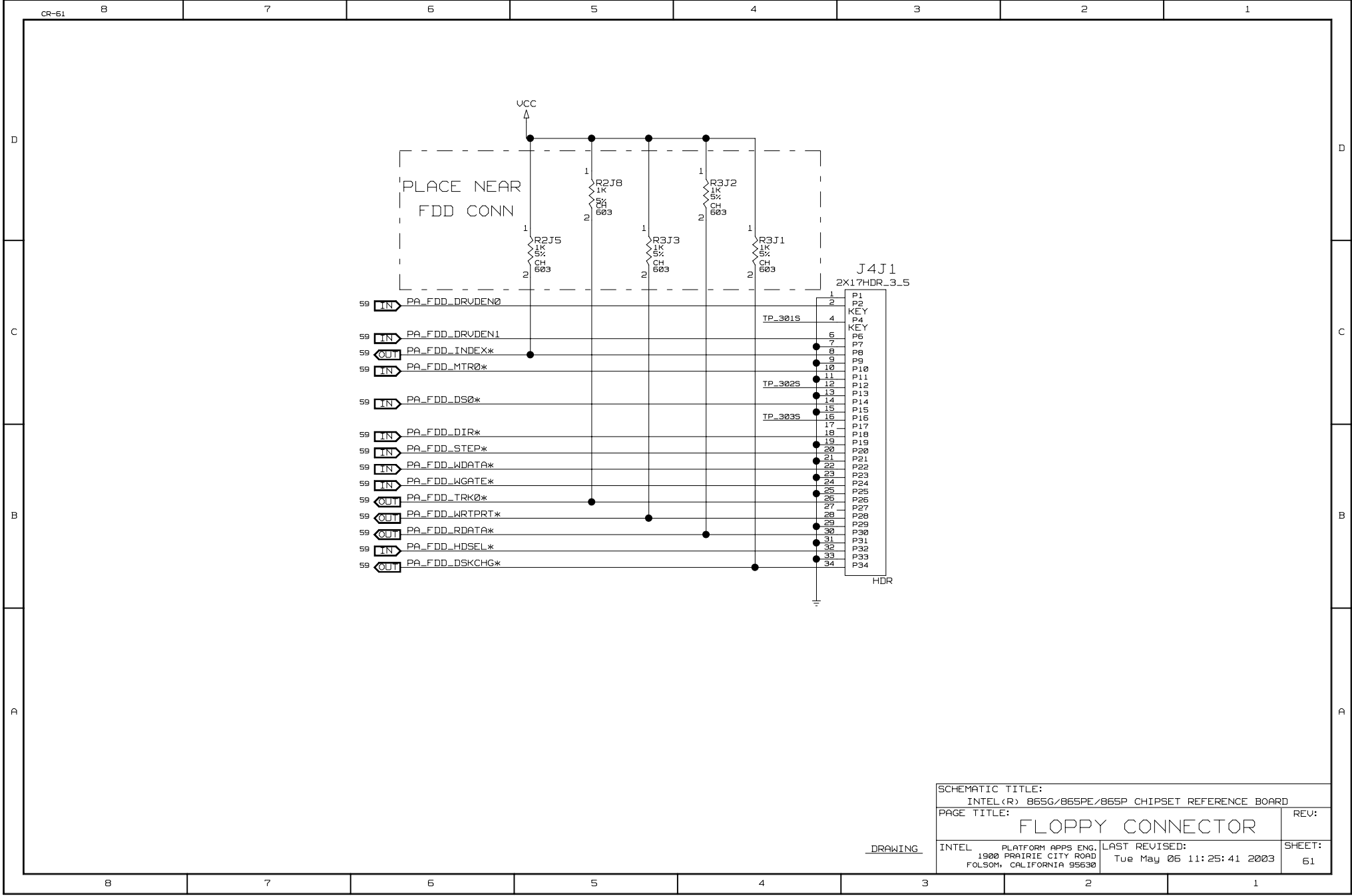


SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	TPM (TRUSTED PLATFORM MODULE)	REV:
INTEL	PLATFORM APPS ENG.	LAST REVISED:
1900 PRAIRIE CITY ROAD	FOLSOM, CALIFORNIA 95630	Tue May 06 11:25:38 2003
DRAWING		SHEET: 56

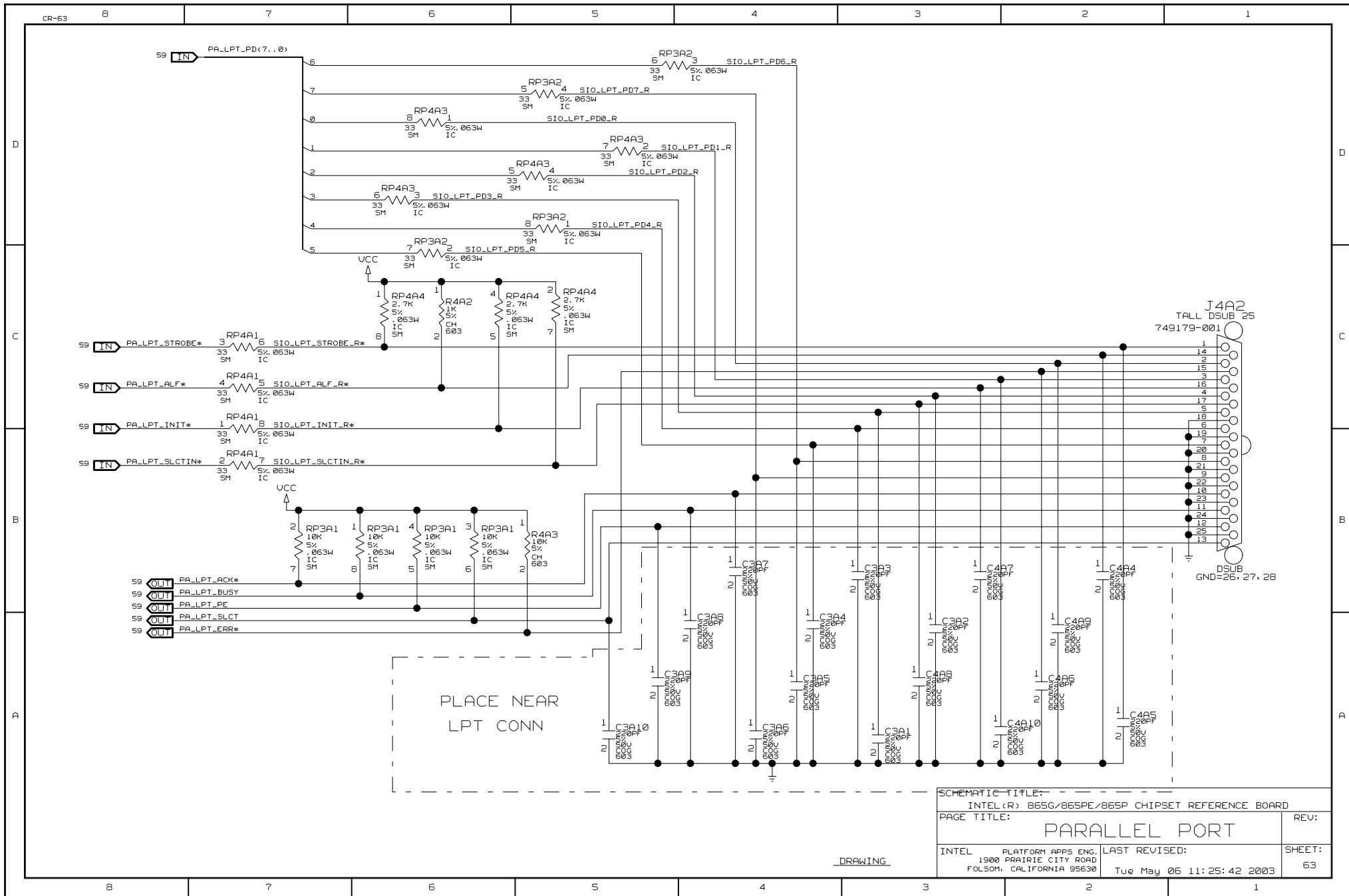






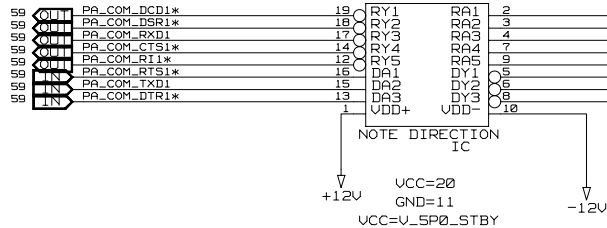


SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	FLOPPY CONNECTOR	REV:
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 05 11:25:41 2003
DRAWING		SHEET: 61



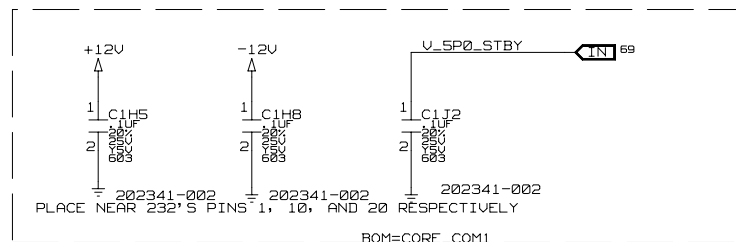
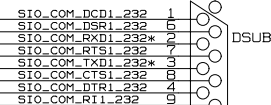
DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

U1H1
GD75232S 621111-103



SERIAL PORT A
J2A1

749218-001
2 ROW 10

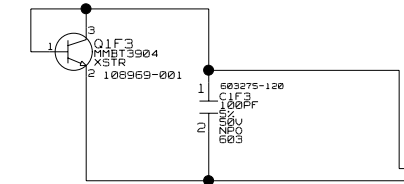


SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	SERIAL PORT	REV:
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 05 11:25:43 2003	SHEET: 64

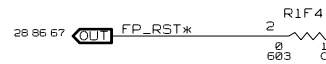
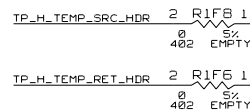
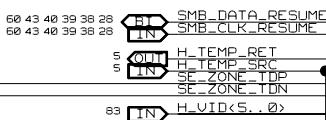
DRAWING

CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS

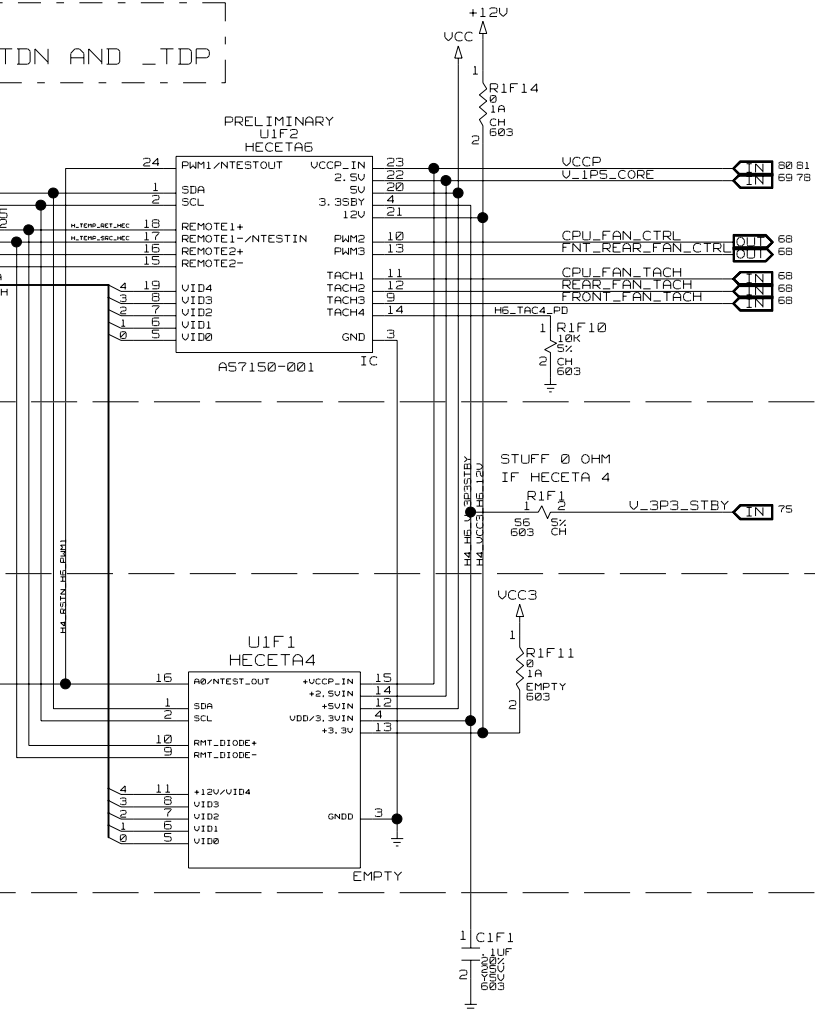
CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP



ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4

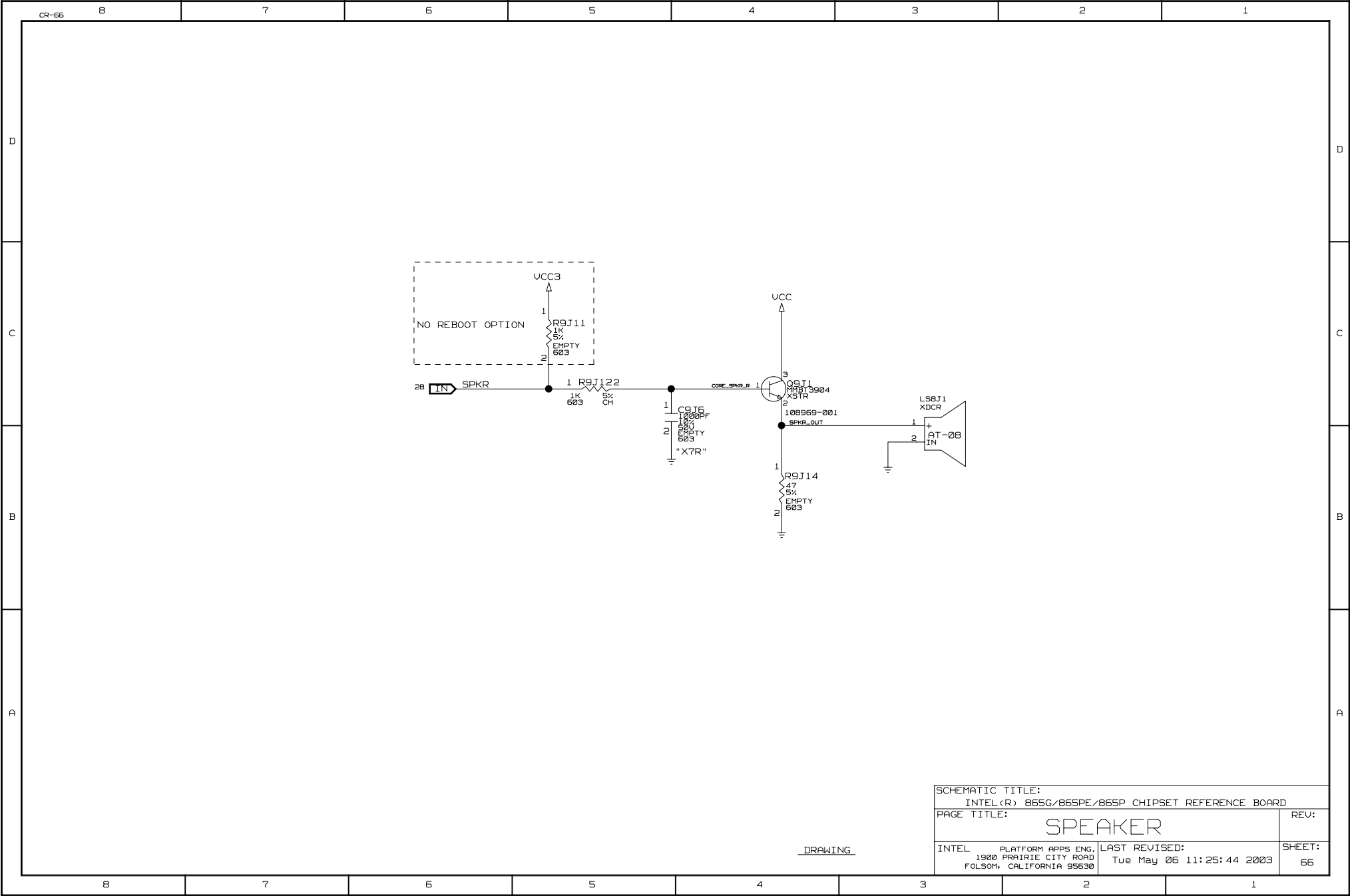


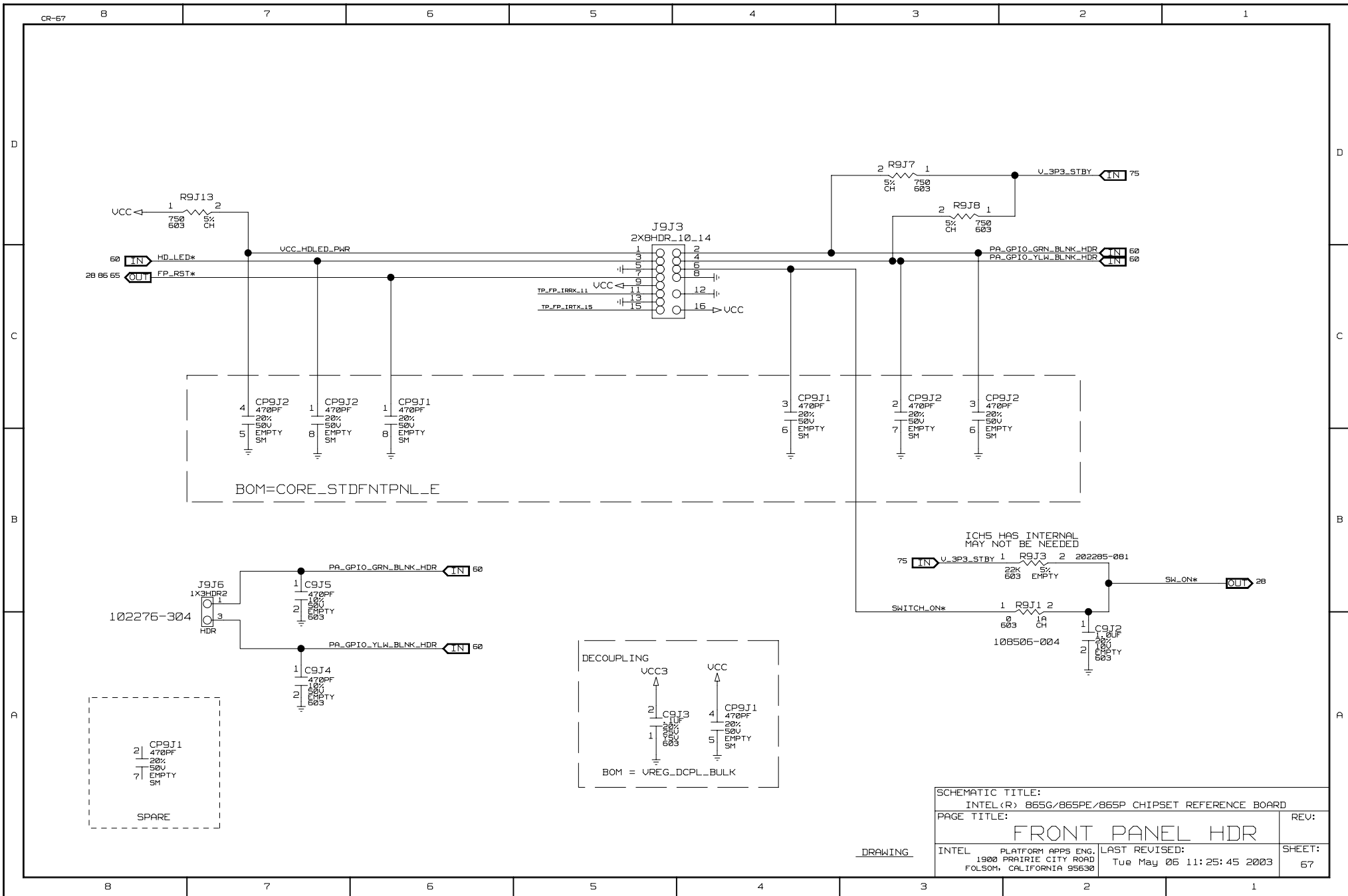
ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6

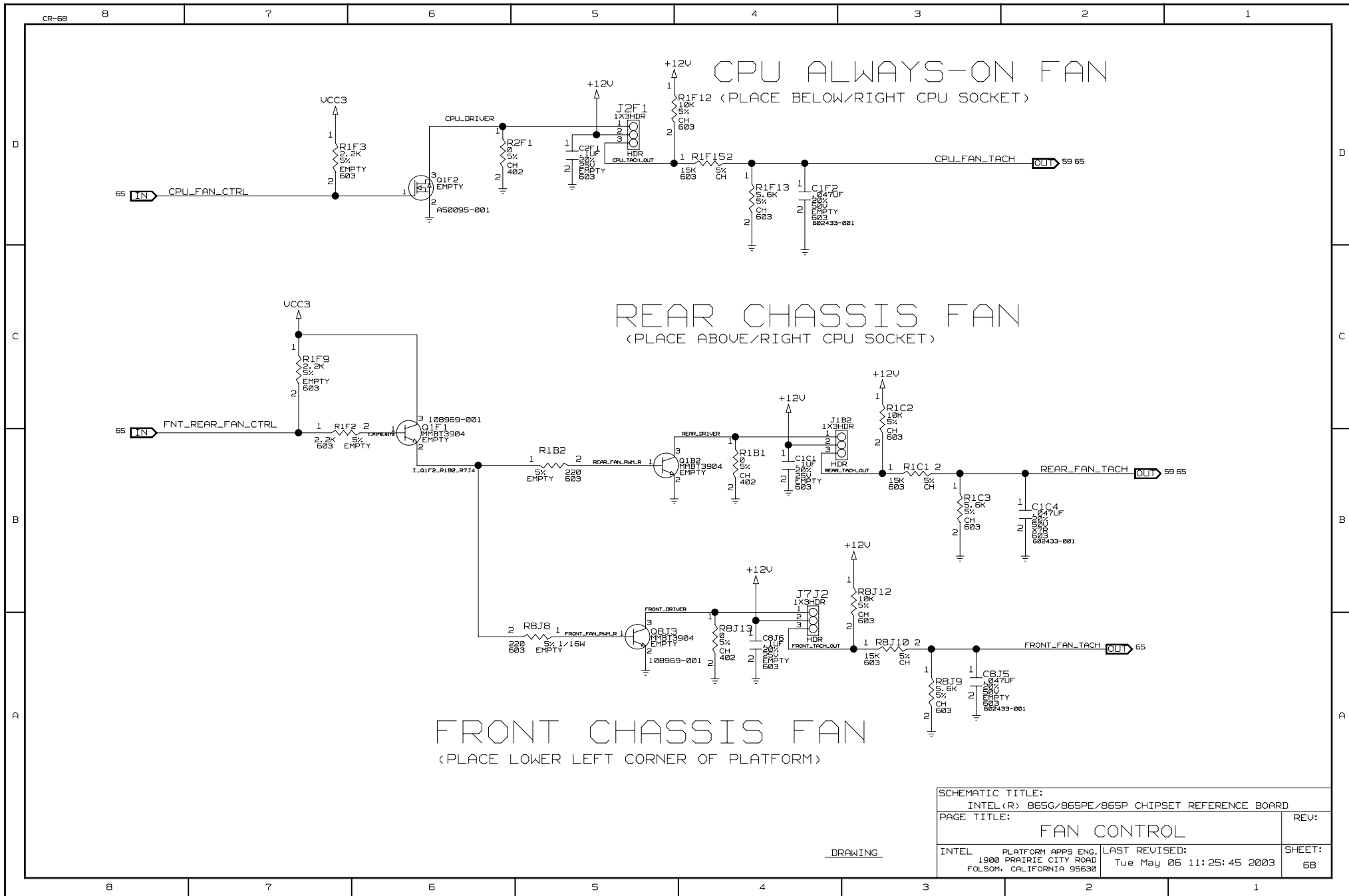


SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	HECETA	REV:
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:44 2003
		SHEET: 65

DRAWING

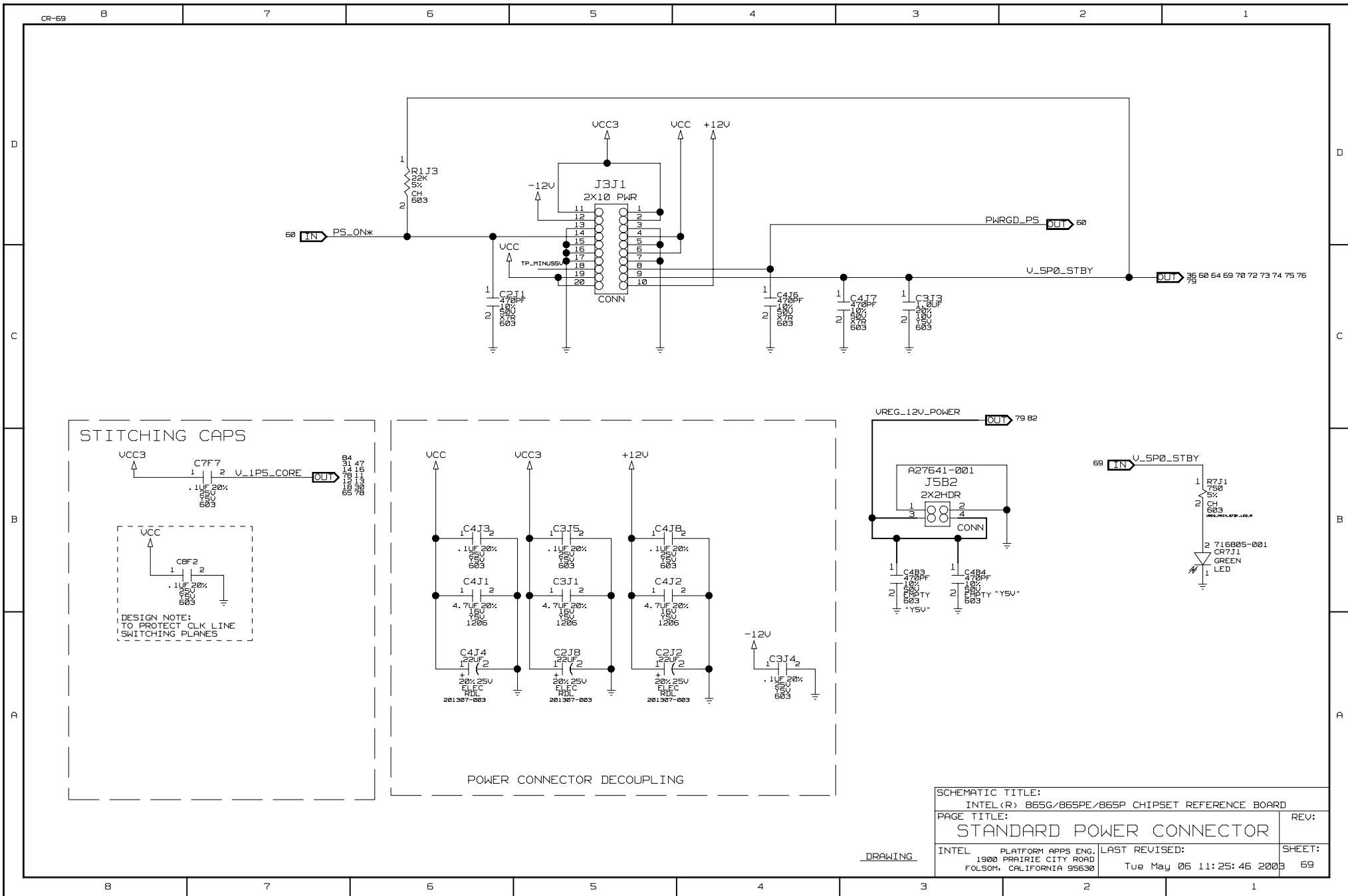






SCHEMATIC TITLE:	
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE:	REV:
FAN CONTROL	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 05 11:25:45 2003
	SHEET: 68

DRAWING



CR-70

8

7

6

5

4

3

2

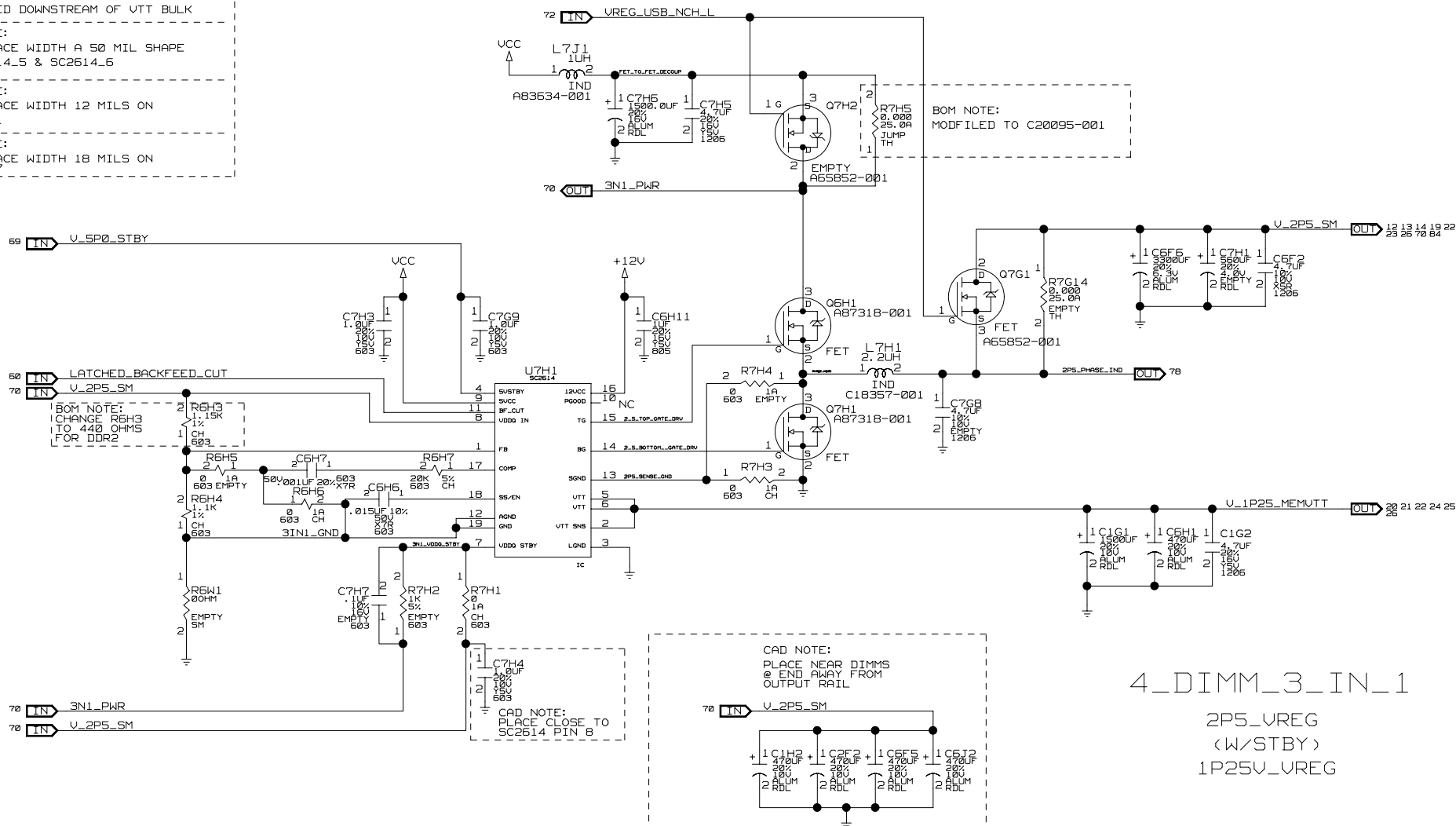
1

CAD NOTE:
MAKE TRACE WIDTH 12 MILS
ON SC2614_2
CONNECTED DOWNSTREAM OF UTT BULK

CAD NOTE:
MAKE TRACE WIDTH A 50 MIL SHAPE
ON SC2614_5 & SC2614_6

CAD NOTE:
MAKE TRACE WIDTH 12 MILS ON
SC2614_1

CAD NOTE:
MAKE TRACE WIDTH 18 MILS ON
SC2614_7



SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:		REV:
2P5_VREG AND 1P25V_VREG		
INTEL	PLATFORM APPS ENG	LAST REVISED:
1900 PRAIRIE CITY ROAD		Tue May 05 11:25:47 2003
FOLSOM, CALIFORNIA 95630		SHEET:
		70

DRAWING

8

7

6

5

4

3

2

1

CR-71

B

7

6

5

4

3

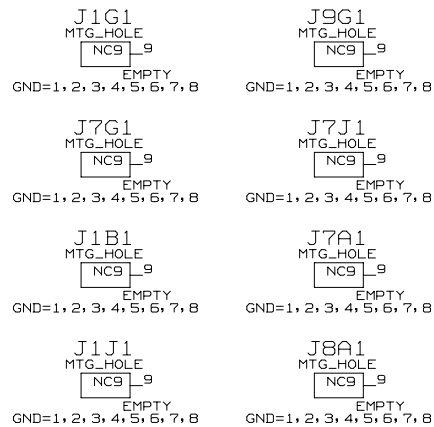
2

1

D

D

PB MOUNTING HOLES



C

C

B

B

A

A

DRAWING

SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	PB MOUNTING HOLES	REV:
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:47 2003
		SHEET: 71

B

7

6

5

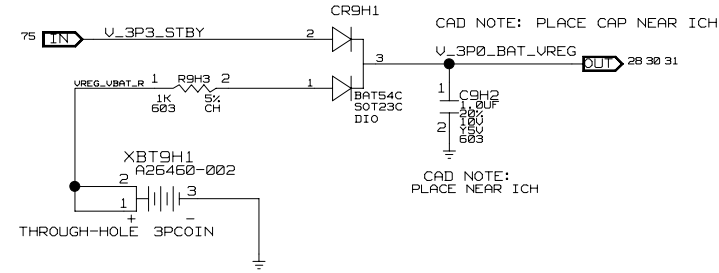
4

3

2

1

BATTERY



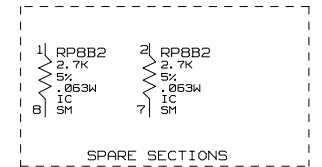
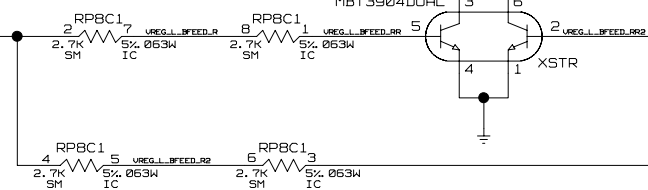
CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

NOTES:

USB/PS2WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF

BOM=VREG
ROOM = VREG UNLESS SPECIFIED

60 IN LATCHED_BACKFEED_CUT

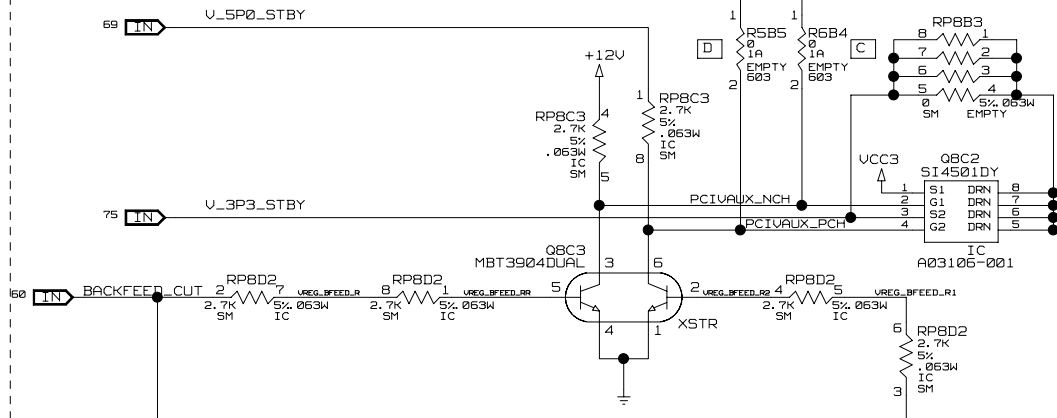


74 73 36 72 UREG_USB_NCH

74 73 36 72 UREG_USB_PCH

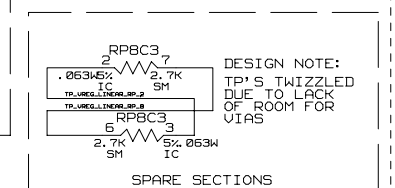
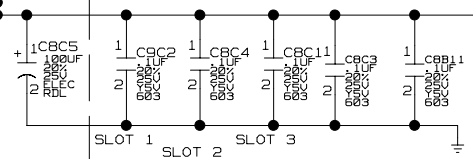
69 IN U_5P0_STBY

75 IN U_3P3_STBY



CAD NOTE: PLACE ONE AT EACH PCI SLOT

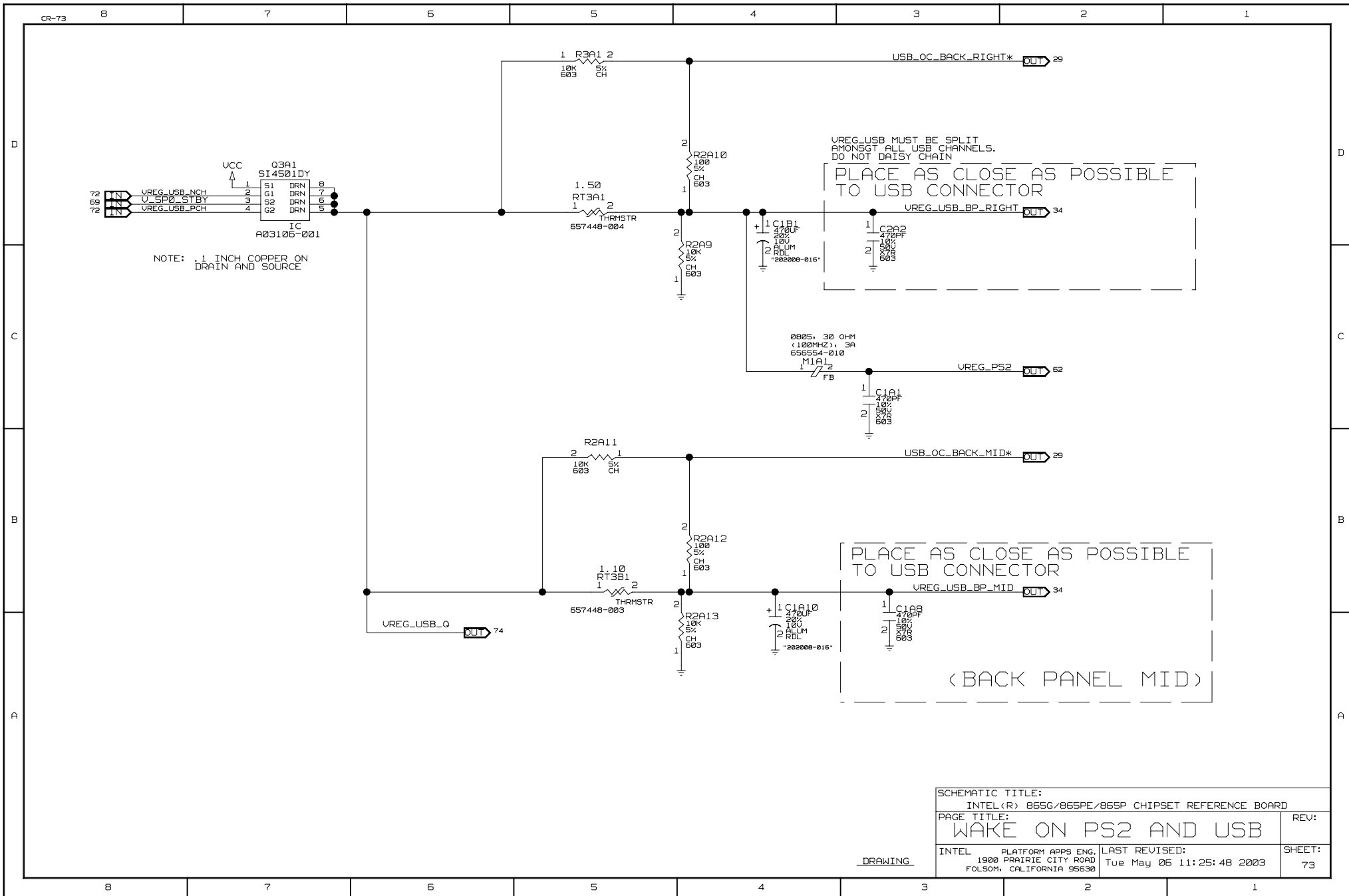
U_3P3_PCIVAU OUT 15 38 39 40 42 43 44 45 77

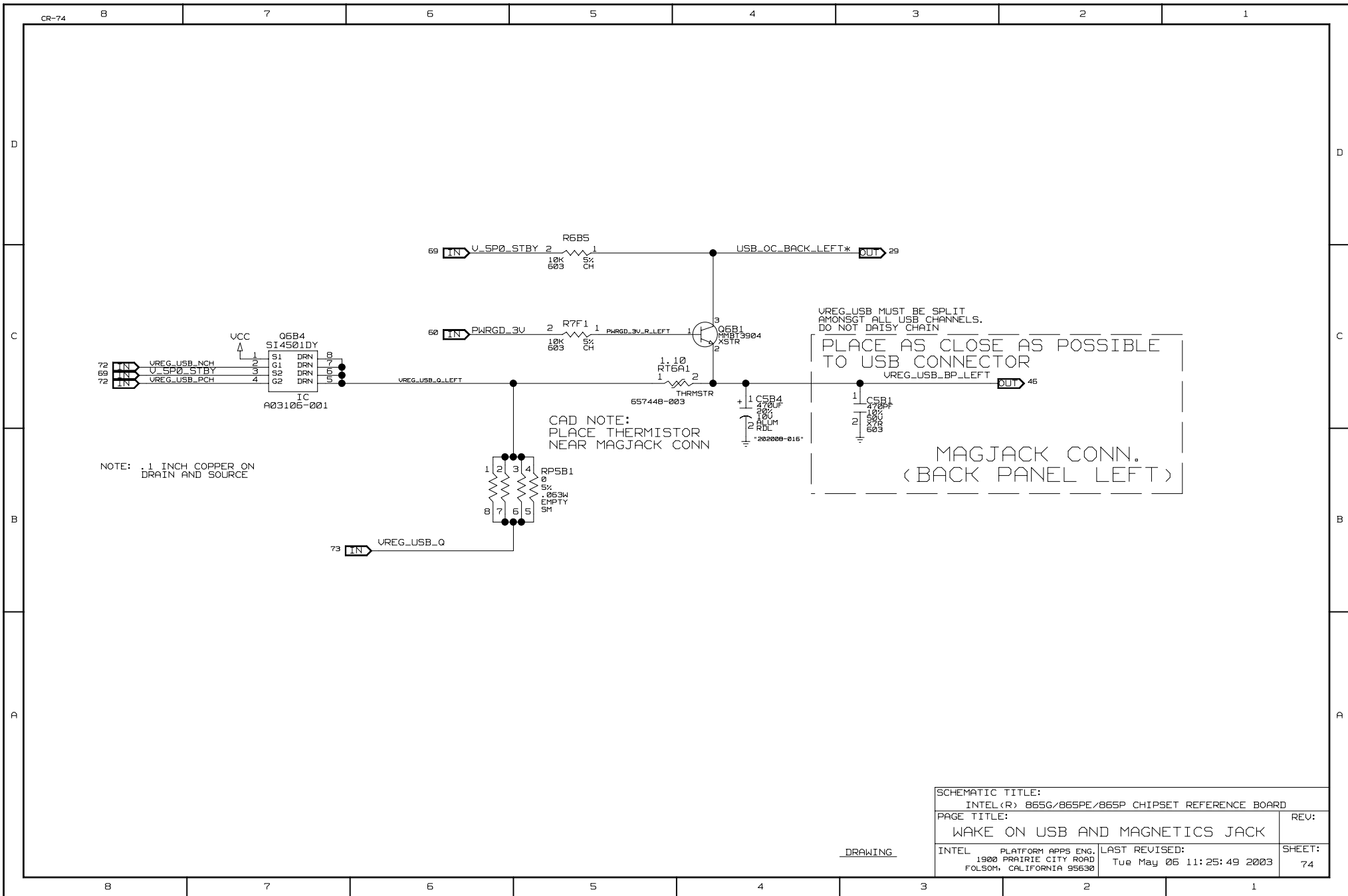


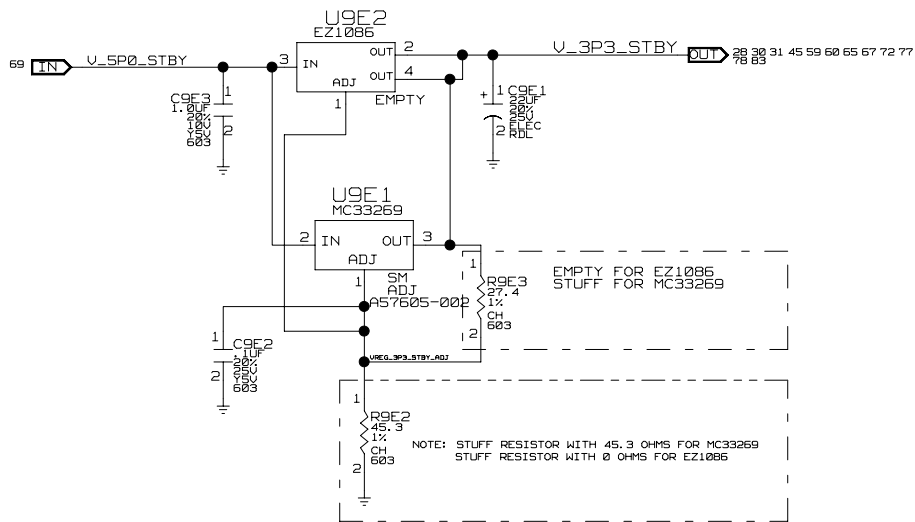
DESIGN NOTE:
TP'S TWIZZLED
DUE TO LACK
OF ROOM FOR
VIAS

PCI VAUX

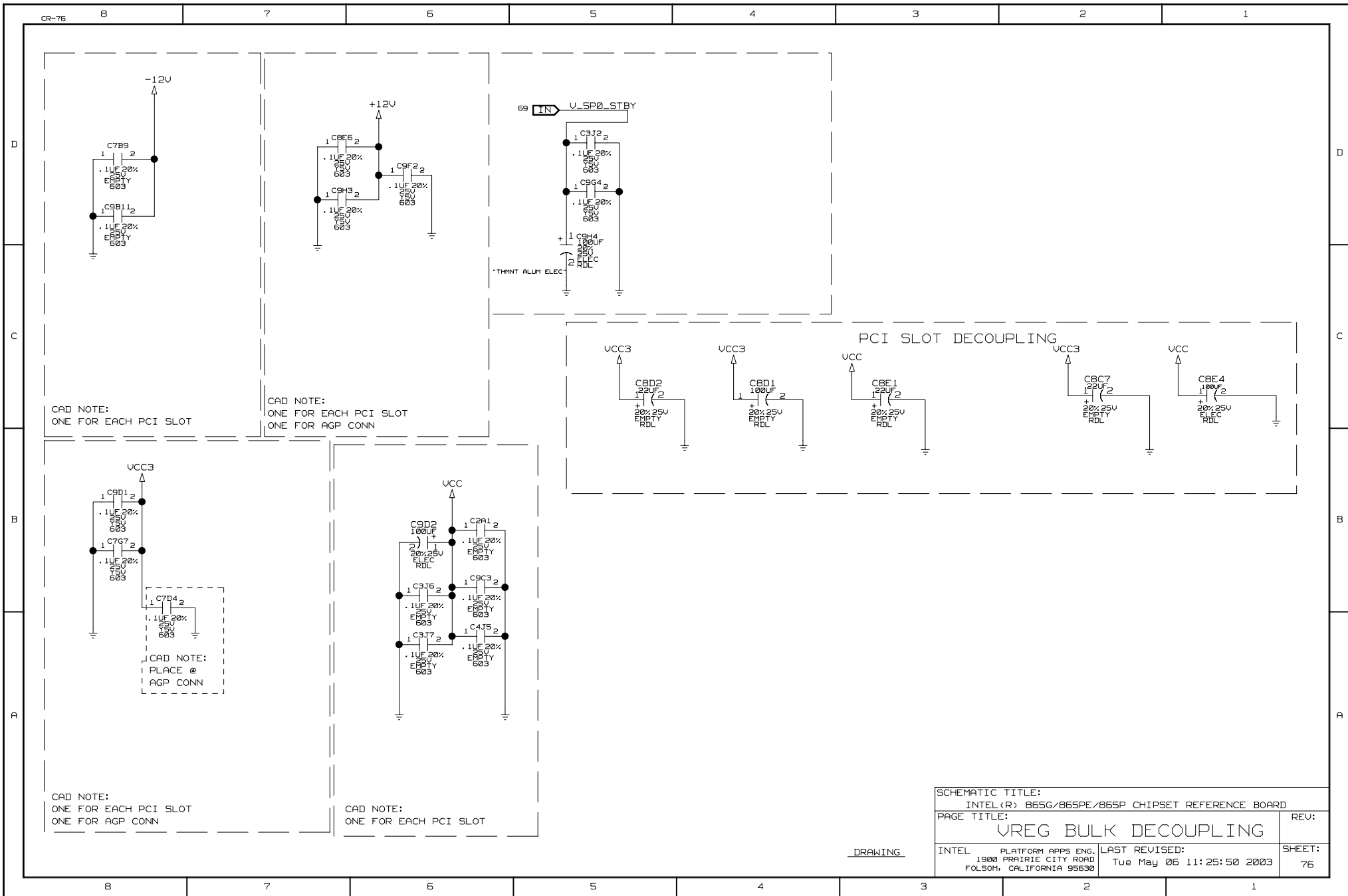
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: WAKE ON PS2 & USB (BACK PANEL RIGHT)	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	REV: LAST REVISED: Tue May 06 11:25:48 2003
DRAWING	SHEET: 72

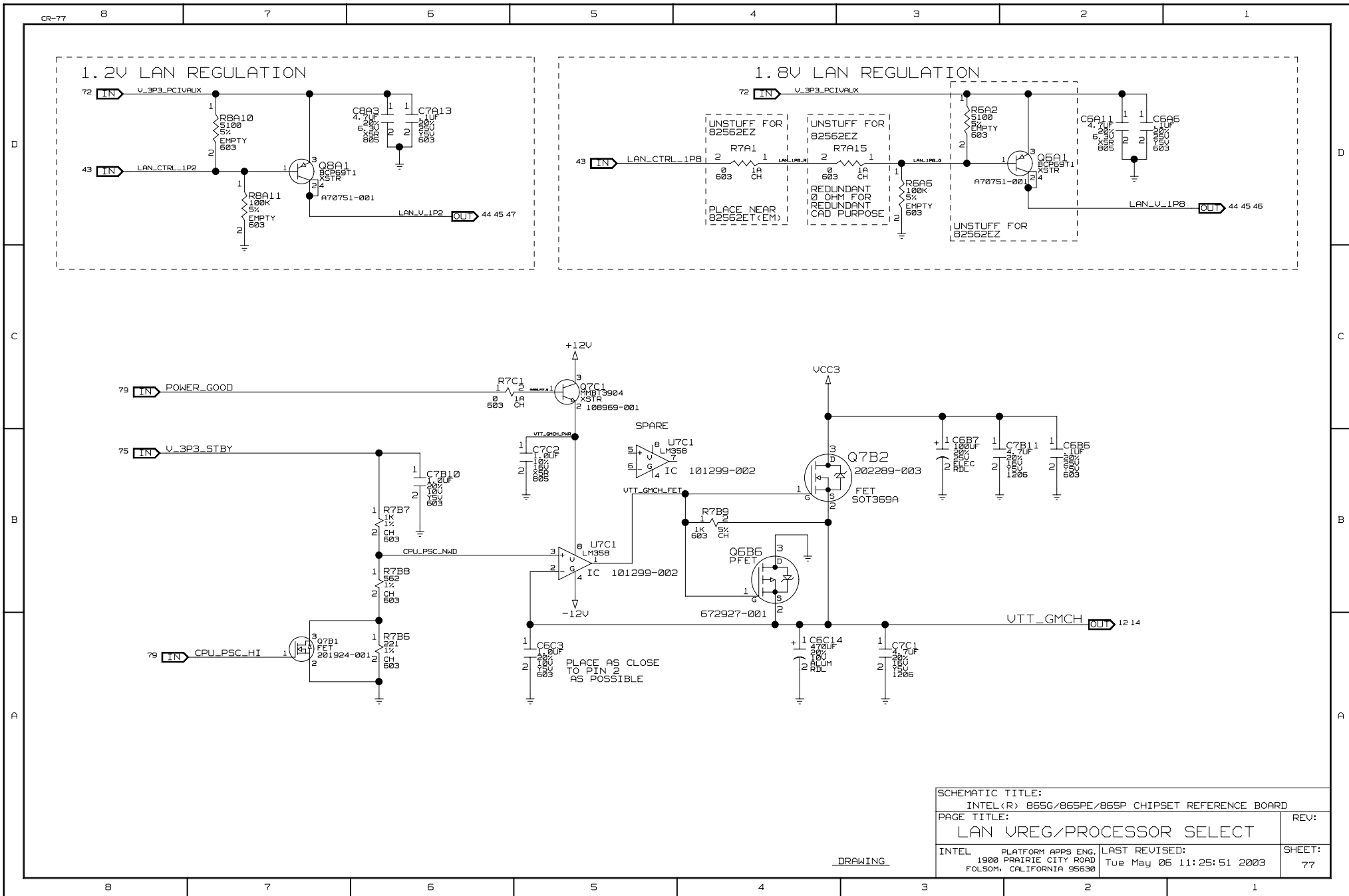


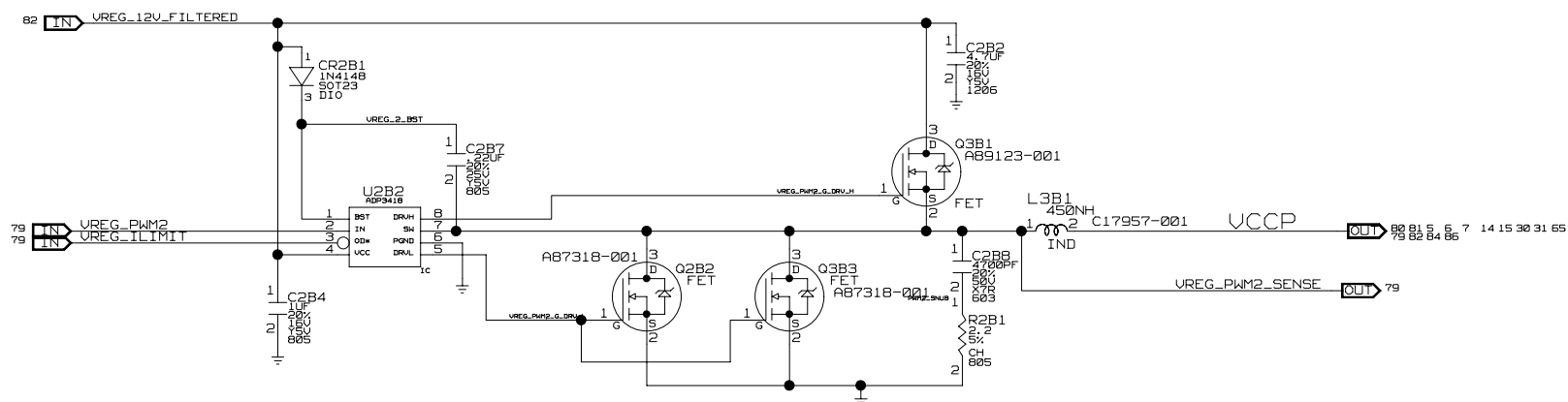
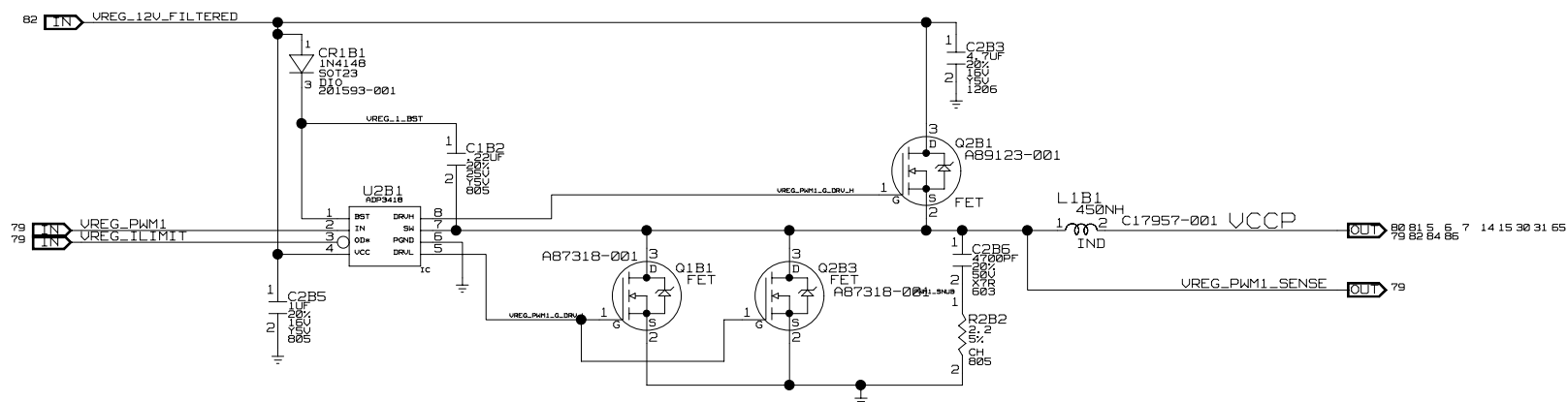




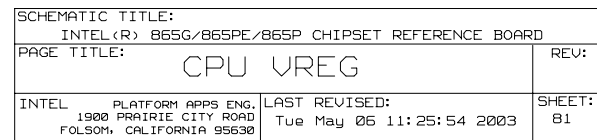
SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:		REV:
3.3V STANDBY & 1.7V DAC		
INTEL	PLATFORM APPS ENG.	LAST REVISED:
1900 PRAIRIE CITY ROAD	FOLSOM, CALIFORNIA 95630	Tue May 06 11:25:50 2003
DRAWING		SHEET:
		75

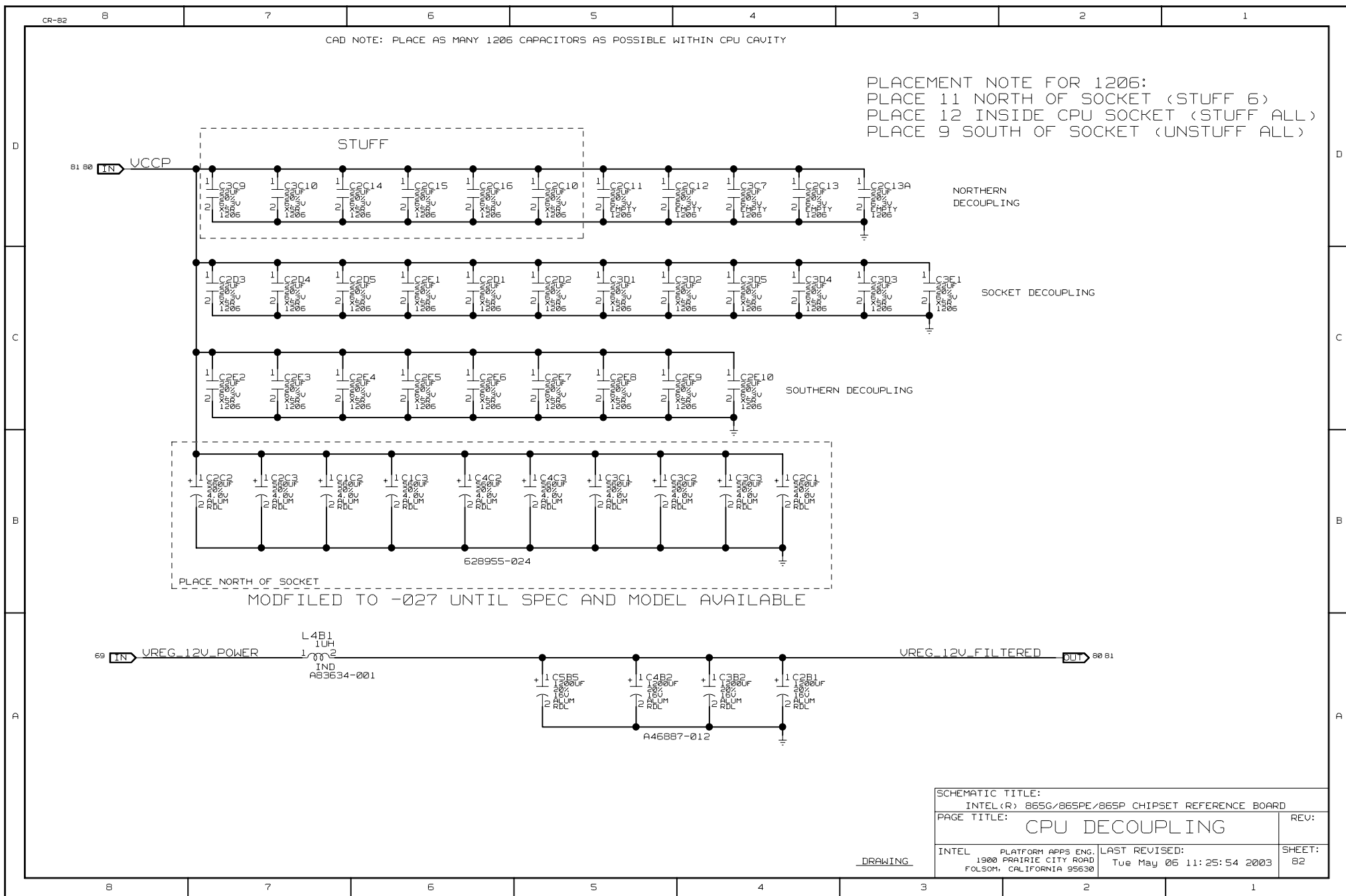




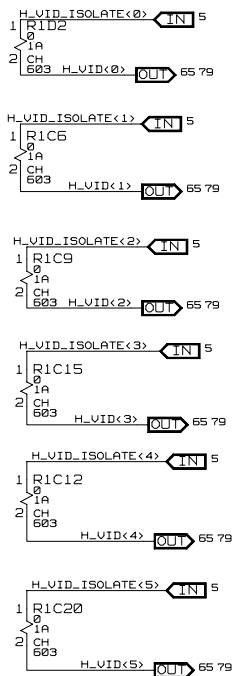


SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CPU VREG		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:53 2003	SHEET: 80

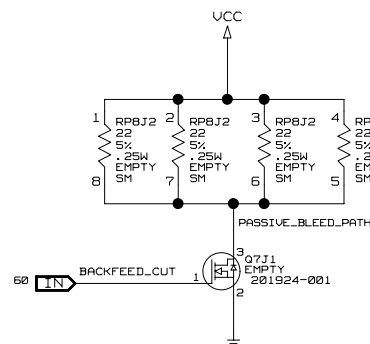
DRAWING



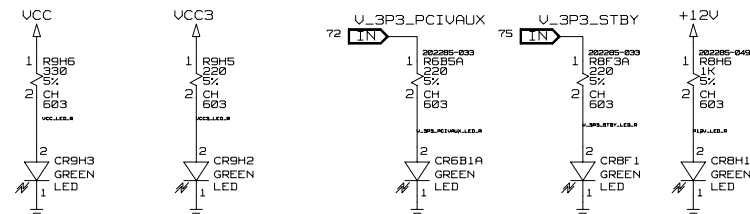
VID JUMPER RESISTORS



PASSIVE BLEED CIRCUIT

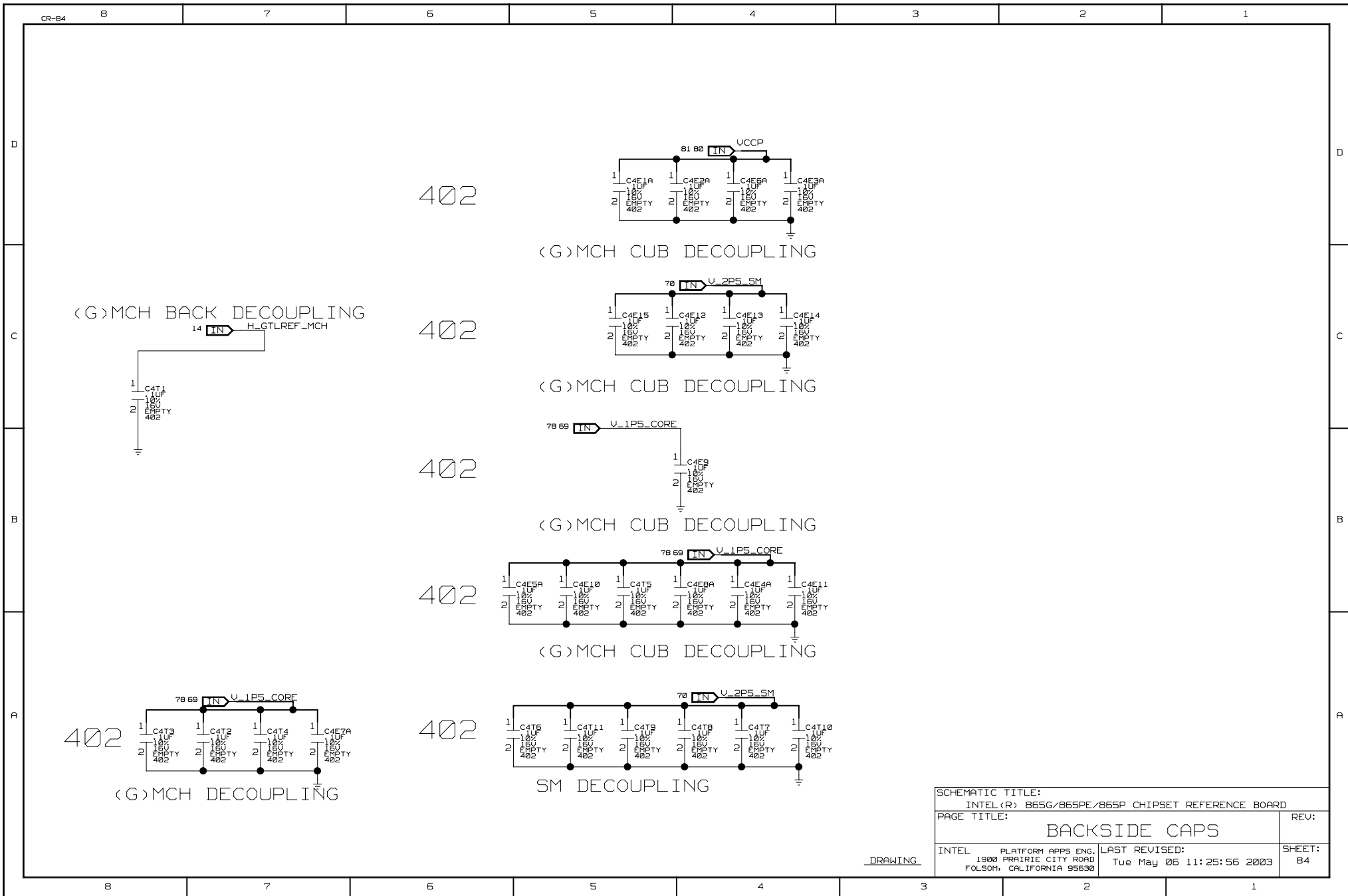


POWER RAIL STATUS LED'S



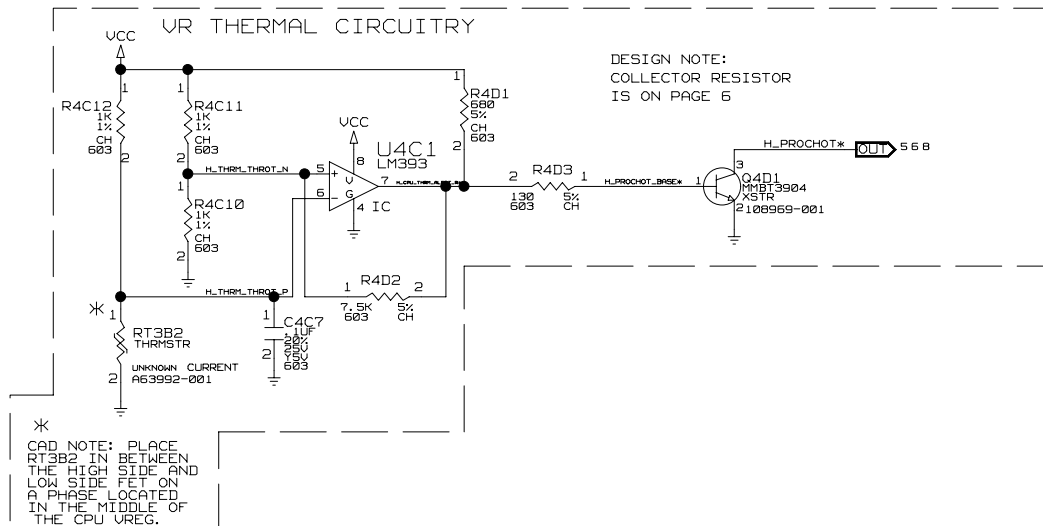
SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:		REV:
PASSIVE BLEED CRKT/STATUS LEDS/FRNT PANEL SWITCHES/VID JMPS		
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:55 2003	SHEET: 83

DRAWING



SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	BACKSIDE CAPS	REV:
INTEL	PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:56 2003
		SHEET: 84

DRAWING



SCHEMATIC TITLE:		
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE:	VR THERMAL CIRCUITRY	REV:
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 05 11:25:56 2003
		SHEET: 85

DRAWING

1