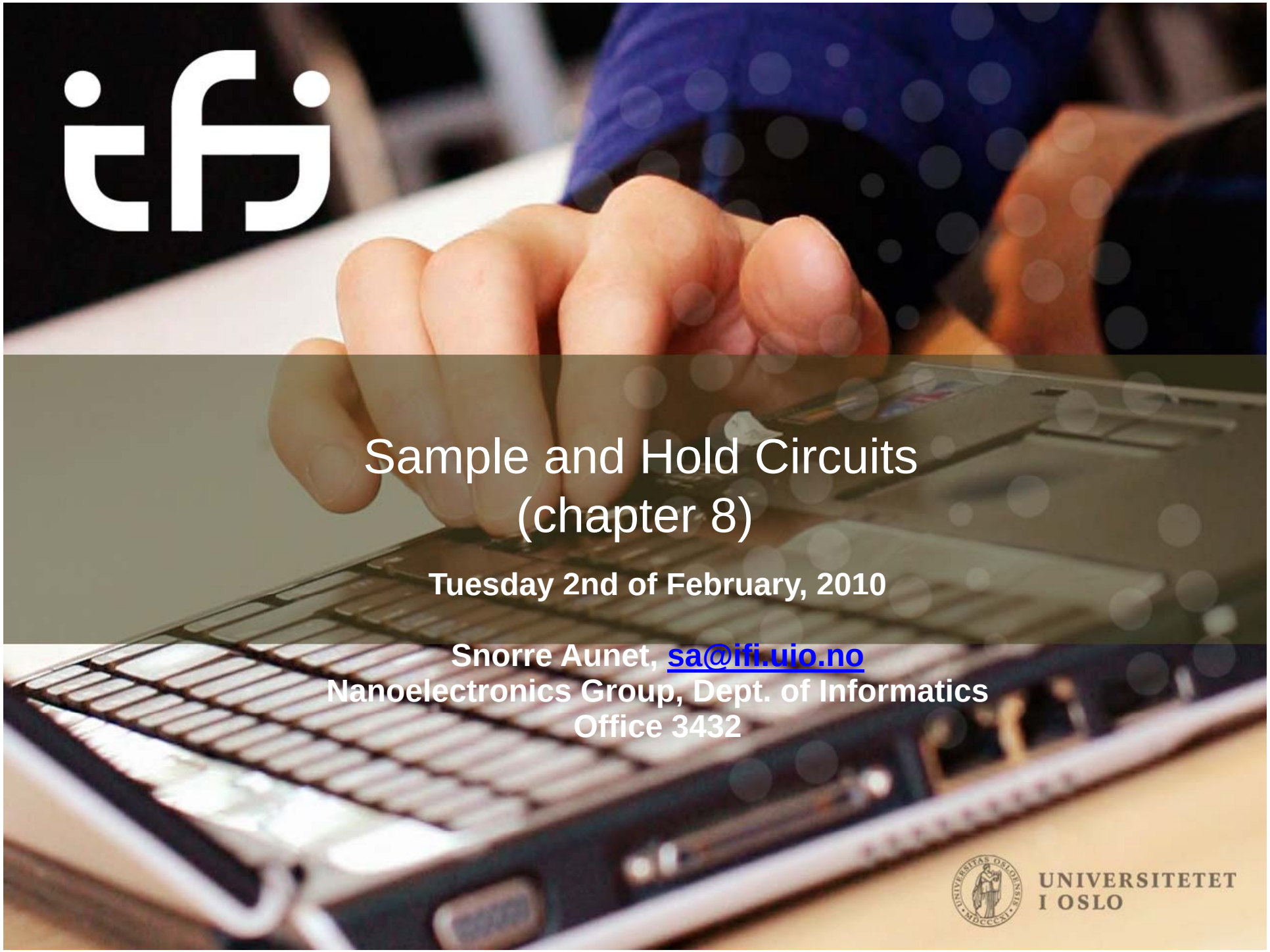


Sample and Hold Circuits (chapter 8)

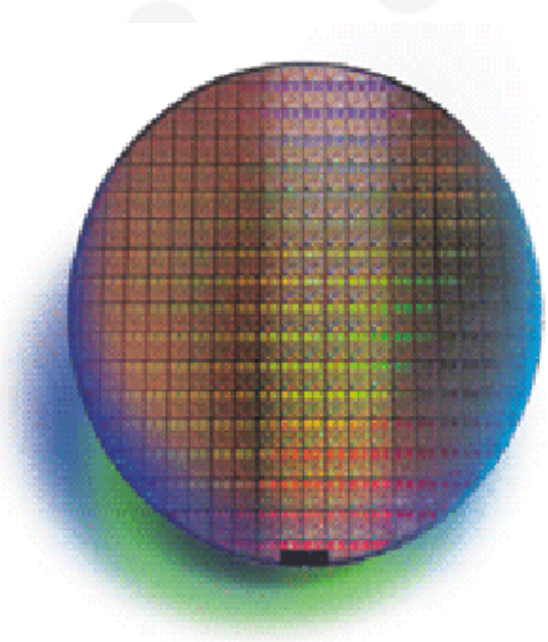
Tuesday 2nd of February, 2010

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

UNIVERSITETET I OSLO

Last time – Tuesday 26th of January

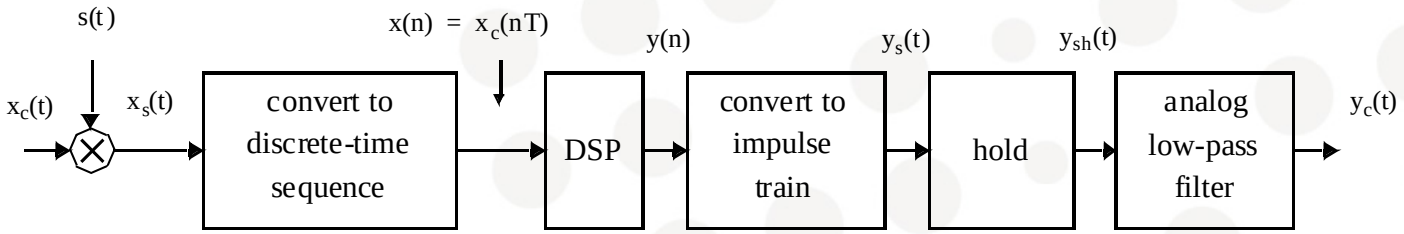
- Practical issues
- Learning goals
- Design project, tools and methods
- Syllabus
- Very brief introduction to various circuit building blocks
  (sample-and-holds, bandgap references, switched capacitor circuits, nyquist- and oversampling data converters, phase-locked loops)

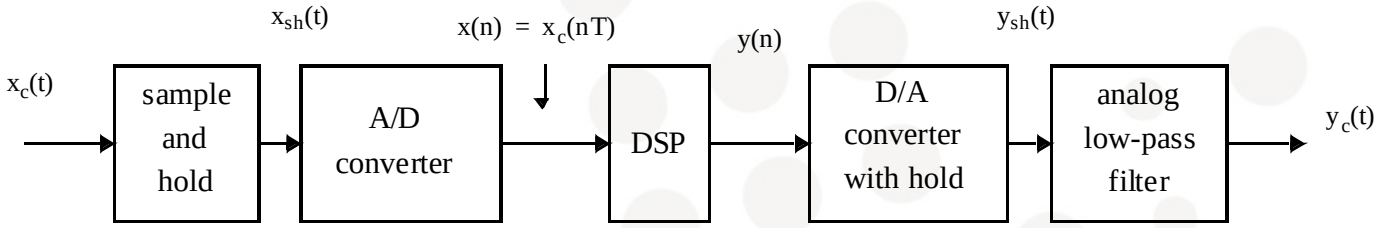


Sample and Holds (S/H) – What are the purposes?

- Mainly used in Analog-to-Digital Converters (ADC)
  - Samples analog input signal and holds value between clock cycles
  - Stable input value is required in many ADC-topologies
  - Reduces ADC-error caused by internal ADC delay variations
- Sometimes referred to as Track and Hold (T/H)
- Important parameters for S/H's
  - Hold step: Voltage error during S/H-transition
  - Signal isolation in hold mode
  - Input signal tracking speed in sample mode
  - Droop rate in hold mode: Small change in output voltage
  - Aperture jitter: Sampling time uncertainty

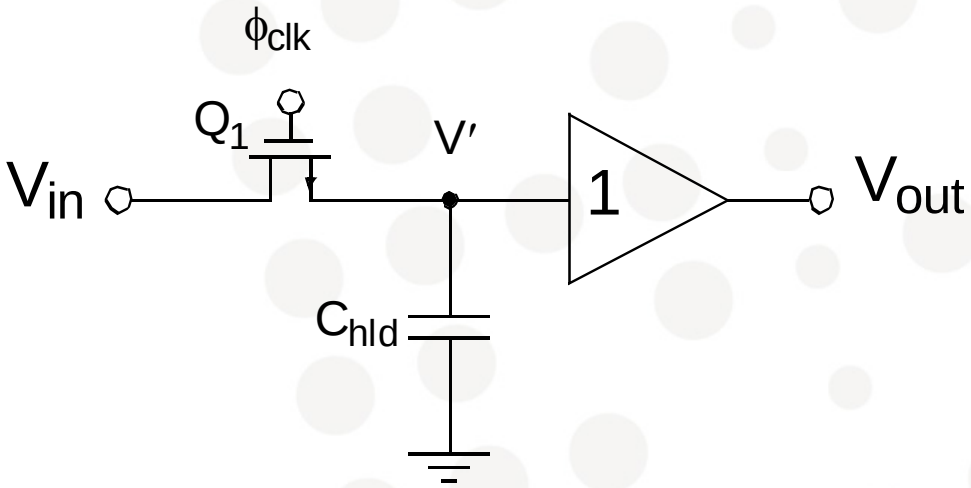
Overview of signal spectra – conceptual and physical realizations





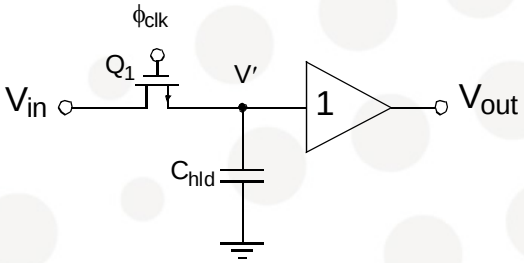
- An anti-aliasing filter (not shown) is assumed to band limit the continous time signal, $x_c(t)$.
- DSP (”discrete-time signal processing”) may be accomplished using fully digital processing or discrete-time analog circuits (ex.: SC-circ.)

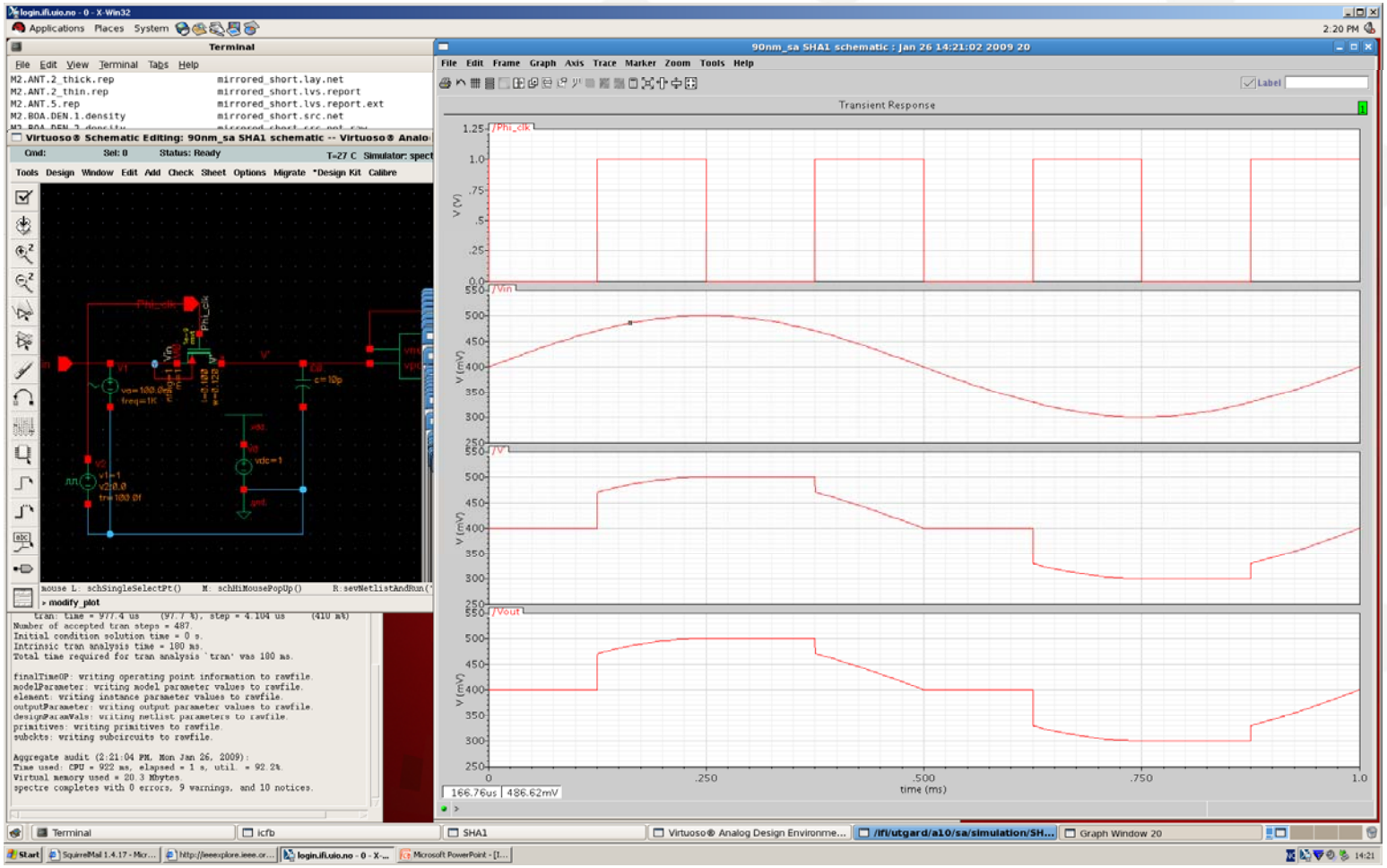
Basic S/H-topology



- Hold step:
  - Switch charge injection causes signal dependent hold step
- Aperture jitter:
  - Sampling-time variations causes signal dependent errors

Basic S/H-topology

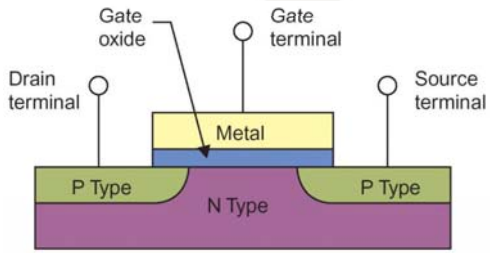




Charge injection due to channel capacitance

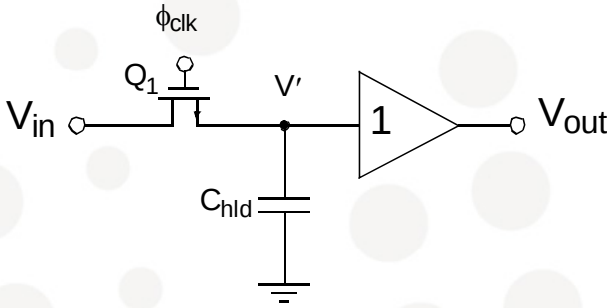
When ϕ_{clk} goes low, the channel charge of Q_1 is equally distributed between source and drain, leaving 50% of the charge across Chld:

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox} W L V_{eff\text{-}1}}{2}$$



$$V_{eff\text{-}1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in}$$

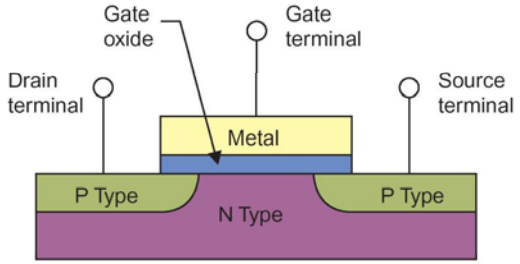
$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{ox} W L (V_{DD} - V_{tn} - V_{in})}{2 C_{hld}}$$



- $\Delta V'$ is linearly related to V_{in}, resulting in a gain error for the S/H. There is also a linear relationship to Vtn, which is nonlinearly related to Vin (through Vsb) resulting in distortion for the overall S/H.

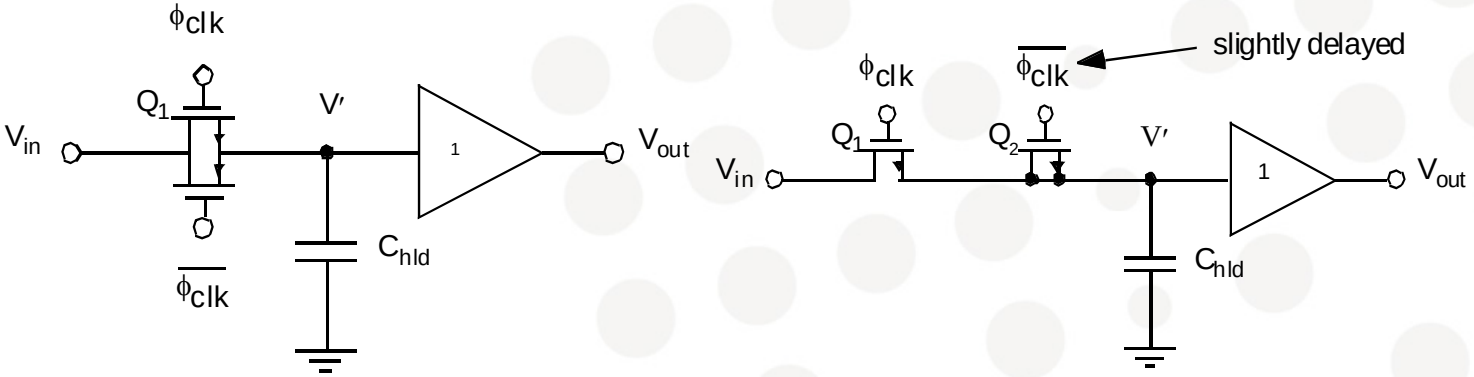
Charge injection due to the gate overlap capacitance:

- $$\Delta V' \cong -\frac{C_{ox} W L_{ov} (V_{DD} - V_{SS})}{C_{hld}}$$



- (See eq. 7.8) This component is usually smaller than that due to the channel charge, and appears as an offset, since it's signal independent. Thus it may be removed in most systems.
- The clock signal should be relatively noise free, as the power-supply rejection of this S/H might be poor. (if for example clock signal comes from an inverter with common Vdd and Vss)

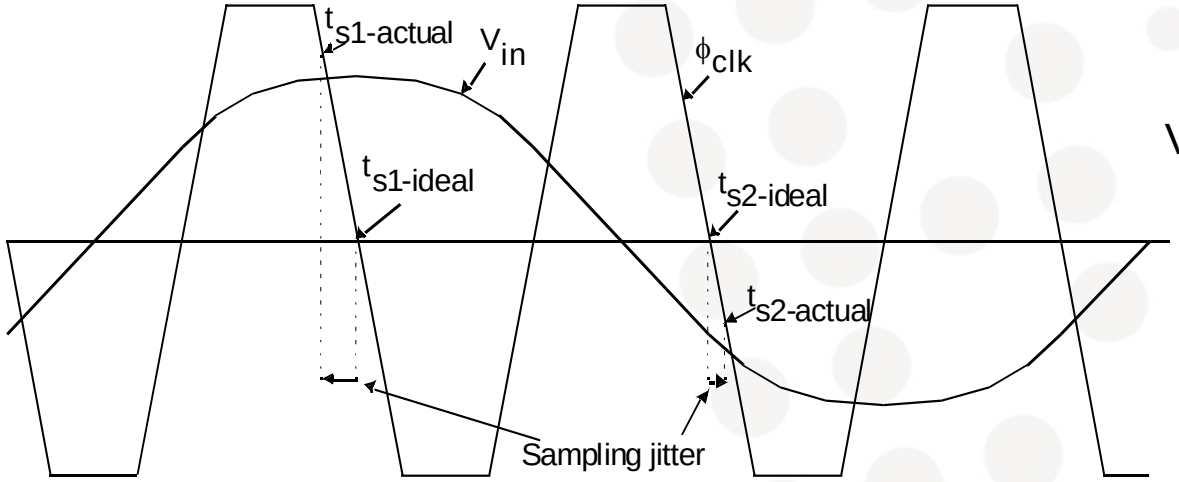
Hold step reduction

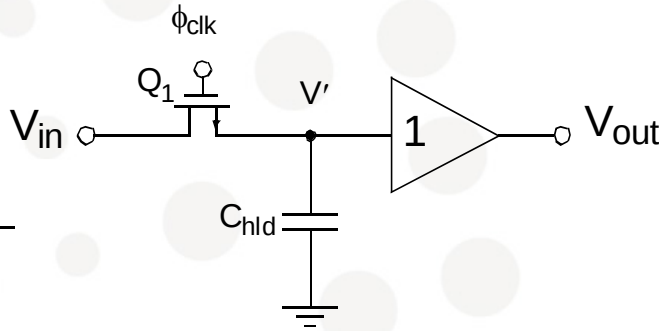


CMOS transmission gate **Dummy switch**

- Transmission gate reduces charge injection since the charge carriers in the NMOS and PMOS have inversed polarity -> The negative charge from the NMOS cancels the positive charge from the PMOS
    - PMOS and NMOS are however hard to match in size, reducing the benefit.
- A NMOS dummy switch (S and D short-circuited) of half channel area clocked on inverted clock may be used to absorb charge
    - Hold step reduced by approximately 80%
    - The dummy switch clock must be slightly delayed to ensure that no charge leaks through Q1 while it is still open

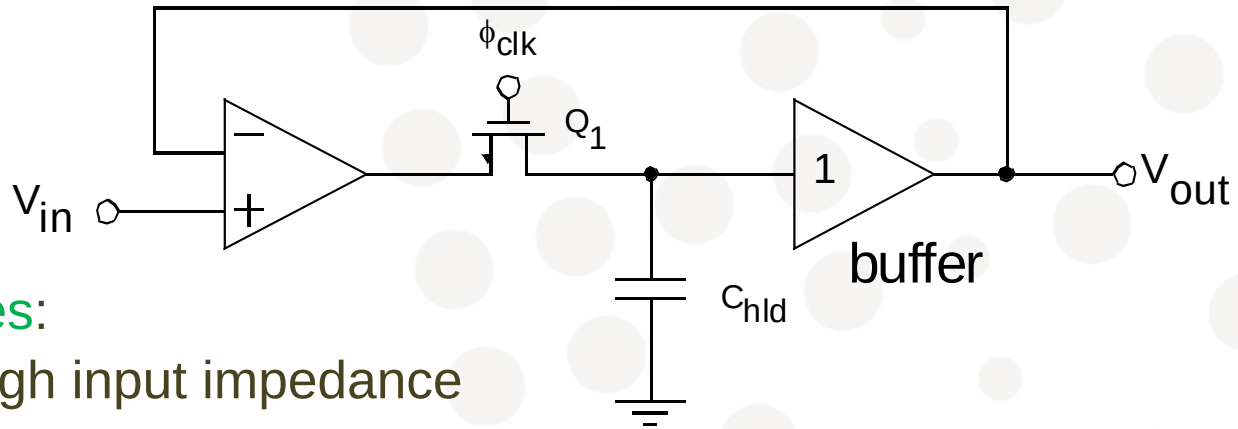
Aperture jitter





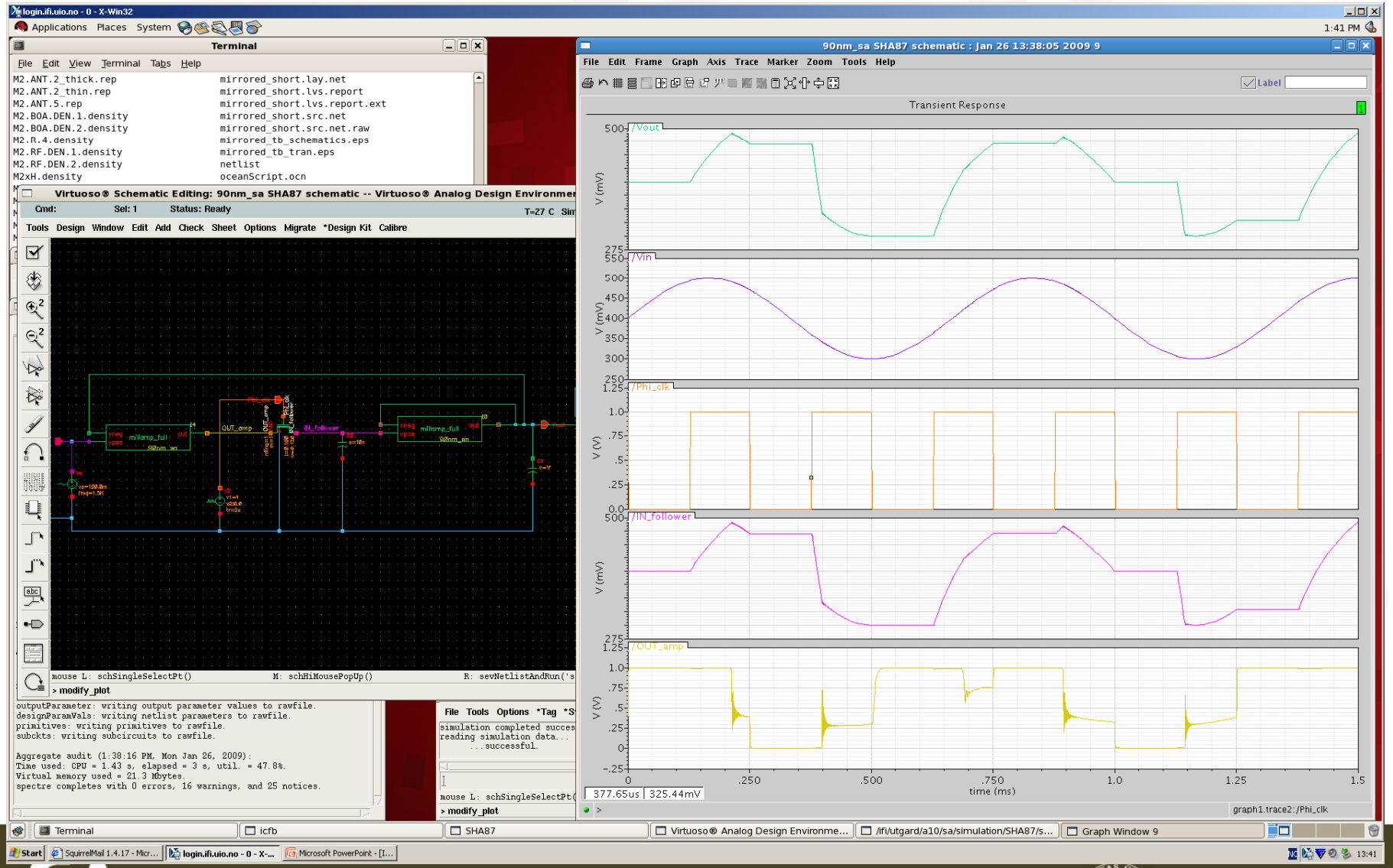
- If the input voltage is lower than the capacitor voltage, V_{in} is the source of the transistor used as a switch
- Vgs is then depending on V_{in}. For high values of V_{in}, the switch turns off too fast while for low values of V_{in} it turns off too late causing **distortion**

S/H (fig. 8.7)

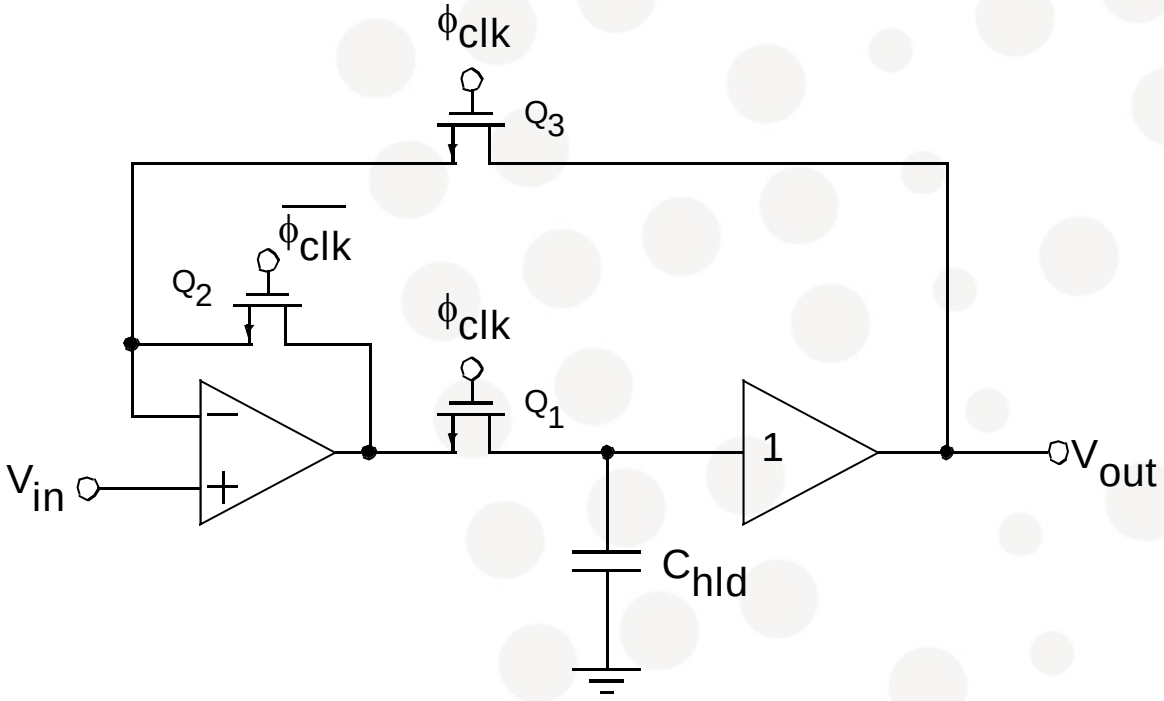


- Advantages:
  - High input impedance
  - Buffer offset voltage is divided by the gain of the input opamp, due to negative feedback. Simple voltage follower may be used at the output.
- Disadvantages:
  - Errors due to finite clock rise- and fall-times (PMOS and NMOS are not switched off at the same time)
  - Signal dependent charge injection -> Distortion
  - Feedback loop and need for stability limit maximum speed
  - In Hold mode, the first opamp output goes to either rail. Must slew back

Sample-and-Hold from fig. 8.7

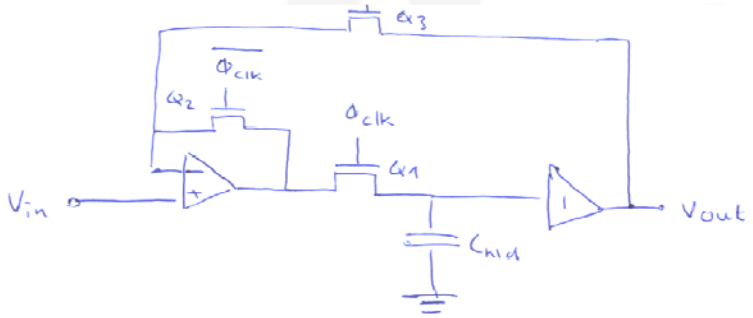


Increased speed (fig. 8.8)

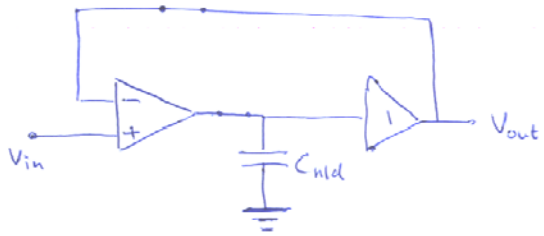


- During hold mode the opamp output is tracking the input
  - Leads to increased speed
- Disadvantages in common with the previous circuit

SAMPLE (= Track) / HOLD modes (fig 8.8)



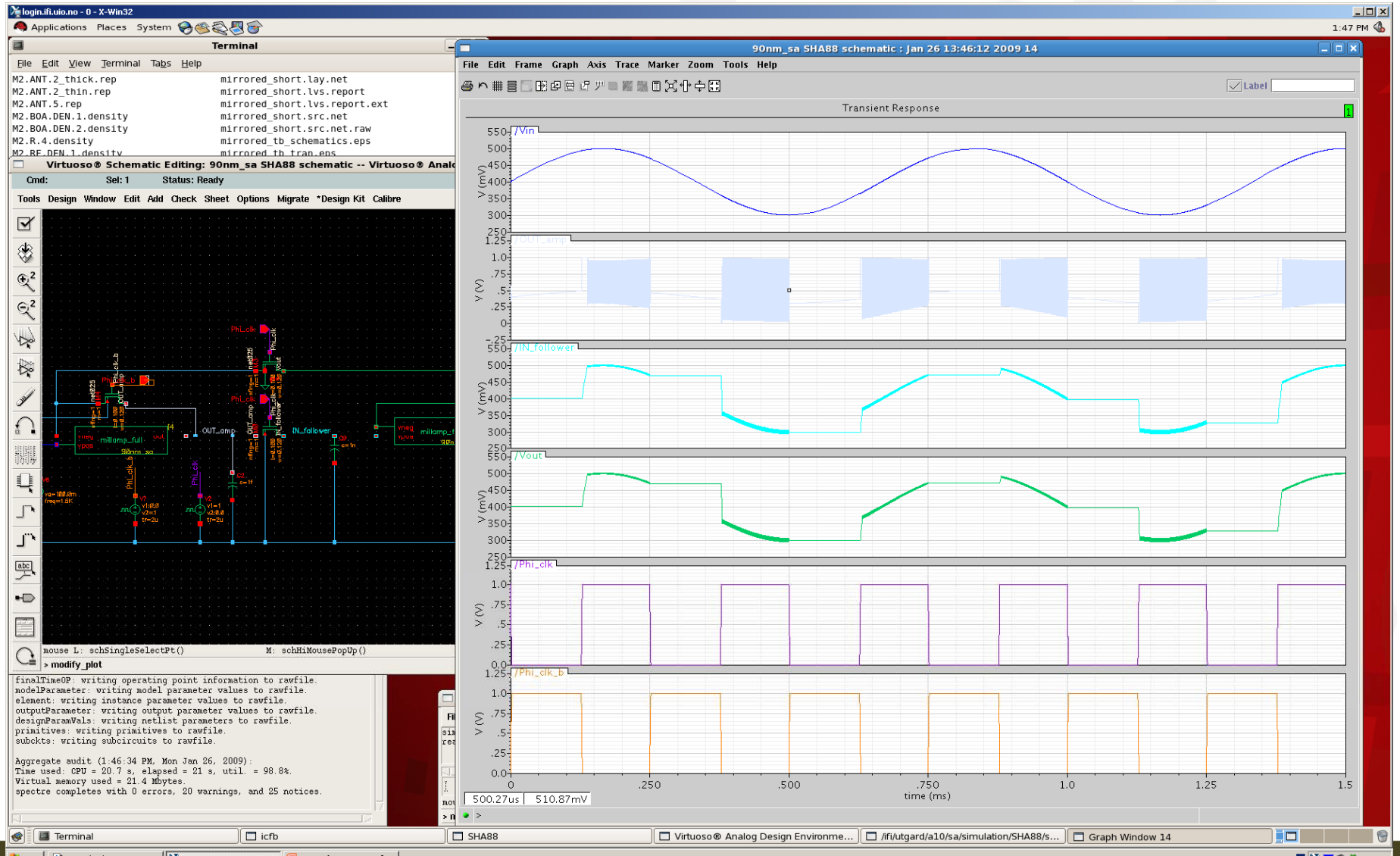
TRACK (SAMPLE):



HOLD:

α_2 keeps the output of the 1st OPAMP close to the voltage it will need to be at when track (sample) mode is entered.

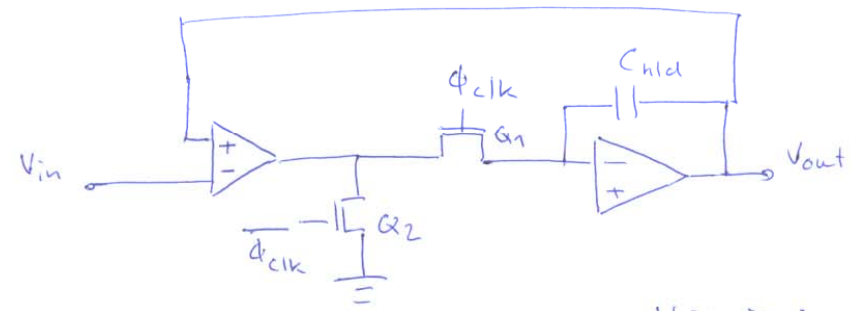
Sample-and-Hold from fig. 8.8



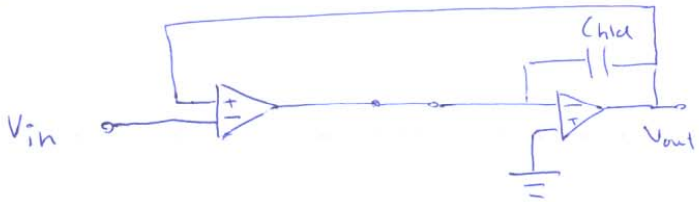
UNIVERSITETET I OSLO

Another S/H: Fig 8.9 (Improved version of the S/H from fig. 8.8)

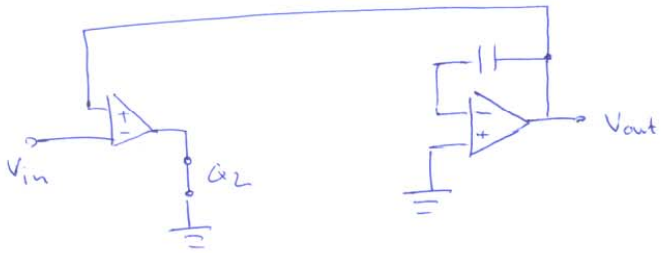
Fig. 8.9:



SAMPLE:

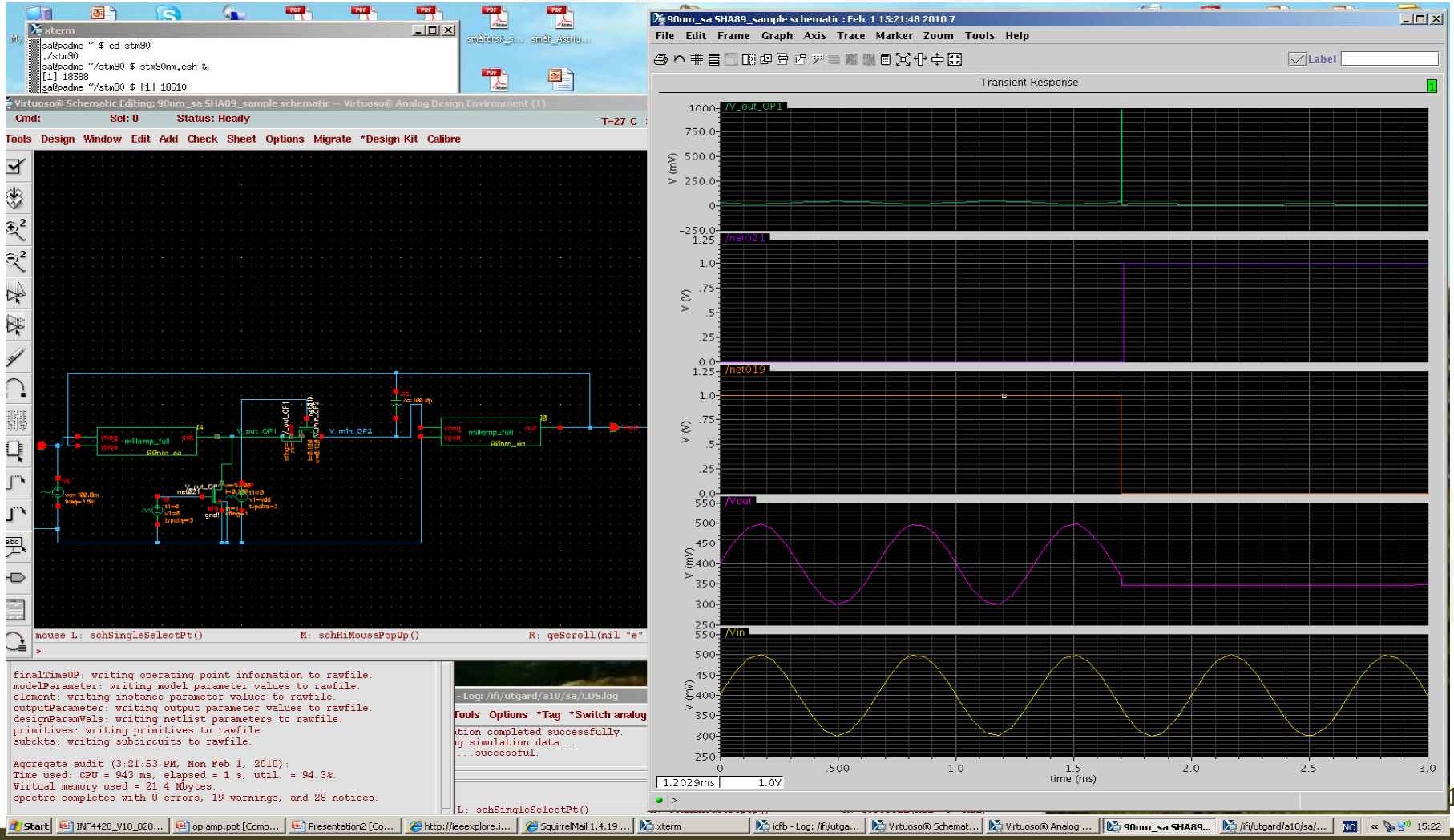


HOLD:

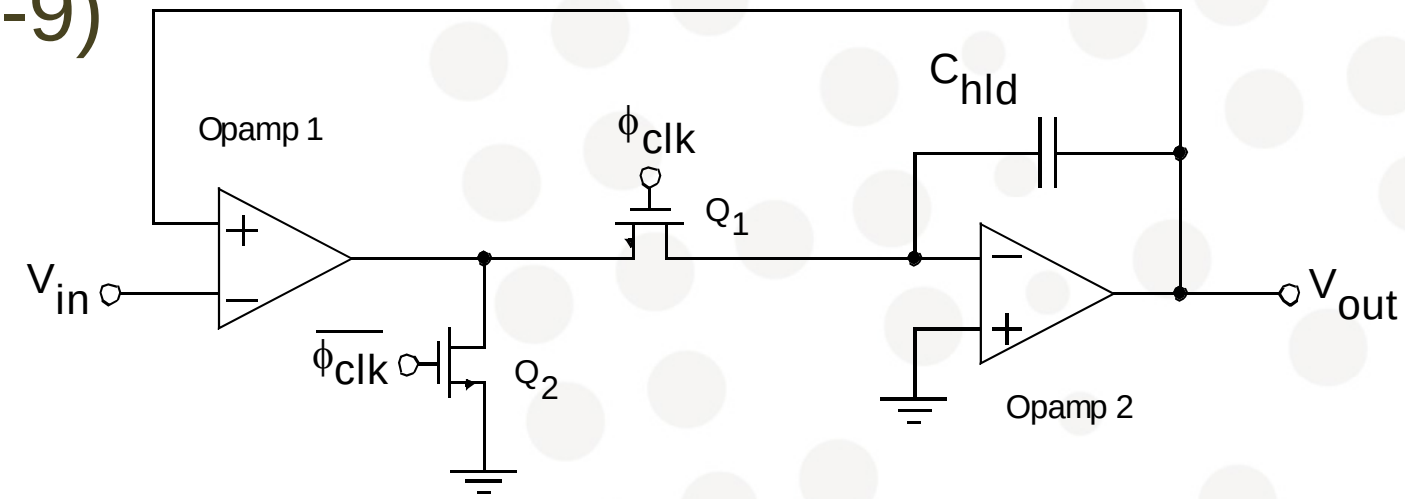


Q_2 grounds the output of OPAMP1 during HOLD. Then the output is close to where it will be when changing to SAMPLE-/TRACK-mo

Sample (track) mode to Hold mode (the S/H in fig. 8.9) signals, from top: $V_{outopamp1}$, $V_{(Q2)}$, $V_{(Q1)}$, V_{out} , V_{in}



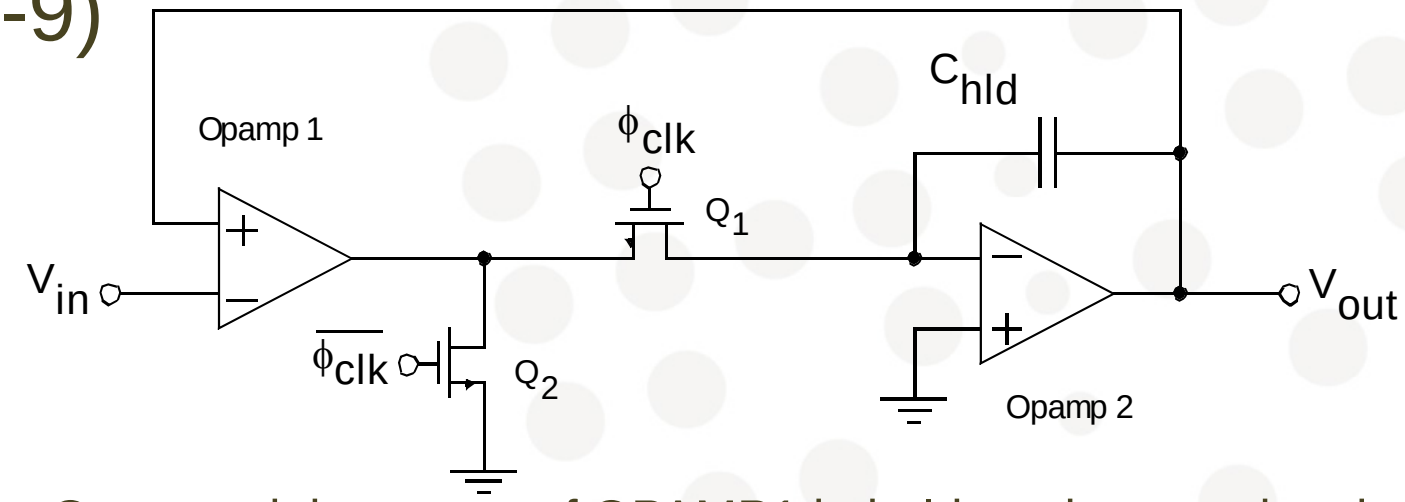
S/H with hold step independent of input signal (fig. 8-9)



+ : Both sides of Q_1 are nearly signal independent, so that the charge injection is (nearly) signal independent, provided a sufficient gain in the 2nd Opamp. The charge injection on C_{hld} causes the output of the 2nd Opamp to have a positive hold step, which is just a dc offset, with no signal distortion, and signal independent.

+: Sampling time will not change due to finite slopes of the sampling clock → less aperture jitter / aperture uncertainty → sample value closer to the ideal one.

S/H with hold step independent of input signal (fig. 8-9)



+ : Q_2 ground the output of OPAMP1 in hold mode, meaning that it's close to (and quickly getting to) the voltage it should have in S. mode, which improves speed.

- Preventing instability reduces speed
  - Worsened due to two opamps in the feedback loop

- More relevant information: K. R. Stafford, P. R. Gray, R. A. Blanchard: "A Complete Monolithic Sample/Hold Amplifier", IEEE Journal of Solid-State Circuits, Dec. 1974. (available from http://ieeexplore.ieee.org , when on UiO IP-address)

”New(er) architecture”

FIGURE 9. Closed-Loop Architecture with Integrator Output

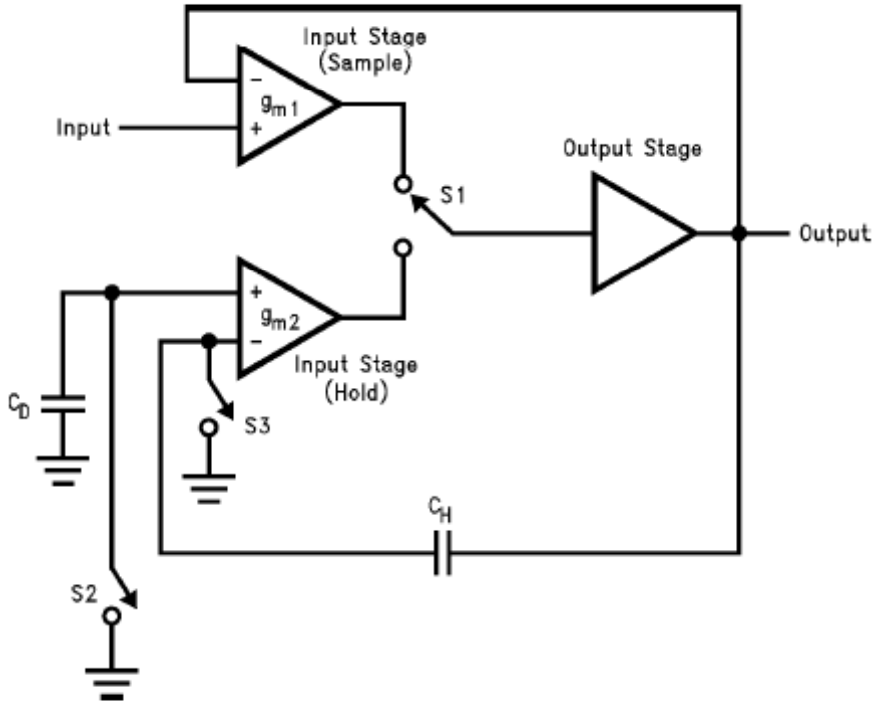


FIGURE 10. Current Multiplexed Architecture

A new architecture which combines the speed of the open-loop configuration and the accuracy of the closed-loop configuration is the current-multiplexed architecture shown in *Figure 10*. The LF6197, National's High Performance VIP™ Sample-and-Hold Amplifier used this architecture. This architecture provides for a cancellation of charge injection, allowing one to use a small hold capacitor to get high speeds without the disadvantage of a large hold step.

Specifications and Architectures of Sample-and-Hold Amplifiers

National Semiconductor
Application Note 775
July 1992

Continous efforts to improve S/H circuits..

A Sample/Hold Circuit for 80MSPS 14-bit A/D Converter

Xiao Kunguang[1,2], Wang Yuxing[1,2], Xu Minyuan[1,2], and Zhu Chan[1,2]

454 IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, VOL. 3, NO. 3, JUNE 2009

Digital Calibration of a Nonlinear S/H

Patrick Satarzadeh, *Student Member, IEEE*, Bernard C. Levy, *Fellow, IEEE*, and Paul J. Hurst, *Fellow, IEEE*

A High-Speed Highly-Linear CMOS S/H Circuit

Mahmoud Sadollahy[1, 2], Khayrollah Hadidi[2]
[1] *Azad Islamic University, Sofian Branch*
[2] *Microelectronic Research Laboratory, Urmia Universit*
st_msadollahy@mail.urmia.ac.ir

978-1-4244-1692-9/08/$25.00 ©2008 IEEE

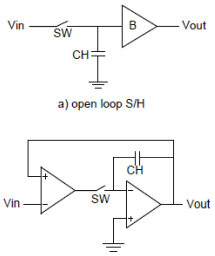


Figure 1. Sample and hold architectures

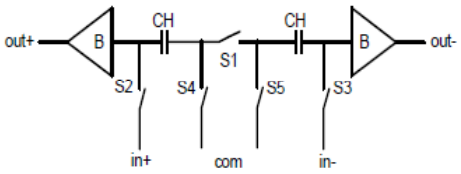
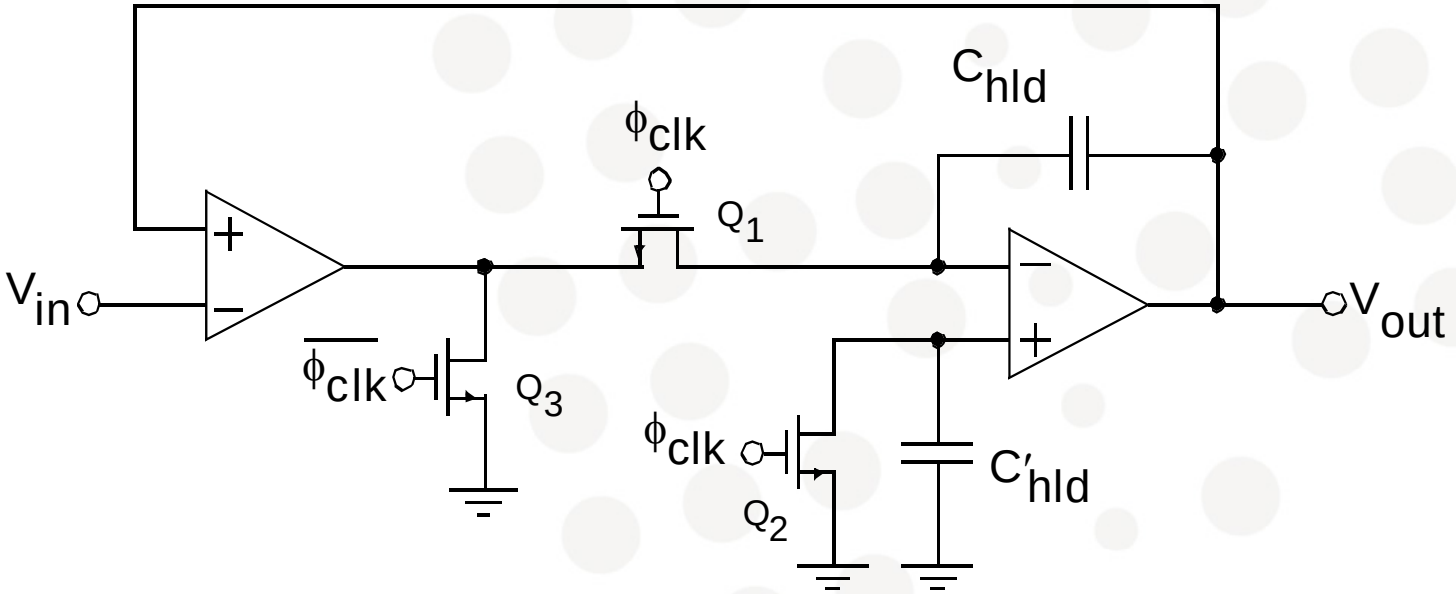


Figure 2. **Proposed open loop S/H architecture**

- IEEEXplore may provide State-of-the-Art solutions

Reduced DC-error (fig. 8-10)

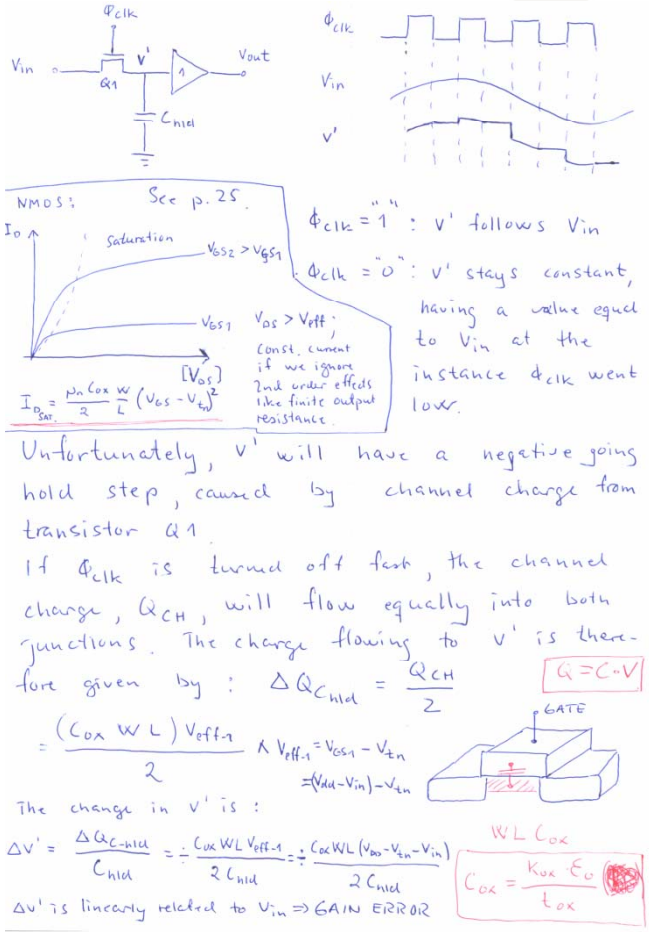


- Improved version of previous circuit (in fig. 8.9)
- By placing a copy of Q1 and Chld in parallel between ground and the positive input of the second opamp, the voltage change due to charge injection will be equal on both inputs. Error is cancelled by opamp CMRR.
  The **common-mode rejection ratio** (CMRR) of a differential amplifier (or other device) measures the tendency of the device to reject input signals common to both input leads.

Additional Background Litterature, S/H circuits

- A. S. Sedra, K. C. Smith: ”Microelectronic Circuits”, Saunders College Publishing, 1991.
- R. Gregorian, G. C. Temes: ”Analog MOS Integrated Circuits for signal processing”, Wiley, 1986.
- K. R. Stafford, P. R. Gray, R. A. Blanchard: ”A Complete Monolithic Sample/Hold Amplifier”, IEEE Journal of Solid-State Circuits, Dec. 1974.
- F. F. Kuo:”Network Analysis and Synthesis”, Wiley, 1966.
- S. Soma: ”Grunnbok i elektronikk”, Universitetsforlaget, 1979.
- National Semiconductor: ”Specifcations and Architectures of Sample-and-Hold Architectures”, App. Note 775, July 1992.
- S. Aunet: ”BiCMOS Sample-and-Hold for Satelittkommunikasjon”, hovedfagsoppgave, UiO, 1993.

S/H stuff..



$$\Delta V' = -\frac{C_{ox} W L (V_{DD} - V_{tn} - V_{in})}{2 C_{hold}}$$

$\Delta V'$ is also linearly related to V_{tn}, which is nonlinearly related to the input signal, V_{in}, due to variations in the source - substrate voltage (assuming the substrate is tied to one of the voltage rails).

⇒ This nonlinear relationship with V_{in} results in distortion for the overall sample-and-hold circuit.

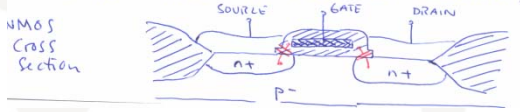
Additional charge in V' due to the gate overlap capacitance.

Using a derivation similar to that used to find (7.8), we have:

$$\Delta V' \cong -\frac{C_{ox} W L_{ov} (V_{DD} - V_{SS})}{C_{hold}}$$

INF3410

This component is usually smaller than the one due to the channel charge and signal independent. This means it can be removed.



See page 17