the incredible shrinking (unregulated) power supply

by Dr. Ray Ridley

In the last issue of SPM, we brought to your attention the new Vicor power supply. This new product offers 800 W/in^3 with a 48-V input, 12-V output and 95% efficiency. We thought the unregulated output was significant, but this was still a quantum leap in power density.

We predicted that industry would respond quickly to Vicor's new technology. That is, if unregulated supplies are in demand. Packaging technologies have advanced rapidly in the last few years with fierce competition in the high-density dc-dc converter market, and many of the companies are poised to produce similar products.

Well, we were right. At our last design workshop, International Rectifier sent us demo boards highlighting their DirectFET parts and half-bridge drivers. These boards show what happens if you take conventional PWM technology, and optimize a power stage without any regulation. The results are surprising.

We tested some of the IR power supplies on the bench, and were pleased to find that they performed as advertised. We also found out why unregulated designs lead naturally to high density, and where corners are cut to improve density even further.

Conventional PWM Converter Design

As power levels go up, the flyback is no longer a viable topology for reasonable design, especially for low output voltages. The peak secondary currents very quickly become excessive. So let's start with the forward converter, the industry mainstay for higher power levels. Figure 1 shows a conventional forward PWM converter, conservatively designed for 100 kHz operation, at 50 W output power.

This power supply is designed to run full at power indefinitely with no airflow, using typical low-cost parts such as standard cores, a double-sided PCB, and electrolytic capacitors. It is also built with multiple protection circuits to withstand abuse in a teaching lab environment. Properly packaged, the power supply measures about 9 cubic inches– about 5.5 W/in^3. This is a far cry from the 800 W/in^3 offered by new technologies.

Figure 1 also shows in the foreground the IR half bridge circuit which achieves a density of about 500 W/ in^3. You can see that the two converters are far apart in terms of density.

So how do they get there? What does it take to raise the density of the power supply an order of magnitude or more? There are several necessary steps to overcome the usual obstacles of power supply density:

1. The switching frequency must be raised above 100 kHz without introducing excessive losses.
2. The output rectifier dissipation must be reduced.
3. Magnetics losses must be reduced.
4. Inductor size and dissipation must be reduced.
5. Output filter capacitor size must be reduced.
6. Reduction or removal of snubbers.

And, most importantly,

7. Specifications must be relaxed, and
8. More money must be spent on parts.

For most custom power supply designs, items 7 and 8 usually drive the process. For many users, power density is not nearly as important as cost, and performance specifications are fixed. However, let's throw cost, specifications, and caution to the wind, and see what is possible.

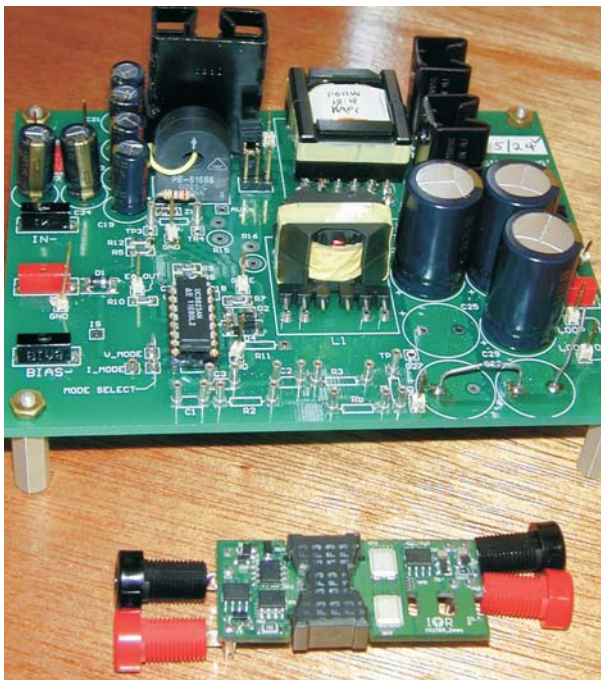

Figure 1: 50 W forward converter compared to IR's 200 W half-bridge evaluation board

Transformer Turns Ratio Design

First we start with a standard forward converter, with the following specifications:

Input:	40 to 60 VDC
Output:	10 V at 20 A, regulated
Frequency:	200 kHz

The first step in design is to choose the transformer turns ratio. The step down must be as large as possible to minimize the primary currents and the secondary voltages. However, we have to make sure the converter can regulate at low line with the available duty cycle and convertion ratio of the converter power stage itself.

The maximum allowable duty cycle for a forward converter to ensure that the core is properly reset, is 0.5 under worst-case conditions. You cannot actually run the converter at this duty cycle in steady state, because this allows no headroom for controlling the converter with step changes. You also have no margin for component variation or temperature changes if you design to the limit of 0.5. A reasonable design maximum at low line for control of step changes is 0.4.

The required turns ratio for this operating point is 1.43:1. This gives a peak switch current of 16.9 A, shown in Figure 2a. The RMS current is 9.4 A, corresponding to 4.4 W loss for a 50 mOhm on-resistance. This is the baseline for a converter design. Now we can proceed with modifications to the power supply specifications to see the effect on the design.

Modification 1: The input line variation is removed, with the input voltage fixed at 60 V. The required turns ratio is now 2.14:1, with switch currents and dissipation as shown in Table I. Duty cycle headroom is still allowed to compensate for step changes in load that may occur. The nominal steady-state duty cycle is set at D=0.4. The increased step down in the transformer reduces the primary current, and the secondary voltage.

Modification 2: Remove the duty cycle headroom for regulation, allowing it to reach 50% under steady-state conditions. When we do this, we lose the ability to regulate the output voltage with changes in the load current. (Also, as we will see later, we cannot control the resonance of the output LC filter.) The turns ratio now changes to 2.7:1, with a corresponding drop in primary currents and secondary voltages.

Modification 3: Replace the output diode drop with a synchronous rectifier that has an on-resistance of 3.3 mOhm. This allows the turns ratio to increase to 2.9:1.

After all of these changes, the peak current drops substantially from 16.9 A to 8.3 A, and the dissipation in the power switch drops more than a factor of three. This is a surprising result when changing from an input voltage range of only +/- 20%.

The improvements reach beyond just the power switch and its dissipation. The primary and secondary windings of the transformer will also see similar drops in dissipation due to the improved turns ratio.

Furthermore, the larger step down reduces the voltage applied to the output diode from 42.9 V to 20.7 V. This provides the opportunity to use low-voltage synchronous rectifiers, which are now available at low cost from many vendors (including IR, Toshiba, Phillips and others).

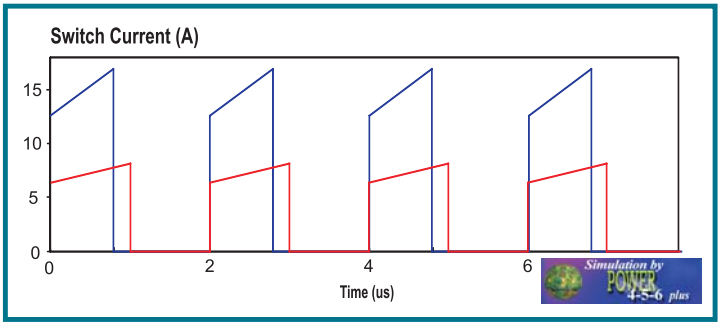

Figure 2a: MOSFET currents for forward converter with and without regulation

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Table I - Effect of Changing Specifications on Transformer Turns Ratio Selection

	Turns Ratio	Peak Switch Current	RMS Switch Current	Conduction Loss (50 mOhm)	Diode Voltage Stress	Inductor (4A Ripple)
Regulated Forward 40-60 V	1.43:1	16.9 A	9.4 A	4.4 W	42 V	8 uH
Regulated Forward 60 V only	2.14:1	11.3 A	6.3 A	1.9 W	28 V	8 uH
Non-regulated Forward 60 V only	2.7:1	8.9 A	5.5 A	1.5 W	22 V	7 uH
Non-regulated forward 60 V only synchronous rectifier	2.9:1	8.3 A	5.2 A	1.3 W	20.8 V	6.8 uH

Transformer Design

For the 200 kHz forward converter transformer design, we can use an 8:3 turns ratio, on a core with a 0.54 cm^2 cross-sectional area. This corresponds to an RM-8 core. The core loss with this design, using a planar version of the core, would be 0.65 W.

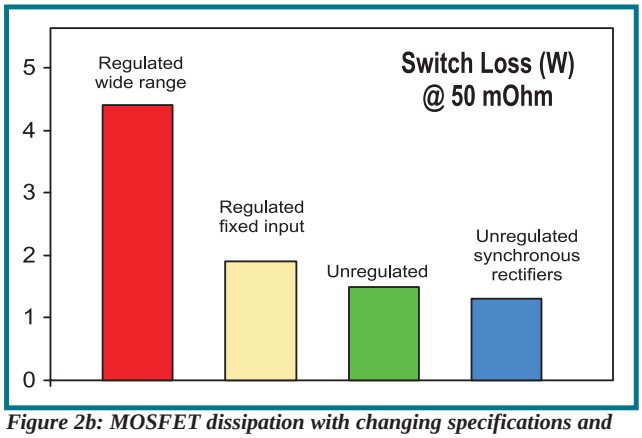


Figure 2b: MOSFET dissipation with changing specifications and fixed on-resistance

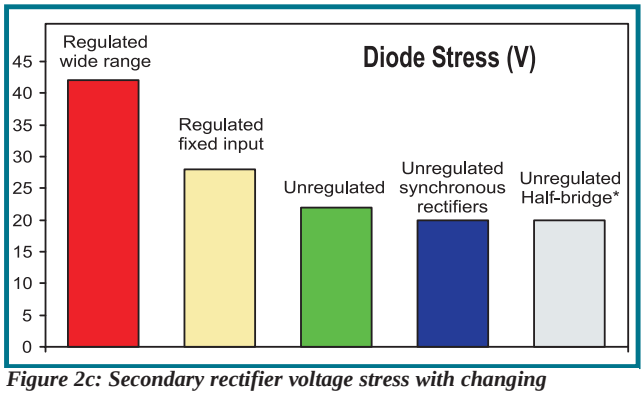


Figure 2c: Secondary rectifier voltage stress with changing specifications

Modification 4: Raise the frequency to 500 kHz to reduce the turns count and winding dissipation in the transformer. With this switching frequency, a 3:1 turns ratio can just barely be used, which will not quite provide the output voltage that is needed, but is good for experimentation. This design is very aggressive, pushing to a high B_{sat} on every cycle, and high core losses of 4.5 W. This is clearly not an acceptable number.

The 3F3 material is one of the best available on the market. Options for reducing core loss are to either increase the primary turns count, leading to more winding loss and too little voltage on the secondary, raise the frequency even higher, or change topologies.

Modification 5: Change the topology from a forward to a half-bridge converter. Using the same 3:1 turns ratio, the core is now operated at half the output ripple frequency. One side of the bridge pushes the core in one direction, the other side back again, completing the cycle in 4 us. The forward converter, moves the core to a high flux level, and back to zero every 2 us. We also gain the benefit of the bi-directional nature of the core usage cutting the peak flux in half, once the converter has reached steady state. This produces a more conservative design that is very practical to build using planar technology and PCB windings.

Output Inductor Design

So far, modifying the specifications, frequency, and topology has greatly impacted the design of the FET, output rectifier, and transformer. The final large component is the output inductor.

Table II - Effect of Changing Specifications on Transformer Design

	Frequency	Core Area	Transformer Turns	Core Loss
Non-regulated Forward 60 V only Synchronous Rectifier	200 kHz	0.54 cm^2	8:3	0.65 W
Non-regulated Forward 60 V only Synchronous Rectifier	500 kHz	0.54 cm^2	3:1*	4.5 W
Half Bridge	500 kHz	0.54 cm^2	3:1	1.25 W

** Closest available turns ratio - Bmax is very high with no design margin*

The original 200 kHz forward converter, needed an 8 uH inductor. Removing the need for regulation, and fixing the input voltage allows this value to drop a modest amount to 6.8 uH, assuming a 4 A peak-peak ripple current in the inductor. There is not much change in the inductor since the off-time remains close to the same value, and this determines the current ripple.

In order to build a 6.8 uH inductor on an RM4 core, there would have to be 37 turns. This would have 90 mOhms winding resistance, and 17.4 W of loss. This is obviously an unacceptable design.

Raising the frequency of the forward converter to 500 kHz allows the inductor to be reduced to 2.6 uH. This requires 14 turns on an RM4 core, with 3.5 W dissipation if conventional foil windings are used. This is still too high, and will increase substantially if we try to make the windings from PCB traces, which is the ultimate design objective. This is about as good as can be done with the forward converter. The next option is to change topology to a half bridge converter, running as close as possible to 100% duty cycle. We can drop to less that 100 nH to get the same ripple performace, now just a single turn on the RM4 core. This is trivial to implement with PCB turns.

Figure 3a compares the inductor currents for the forward and half bridge converters under the same conditions. Figure 3b shows the reduction in inductance that is achieved with each step of design change described in this section. This drop in inductance is dramatic, but be careful. If the maximum duty cycle drops just a couple of percentage points with temperature or other changes, the ripple current increases dramatically.

Half Bridge Converter Experimental Results

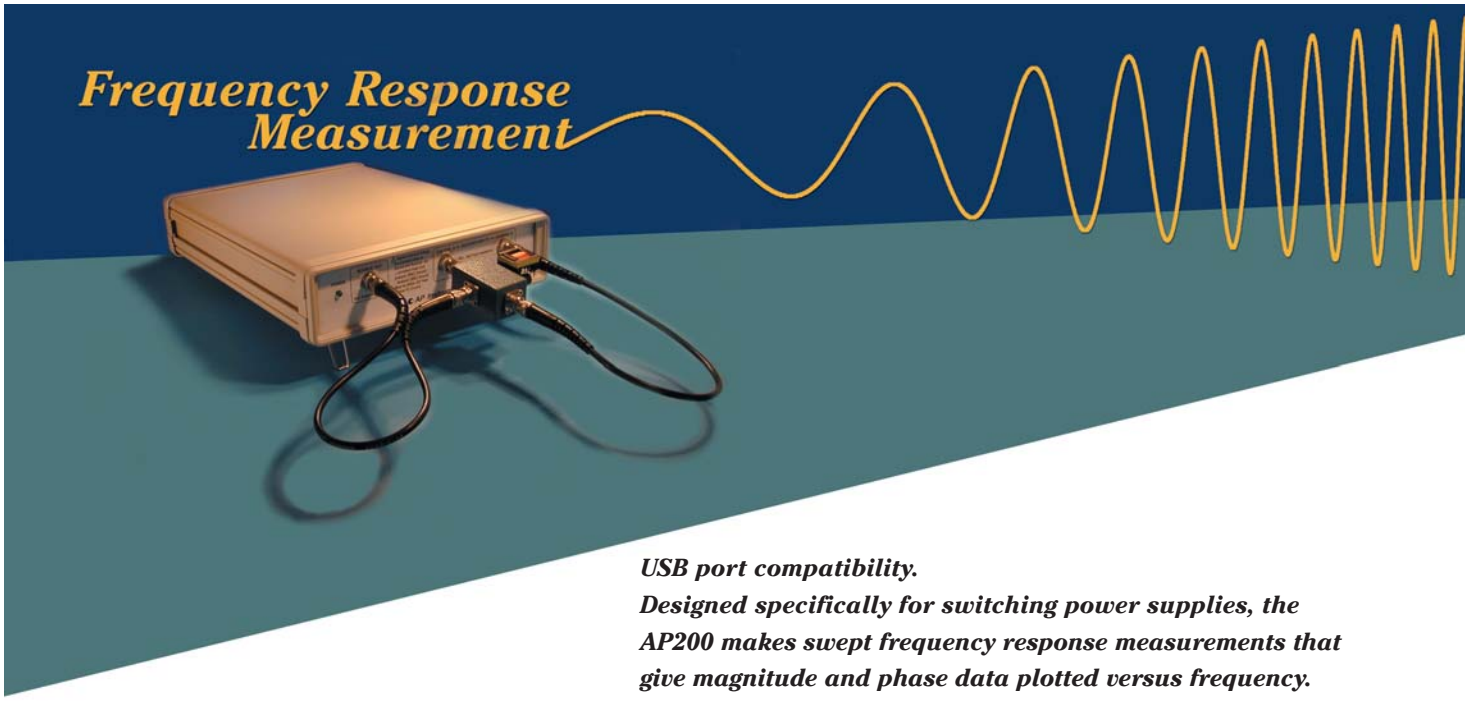
Everything looks good on paper for the half-bridge unregulated converter. We tested the IR half-bridge evaluation board to see how well the hardware would really perform. Figure 4 shows a simplified schematic of the half bridge power stage. (Full details can be obtained at www.irf.com.)

There are several important features to point out in this design. Firstly, there are no snubbers on either the primary or secondary. This is possible because the converter runs at close to 100% duty cycle, and the natural clamping action of the alternate FET turning on eliminates the need for snubbers.

Table III - Effect of Changing Specifications on Inductor Design

	Frequency	Frequency	Frequency	Frequency
Non-regulated Forward 60 V only Synchronous Rectifier	200 kHz	6.8 uH	33	17.4 W
Non-regulated Forward 60 V only Synchronous Rectifier	500 kHz	2.6 uH	14	3.5 W
Half Bridge	500 kHz	<100 nH**	3:1	0.2 W

*** Assumes a maximum available duty cycle of 97.5%*



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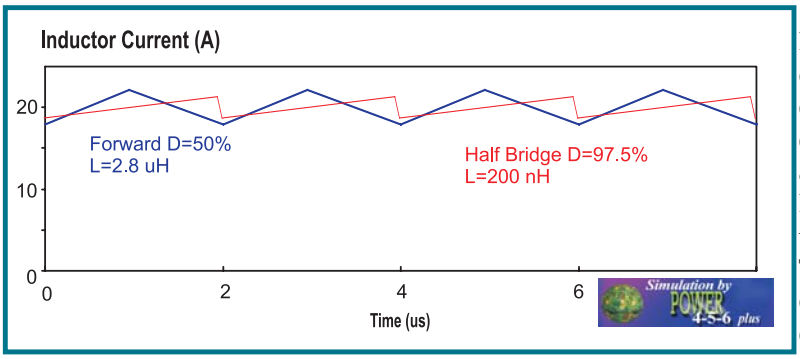

Figure 3a: Inductor currents for unregulated forward and half-bridge

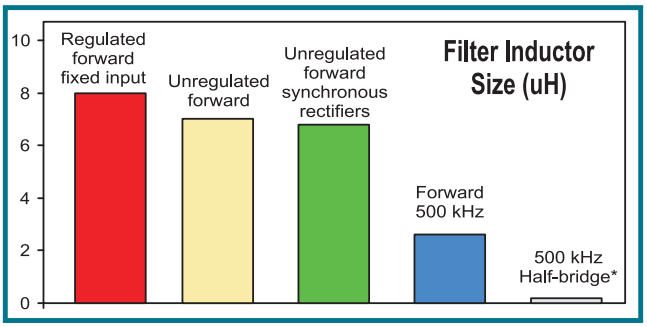

Figure 3b: Forward and half-bridge inductors

Secondly, the synchronous rectifiers are naturally driven from the transformer secondary. This is a crucial part of the design.

Building IC drivers on the secondary wastes a lot of power, produces complex timing issues, and uses many more parts. The self-driven secondary is again a natural consequence of using a circuit at close to 100% duty cycle. It also provides conservation of gate energy from one rectifier to the other. Clamps are added to the gate drives to prevent overdriving the sensitive devices.

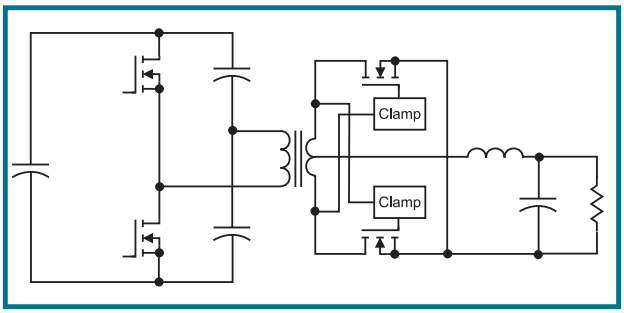

Figure 4: Half bridge converter schematic

All of these benefits can be obtained with other power stages, as Synqor realized several years ago in the design of their push-pull isolation stages of their high-density converters. (See the last issue of SPM for details.)

Figure 5 shows the secondary voltage on the half-bridge converter. There is a dead time of 50 ns corresponding to a duty cycle of 97.5% at 500 kHz. This allows the use of a very small inductor. Figure 6a shows the output voltage of the converter at just above half load. The ripple is somewhat high, but this can be attenuated with more load capacitors. Figure 6b shows the input voltage ripple of the supply. Again, this ripple is excessive, and further filtering would be needed for quiet design.

Figure 7 shows the output voltage step load response, indicating another area of concern in the converter. The output filter is undamped, leading to a significant amount of ringing, in this case with just a 1 A step load. This is a more problematic issue to fix. The output filter must be properly damped to avoid this ringing. Since the output inductor is already as small as is reasonable, the output capacitor must be increased substantially to damp this ringing.

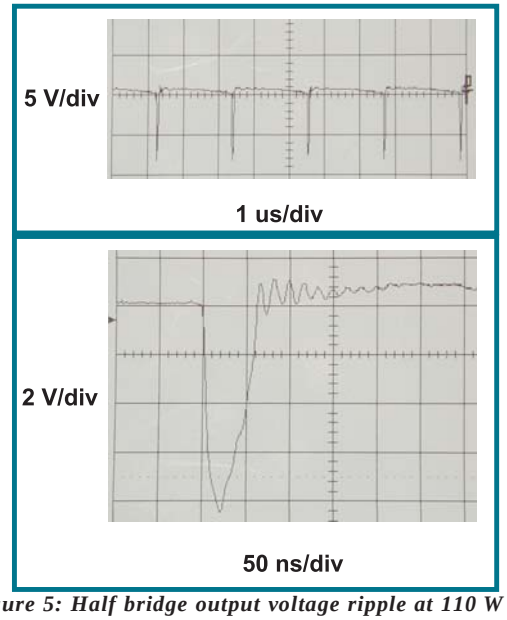

Figure 5: Half bridge output voltage ripple at 110 W load

Notwithstanding these shortcomings, which can reasonably be overcome with additional components, the half-bridge power stage is a remarkable achievement in terms of density and efficiency. It shows clearly why many systems designers are looking at the distributed bus architecture to take advantage of this kind of power technology.

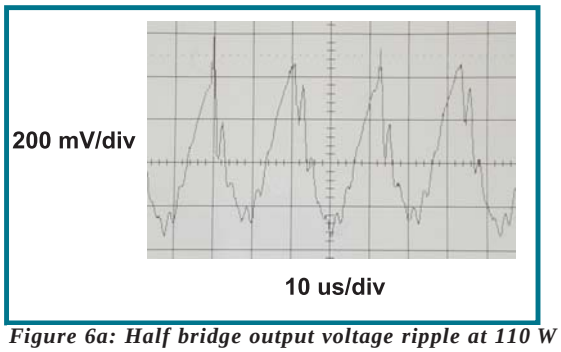

Figure 6a: Half bridge output voltage ripple at 110 W

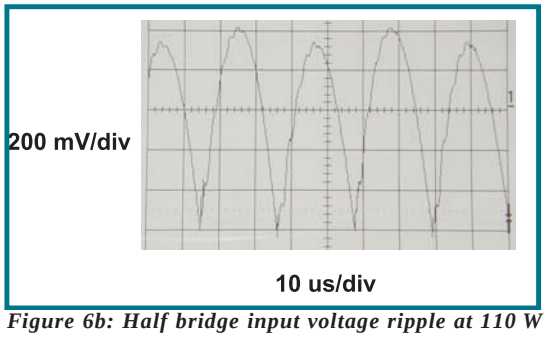

Figure 6b: Half bridge input voltage ripple at 110 W load

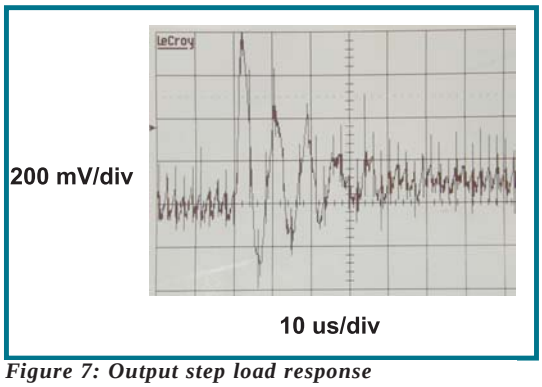

Figure 7: Output step load response

Is the Half Bridge the Ideal High-Density Topology?

Given this extraordinary power density, should every power design use the half-bridge converter? Well, it's not quite that easy. First, the power supply described is unregulated. Another power stage must be built to provide the regulation ahead of the half bridge. restoring the need for a large inductor. A regulated stage is not too hard to build with high density if it does not need isolation. With the falling prices of outstanding FETs in innovative packages, a two-stage conversion approach is definitely not unreasonable.

For offline approaches, also, a two-stage approach may be reasonable in some systems, although once you reintroduce a power transformer into the regulation stage, the advantages are less obvious. But you should by all means give it some consideration for your custom power design. Some applications fit very neatly into this architecture-especially if you need multiple outputs with moderate regulation distributed throughout your system.

What if we want to save parts, and revert back to a regulated converter? Is the half-bridge a better choice than a forward converter, based upon the results above? The following issues must be taken into consideration in making trade-offs:

1. The output inductor becomes much larger once the half-bridge has to regulate.
2. A self-driven secondary is very complex for the three-states needed for a regulated half-bridge.
3. The half-bridge converter does not work well with current-mode control. Additional circuitry must be added to balance the input voltage on the divider capacitors
4. At higher voltages, shoot-through is an issue in the half-bridge. A gate drive transformer is the best way to provide immunity.
5. During start-up, there will be asymmetry in the primary voltage drives as the divider capacitors adjust to split the input voltage. This will place additional stress on the secondary rectifiers.

When these considerations are balanced with the advantages that can be obtained in the transformer at high frequency, the forward and half bridge converters are fairly evenly matched. The choice will depend upon your particular application, but there is no single correct solution. Industry standard rules for topology selection are changing to take advantage of the latest components, and you should not just be blindly choosing topologies that have worked well for you in the past.

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- Inductor Design
- Transformer Design
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Afternoon Lab
- Design and Build Flyback Transformer
- Design and Build Forward Transformer
- Design and Build Forward Inductor
- Magnetics Characterization
- Snubber Design
- Flyback and Forward Circuit Testing

Day 2

Morning Theory
- Small Signal Analysis of Power Stages
- CCM and DCM Operation
- Converter Characteristics
- Voltage-Mode Control
- Closed-Loop Design with Power 4-5-6

Afternoon Lab
- Measuring Power Stage Transfer Functions
- Compensation Design
- Loop Gain Measurement
- Closed Loop Performance

Day 3

Morning Theory
- Current-Mode Control
- Circuit Implementation
- Modeling of Current Mode
- Problems with Current Mode
- Closed-Loop Design for Current Mode w/Power 4-5-6

Afternoon Lab
- Closing the Current Loop
- New Power Stage Transfer Functions
- Closing the Voltage Compensation Loop
- Loop Gain Design and Measurement

Day 4

Morning Theory
- Multiple Output Converters
- Magnetics Proximity Loss
- Magnetics Winding Layout
- Second Stage Filter Design

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