

# Compal confidential

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_PM+ICH9-M core logic

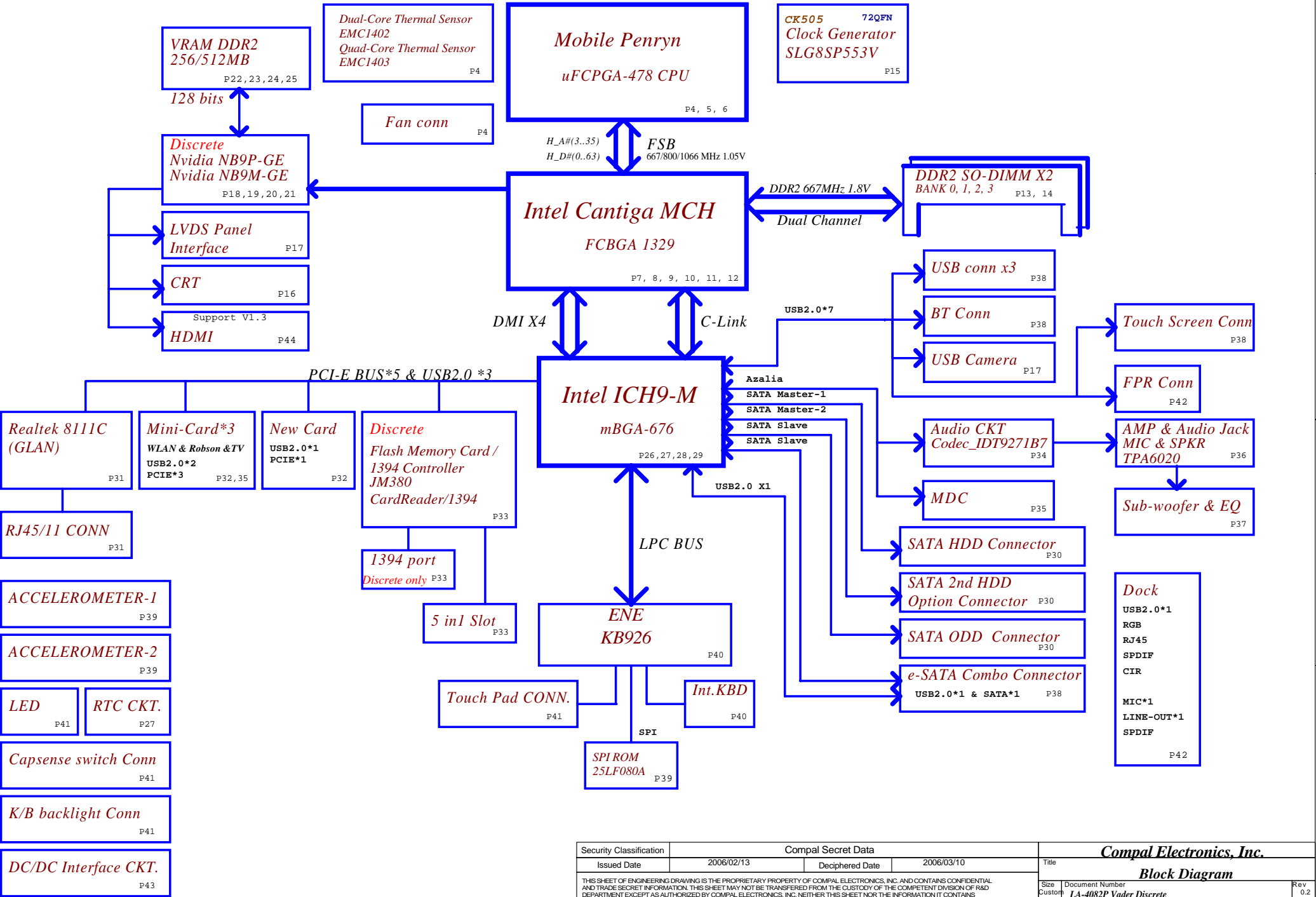
LA-4082P Vader Discrete (NB9P-GS,NB9M-GE)

2007-12-26 Rev 0.4

機 等 密	硬體二部	
	產出人員	
	產出日期	
	解密日期	

Security Classification		Compal Secret Data		Title		
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Montevina Consumer Discrete



power plane  State				+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE  +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
	+B	+5VALW  +3VALW	+1.8V	
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

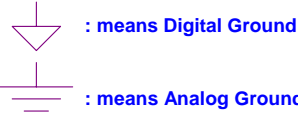
SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
DDC2_CLK DDC2_DATA	NB9M	X	X	X	X	X	X	X	V	X

USB assignment:  
USB-0 Right side  
USB-1 Right side  
USB-2 Left side(with ESATA)  
USB-3 Dock  
USB-4 Camera  
USB-5 WLAN  
USB-6 Bluetooth  
USB-7 Finger Printer  
USB-8 MiniCard(WWAN/TV)  
USB-9 Express  
USB-10 X  
USB-11 X

PCIe assignment:  
PCIe-1 TV tuner/WWAN/Robeson  
PCIe-2 X  
PCIe-3 WLAN  
PCIe-4 New Card  
PCIe-5 Card  
PCIe-6 GLAN (Marvell)

Symbol Note :



@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

EC SM Bus1 address

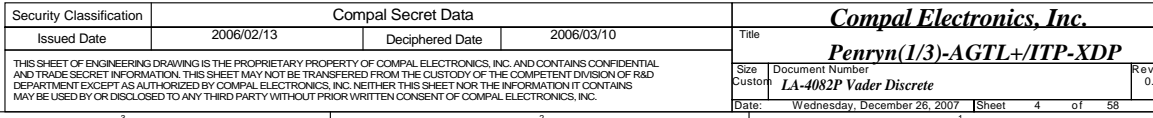
EC SM Bus2 address

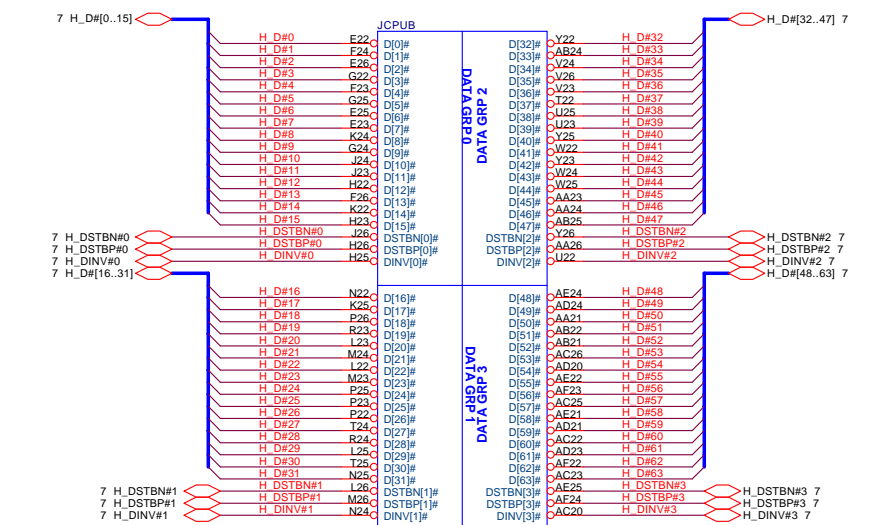
Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X	CPU EMC1402	4CH	1001 1000b
24C16	A0H	1010 000X	VGA	4DH	1001 1010b
CAP BOARD – Cypress	38H				
CAP BOARD – ST	b0H				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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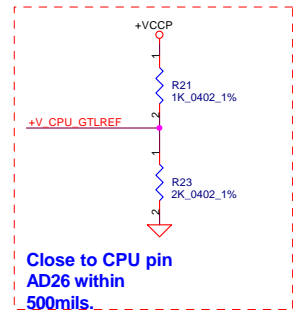




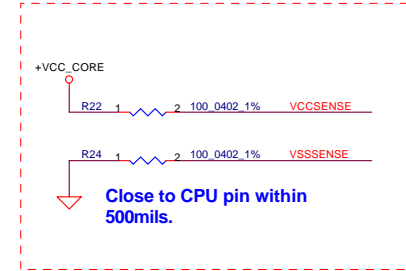
\* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

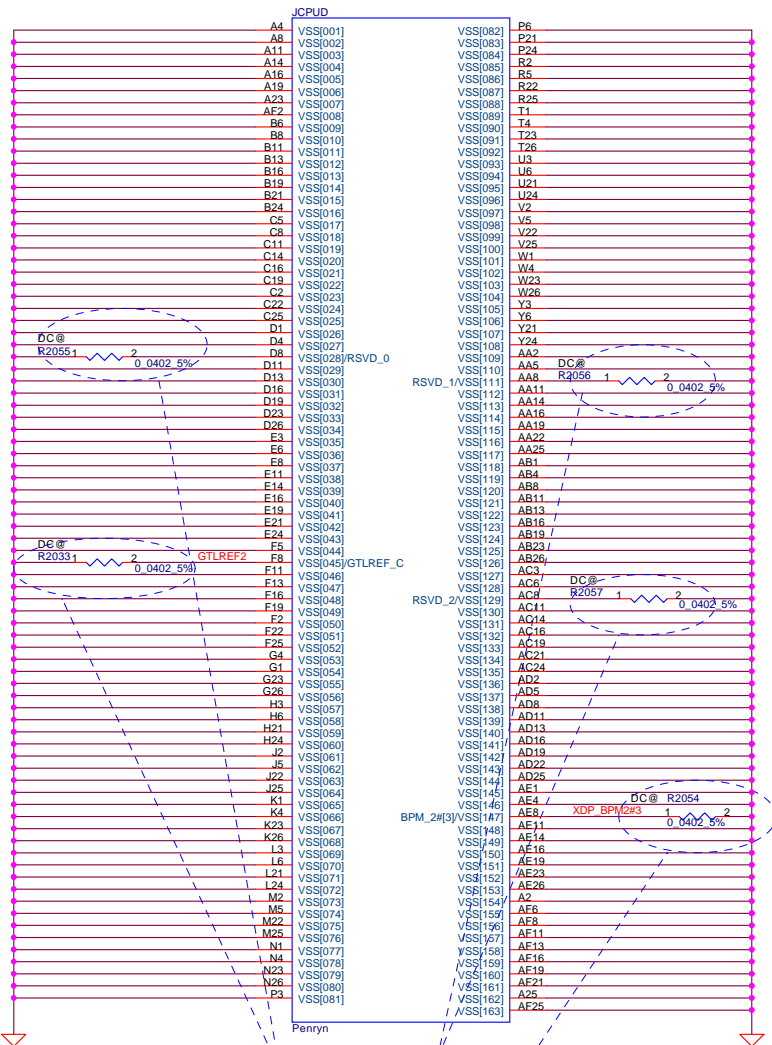
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

1025 For Support Dual core and Quad core



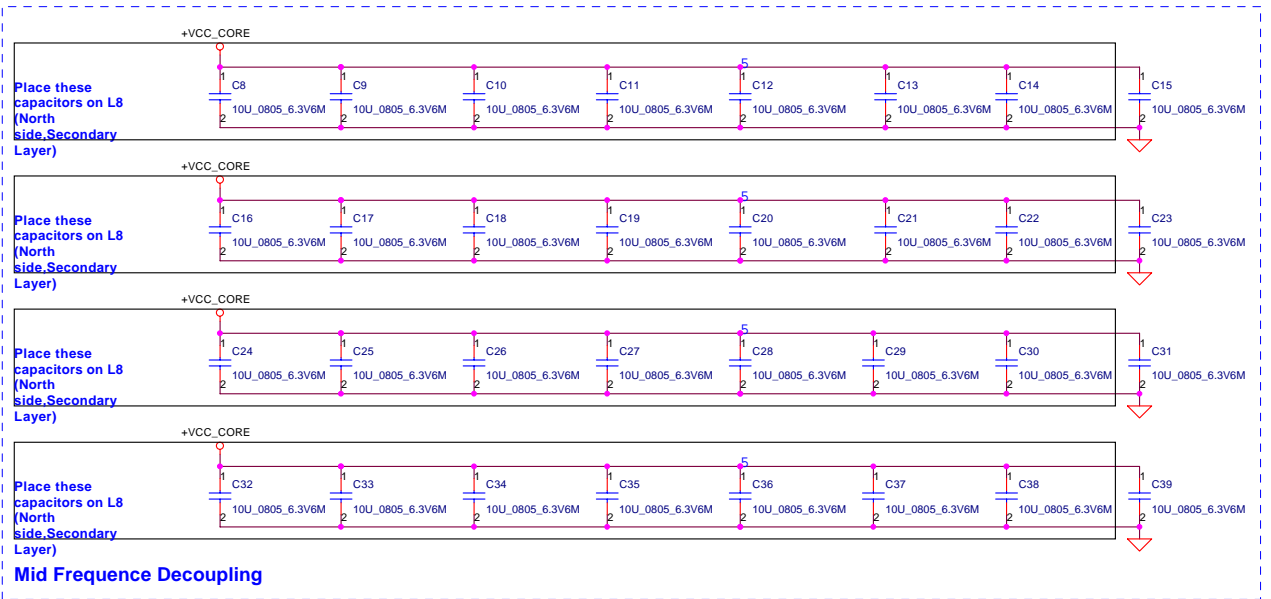
Length match within 25 mils. The trace width/space/other is 20/7/25.



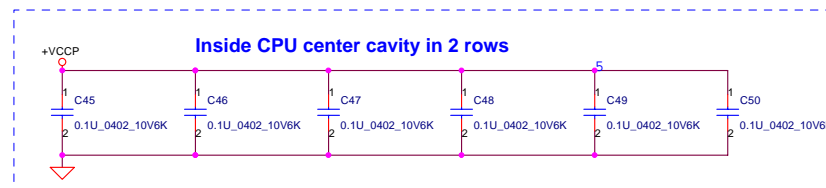
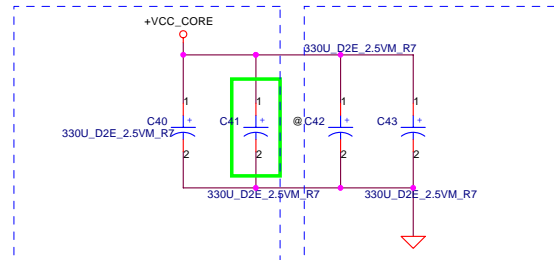


1025 For Support Dual core and Quad core

GTLREF2 → GTLREF2 4  
XDP\_BPM2#3 → XDP\_BPM2#3 4

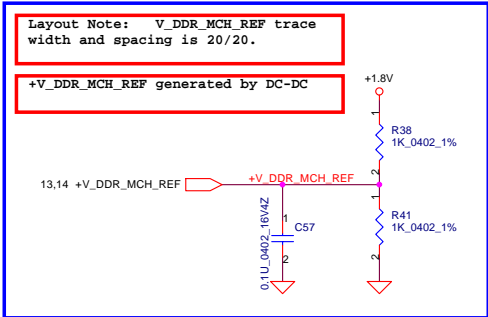


**Near CPU CORE regulator**  
ESR <= 1.5m ohm  
Capacitor > 1980uF



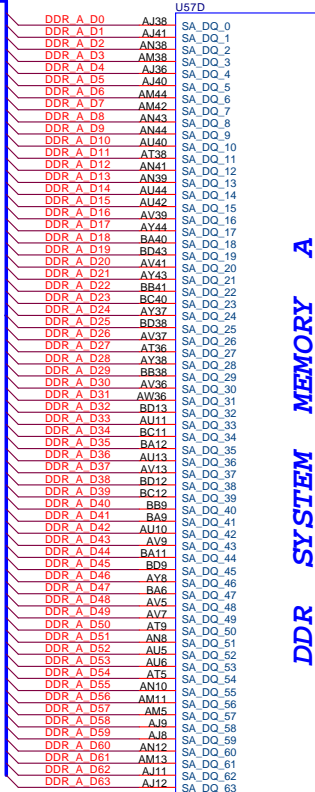
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13 DDR\_A\_D[0..63]



DDR SYSTEM MEMORY A

CANTIGA ES\_FCBGA1329

SA\_BS\_0  
SA\_BS\_1  
SA\_BS\_2  
  
SA\_RAS#  
SA\_CAS#  
SA\_WE#

BD21 DDR A BS0  
BG18 DDR A BS1  
AT25 DDR A BS2  
  
BB20 DDR A RAS#  
BD20 DDR A CAS#  
AY20 DDR A WE#  
  
AM37 DDR A DM0  
AT41 DDR A DM1  
AY41 DDR A DM2  
AU39 DDR A DM3  
BB12 DDR A DM4  
AY6 DDR A DM5  
AT7 DDR A DM6  
AJ5 DDR A DM7

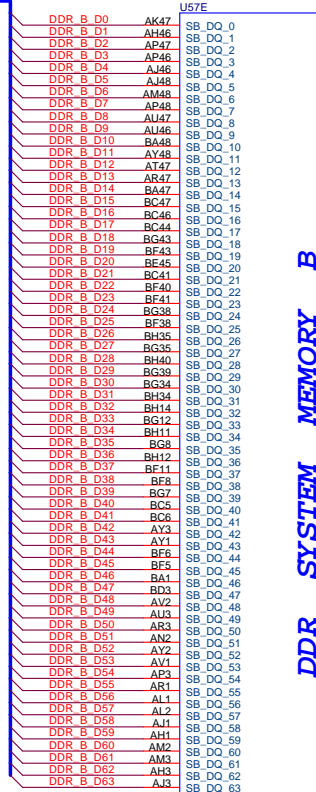
DDR\_A\_DM[0..7] 13  
  
AJ44 DDR A DQS0  
AT44 DDR A DQS1  
BA43 DDR A DQS2  
BC37 DDR A DQS3  
AW12 DDR A DQS4  
BC8 DDR A DQS5  
AJ8 DDR A DQS6  
AM7 DDR A DQS7

DDR\_A\_DQS[0..7] 13  
  
AJ43 DDR A DQS#0  
AT43 DDR A DQS#1  
BA44 DDR A DQS#2  
BD37 DDR A DQS#3  
AY12 DDR A DQS#4  
BD8 DDR A DQS#5  
AU9 DDR A DQS#6  
AM8 DDR A DQS#7

DDR\_A\_DQS[0..7] 13  
  
BA21 DDR A MA0  
BC24 DDR A MA1  
BG24 DDR A MA2  
BH24 DDR A MA3  
BG25 DDR A MA4  
BA24 DDR A MA5  
BD24 DDR A MA6  
BC27 DDR A MA7  
BF25 DDR A MA8  
AW24 DDR A MA9  
BC21 DDR A MA10  
BG26 DDR A MA11  
BH12 DDR A MA12  
BH17 DDR A MA13  
AY25 DDR A MA14

DDR\_A\_MA[0..14] 13  
  
SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

14 DDR\_B\_D[0..63]



DDR SYSTEM MEMORY B

CANTIGA ES\_FCBGA1329

SB\_BS\_0  
SB\_BS\_1  
SB\_BS\_2

BC16 DDR B BS0  
BB17 DDR B BS1  
BB33 DDR B BS2  
  
AU17 DDR B RAS#  
BC16 DDR B CAS#  
BF14 DDR B WE#

DDR\_B\_BS[0..2] 14  
  
DDR\_B\_RAS# 14  
DDR\_B\_CAS# 14  
DDR\_B\_WE# 14

AM47 DDR B DM0  
AY47 DDR B DM1  
BD40 DDR B DM2  
BF35 DDR B DM3  
BG11 DDR B DM4  
BA3 DDR B DM5  
AP1 DDR B DM6  
AK2 DDR B DM7

DDR\_B\_DM[0..7] 14  
  
AL47 DDR B DQS0  
AV48 DDR B DQS1  
BG41 DDR B DQS2  
BC37 DDR B DQS3  
BH9 DDR B DQS4  
BB2 DDR B DQS5  
AU1 DDR B DQS6  
AN6 DDR B DQS7

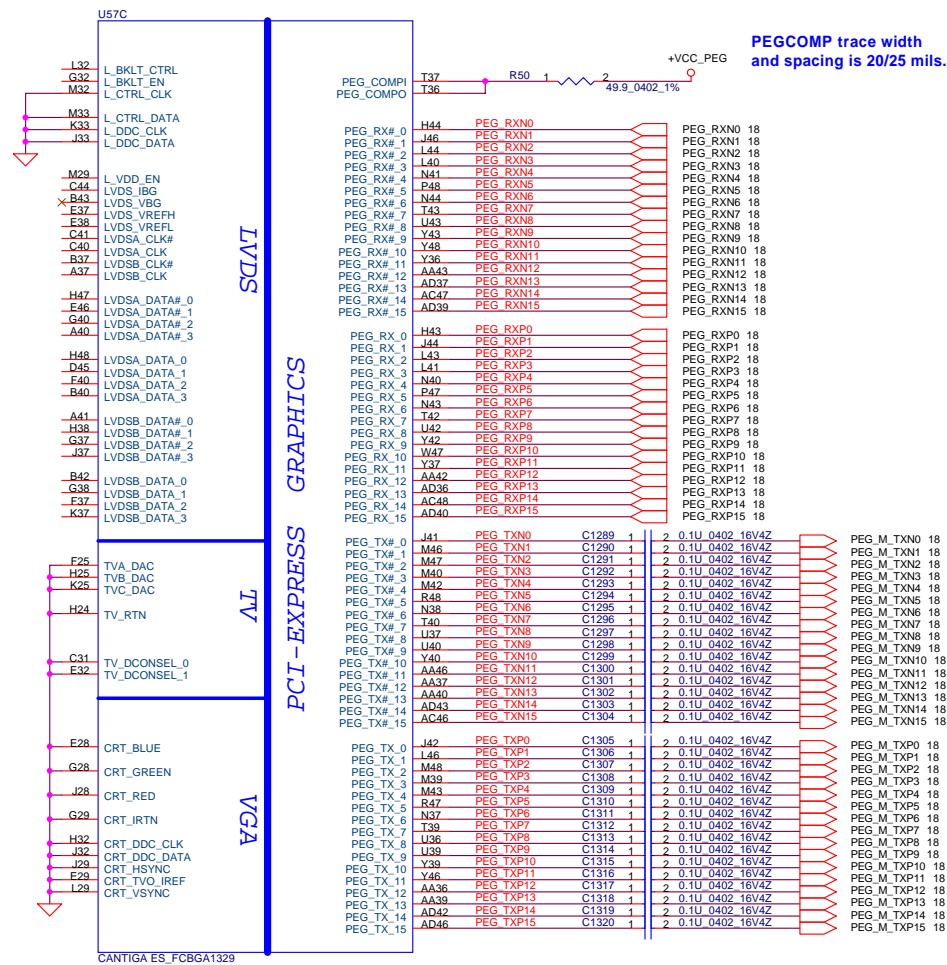
DDR\_B\_DQS[0..7] 14  
  
AL46 DDR B DQS#0  
AV47 DDR B DQS#1  
BH41 DDR B DQS#2  
BH37 DDR B DQS#3  
BG9 DDR B DQS#4  
BC2 DDR B DQS#5  
AT2 DDR B DQS#6  
AN5 DDR B DQS#7

DDR\_B\_DQS[0..7] 14  
  
AV17 DDR B MA0  
BA25 DDR B MA1  
BC25 DDR B MA2  
AU25 DDR B MA3  
AW25 DDR B MA4  
BB28 DDR B MA5  
AU28 DDR B MA6  
AT33 DDR B MA7  
BD33 DDR B MA8  
BB16 DDR B MA9  
AW33 DDR B MA10  
BH15 DDR B MA11  
AU33 DDR B MA12  
AU33 DDR B MA13  
AU33 DDR B MA14

DDR\_B\_MA[0..14] 14  
  
SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
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SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

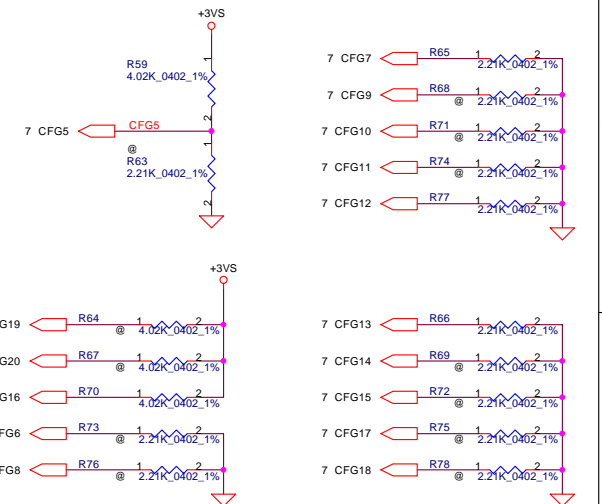
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### Strap Pin Table

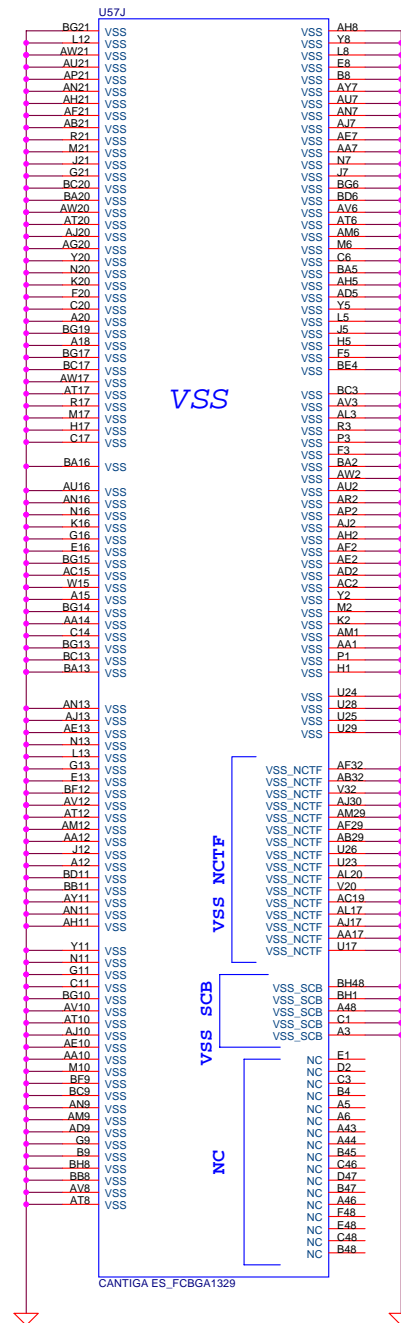
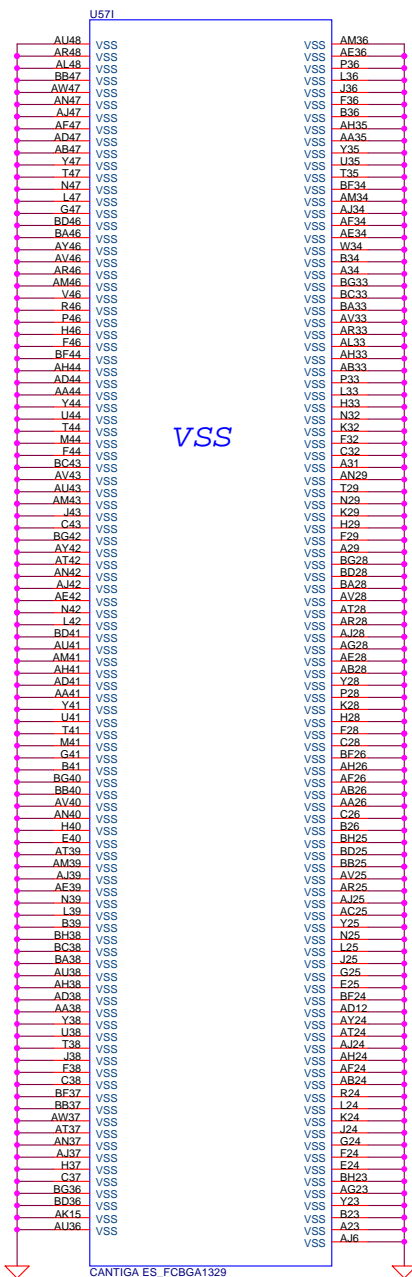
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved	Selected By CPU
CFG[4:3]	Reserved	
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *	
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *	
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *	
CFG8	Reserved	
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *	
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *	
CFG11	Reserved	
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *	
CFG[15:14]	Reserved	
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *	
CFG[18:17]	Reserved	
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse Lane *	
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *	



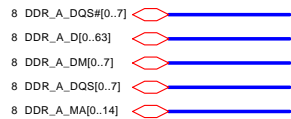
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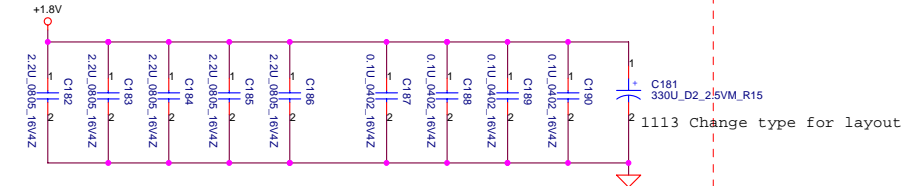




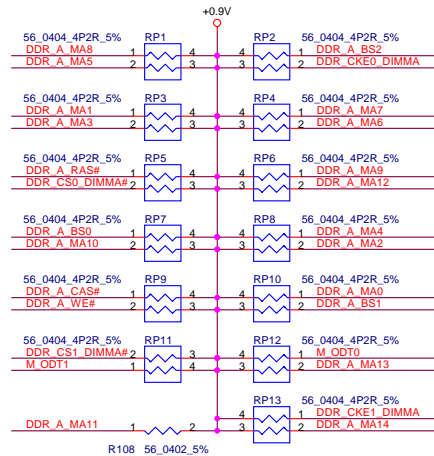
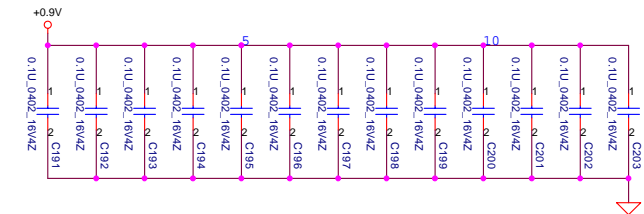
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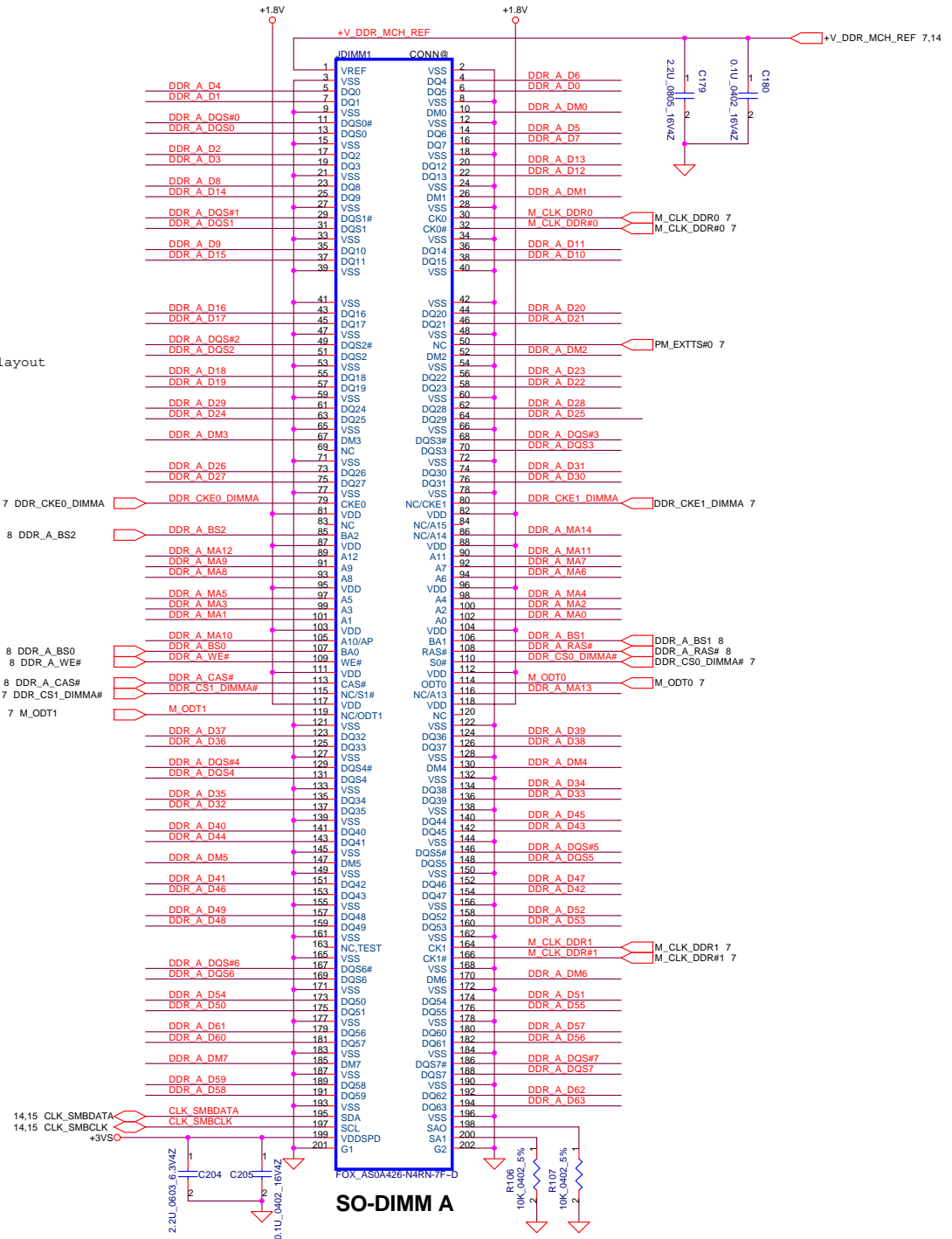
**Layout Note:**  
Place near  
JP3



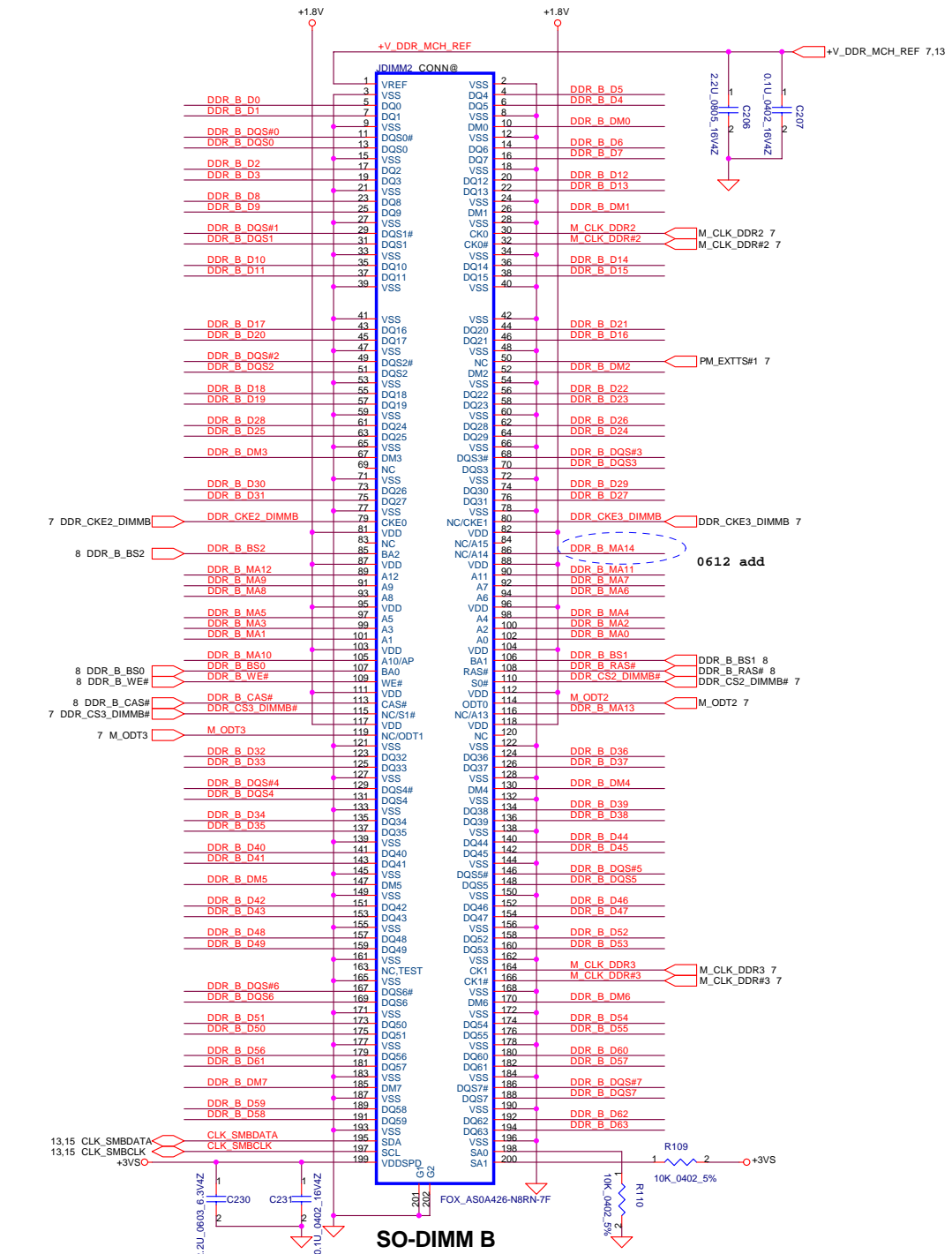
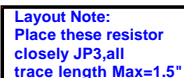
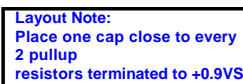
**Layout Note:**  
Place one cap close to every  
2 pullup  
resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor  
closely JP3,all  
trace length Max=1.5"



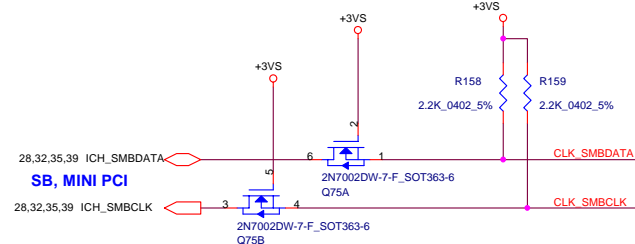
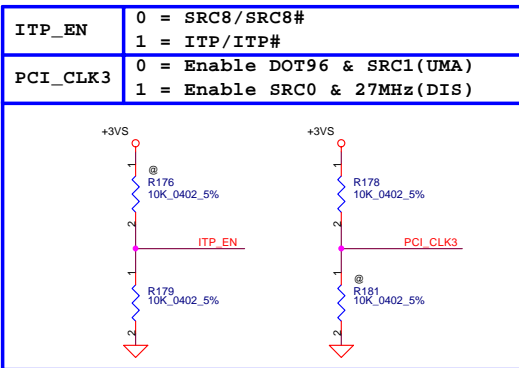
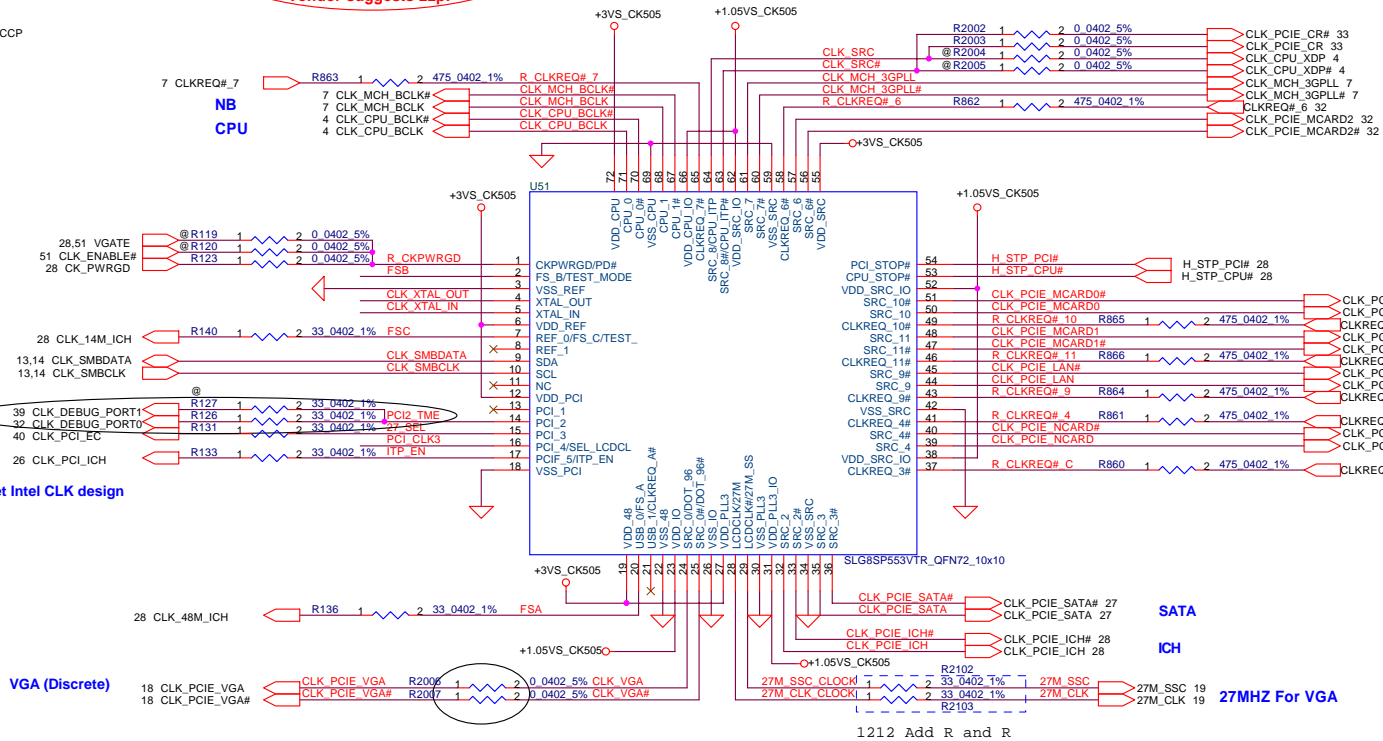
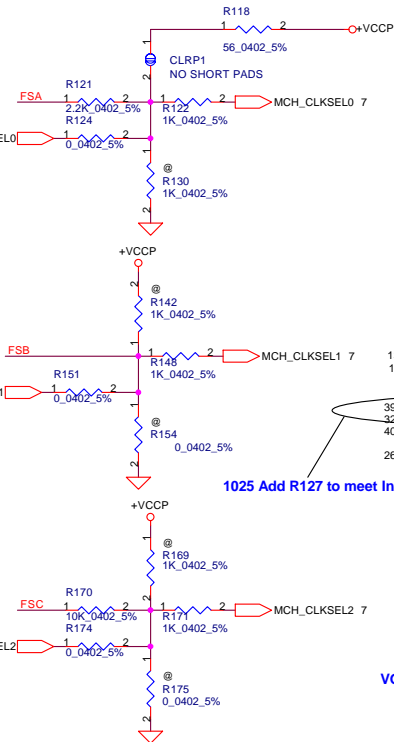
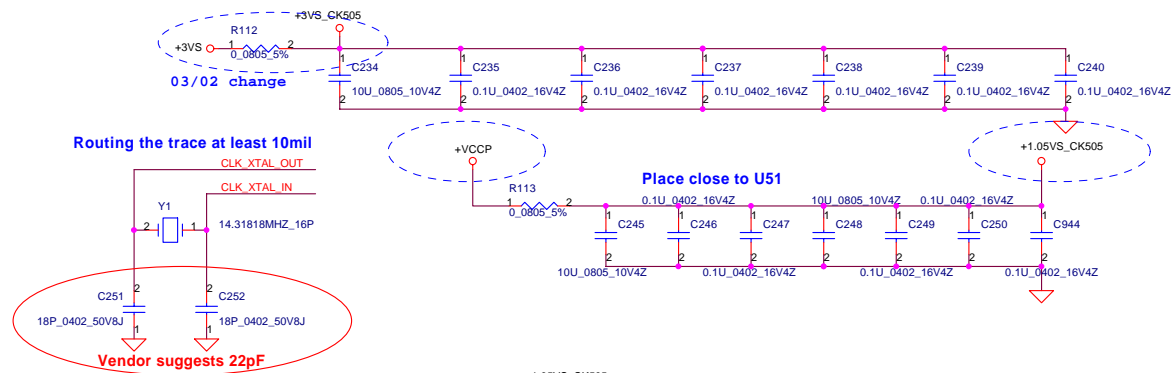
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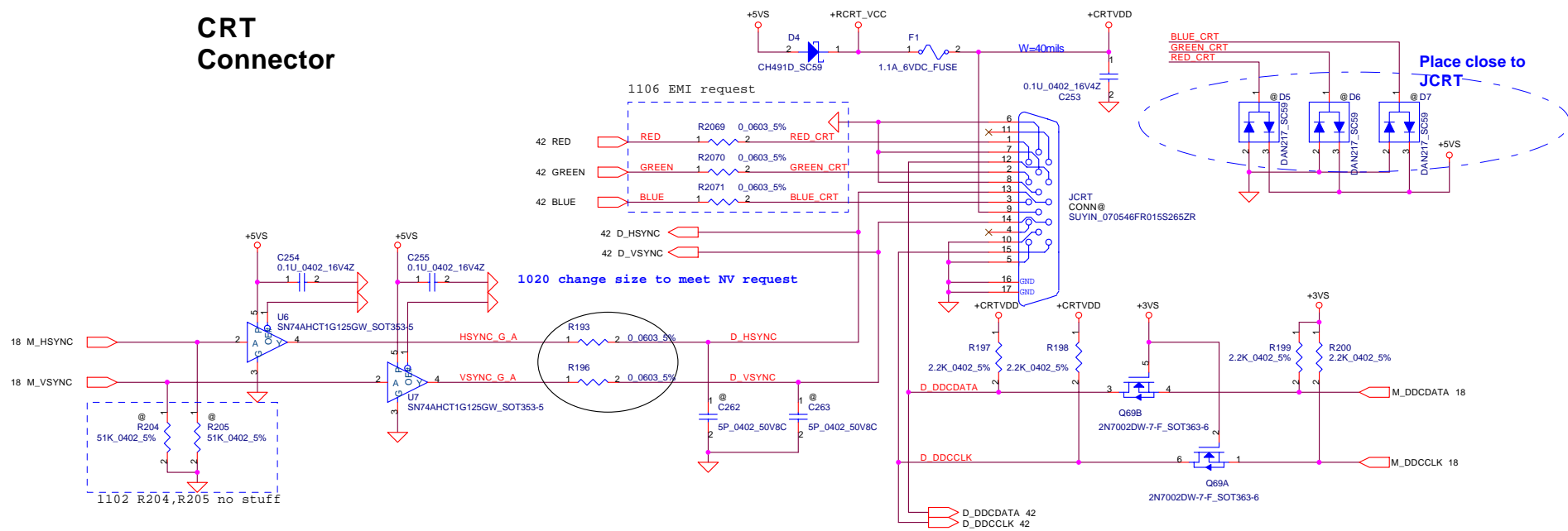
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



@C232	2	1	CLK_48M_ICH
5P_0402_50V8C			
@C233	2	1	CLK_14M_ICH
4.7P_0402_50V8C			
@C241	2	1	CLK_PCI_ICH
4.7P_0402_50V8C			
@C242	2	1	CLK_PCI_EC
4.7P_0402_50V8C			
@C243	2	1	CLK_DEBUG_PORT0
5P_0402_50V8C			

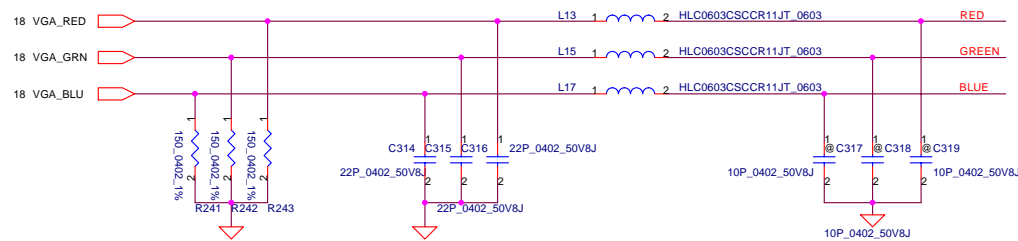
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title <i>Clock Generator CK505</i>		
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# CRT Connector

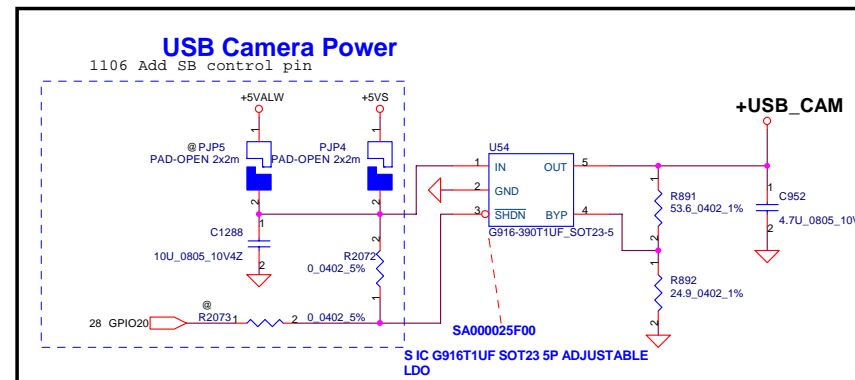
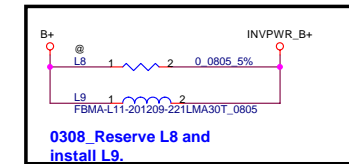
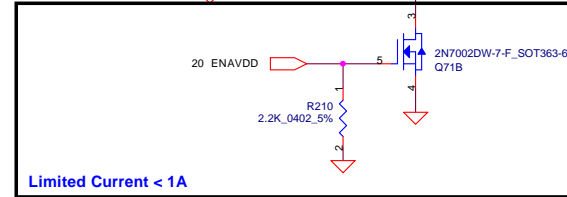
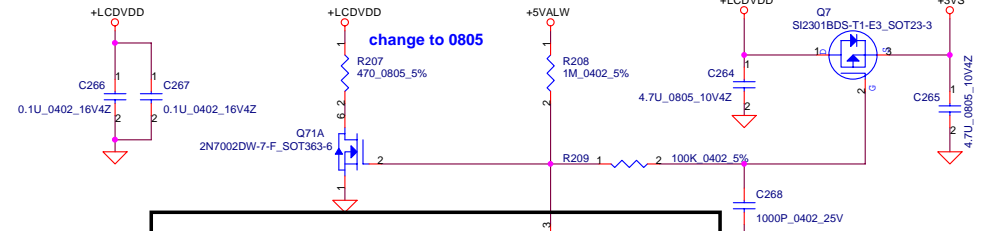
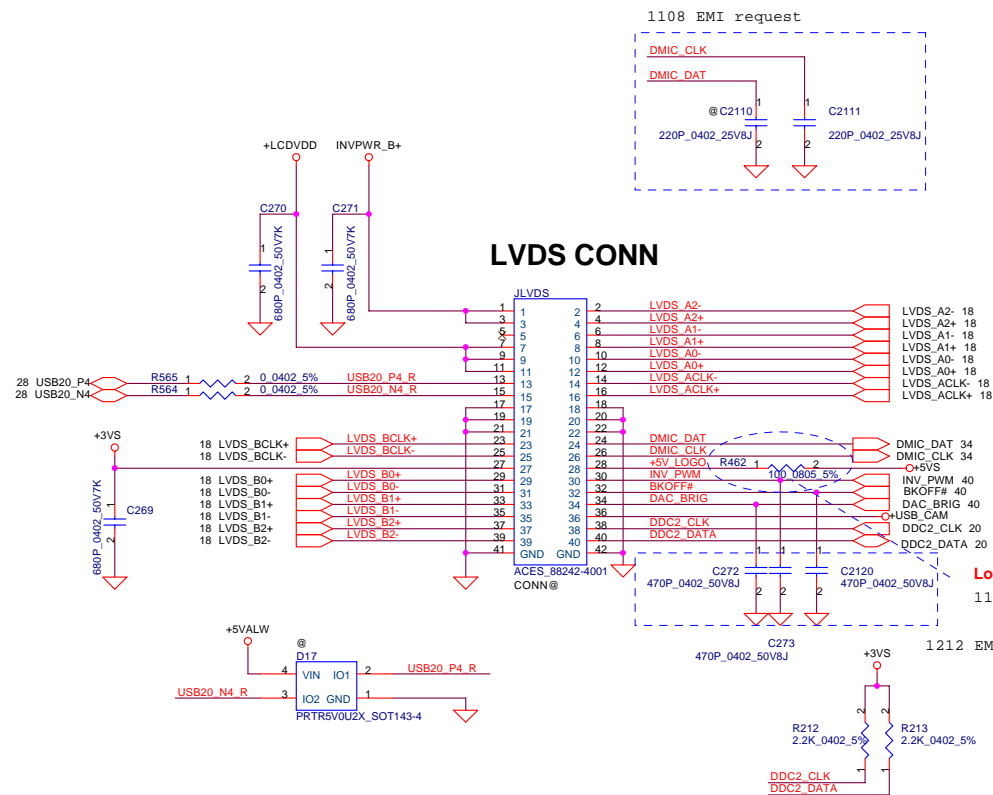


## CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

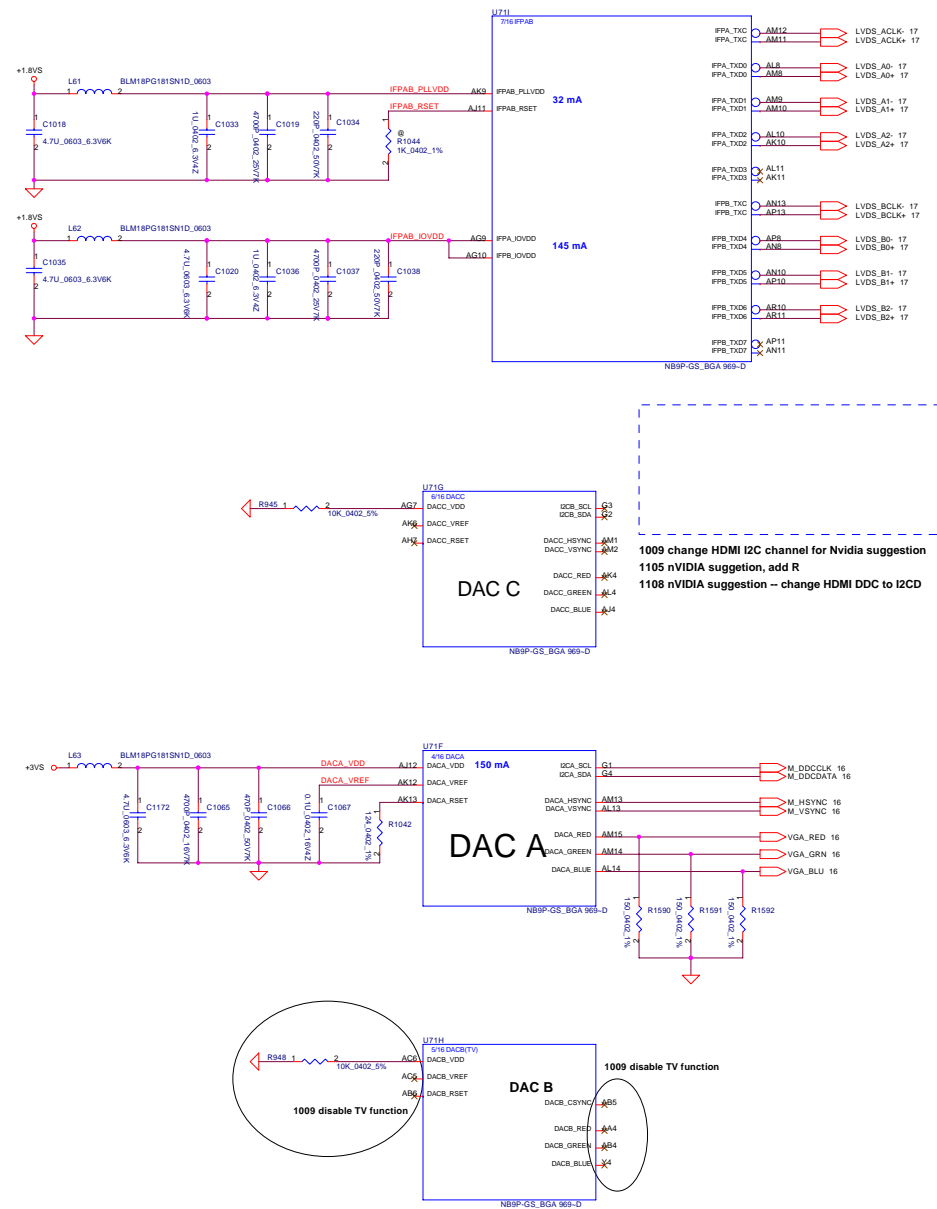


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				Custom	LA-4082P Vader Discrete
				Date	Wednesday, December 26, 2007
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				Rev	0.2

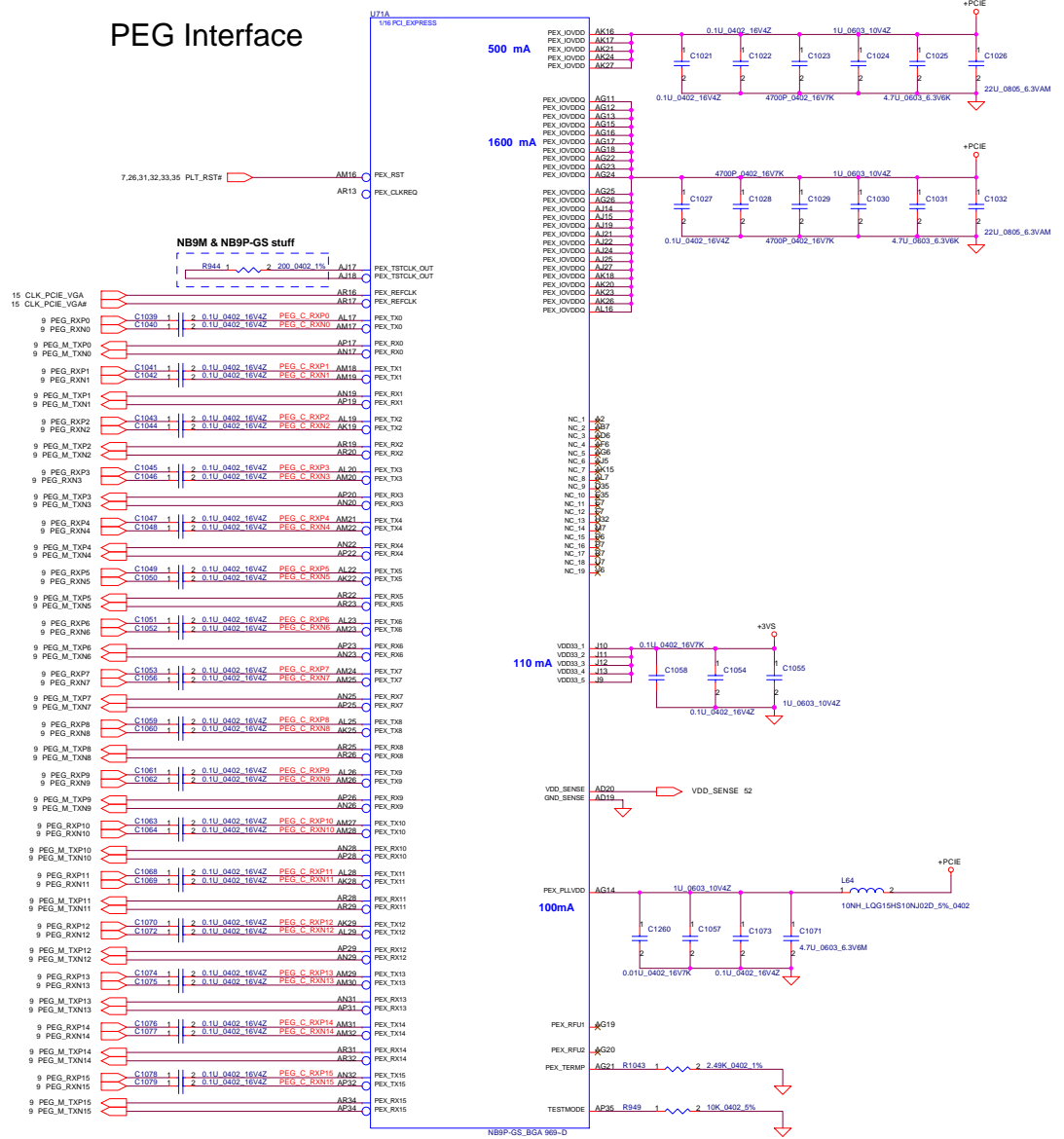


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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Size		Document Number		Rev	
Custom		LA-4082P Vader Discrete		0.2	
Date:		Wednesday, December 26, 2007		Sheet 17 of 58	

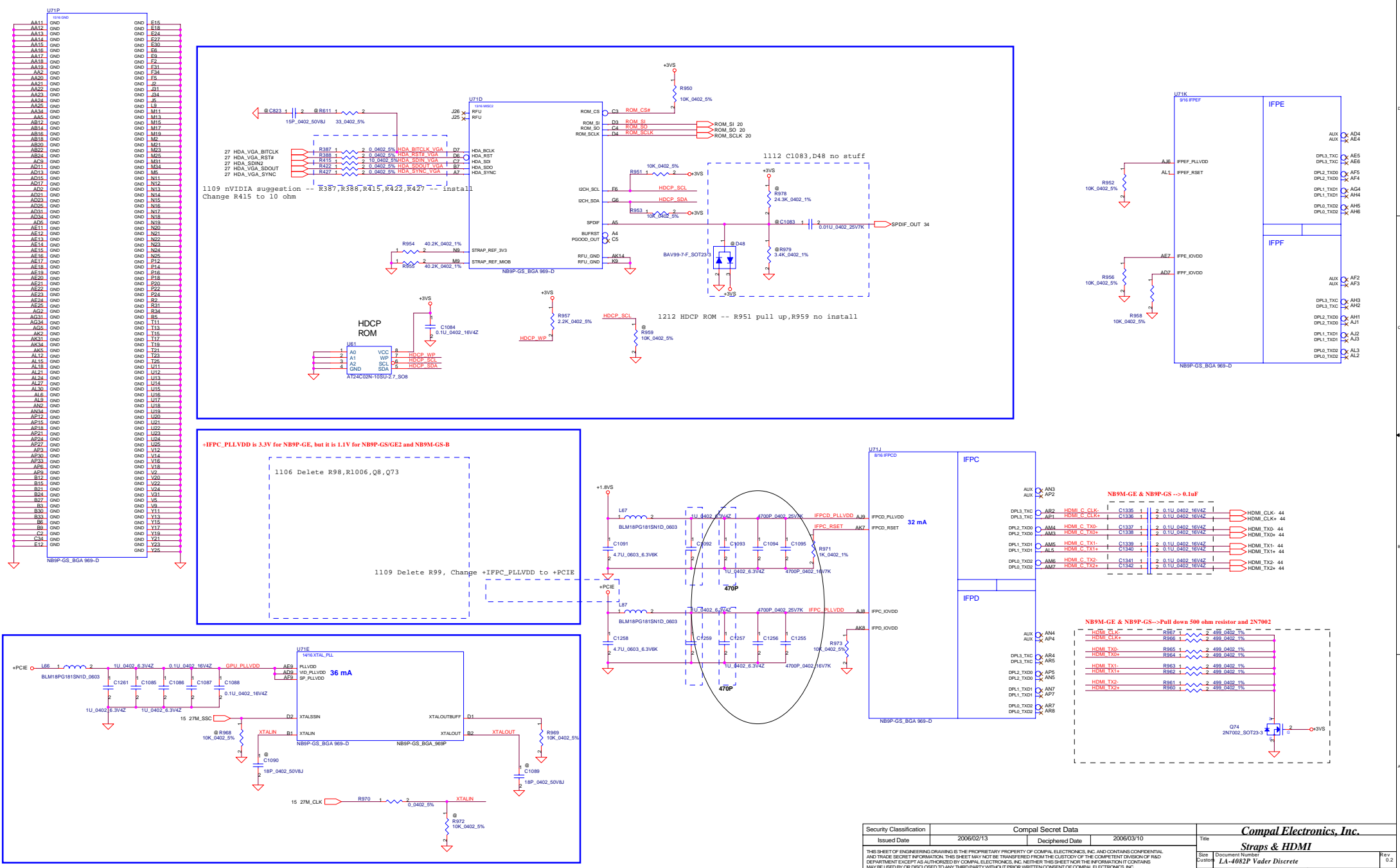
## LVDS & DAC Interface



## PEG Interface

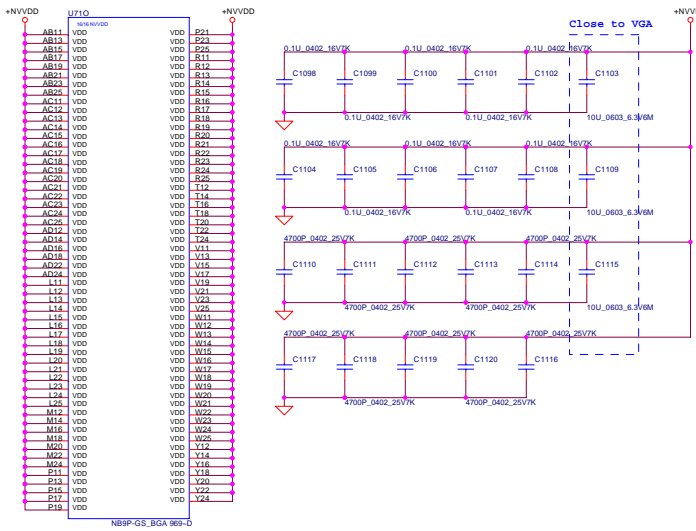


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Issued Date		Deciphered Date		Rev	
2006/02/13		2006/03/10		LA-4082P Vader Discrete	
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Sheet		18		of	
Rev		0.2			



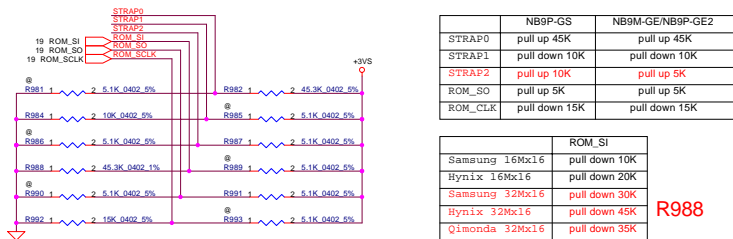
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title
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Size	Document Number	Rev	0.2	
Version	LA-4082P Vader Discrete	Date	Wednesday, December 28, 2007	Sheet 19 of 58

# VGA Core power

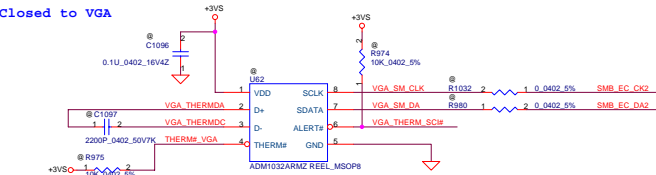


## MULTI LEVEL STRAPS For NB9M-Gx (64bit)

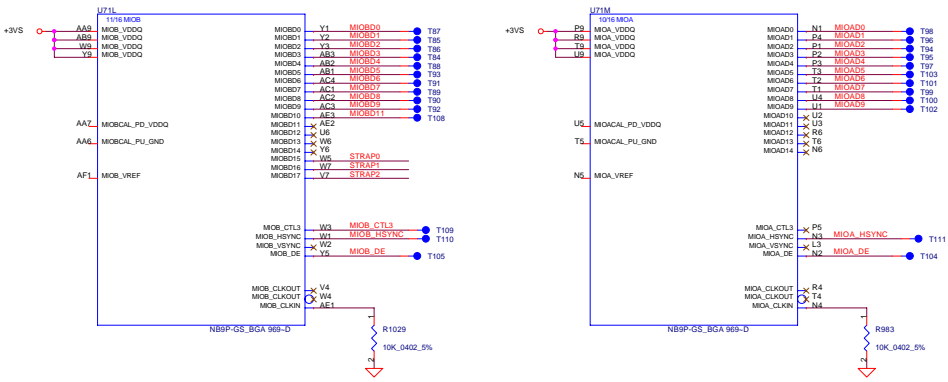
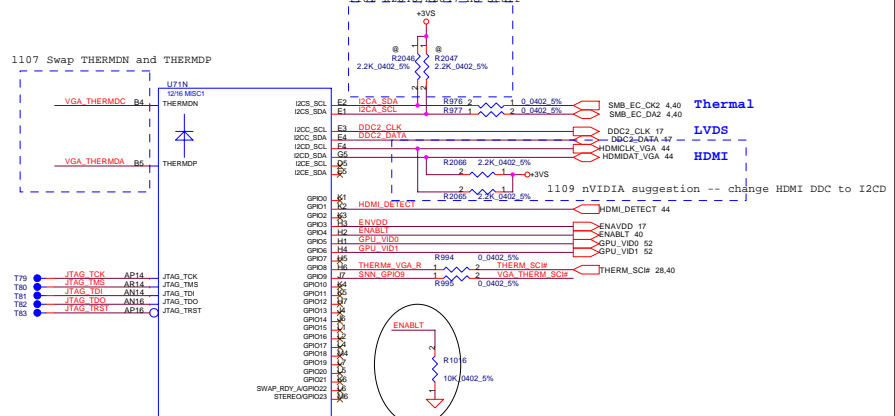
NB9P-GS and NB9P-GE2 is as same as NB9M-GE-B



## VGA Thermal Sensor ADM1032ARMZ



GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



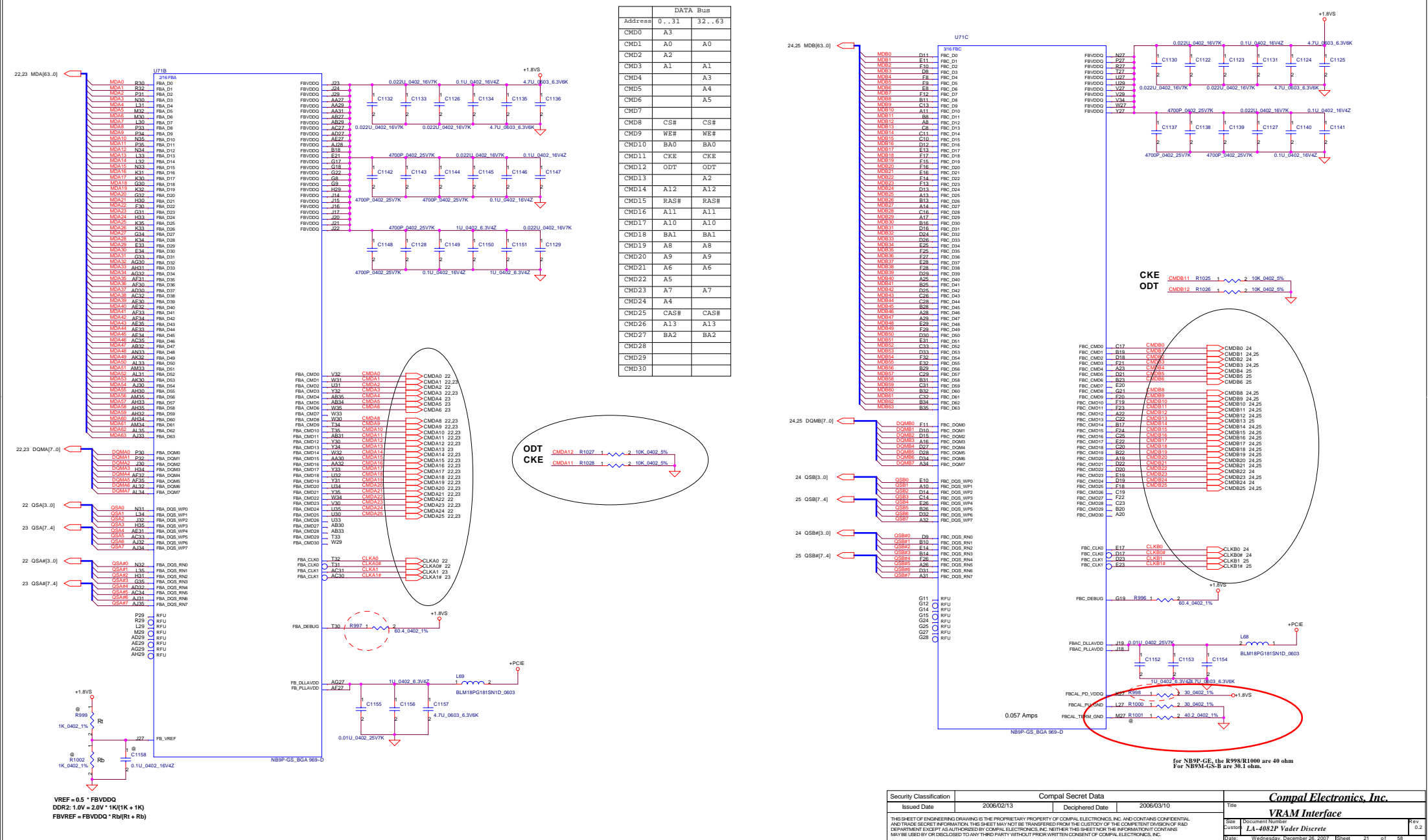
STRAP2 -- R987

R988

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Size	Document Number	Rev	0.2
Custom	LA-4082P Vader Discrete	Date	Wednesday, December 26, 2007
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## VRAM Interface



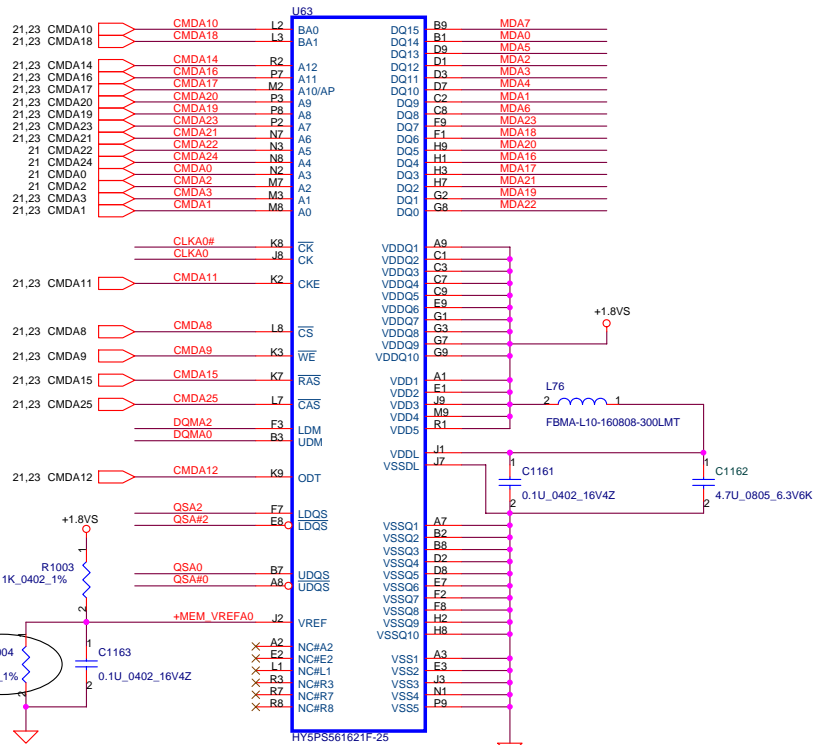
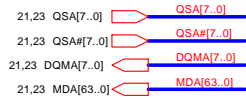
for NB9P-GE, the R998/R1000 are 40 ohm  
For NB9M-GS-B are 30.1 ohm.

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	<b>VRAM Interface</b>		
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Date	Version		Issue		Rev.	
2006/02/13	1.0		1		0.2	

# VRAM DDR2 chips (256MB & 512MB)

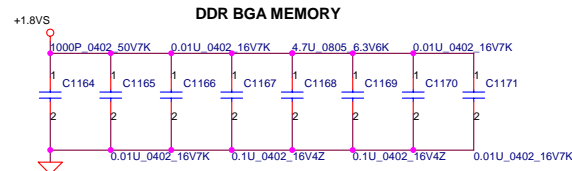
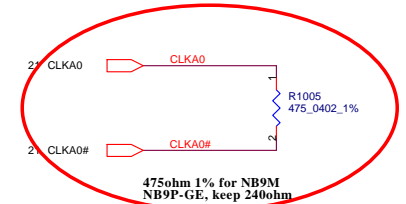
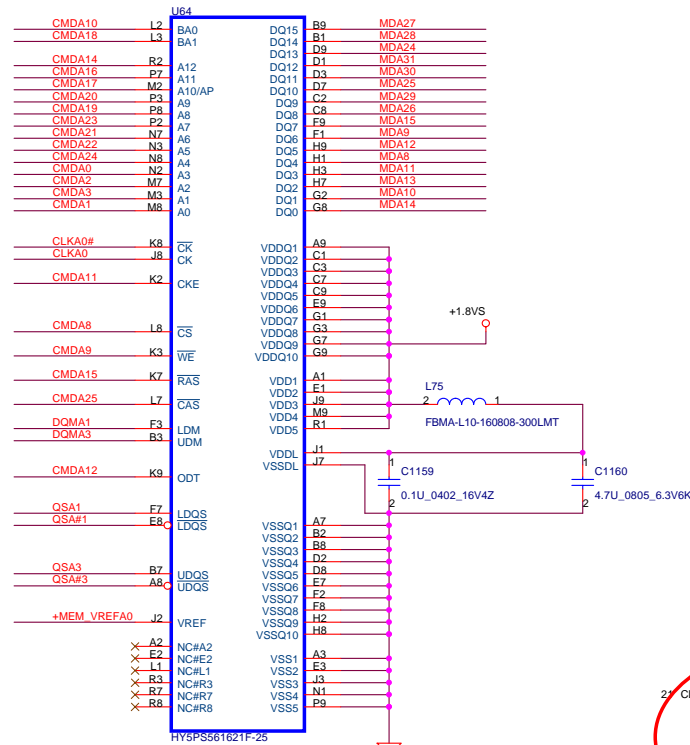
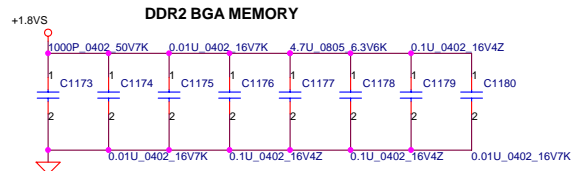
32Mx16 DDR2 400MHz \*8==>512MB

32Mx16 DDR2 400MHz \*4==>256MB



Vref= 0.5\* 1.8V for NB9M, R1004=1K ohm

Vref= 0.5\* 1.8V for NB9P-GS/GE2, R1004=1K ohm

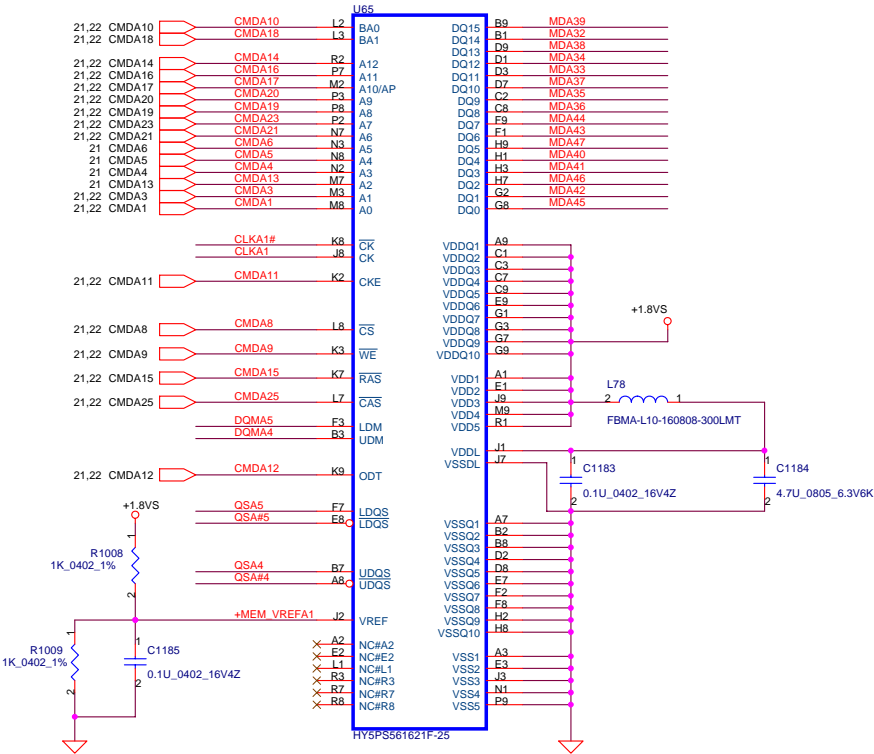
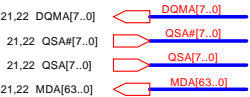


DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD28		
CMD29		
CMD30		

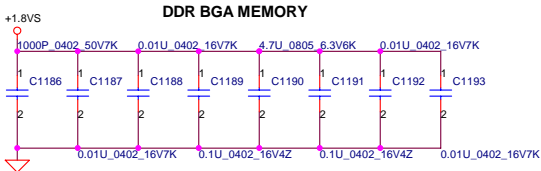
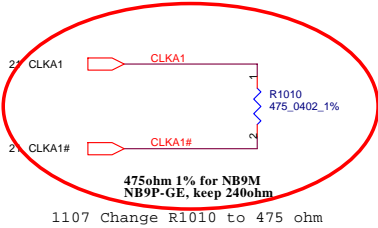
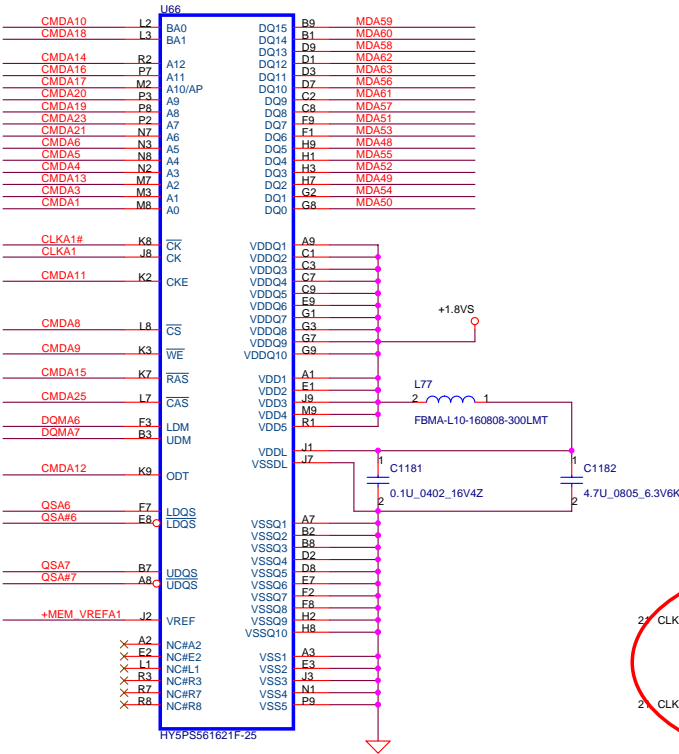
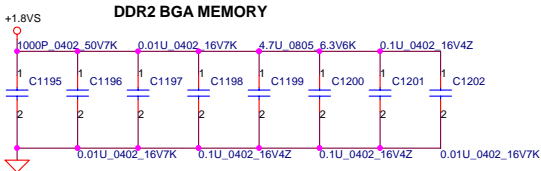
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz \*8==>512MB

32Mx16 DDR2 400MHz \*4==>256MB



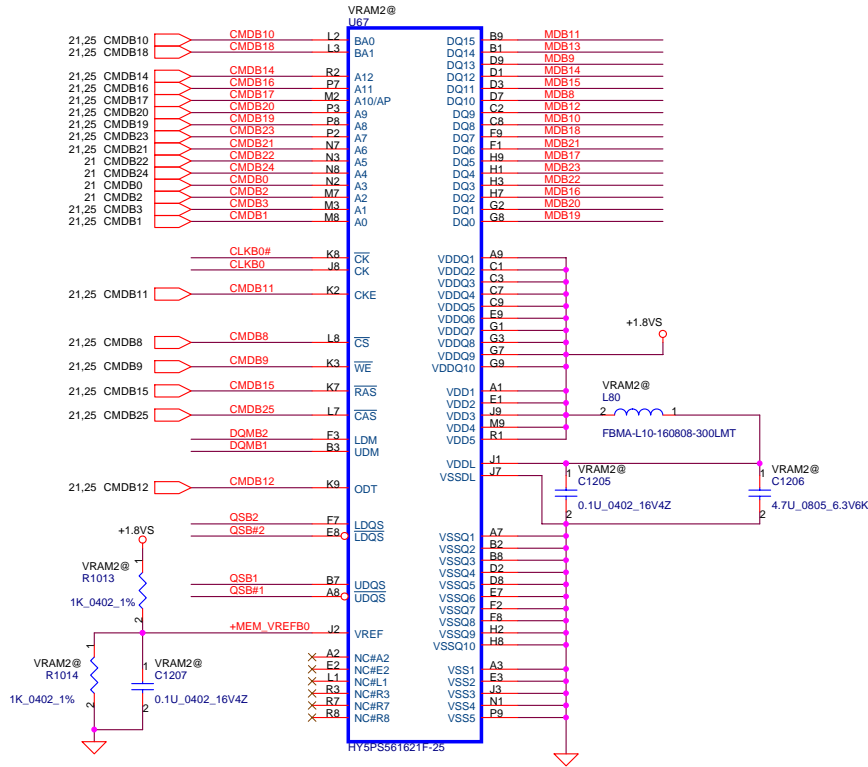
Vref= 0.5\* 1.8V for NB9M, R1009=1K ohm  
Vref= 0.5\* 1.8V for NB9P-GS/GE2, R1009=1K ohm



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

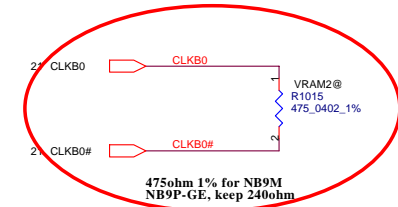
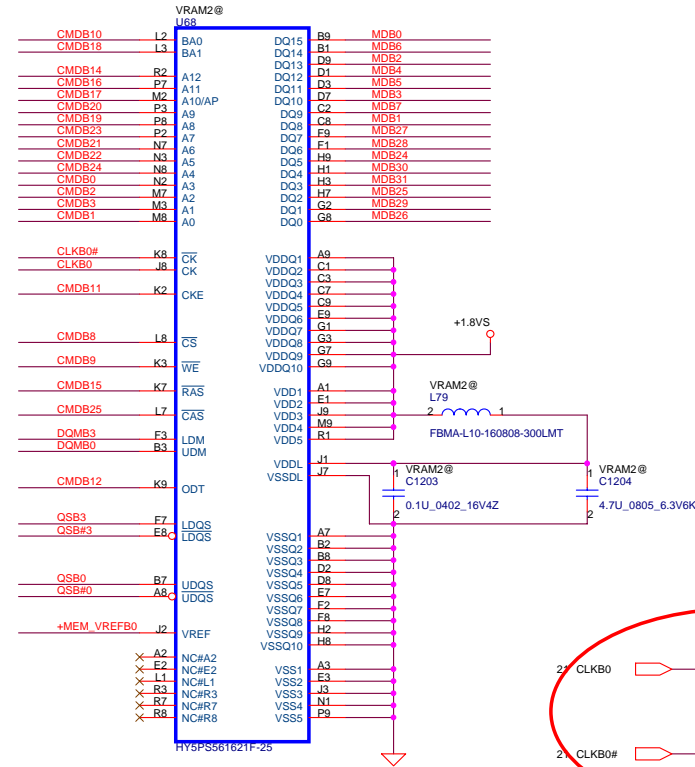
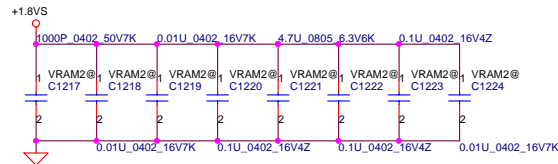
# VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz \*8==>512MB



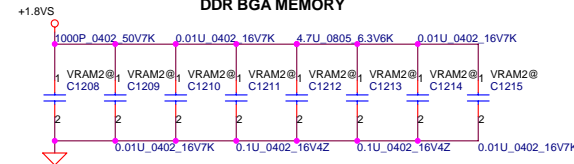
Vref= 0.5\* 1.8V for NB9M, R1014=1K ohm  
Vref= 0.5\* 1.8V for NB9P-GS/GE2, R1014=1K ohm

## DDR2 BGA MEMORY



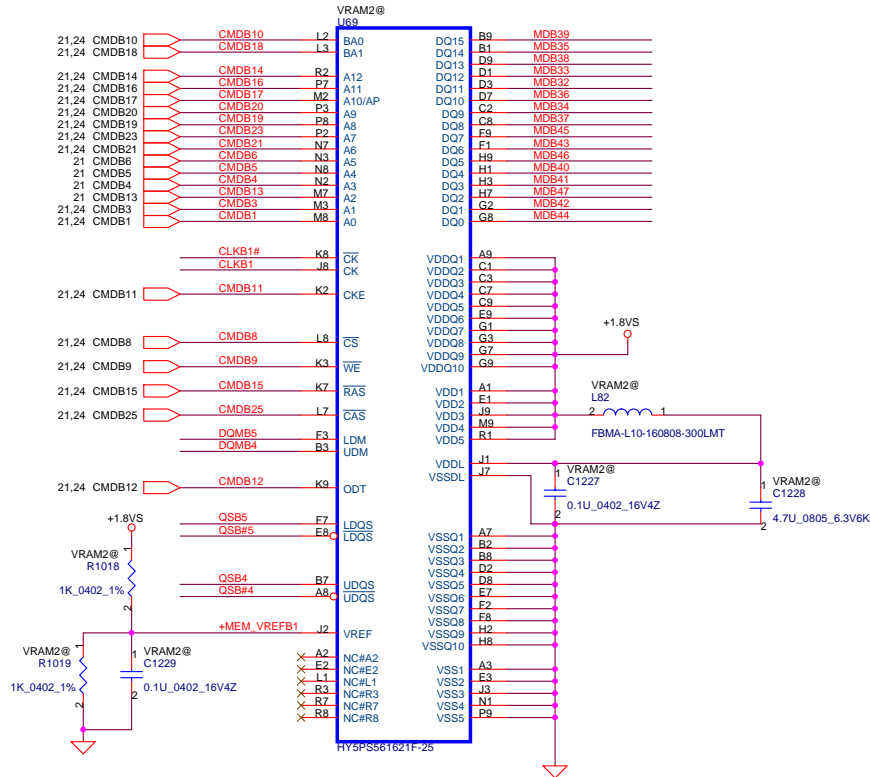
1107 Change R1015 to 475 ohm

## DDR BGA MEMORY

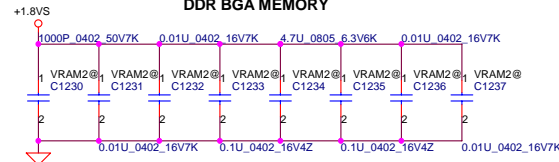
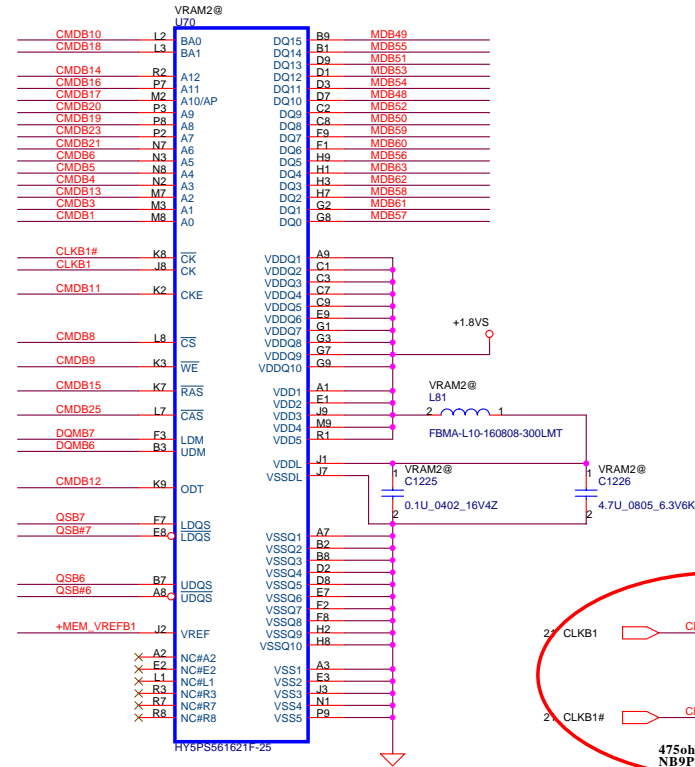


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/02/13				Title			
				Deciphered Date				LA-4082P Vader Discrete			
								Channel B EXT. 256M 1			
								Rev 0.2			
								Date: Wednesday, December 26, 2007			
								Sheet 24 of 58			

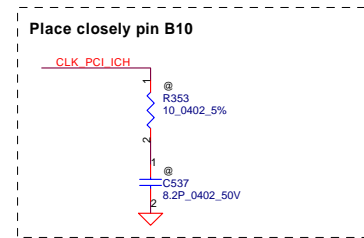
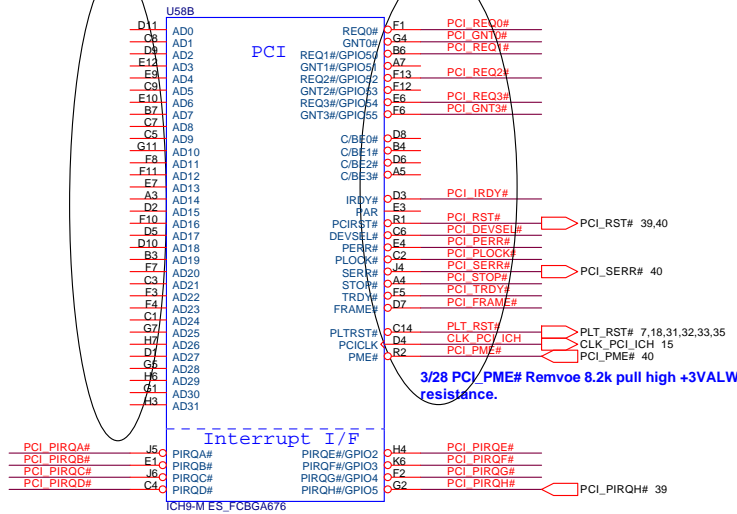
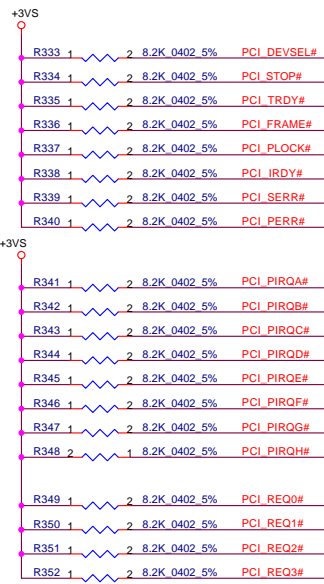
**32Mx16 DDR2 400MHz \*8==>512MB**



**Vref= 0.5\* 1.8V for NB9P-GS/GE2, R1019=1K ohm**



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				Cust	LA-4082P	Vader Discrete	0.2
				Date:	Wednesday, December 26, 2007		
				Sheet	25	of	58



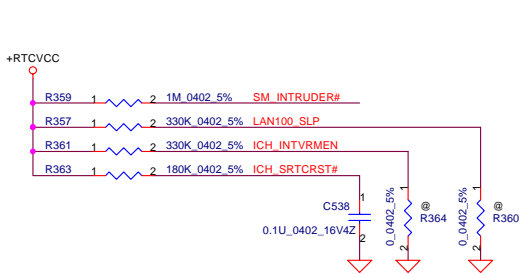
**A16 swap override Strap**

PCI_GNT3#	Low= A16 swap override Enble High= Default *
-----------	---

**Boot BIOS Strap**

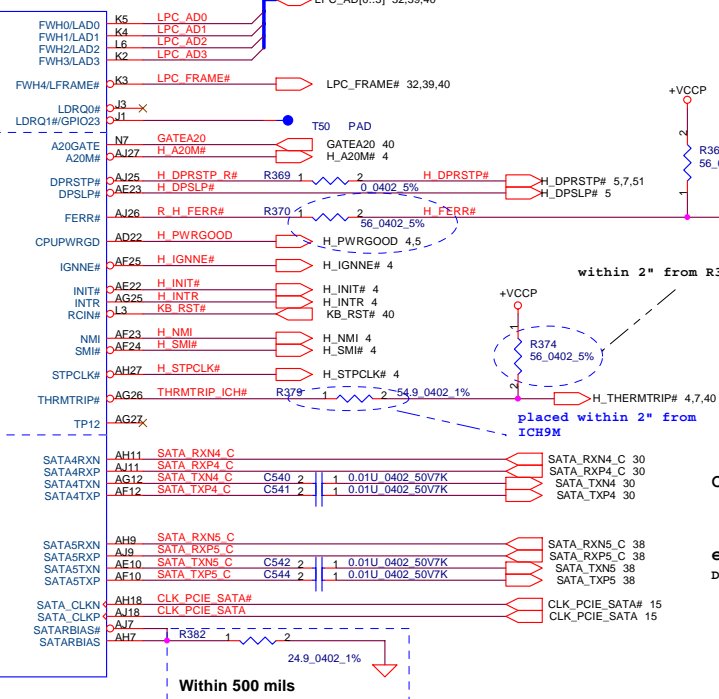
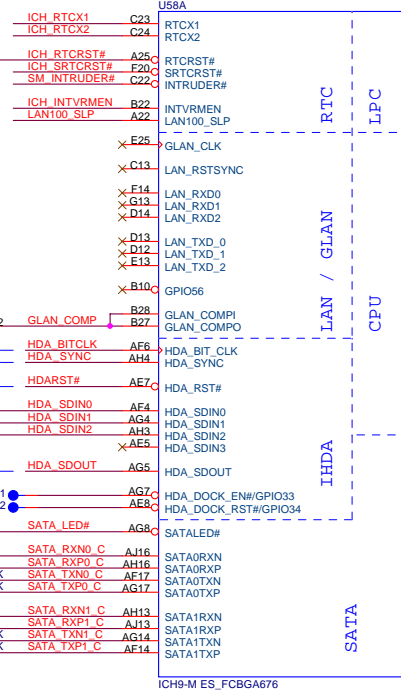
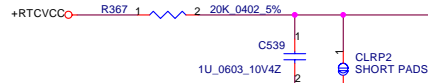
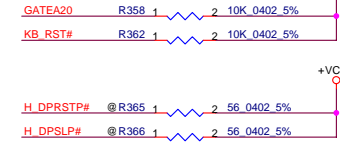
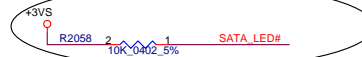
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled	High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled	High = Internal VR Enabled(Default)

1015 add pull up to meet Intel design



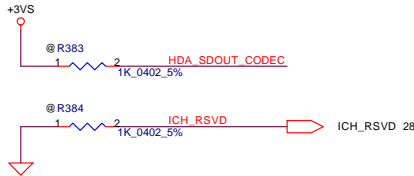
ODD

e-SATA  
De-feature disable

P- HDD  
S- HDD

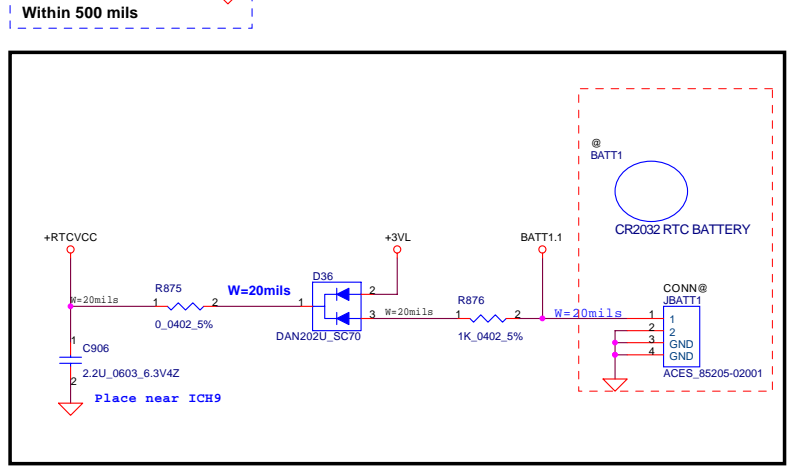
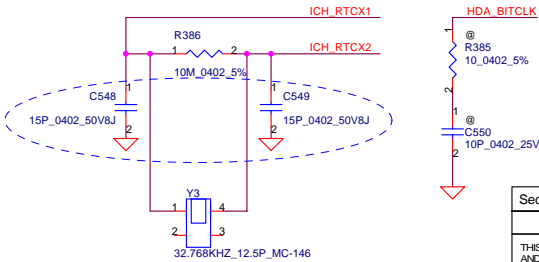
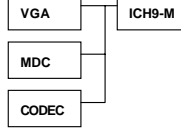
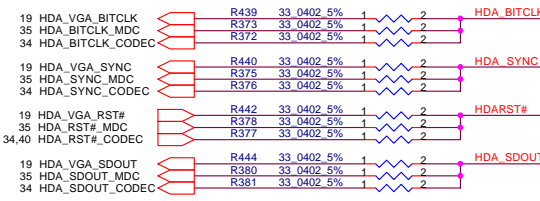
1212 Swap SATA1 and SATA4

XOR CHAIN ENTRANCE STRAP:RSVD

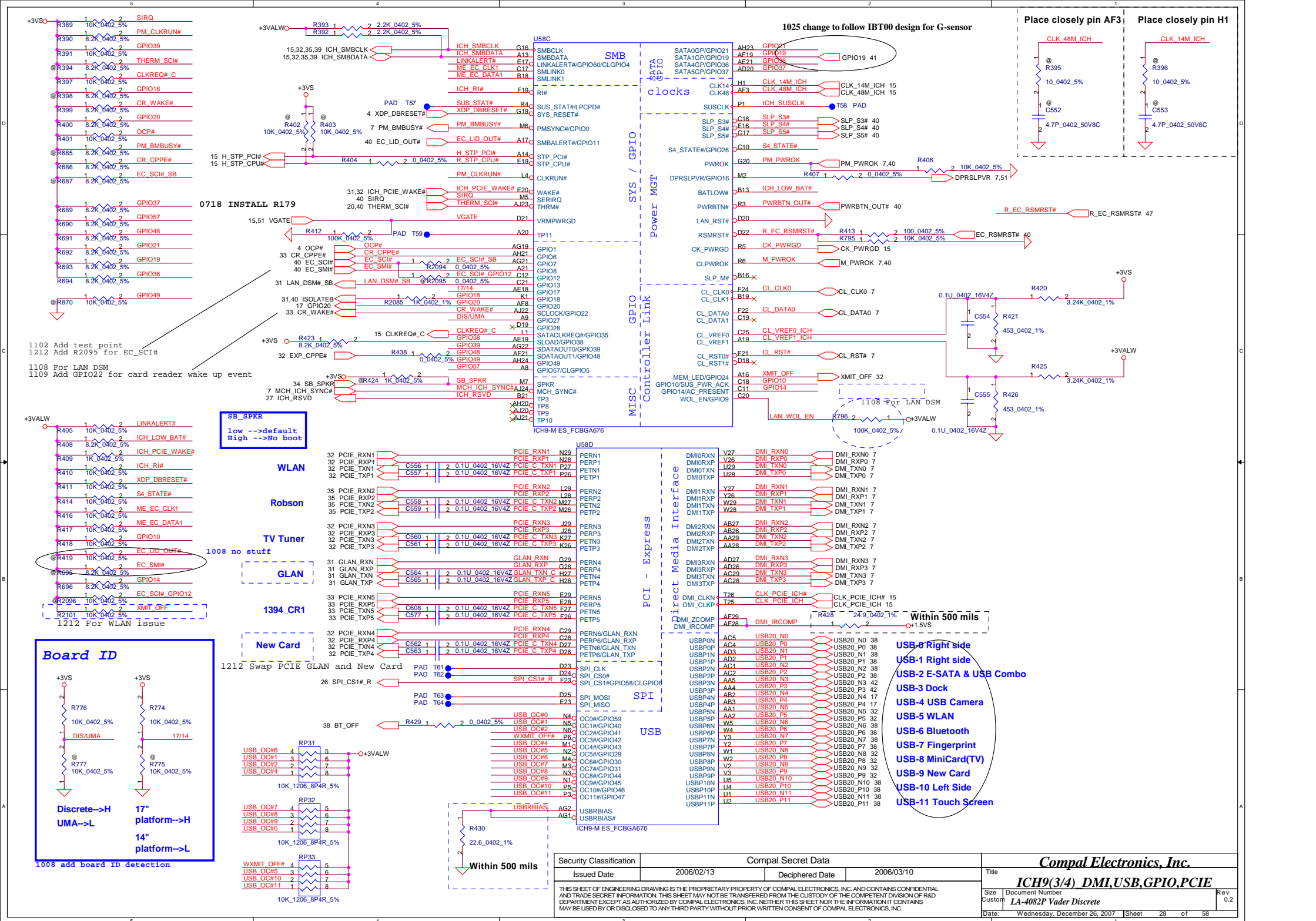


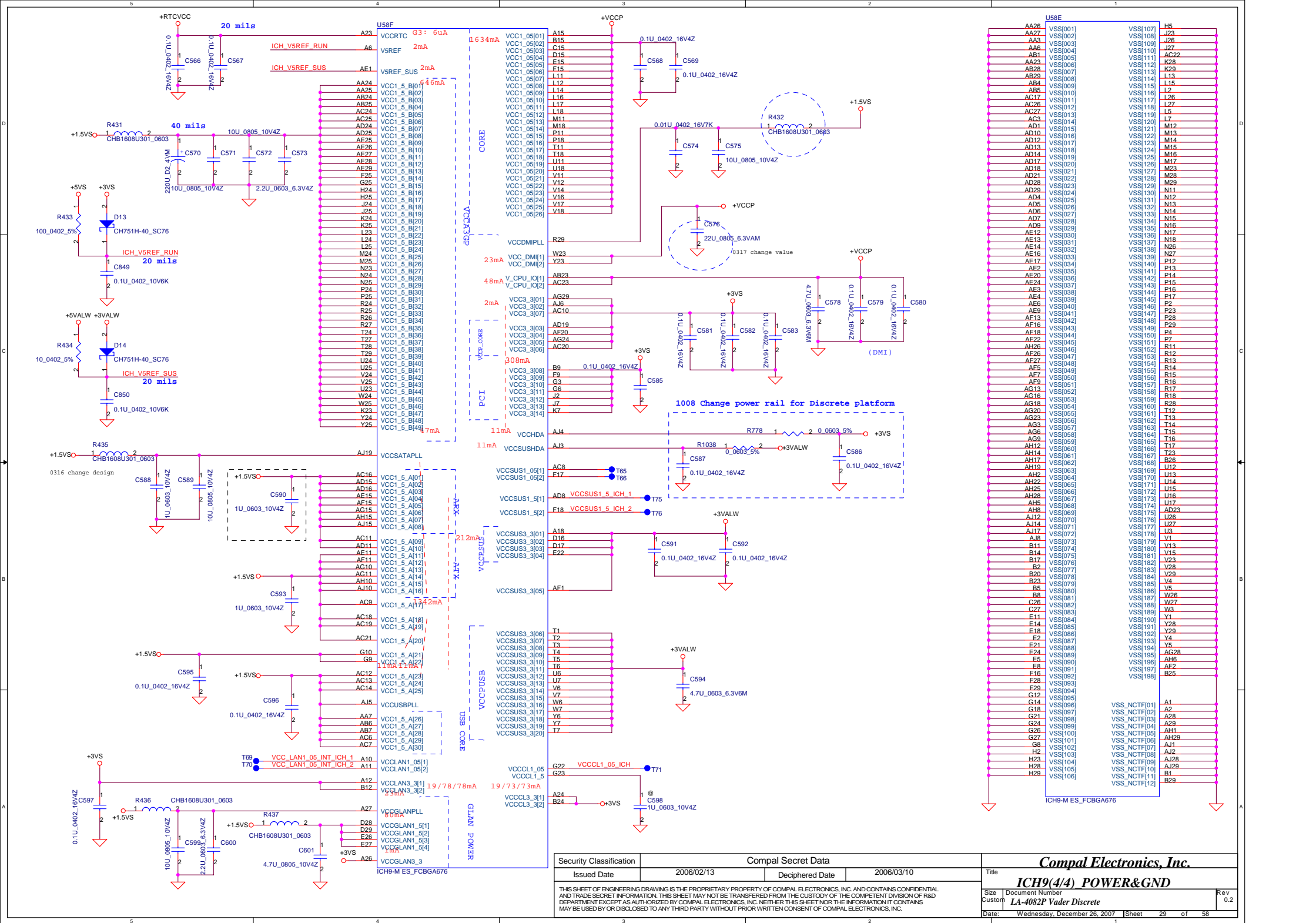
ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

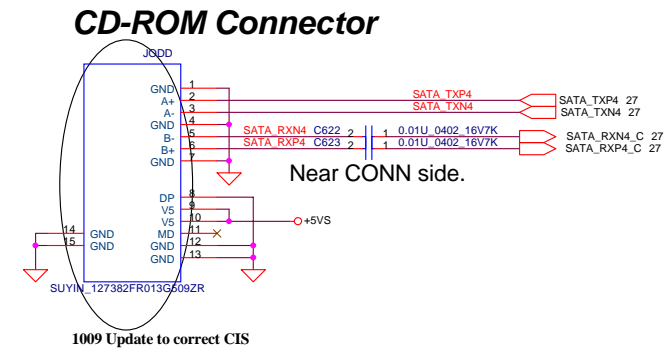
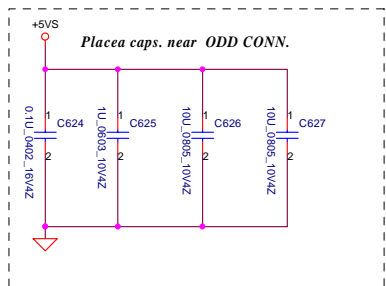
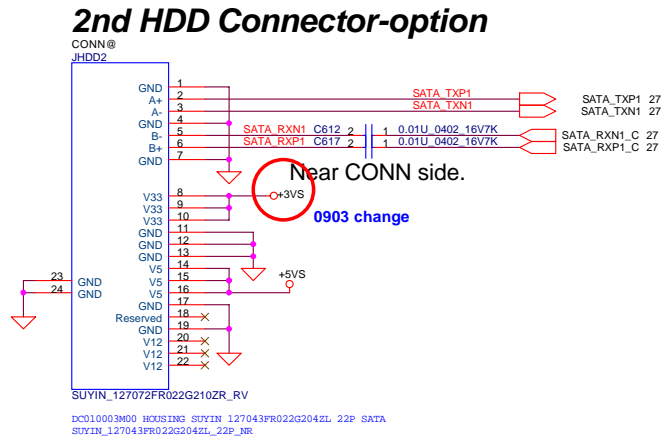
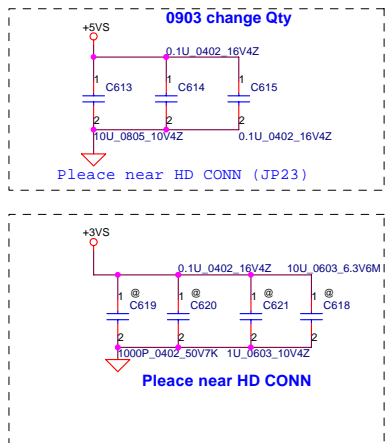
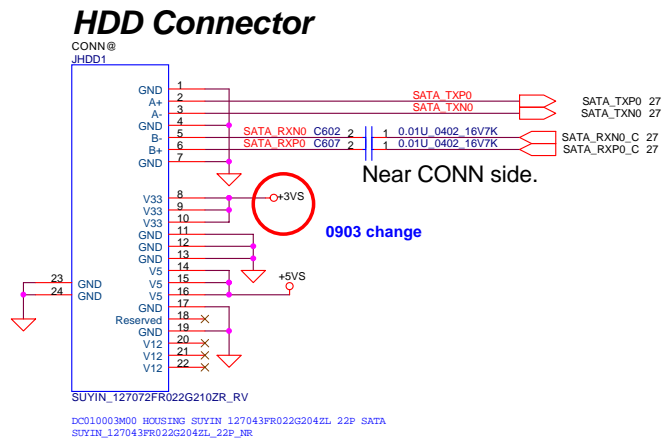
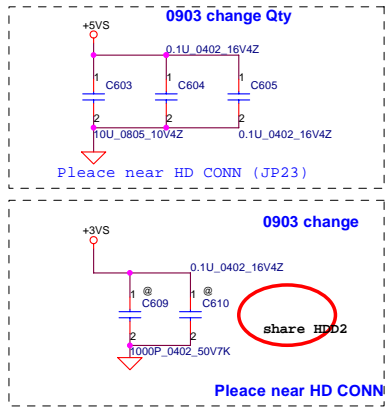
1008 add them for Intel suggestion



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Size	Document Number	Date		Wednesday, December 26, 2007	Rev 0.2
Custom	LA-4082P Vader Discrete	Sheet		27	of 58



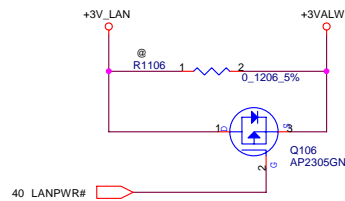




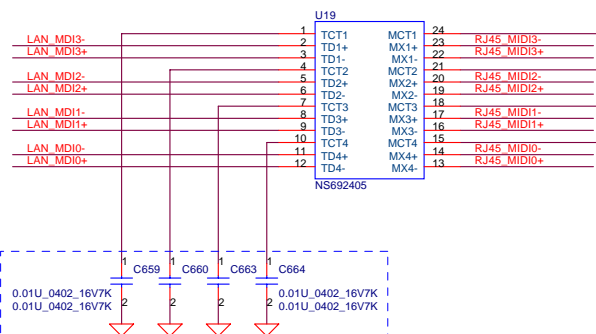
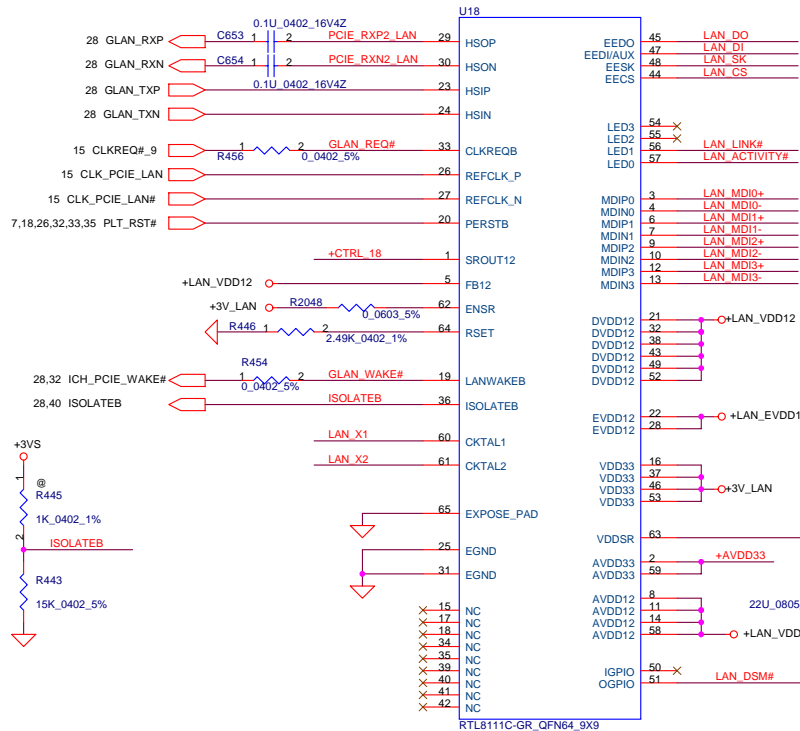
ZZZ1  
LA-4082P

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				Date:	Wednesday, December 26, 2007
				Sheet	30 of 58

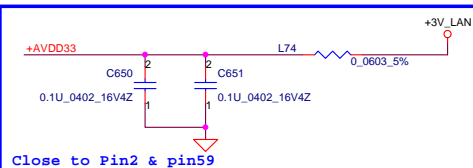
1025 add to meet HP request



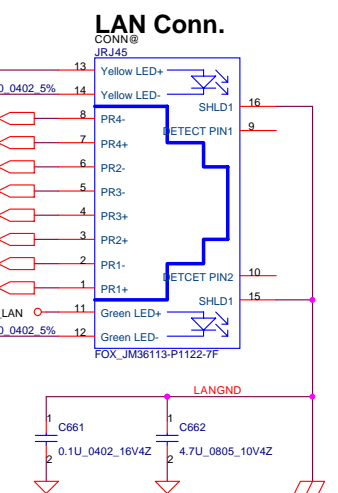
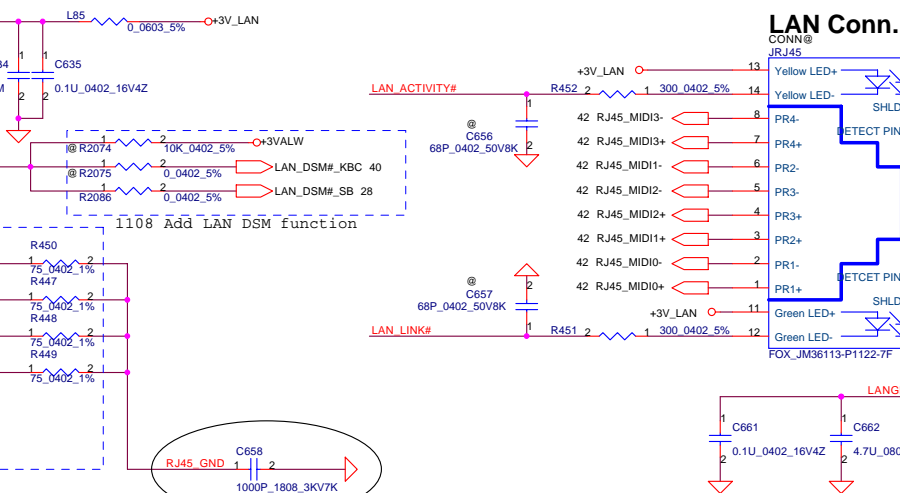
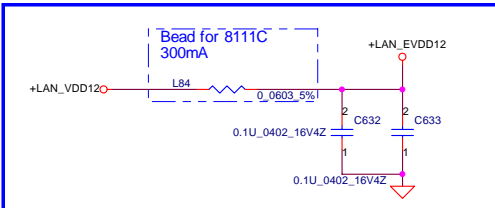
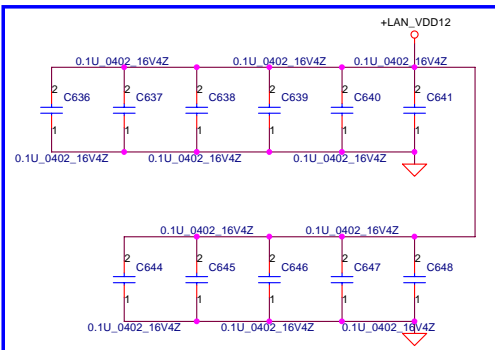
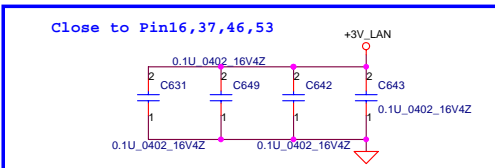
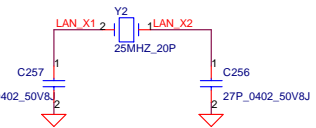
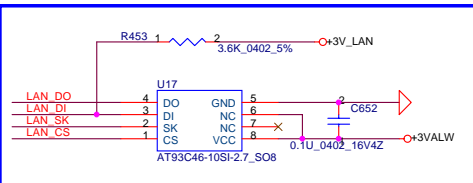
Place Close to Chip



Place these components  
colsed to LAN chip



4.7uH  
choke  
L83  
+CTRL\_18 1 4.7UH\_100  
Close to Pin1

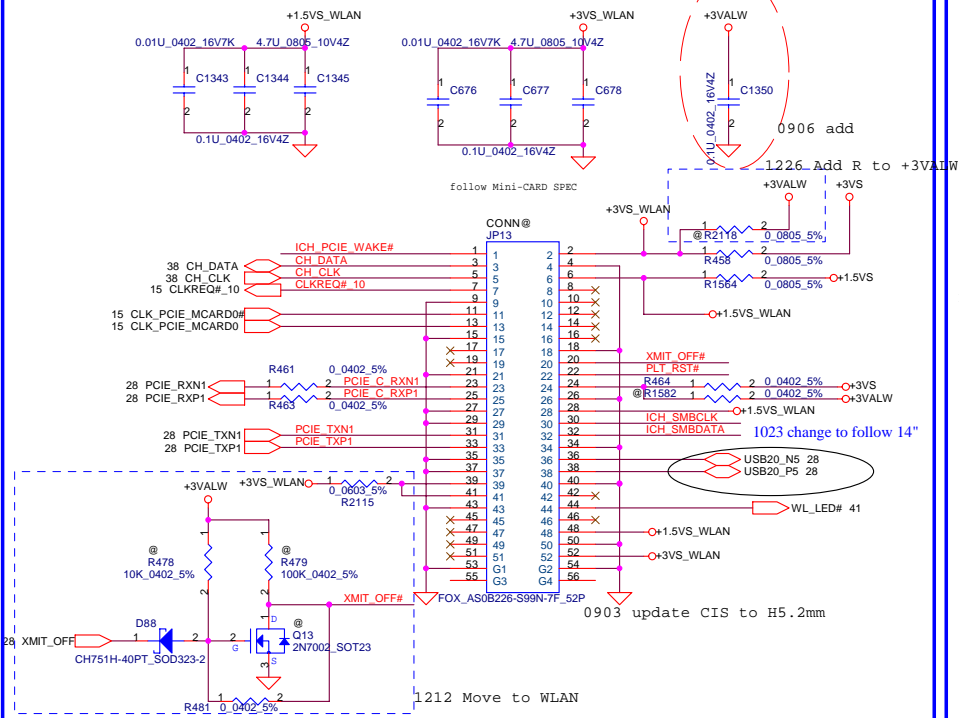


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				Date:	Wednesday, December 26, 2007	Sheet 31 of 58



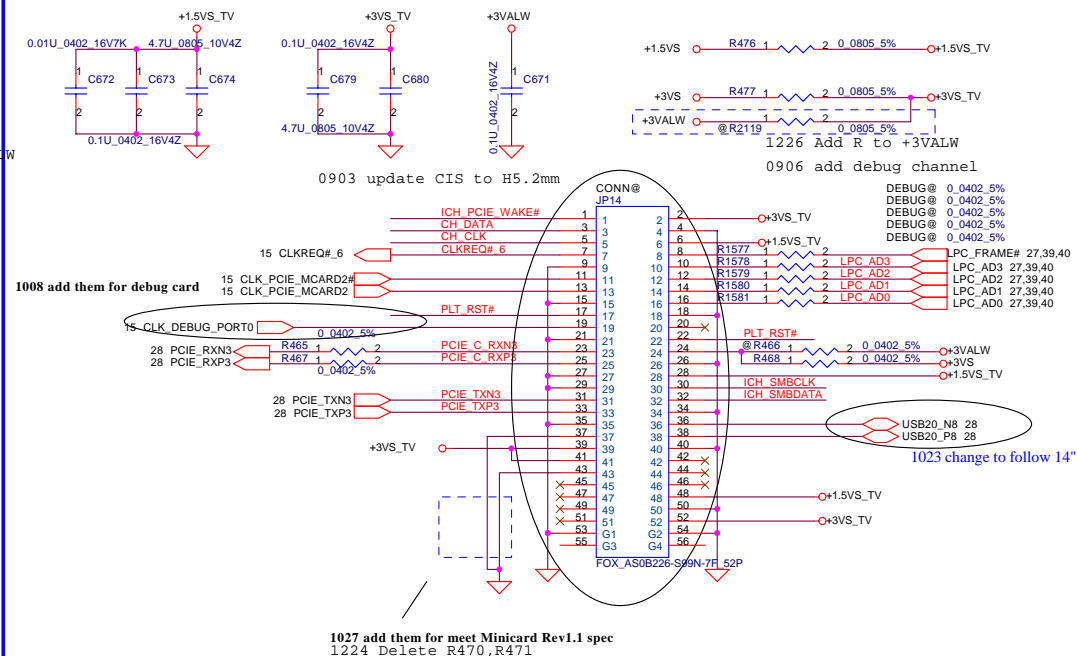
# Mini Card 0--WLAN

1022 change to follow HP design

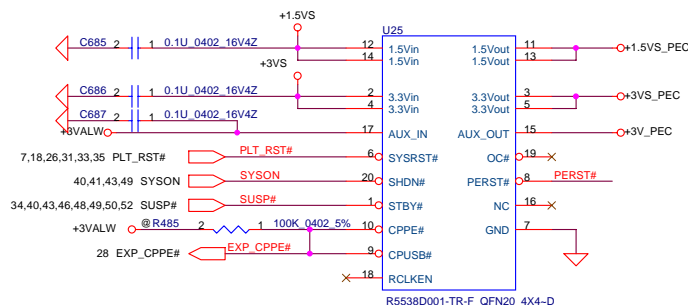


# Mini Card 2---TV tuner

1022 change to follow HP design

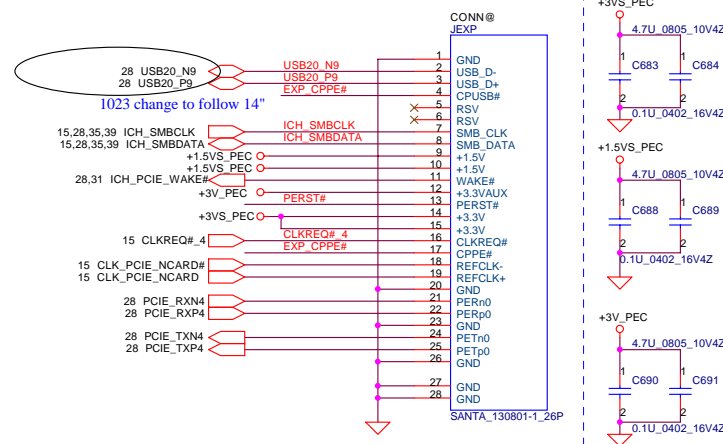


# New Card



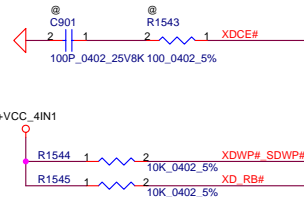
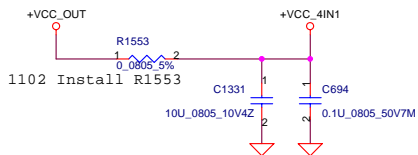
internal pull high to 3.3Vaux-in  
EC need setting at Hi-Z & output Low

# Near to Express Card slot.



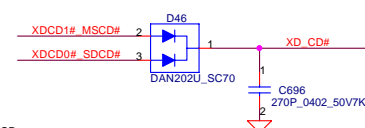
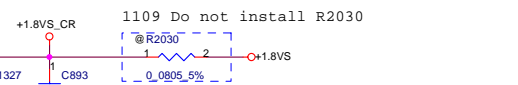
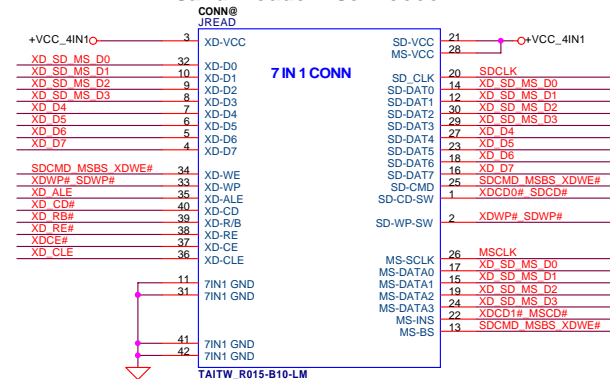
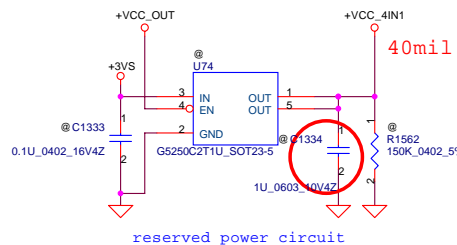
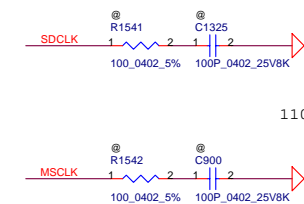
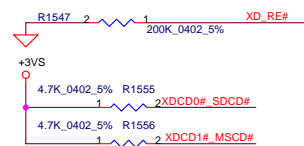
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1023 JMicro suggest to change

1212 Change XD ALE to +3VS



1009 lower LED power consumption

+5VS

R1557  
470\_0402\_5%

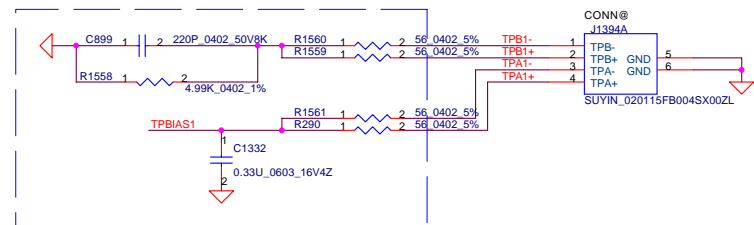
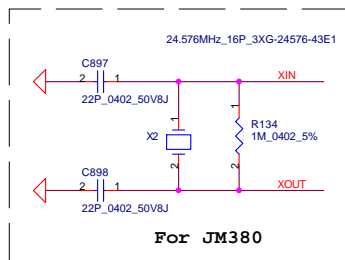
D47  
HT-F196BP5\_WHITE

Q53  
2N7002\_SOT23-3

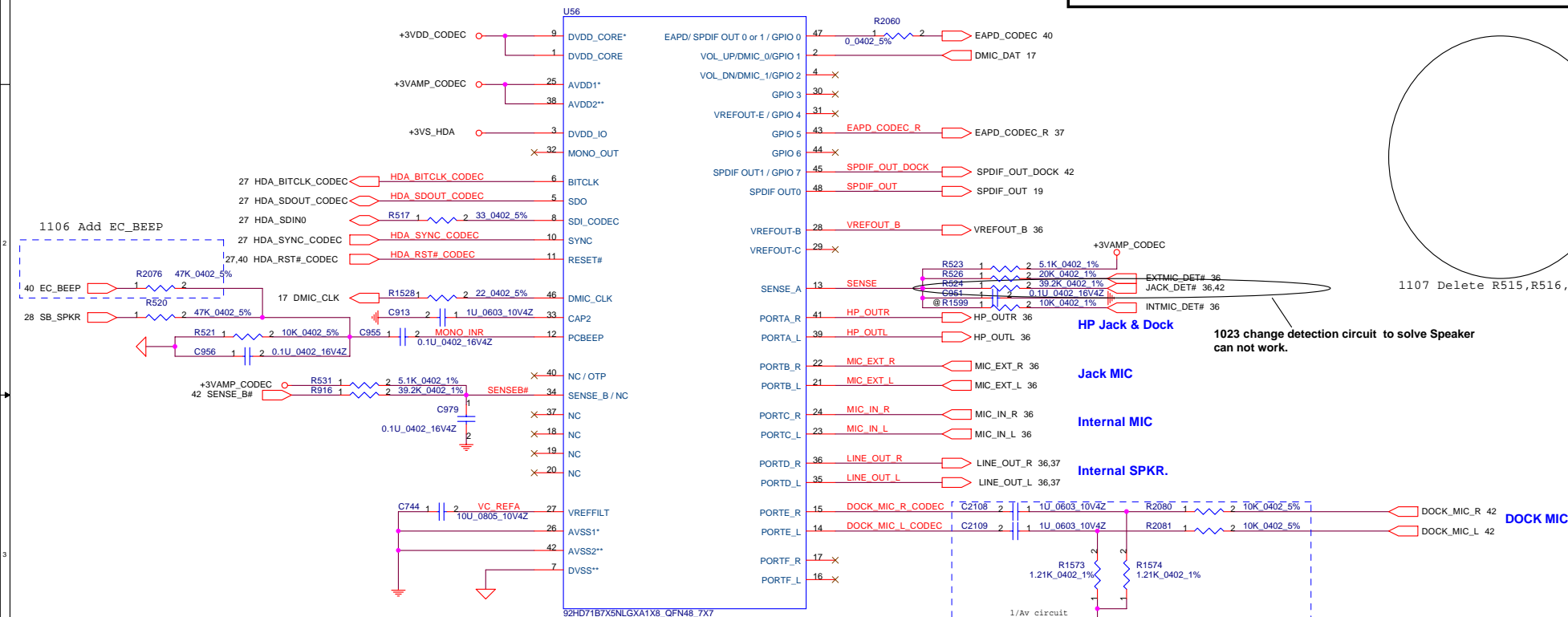
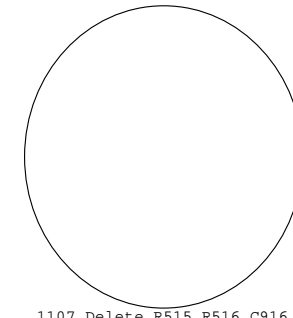
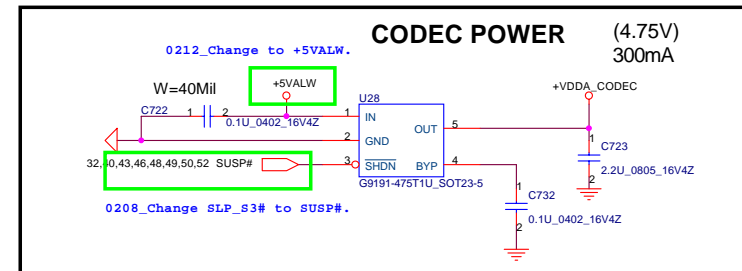
R2097  
4.7K\_0402\_5%

CR\_LED#

1212 Change To high active control

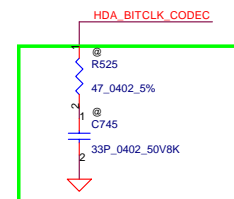
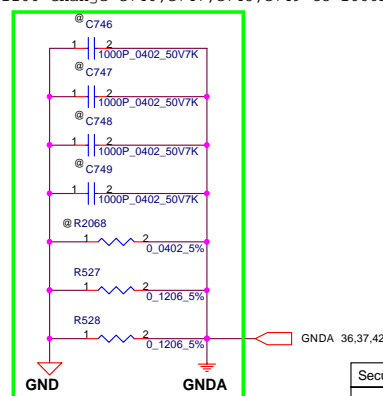


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1107 HP request

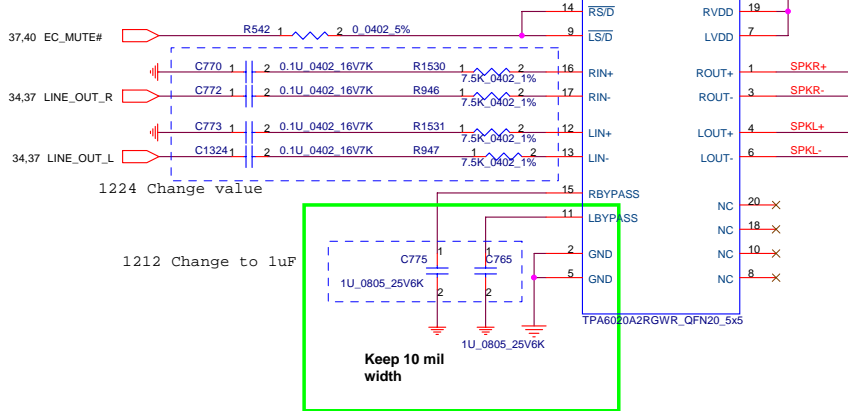
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



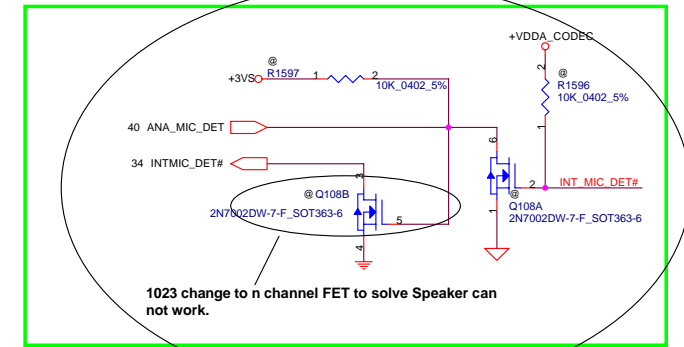
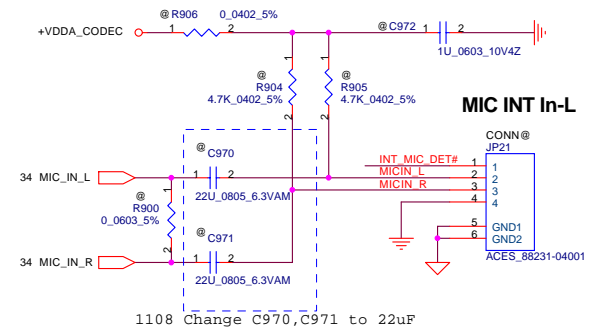
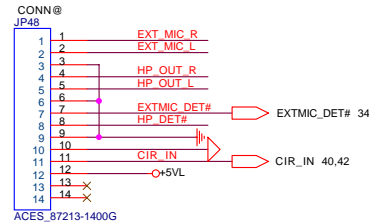
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title <b>Codec IDT92T1B7</b>		
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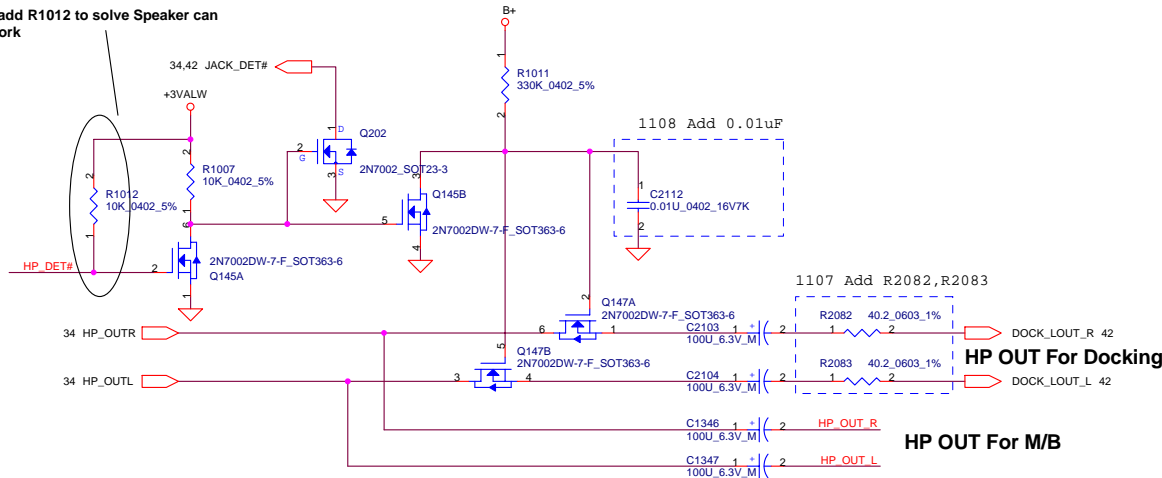
0906 Change  
3/28 from  
NC7SZ04P5X\_SC70-5  
change to 2N7002



0906 Change pin define  
Audio & USB board conn

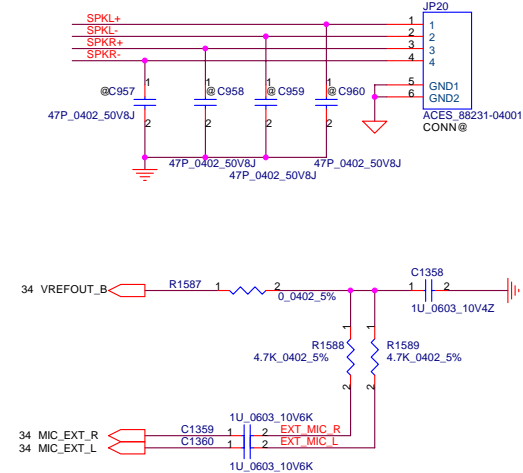


1023 add R1012 to solve Speaker can not work

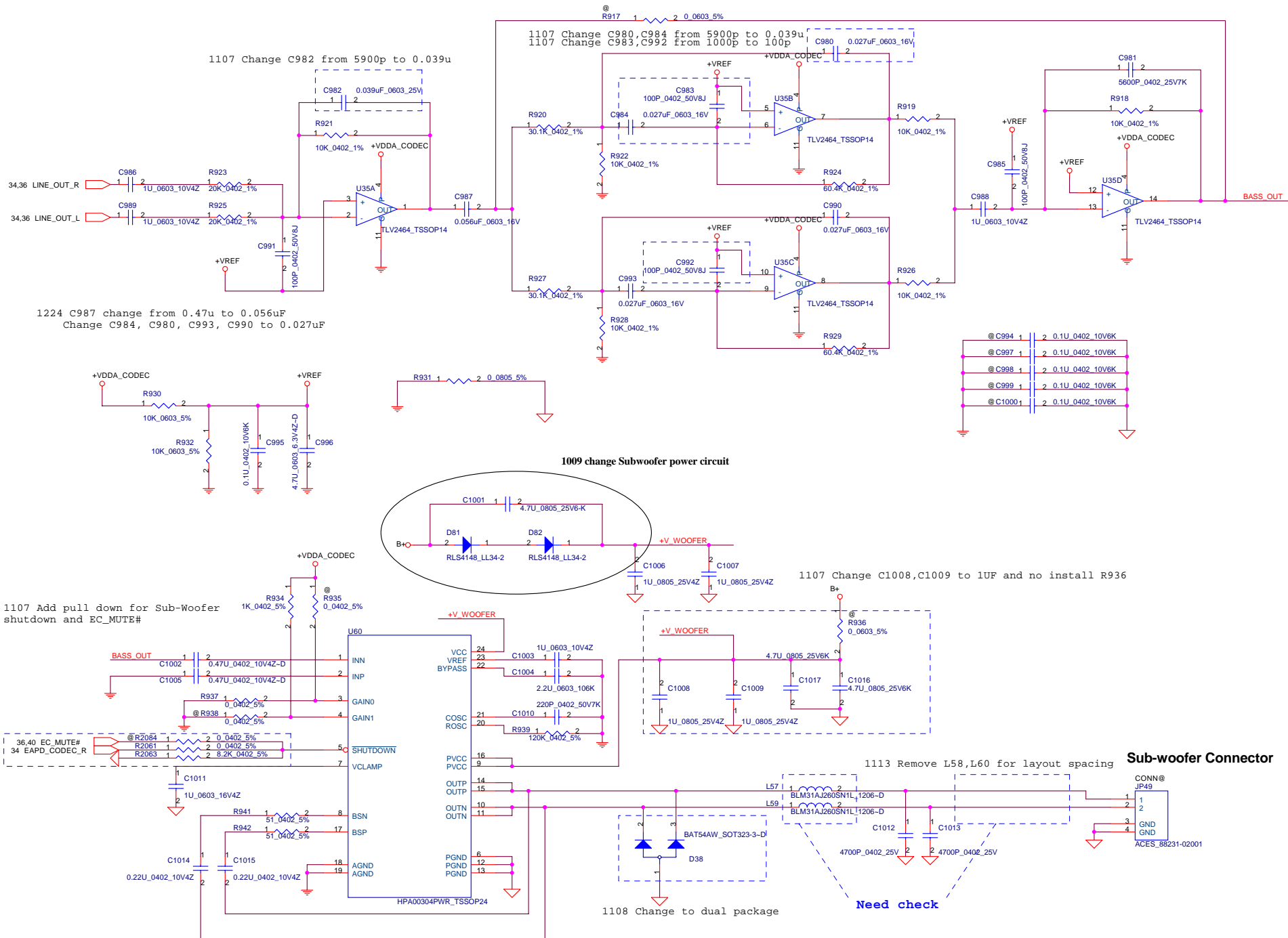


SP02000D000 S W-CONN ACES 85204-04001 4P P1.25

SPEAKER

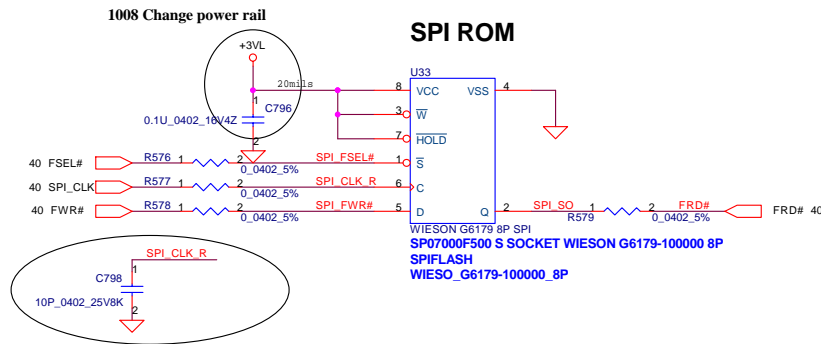
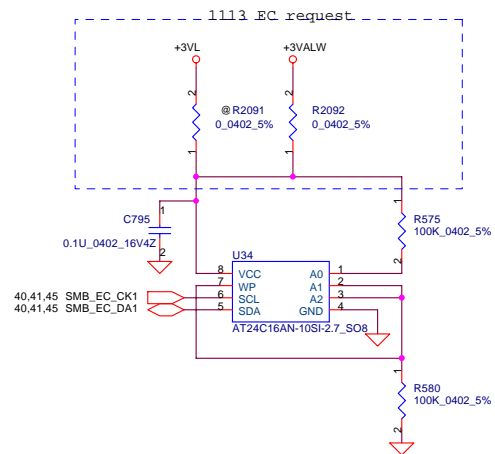


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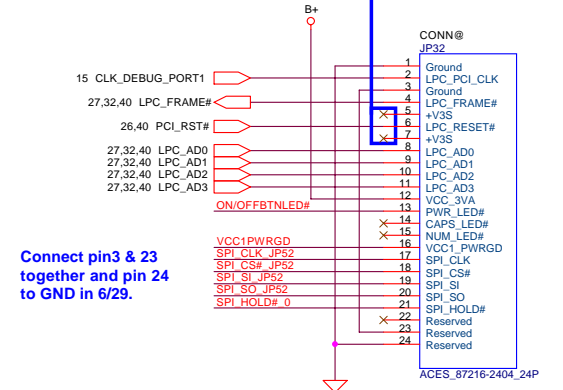
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				Size Custom	Document Number LA-4082P Vader Discrete
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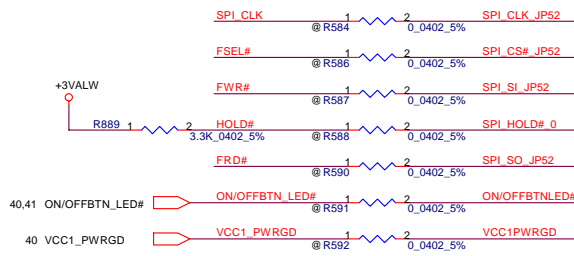


## LPC Debug Port

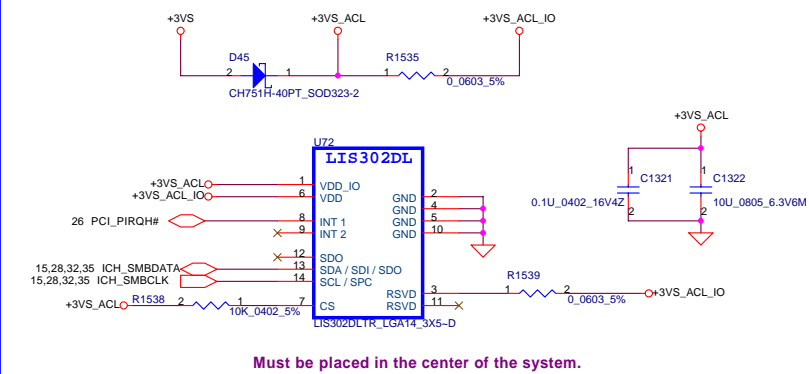
Change from +3VL to +3VS. 6/9  
Removed +3VS. 6/13



Connect pin3 & 23  
together and pin 24  
to GND in 6/29.

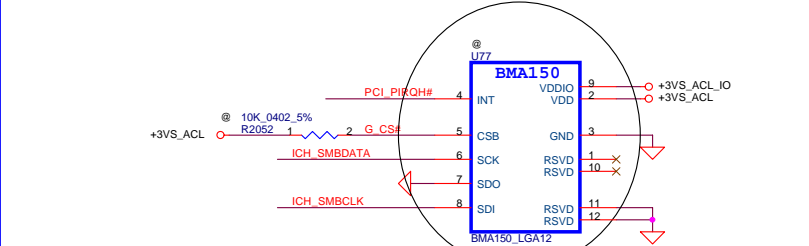


## Acceleromter-1



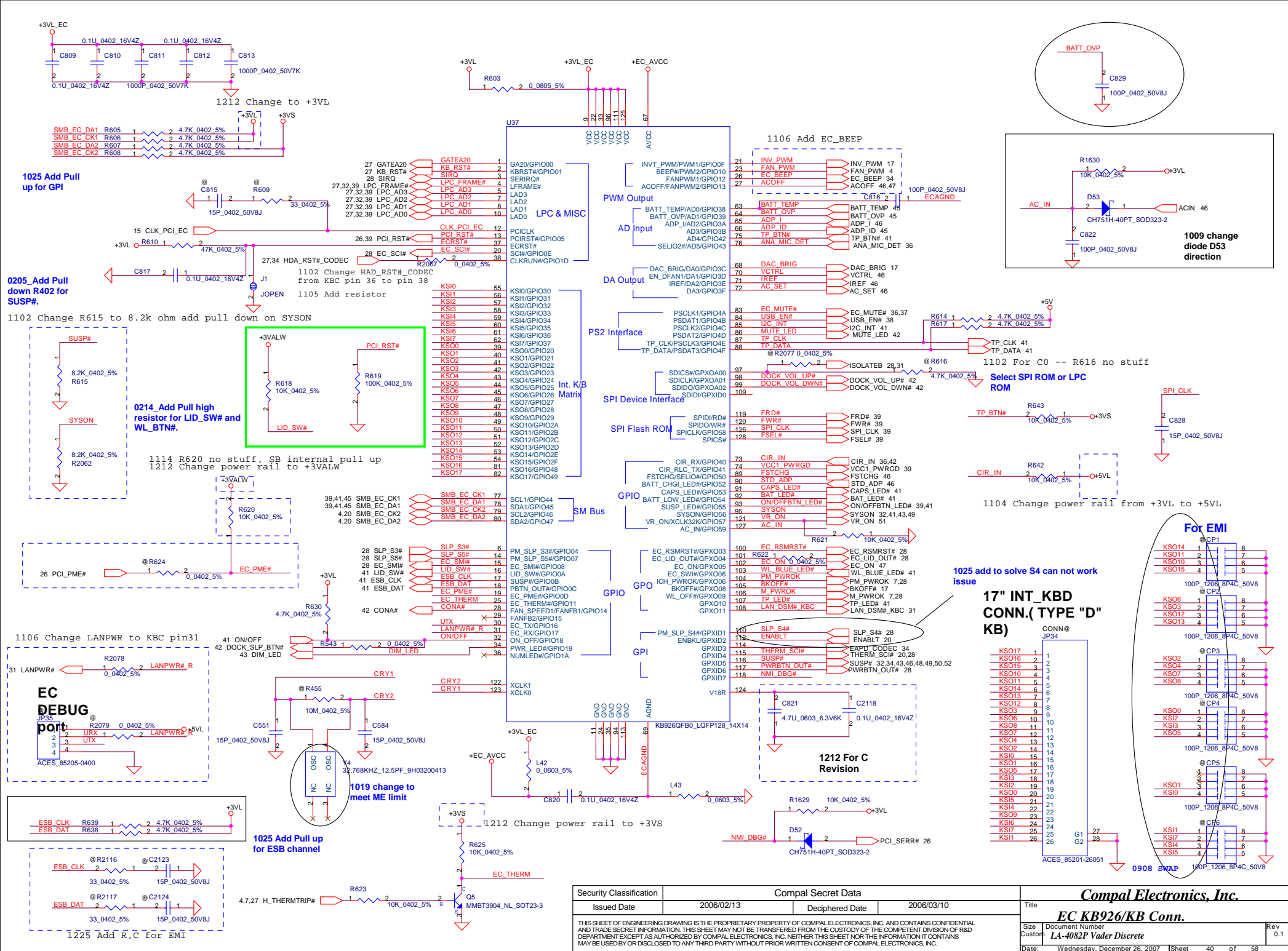
## Acceleromter-2

U72 & U77 must be close  
need to update CIS



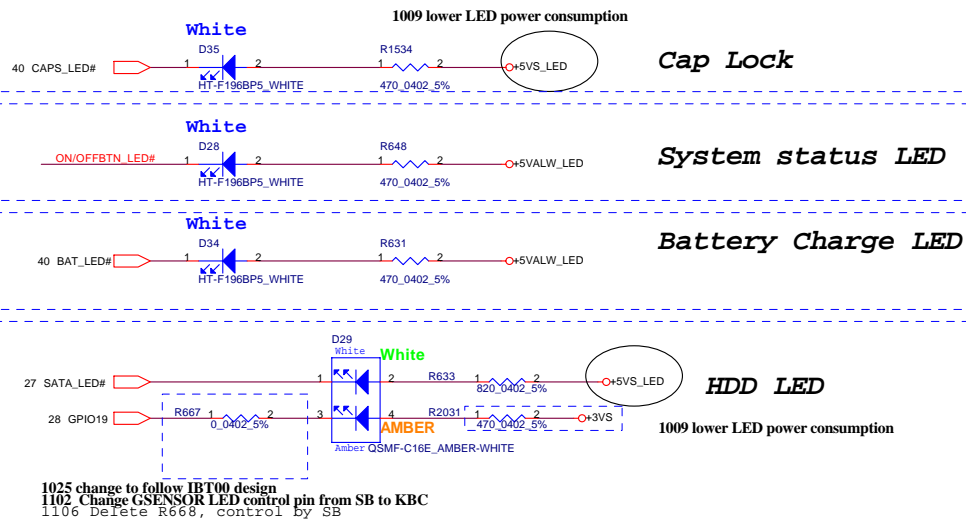
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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				Size Custom	Document Number LA-4082P Vader Discrete
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					Size	Document Number	Rev
						<b>LA-4082P Vader Discrete</b>	0.1
Date:		Wednesday, December 26, 2007	Sheet	40	of	58	

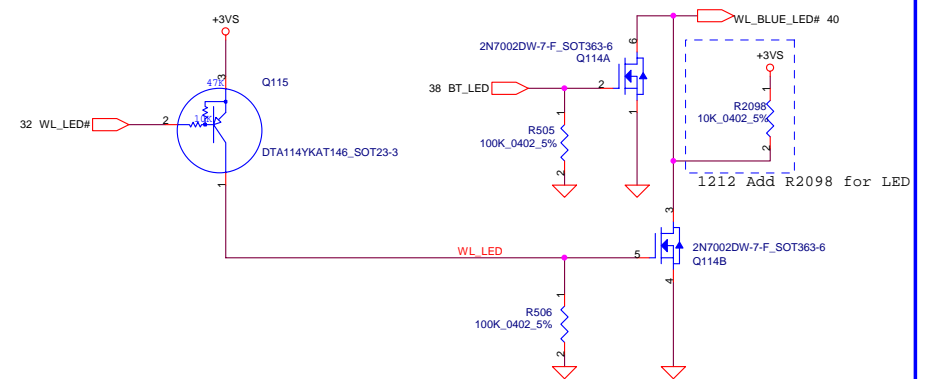
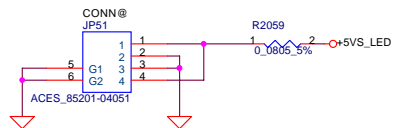
**LED**



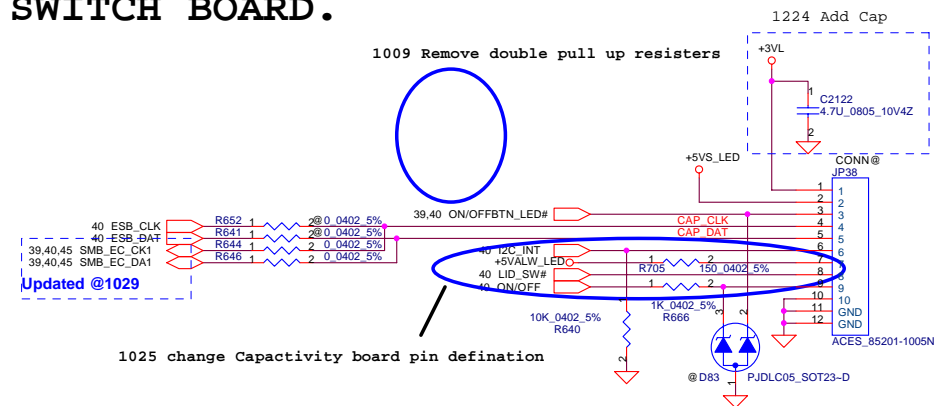
for debug only

```
1212 Delete SW5,SW6
```

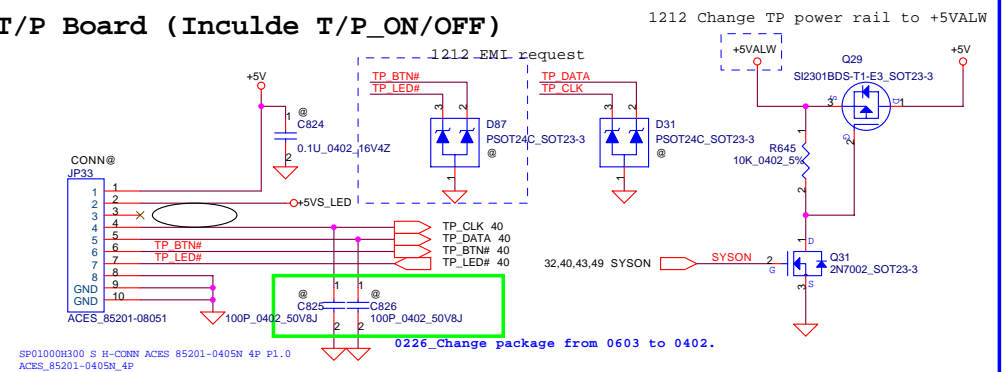
## K/B backlight



**SWITCH BOARD.**

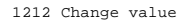
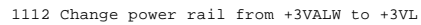


**T/P Board (Inculde T/P\_ON/OFF)**



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4V = Notebook S0, Dock on



### 1009 Remove TV components

need change to reverse type connector



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					Size	Document Number		Rev
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### +5VALW to +5VS Transfer

The diagram illustrates the +5VALW to +5VS Transfer circuit. It features a 330K resistor (R2099) connected to B+ and a 100nF capacitor (C841) connected to +5VALW. The output of the 330K resistor is connected to the gate of a 2N7002DW-7-F MOSFET (Q89B). The MOSFET's source is connected to SUSP and its drain is connected to the +5VS rail. A 470 ohm resistor (R2100) and a 0.01uF capacitor (C2119) are connected between the +5VS rail and ground. A 0.1uF capacitor (C837) is connected between the +5VS rail and ground. A 100nF capacitor (C838) is connected between the +5VS rail and ground. The circuit is labeled "1212 For power sequence".

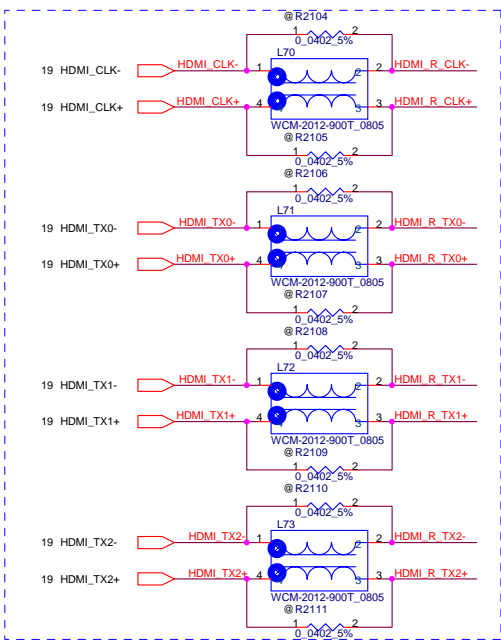
### +3VALW to +3VS Transfer

The diagram illustrates the transfer of the +3VALW signal to the +3VS supply line. The AO4466\_S08 op-amp (U40) is configured as a voltage follower. The non-inverting input (+) is connected to +3VALW through a 330K\_0402\_5% resistor (R656) and a 10u\_0805\_10V4Z capacitor (C836). The inverting input (-) is connected to the output through a 470\_0402\_5% resistor (R657). The output is connected to +3VS through a 0.1u\_0402\_16V4Z capacitor (C839) and a 10u\_0805\_10V4Z capacitor (C840). A MOSFET (Q89A, 2N7002DW-7-F\_SOT363-6) is connected to the output line, with its gate driven by a signal labeled SUSP. The MOSFET's source is grounded, and its drain is connected to the output line. The output line is also connected to a 0.01u\_0402\_16V7K capacitor (C842) to ground.

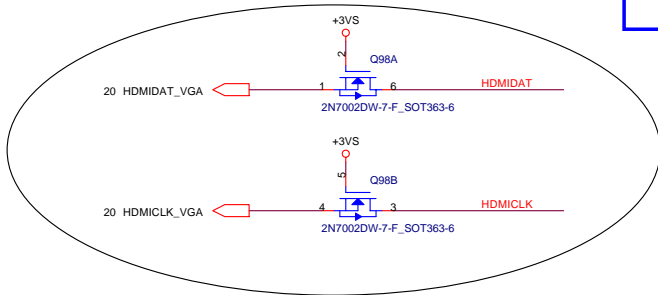
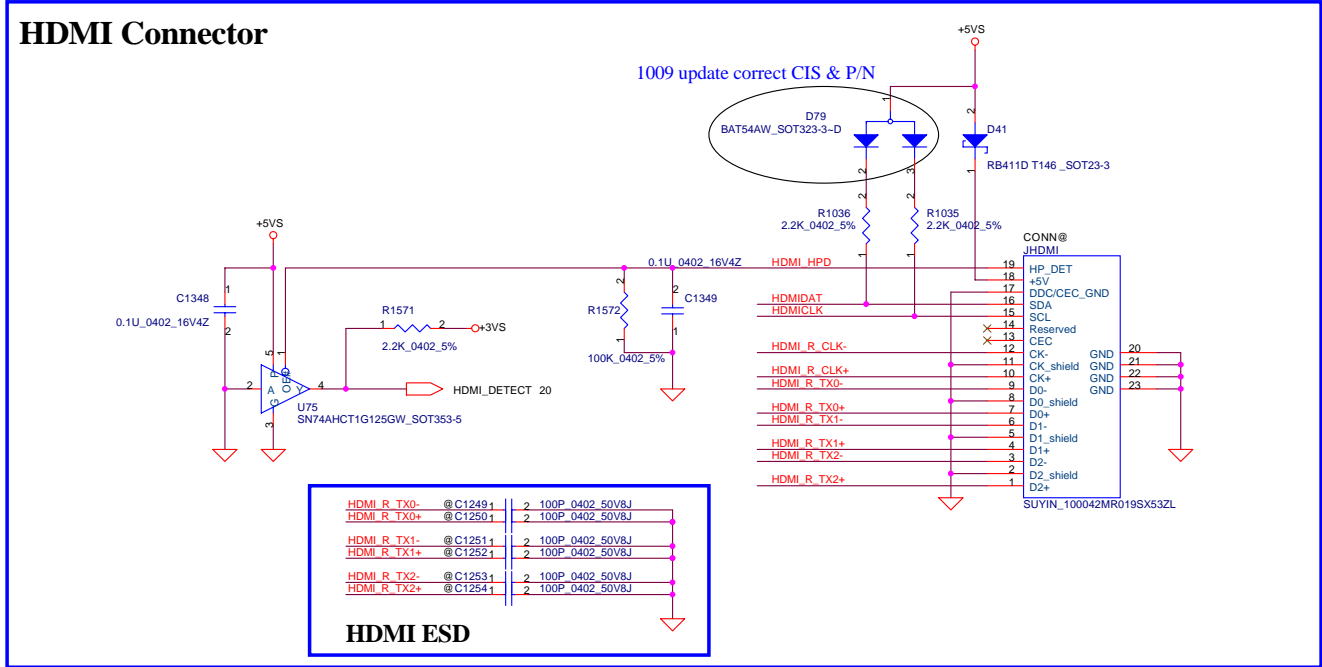
## +1.8V to +1.8VS Transfer

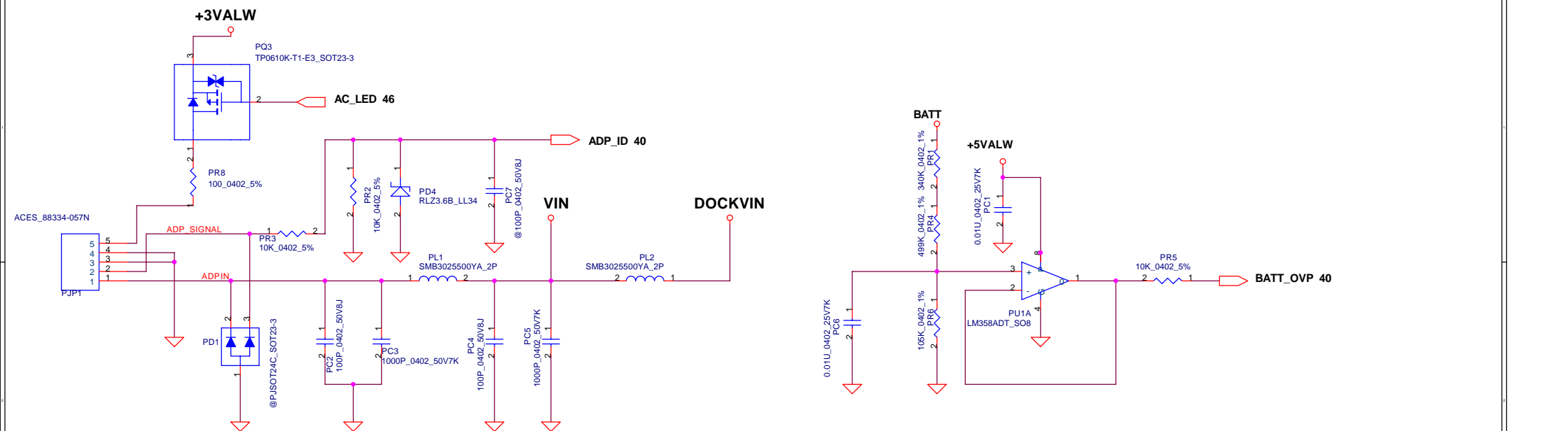
The diagram illustrates the transfer of a +1.8V signal to a +1.8VS signal. The circuit includes a voltage divider consisting of a 220k resistor (R15) and a 6.3V Zener diode (C1618). The output of this divider is connected to a 100nF capacitor (C961) and a 0.1uF capacitor (C962) in parallel. The output is also connected to a 1.8V ON pin (R1932) and a 1.8V ON pin (D78). The output is labeled +1.8VS. The circuit is powered by a 1.8V input and a 1.8VS output.

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				Custom	<b>LA-4082P Vnder Discrete</b>	0.1
				Date:	Wednesday, December 26, 2007	Sheet 43 of 58

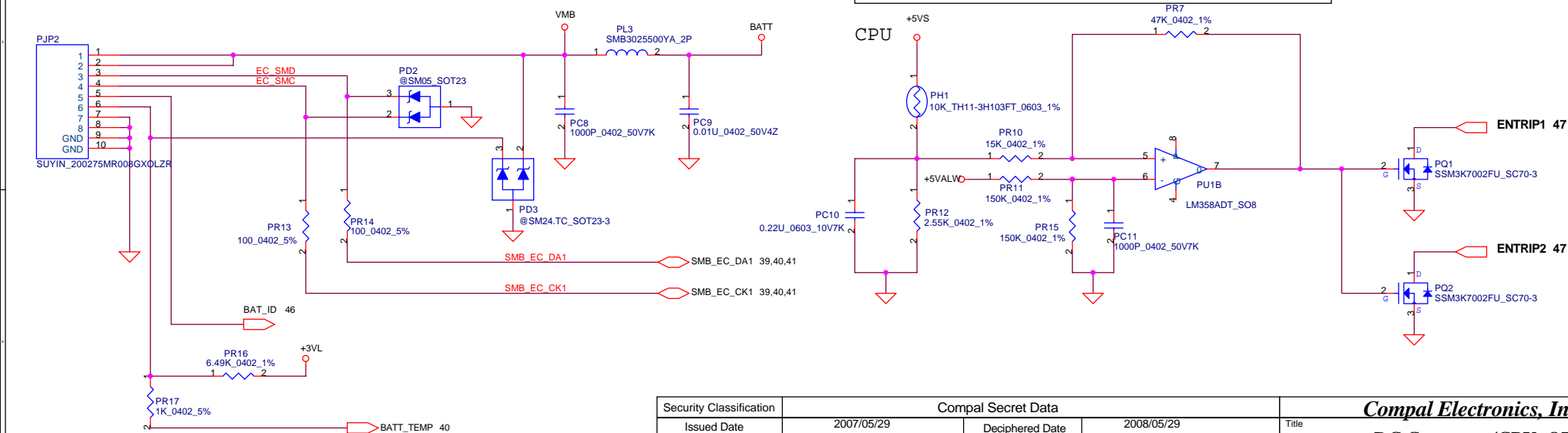


# HDMI Connector





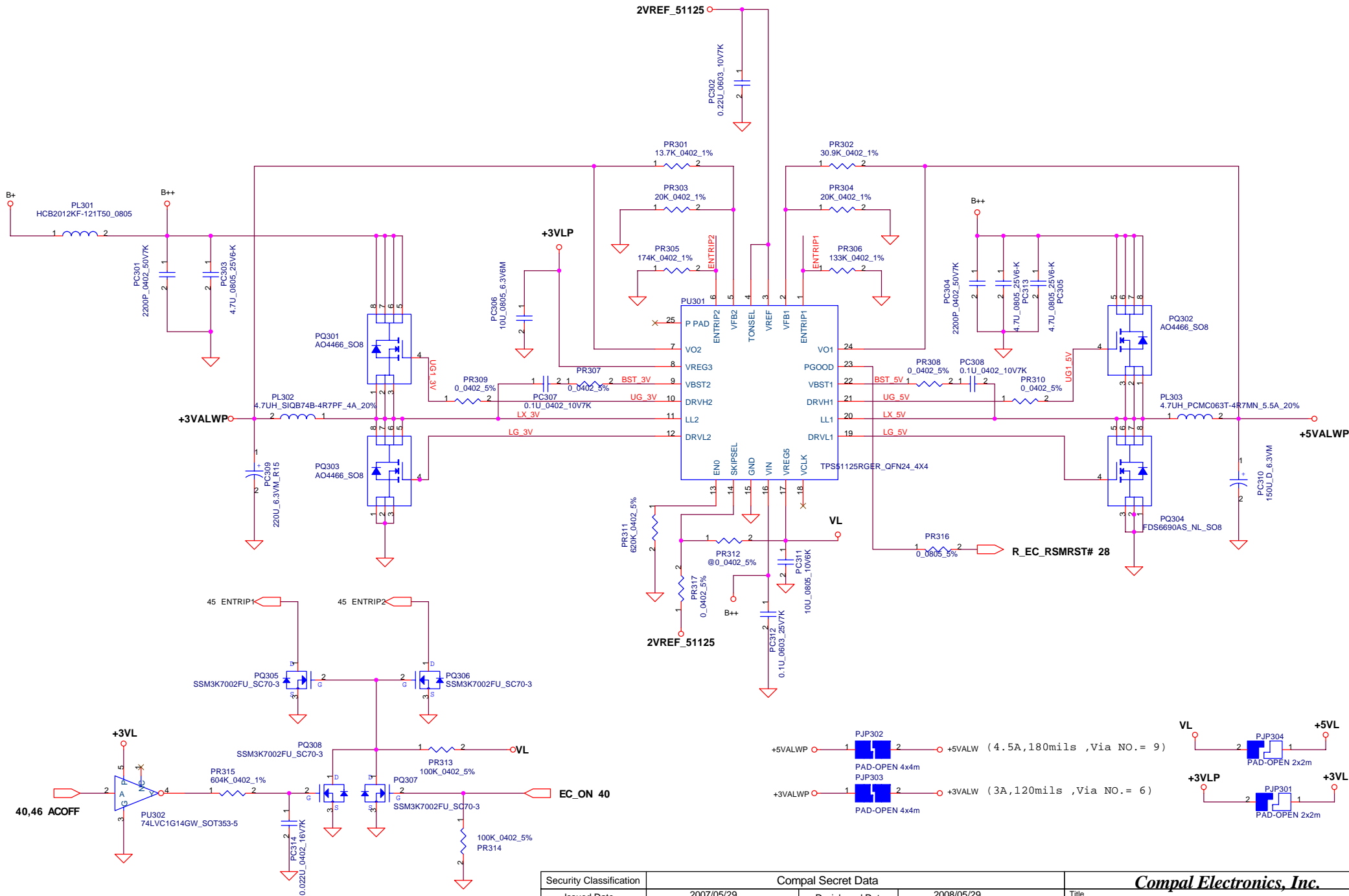
**PH1 under CPU bottom side :**  
 CPU thermal protection at 90 +-3 degree C  
 Recovery at 47 +-3 degree C



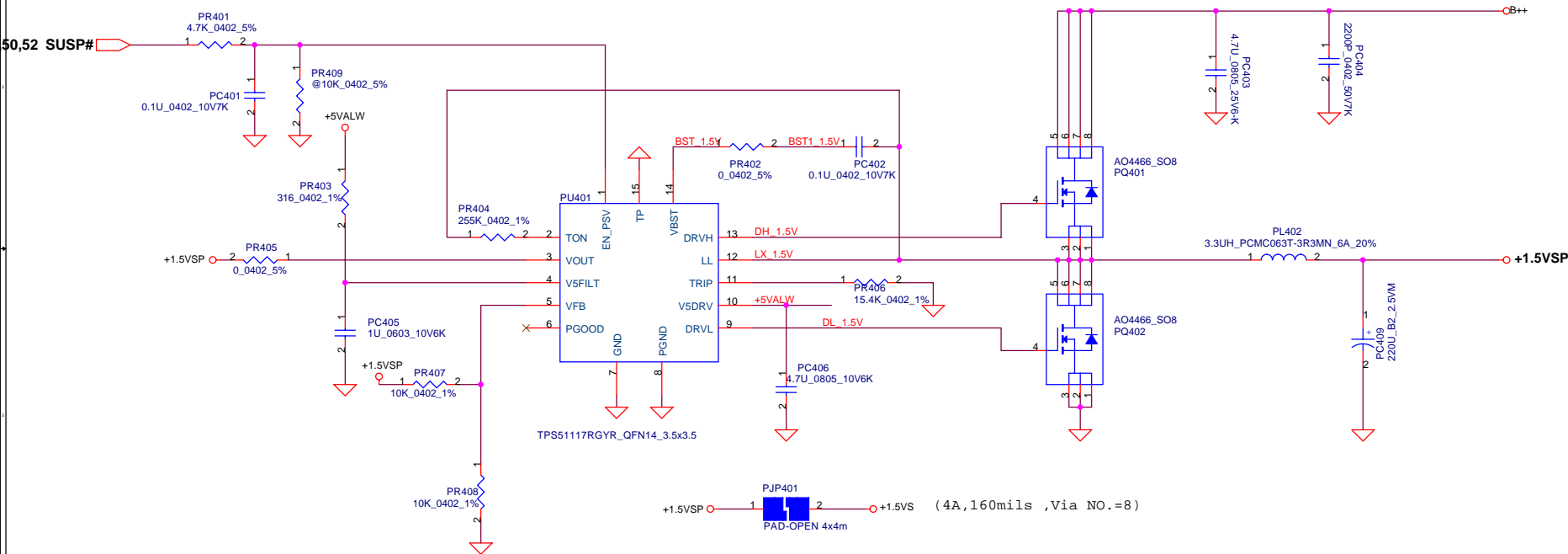
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				Montevina Consumer Discrete	
				Date:	Wednesday, December 26, 2007
				Sheet	45 of 58
				Rev	0.1



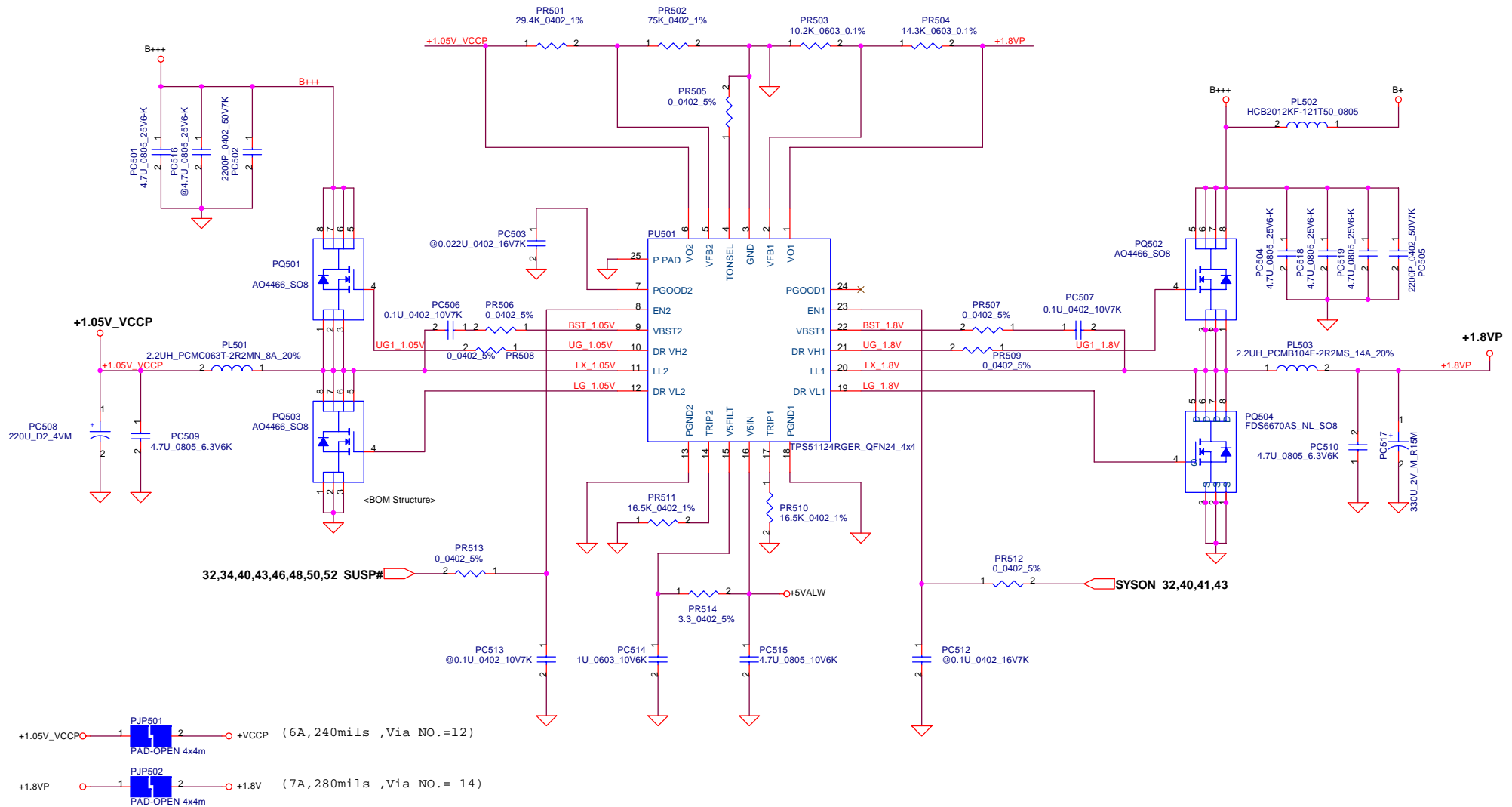




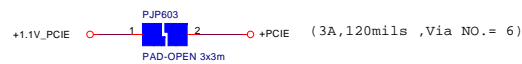
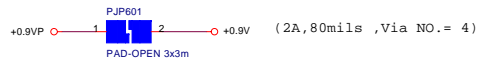
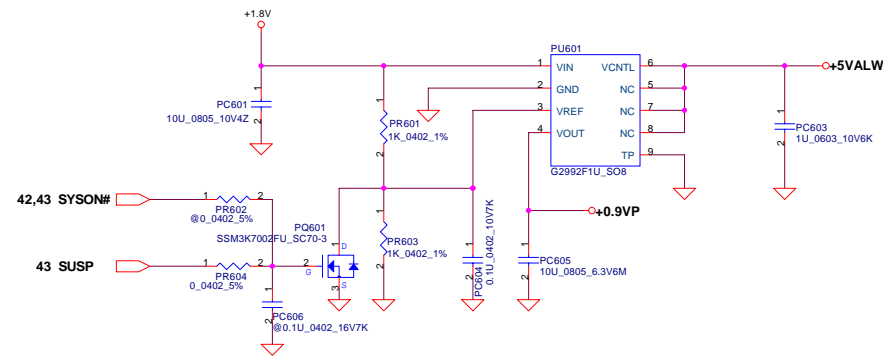
Security Classification		Compal Secret Data		Title	
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				Rev	0.1



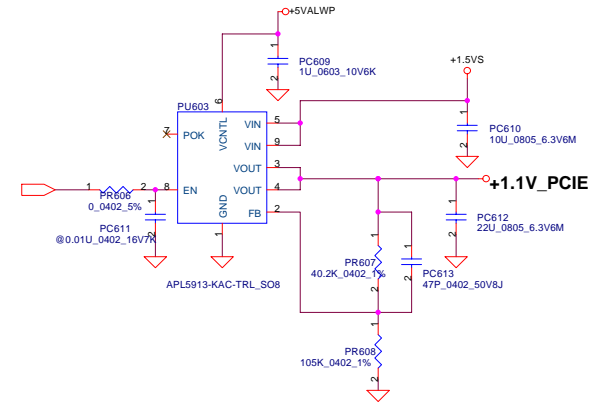
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Size	Document Number	Montevina Consumer Discrete			Rev 0.1
Date:	Wednesday, December 26, 2007	Sheet	48	of	58



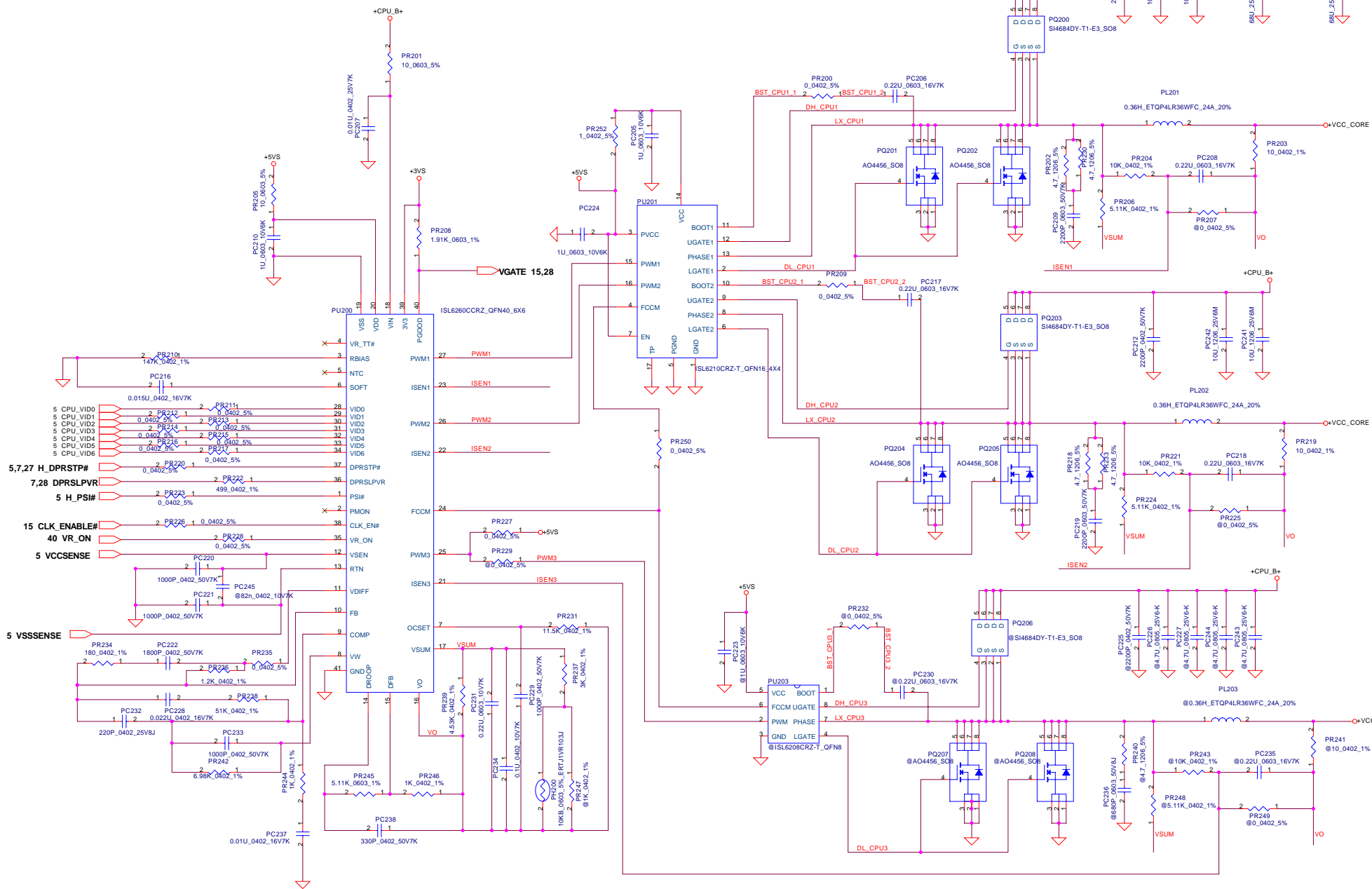
Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	1.05V VCCP/1.8VP	
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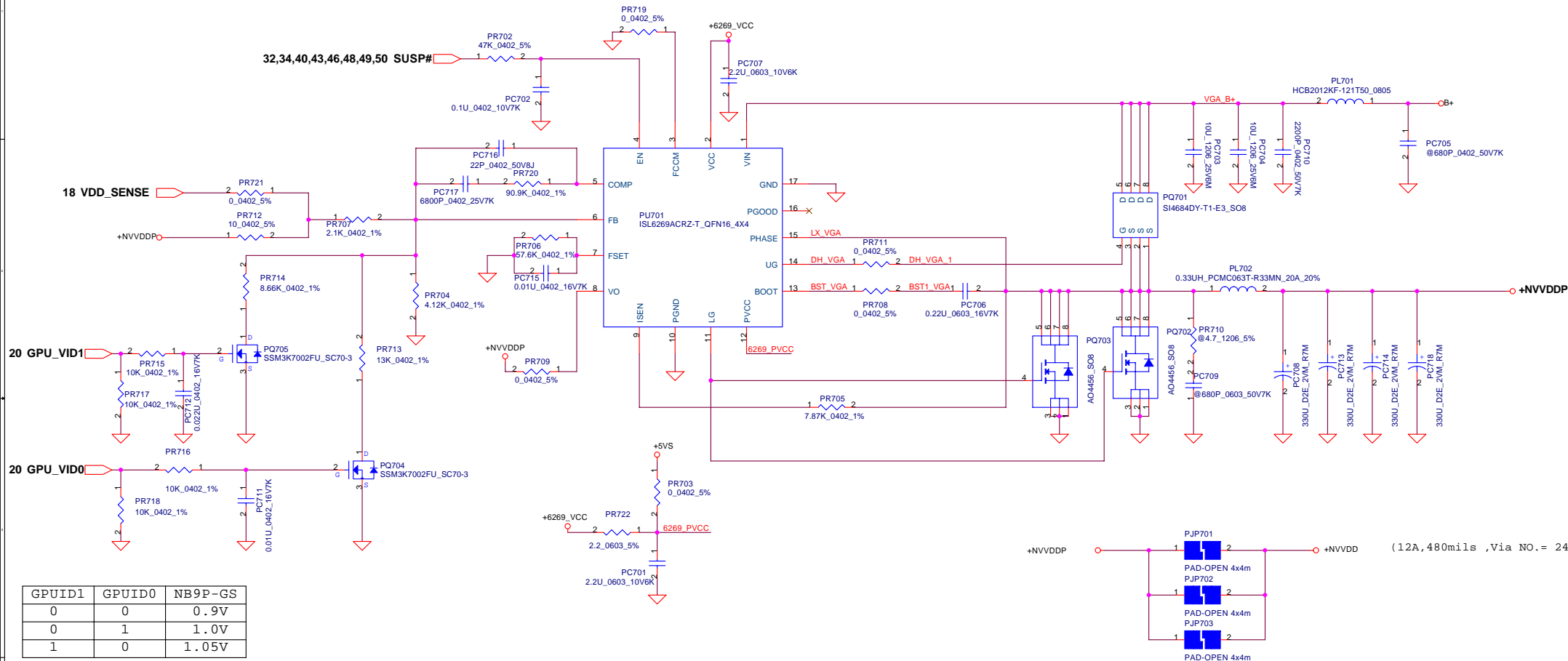
32,34,40,43,46,48,49,52 SUSP#



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		S1		of	
		58			





Version Change List ( P. I. R. List ) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as luf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.10.23>	1	Fix USB loading of SB	follow 14" Blade USB channel design	28 17 32 38 38 42	Chnage all USB channel Change USB channel of Camera Change USB channel of WLAN & TV Tuner & New card Change USB channel of Left side, Right side, E-SATA Change USB channel of Touch screen, Finger print Change USB channel of Dock	0.2
	2		Follow JMicro CardReader Vendor Suggestion	33	Change R114 & R1546 value	0.2
	3		Solve Speak no sound issue	36 36 34	add pullup at HP_DET# Change Q203 to N-channel FET Change R524 pin2 connect to JACK_DET#	0.2
	1		Meet HP request for QC and DC co-lay	4 5 6	add GTLREF and XDP circuits	0.2
	2		Meet Intel request for CLK request	15	Add R127 to meet Intel CLK design	0.2
	3		Solve G-sensor LED control	28, 41	change G-sensor LED control to GPIO19 of SB	0.2
<2007.10.25>	4		Follow Capactivity board design	41	change Pin7 & 7 NET	0.2
	1			34	Use Audio Codec GPIO5 to shutdown Sub-woofer	
	2			40	Connect HDA_RST#_CODEC to EC	
<2007.10.31>	3			34	Separate SPDIF out to VGA and Docking	
	1		Common design	16	R204,R205 no stuff	0.3
	2		Change +5VS_LOGO resistor size to 0805	17	R642 size to 0805	0.3
<2007.11.02>	3		Double pull up	20	R2046,R2047 no stuff	0.3
	4		For card reader power	33	install R1553	0.3
	5		For KBC C0 version	40	R616 no stuff	0.3
	6		Add pull down resistor for SUSP# and SYSON	40	Change R615 to 8.2k and add R2062	0.3
	7		Change HAD_RST#_CODEC from KBC pin 36 to pin 38	40		0.3
	8		Change GSENSOR LED control pin from SB to KBC	41	Install R668, no install R667	0.3
	9		Add pull down for sub-woofer power-down	37	Add R2063	0.3

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