

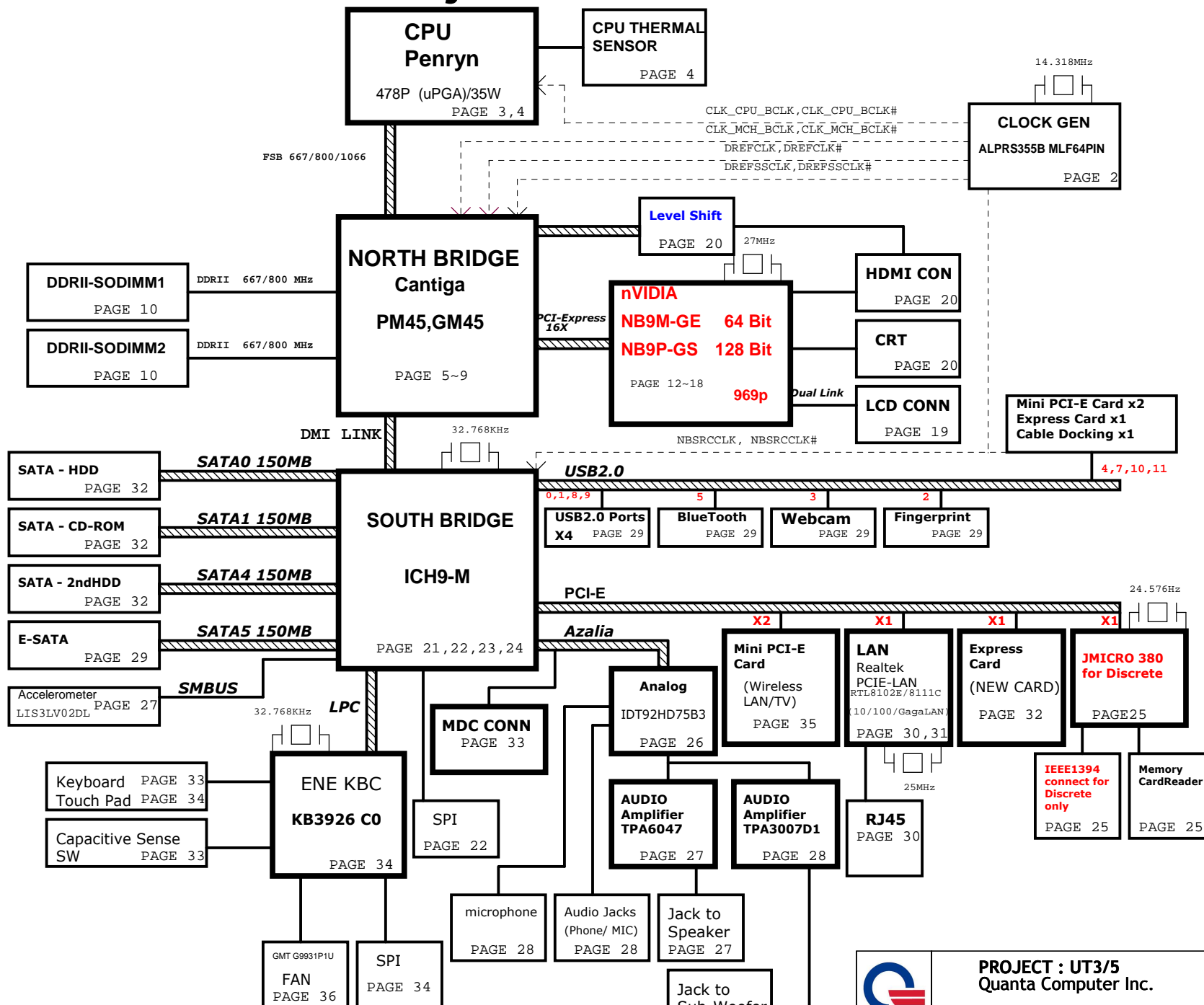
8L Dis.

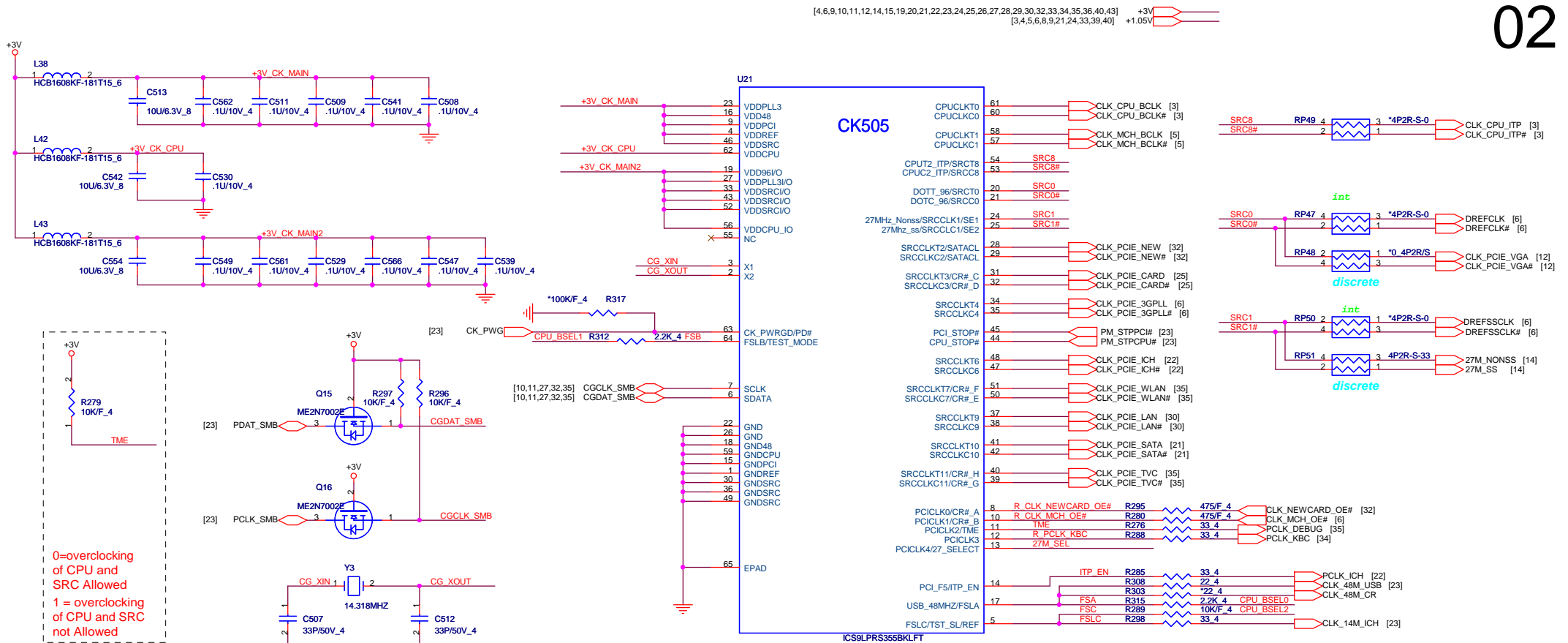
Cable Docking

VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

PAGE 36

CPU CORE ISL6262A PAGE 40





0=overclocking
of CPU and
SRC Allowed
1 = overclocking
of CPU and SRC
not Allowed

0=UMA
1 = External
VGA

Enable ITP CLK

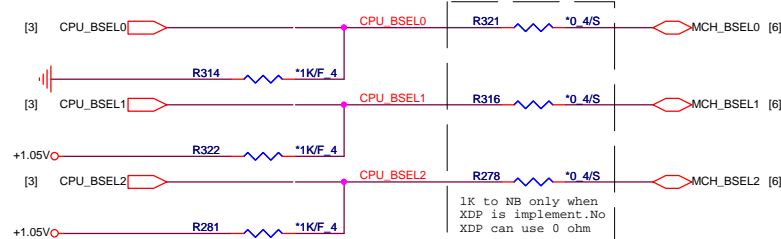
Change to 33p

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

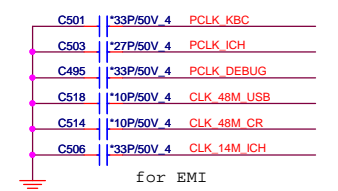
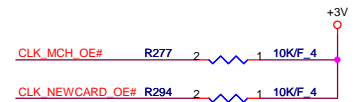
CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
SPECTRALINEAR	SL28541BQCT	AL028541000

CPU Clock select

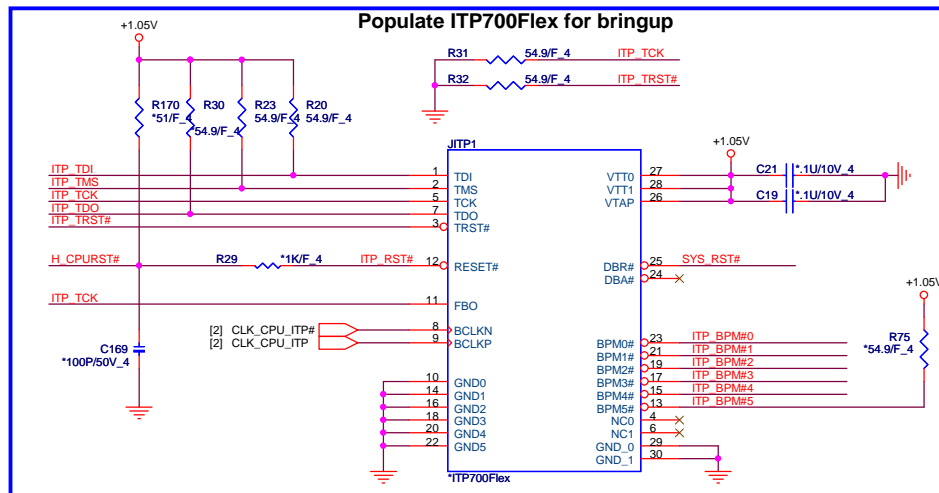
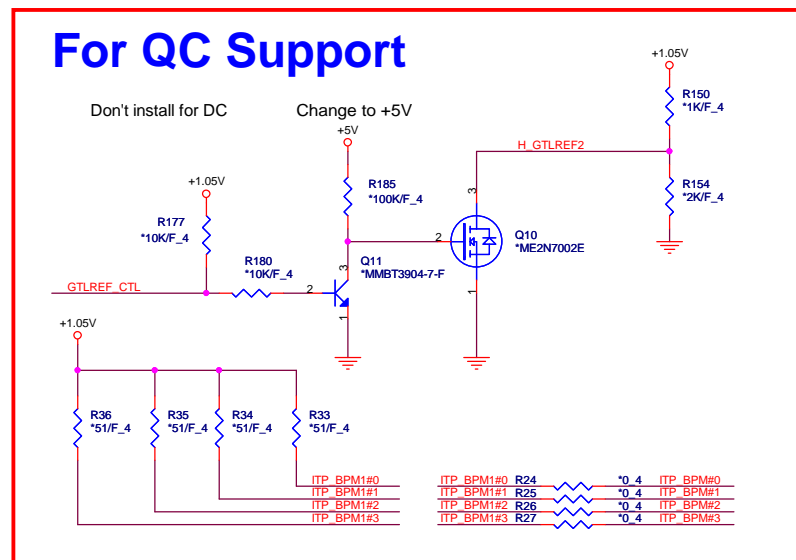


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



PROJECT : UT3/5
Quanta Computer Inc.

Size Custom	Document Number Clock Generator	Rev PV
Date: Monday, October 20, 2008	Sheet 2 of 43	



	COMP0/2	COMP1/3
Qual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Guard Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)



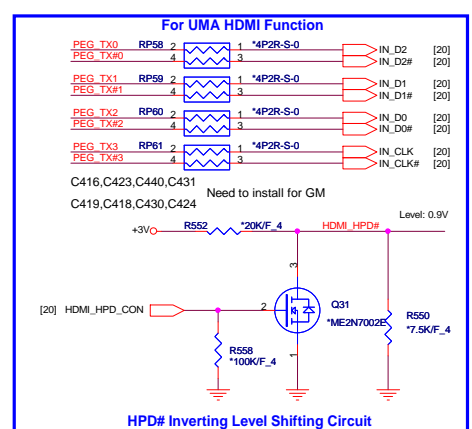
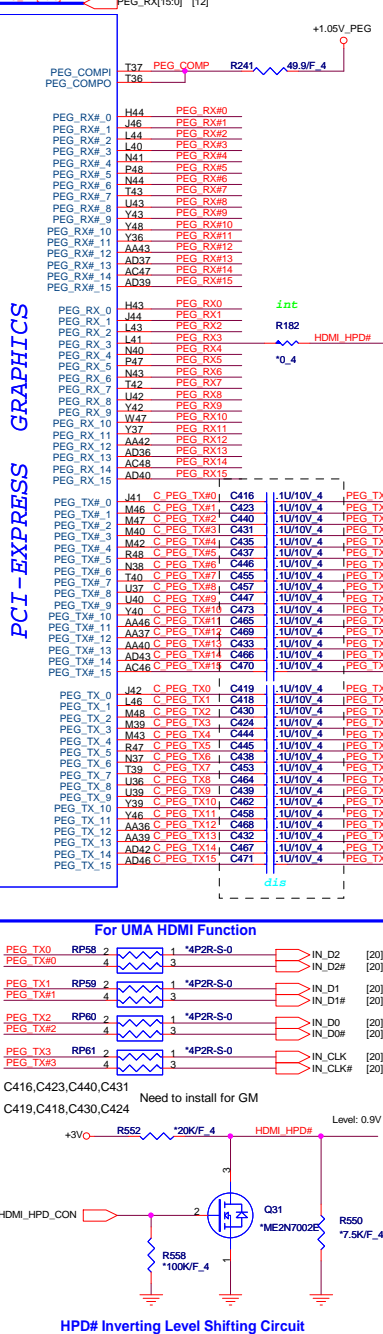
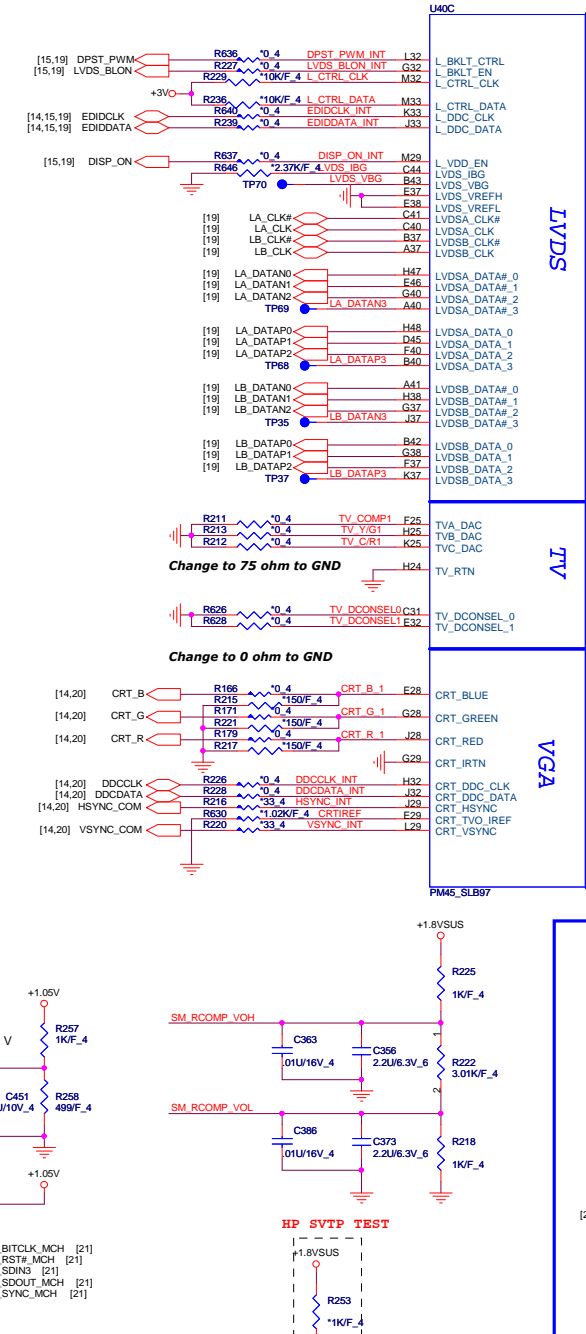
PROJECT : UT3/5
Quanta Computer Inc.

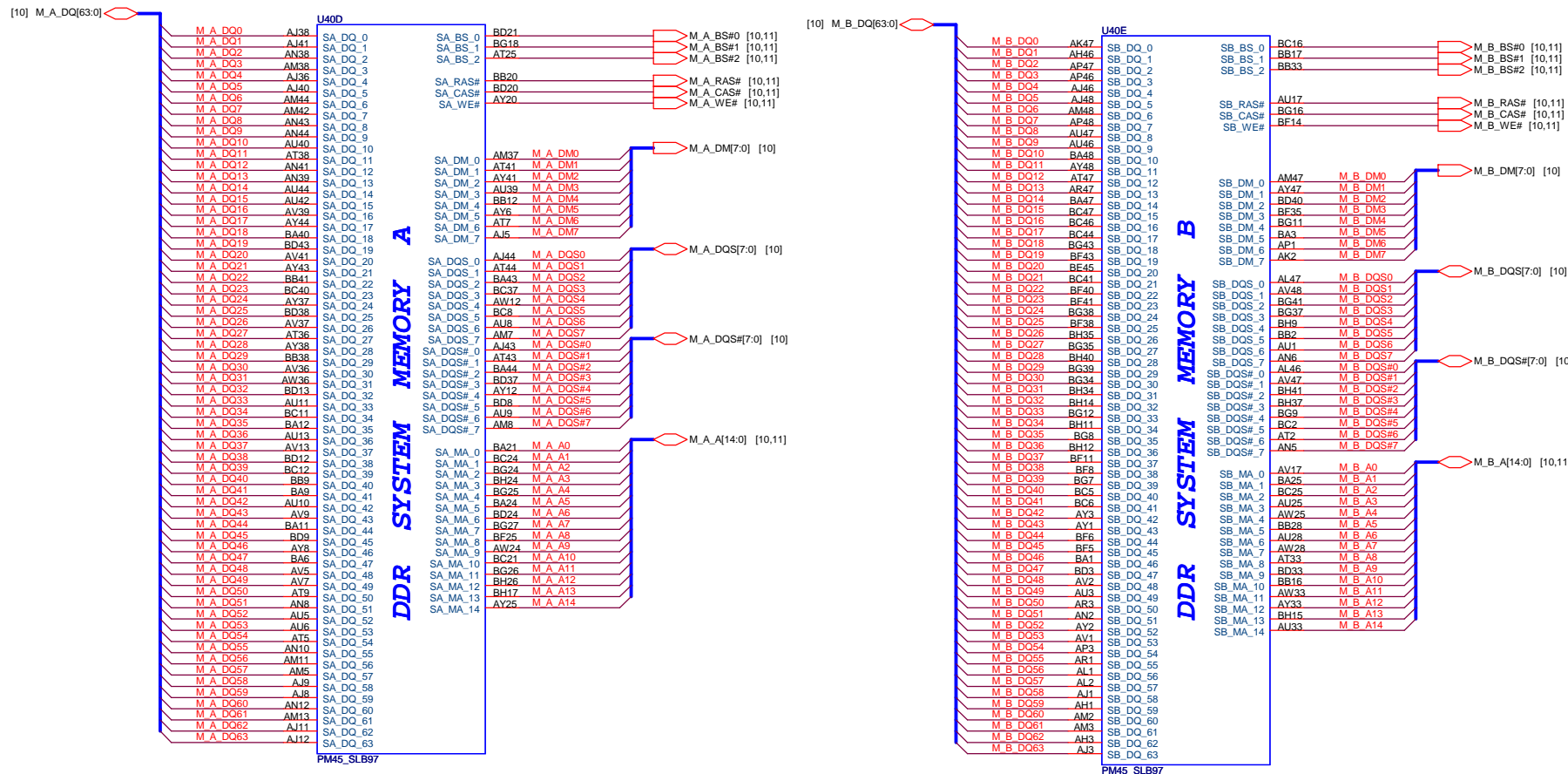
Size Custom	Document Number Penryn 1/2	Rev PV
Date: Monday, October 20, 2008	Sheet 3 of 43	





6



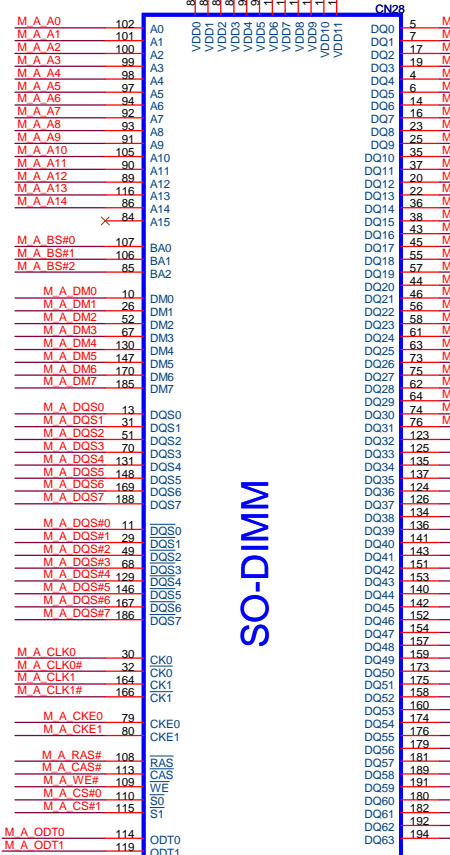
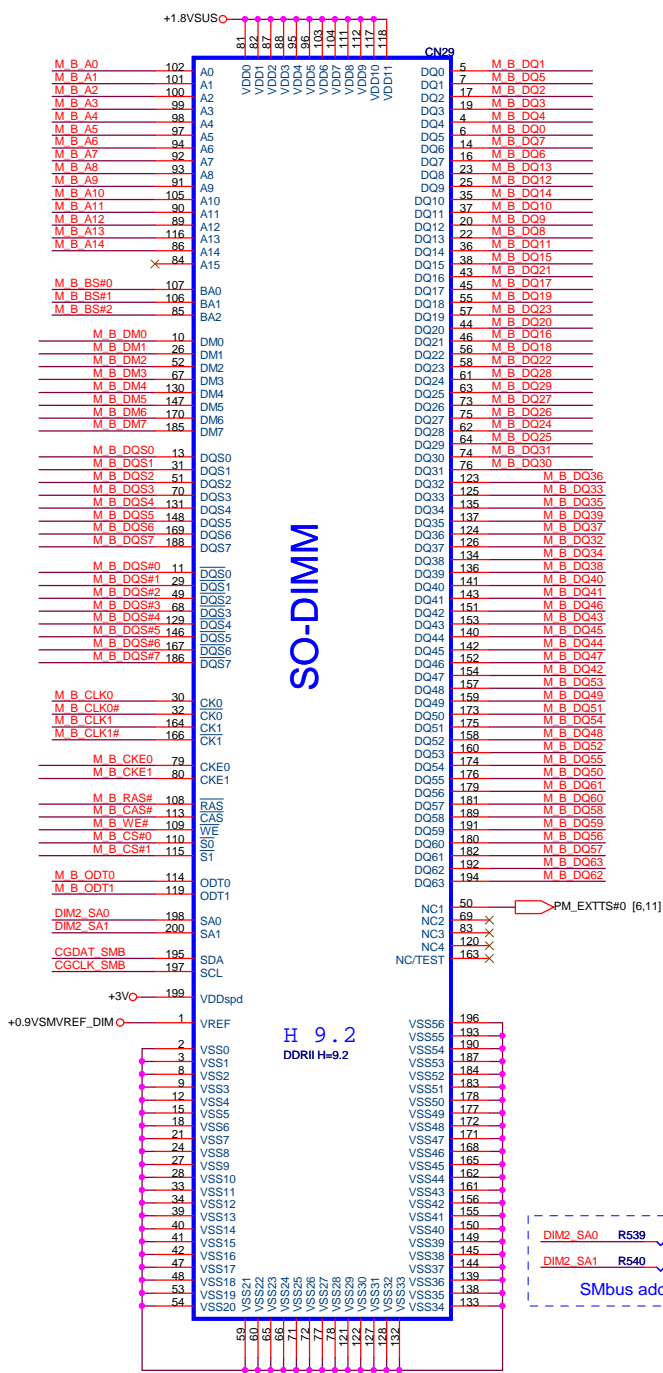
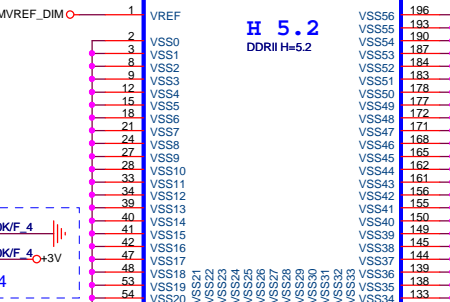
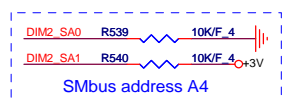
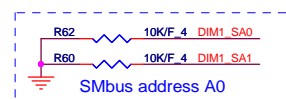
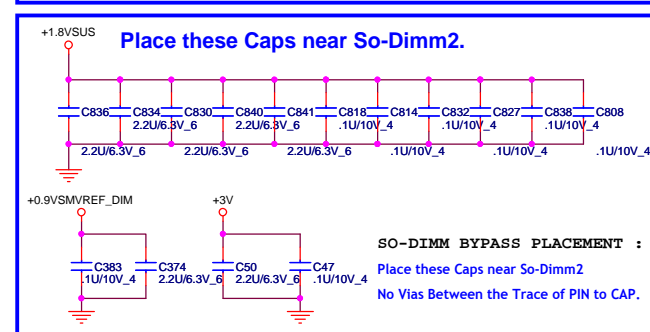
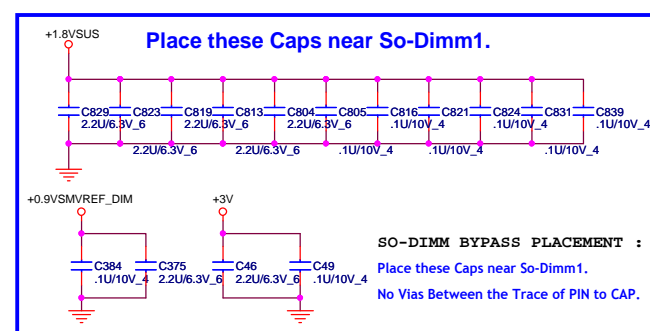
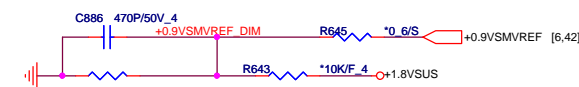
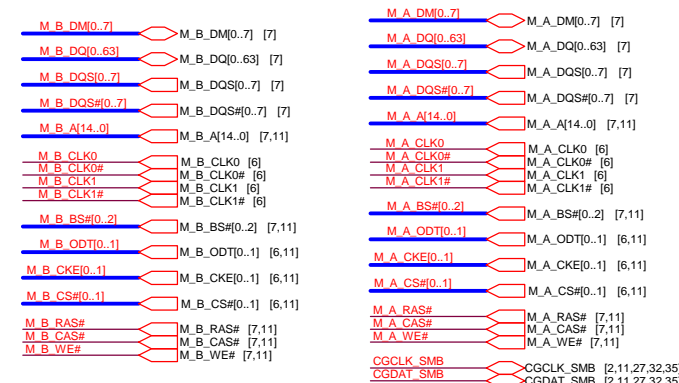


PROJECT : UT3/5
Quanta Computer Inc.

Size Custom Document Number Cantiga DDR2 3/5 Rev PV
Date: Monday, October 20, 2008 Sheet 7 of 43

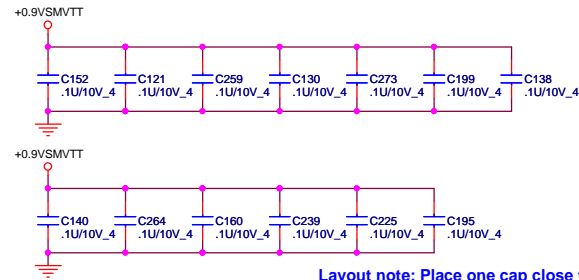






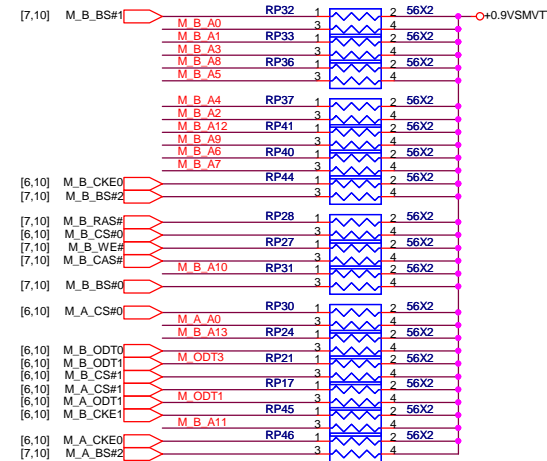
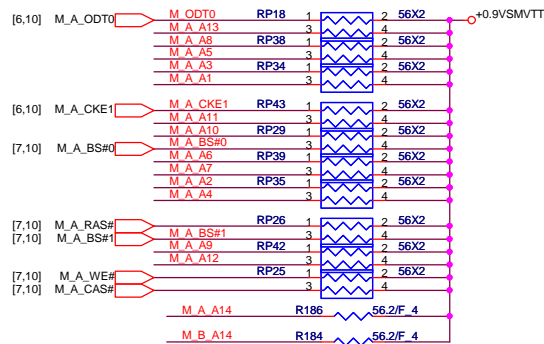
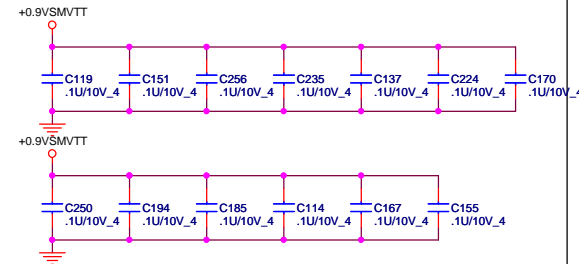
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

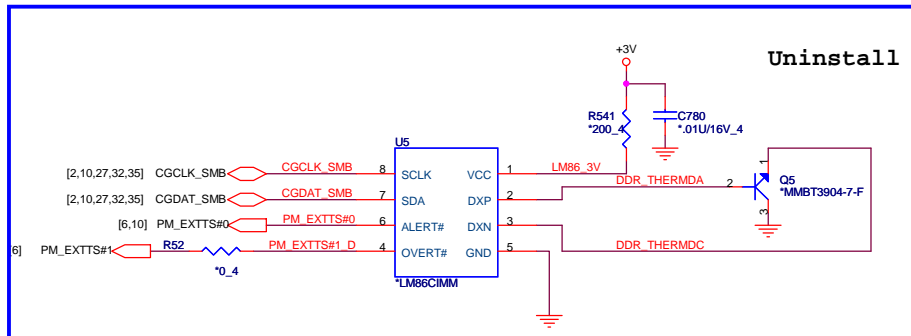


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

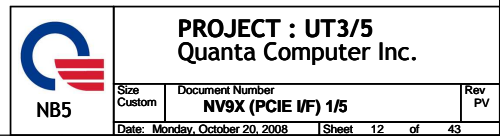
DDRII B CHANNEL



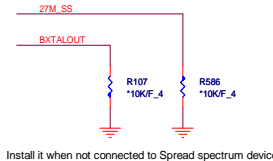
M_B_A[14..0] M_B_A[14..0] [7,10]
M_A_A[14..0] M_A_A[14..0] [7,10]

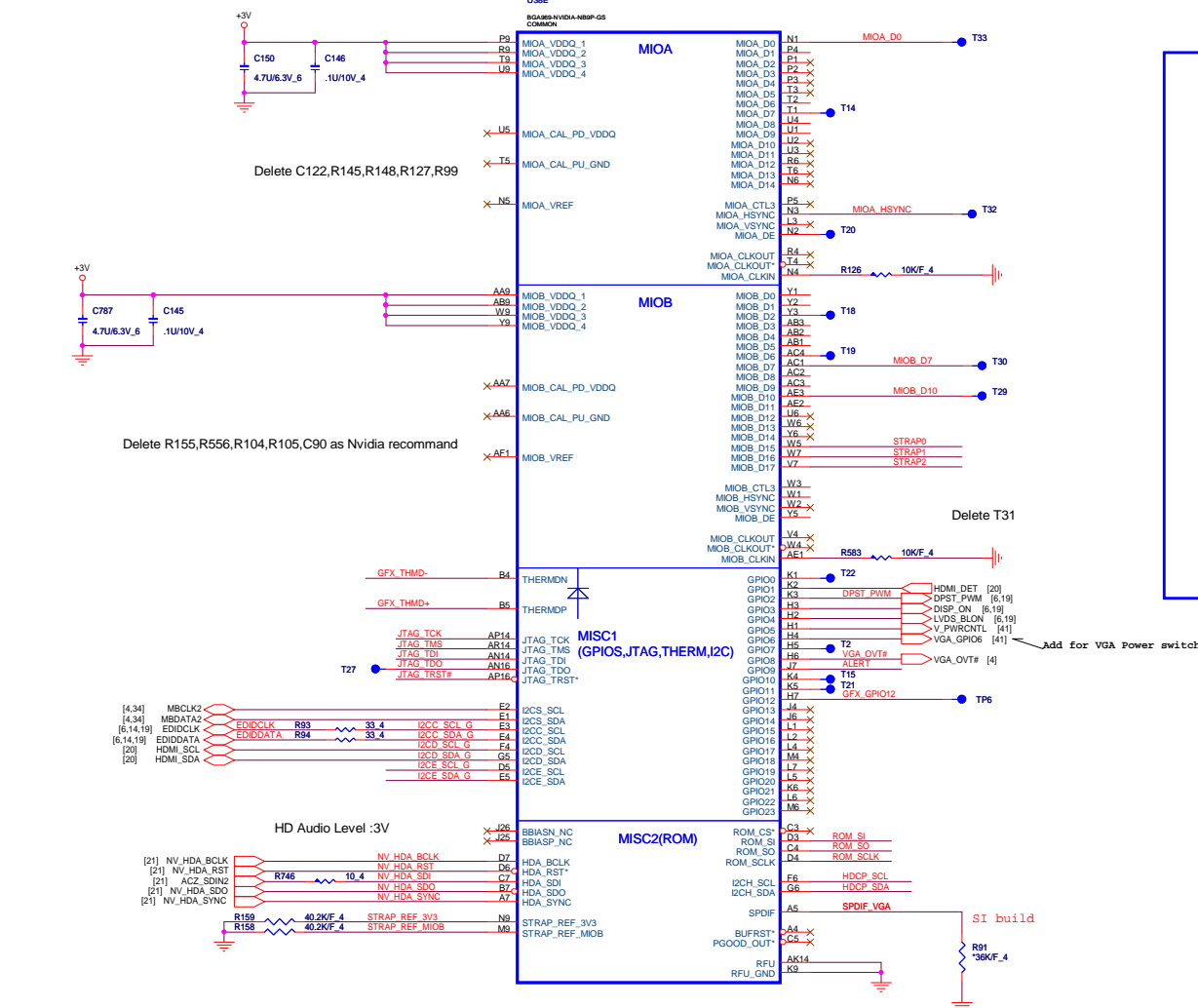


+0.9VSMVTT [42]
+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]



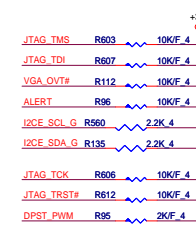
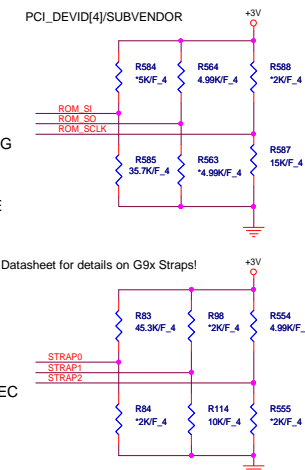






NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

1000
0010
XXXX
XXXX
0001
1111

PCI_DEVID: **STRAP2 R554**

NB9M-GE 0x06E 8 1000 PU 5K
NB9M-GS 0x06E 9 1001 PU 10K
NB9P-GE2 0x064 8 1000 PU 5K
NB9P-GS 0x064 9 1001 PU 10K

CS33012FB18 RES CHIP 30.1K 1/16W +-1% (0402)
CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)
CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

RAM ID: **ROM_SI R585**

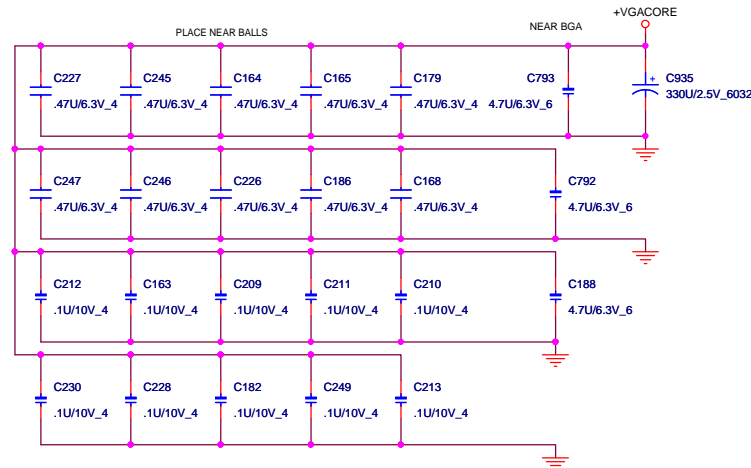
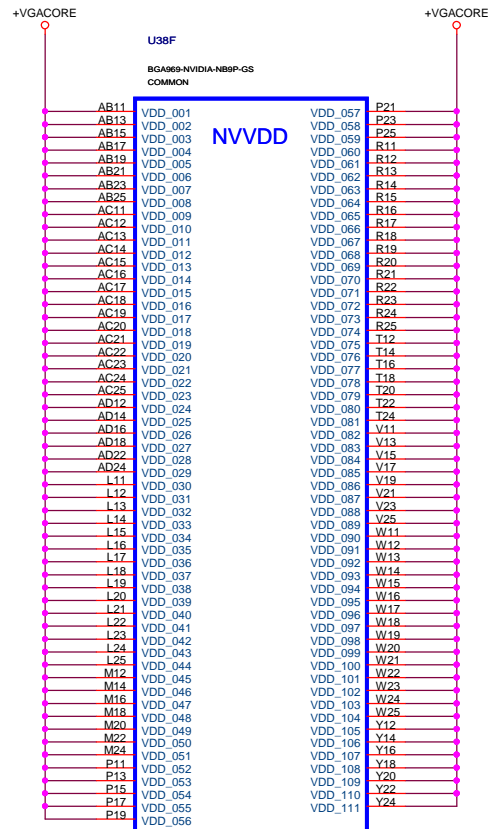
32M*16 SAM 0101 PD 30.1K
QIM 0110 PD 35.7K
HYN 0111 PD 45.3K
64M*16 HYN 0000 PD 5K
SAM 0001 PD 10K



PROJECT : UT3/5
Quanta Computer Inc.

Size C	Document Number	Rev PV
	NV9X (GPIO & STRAPS) 4/5	
Date: Monday, October 20, 2008	Sheet 15 of 43	

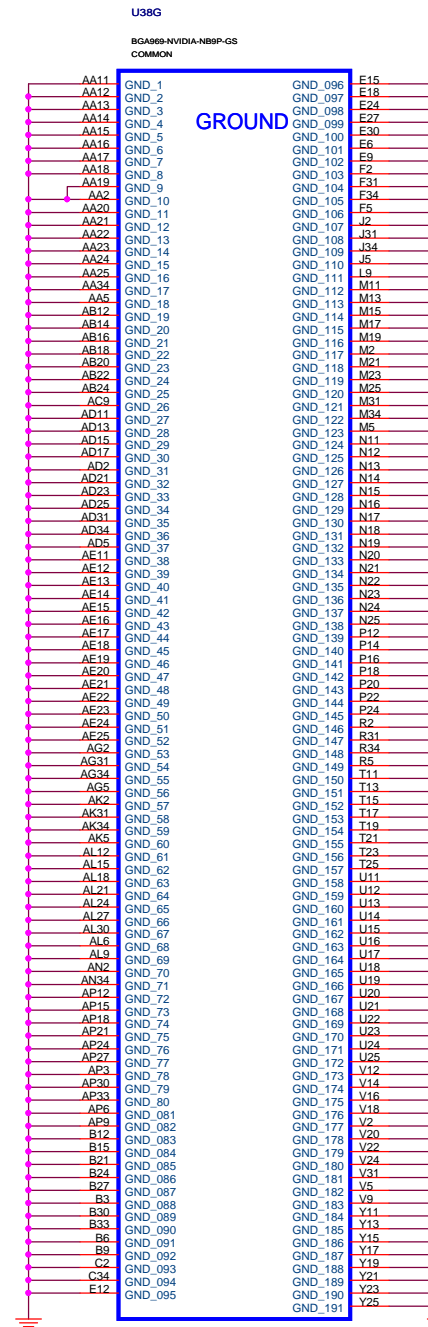
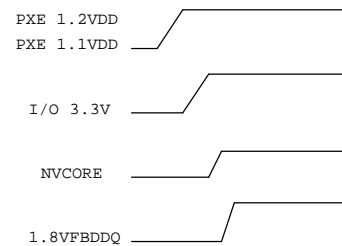
NVVDD Decoupling

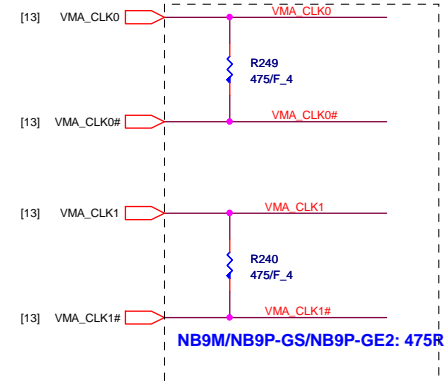
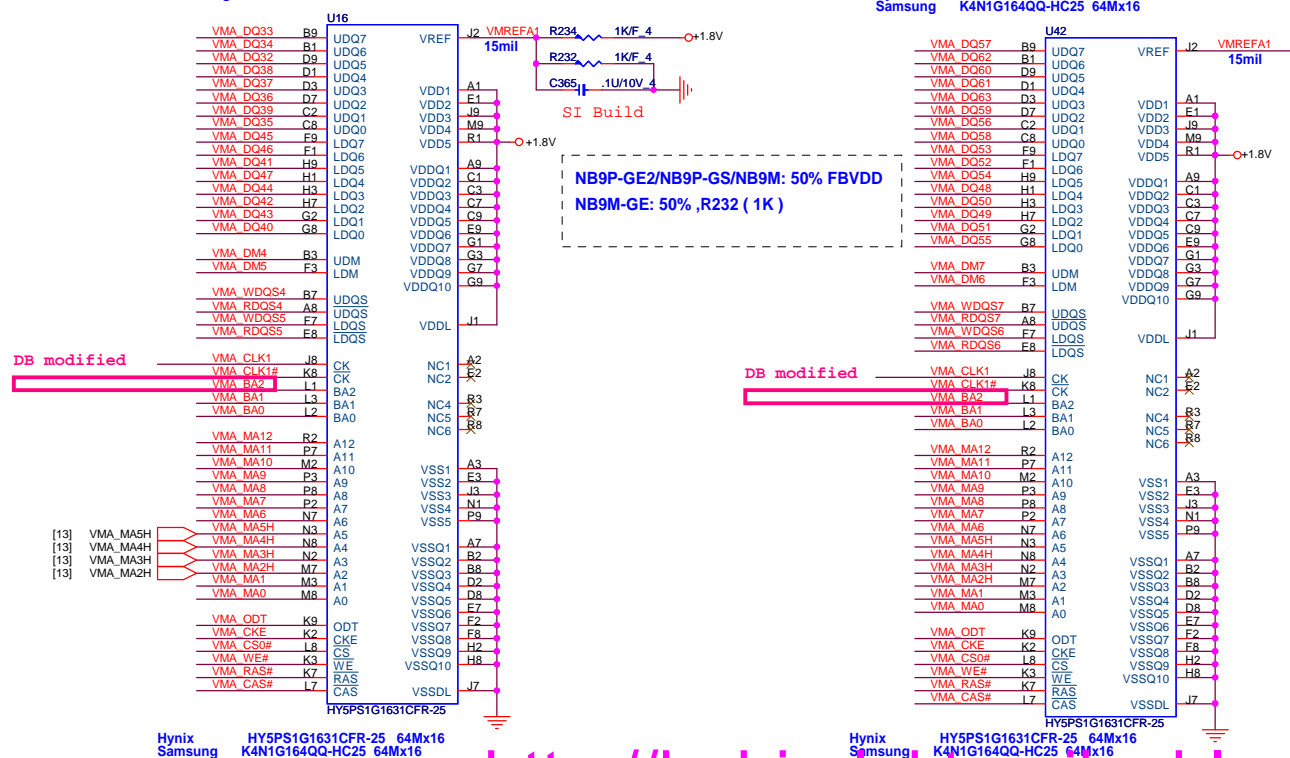
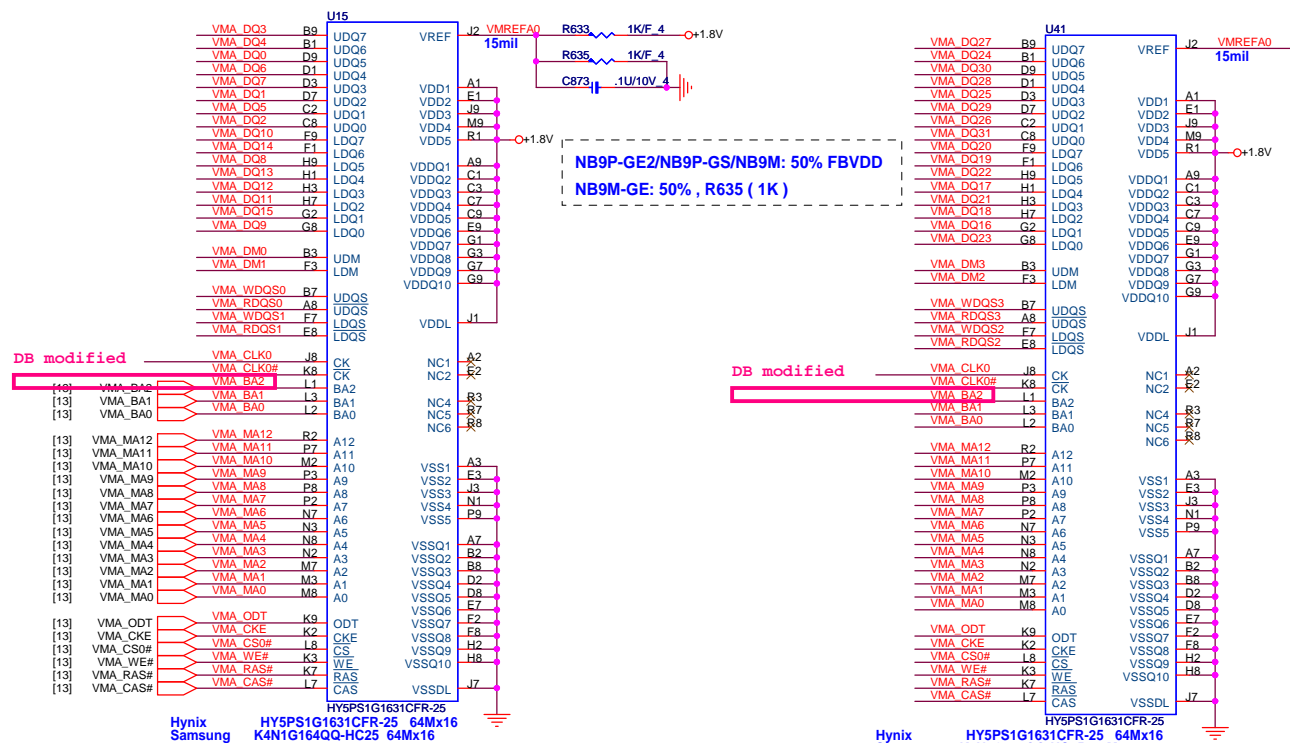


Follow Design Guide DG-03276-001 4.7uFx3
and 0.47x10 uF instead of 0.1uF x10

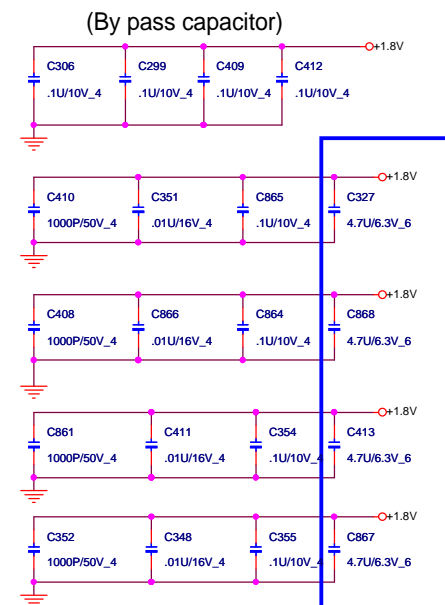
NB9M: VGACORE +0.90V (Normal) , +1.09V



power up sequence











CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



[13] VMA_DQ[63..0]  

[13] VMA_DM[7..0]  

[13] VMA_WDQS[7..0]  

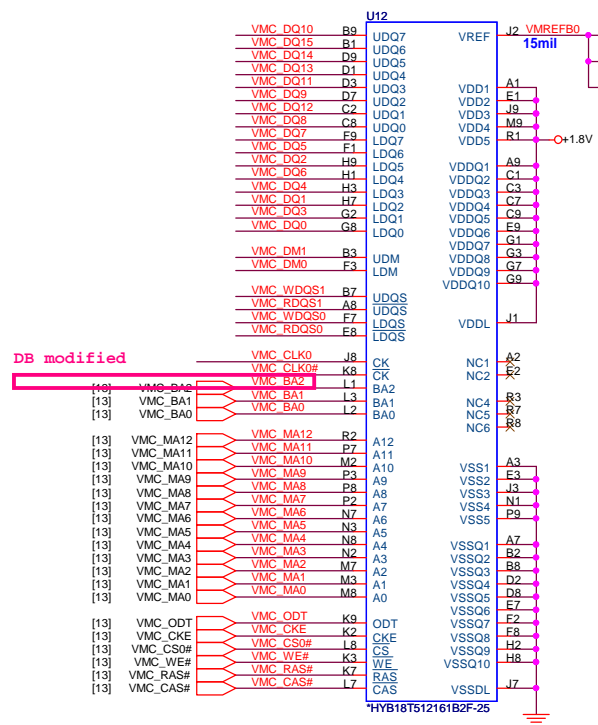
[13] VMA_RDQS[7..0]  

256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01



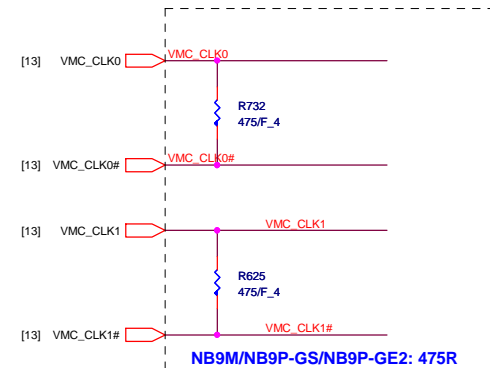
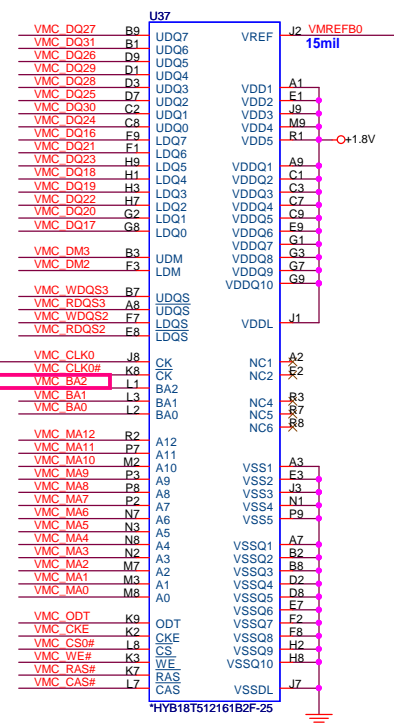
PROJECT : UT3/5
Quanta Computer Inc.

Size Custom	Document Number NV9X VRAM-1(GDDR2 BGA84)	Rev PV
Date: Monday, October 20, 2008		Sheet 17 of 43

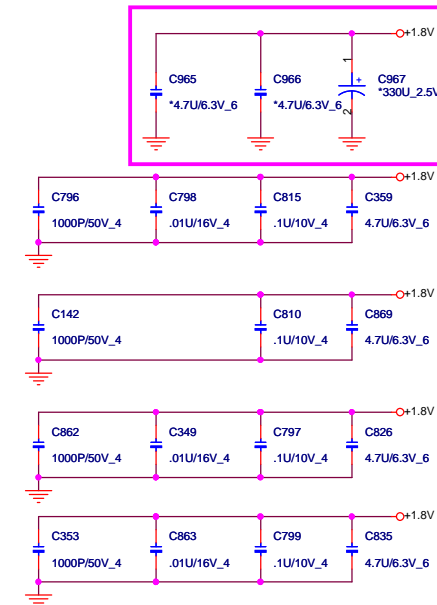


NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE:50%, R133(1K)

DB modified



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



- [13] VMC_DQ[63..0]
[13] VMC_DM[7..0]
[13] VMC_WDQS[7..0]
[13] VMC_RDQS[7..0]

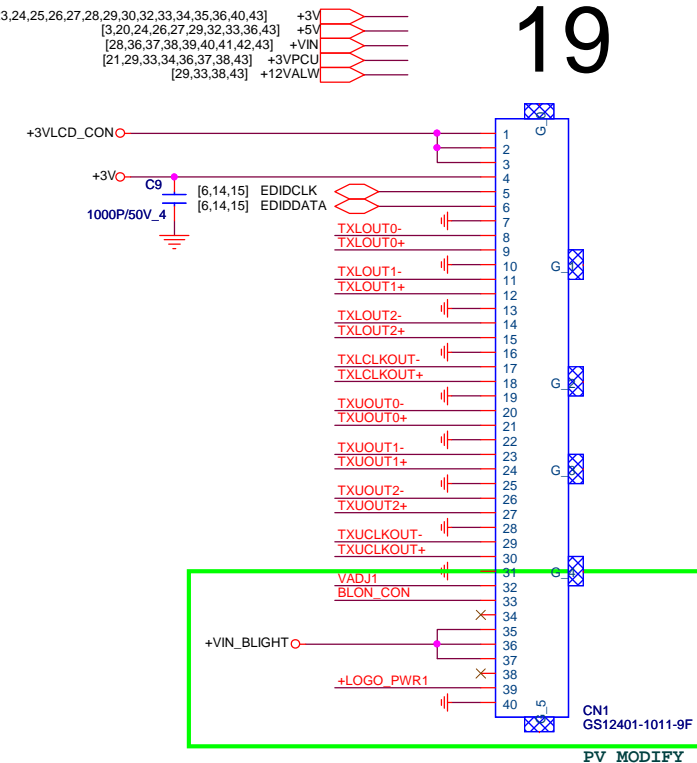
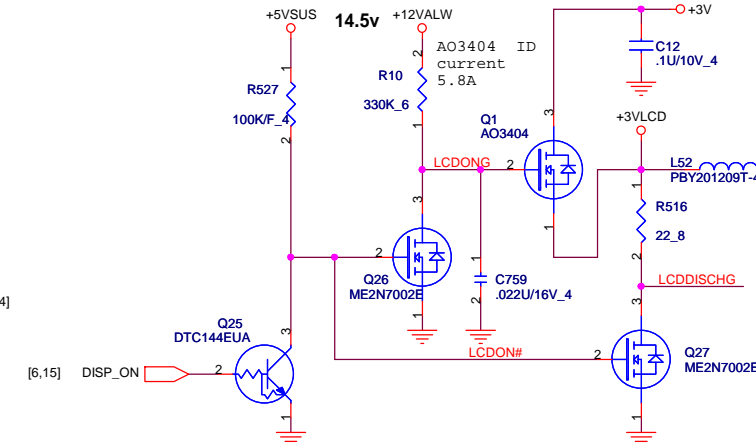
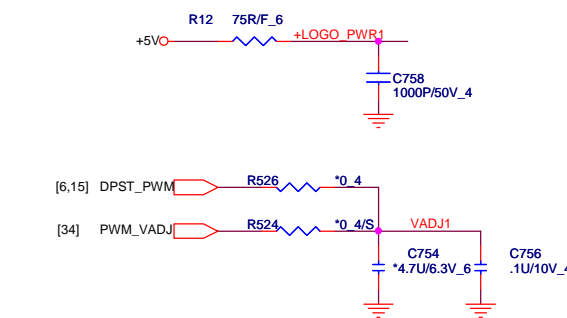
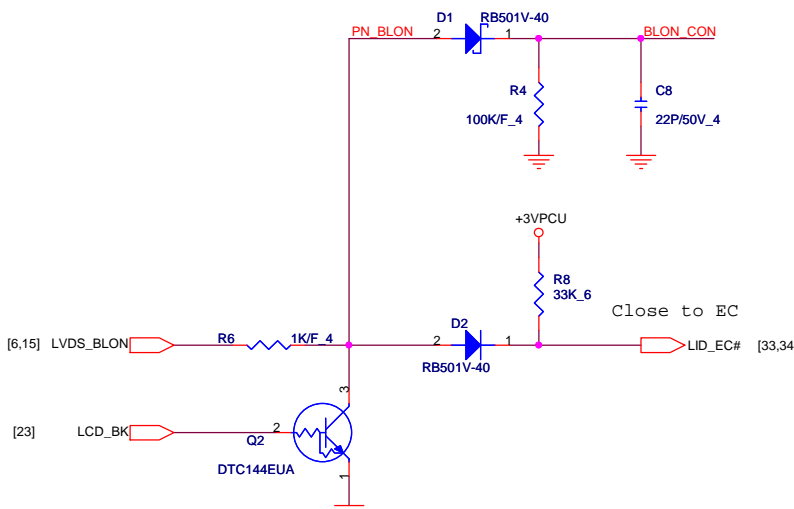
Samsung
Qimonda
Hynix



PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X VRAM-2(GDDR2 BGA84)	PV
Date: Monday, October 20, 2008	Sheet 18 of 43	

- OPTION SIGNAL FROM NB FOR UMA VGA

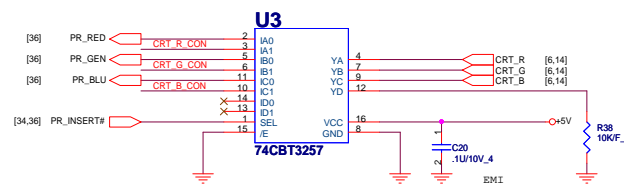


CRT PORT

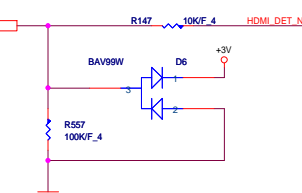
Change Layout footprint to dsb-070546fr015x68zr-15p-v

Change ESD protection to +5V

CRT SWITCH

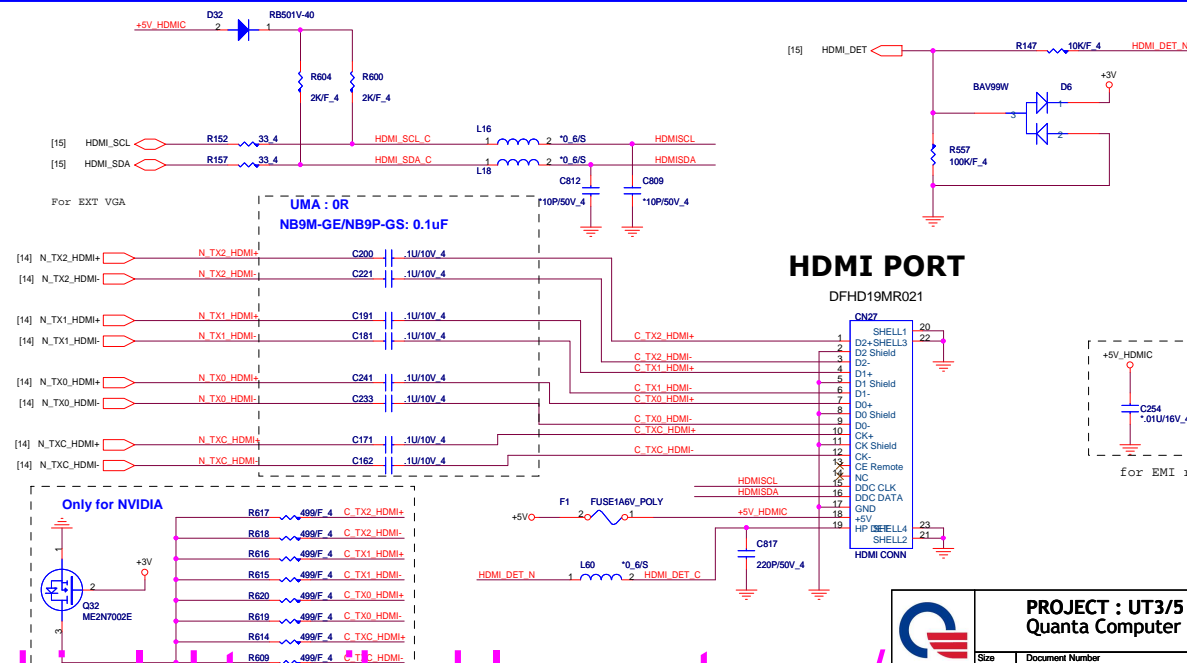


inputs	function
/E SET	
L L	Y - port 0
L H	Y - port 1
H X	Disconnect



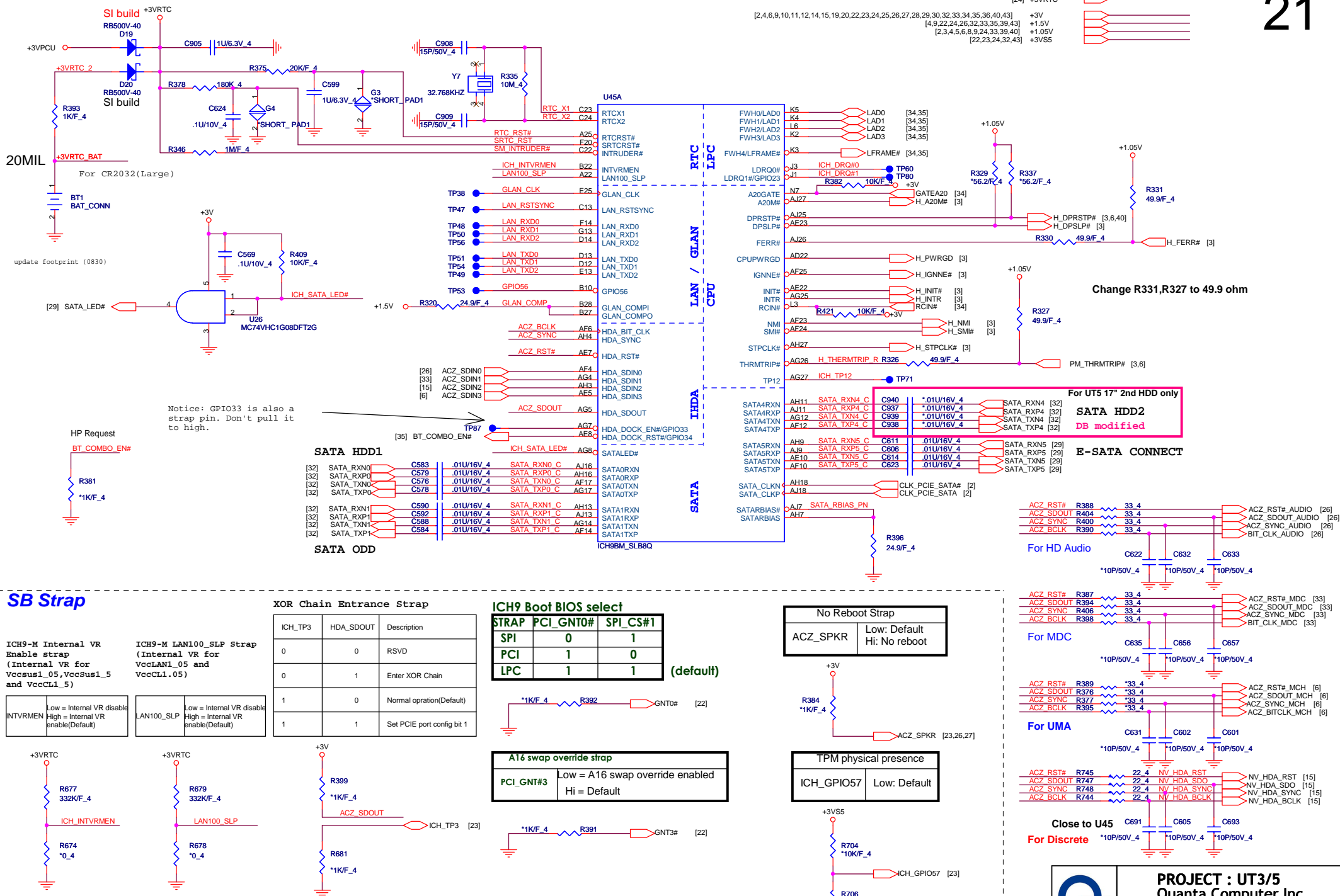
HDMI PORT

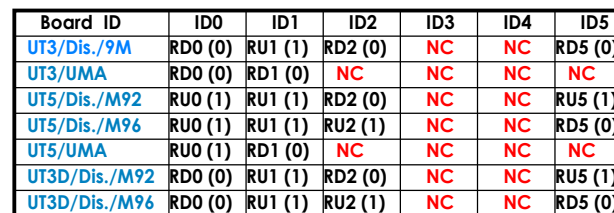
DFHD19MR021



for EMI request

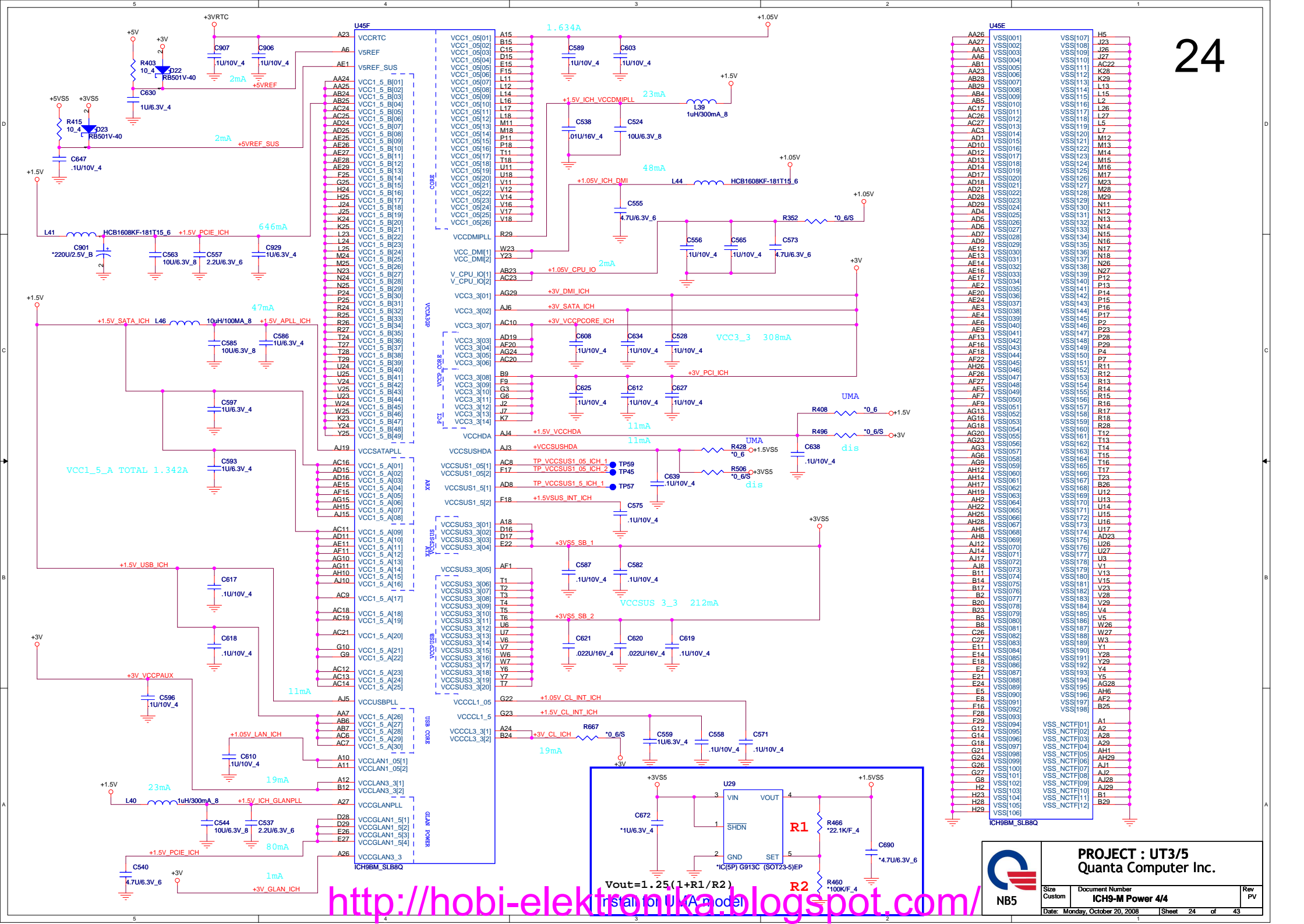
PROJECT : UT3/5
Quanta Computer Inc.

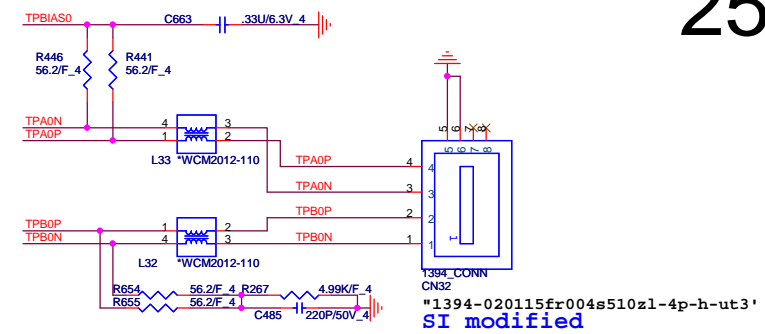
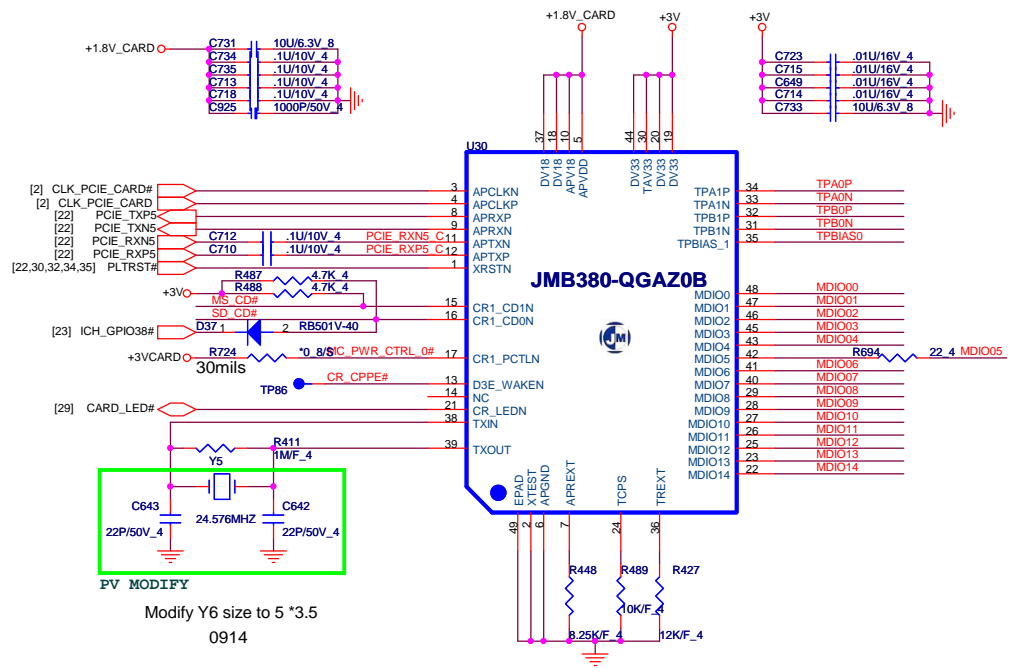




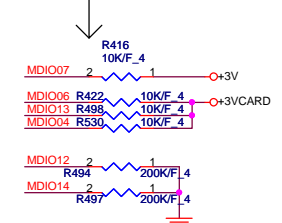
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/5	0=UT3 1=UT5					
UMA/Dis.		0=UMA 1=Dis.				
NV9M			0			0
ATI M92			0			1
ATI M96			1			0







Change to 10K

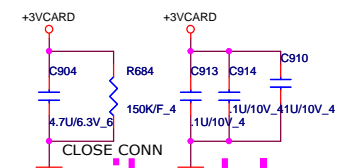
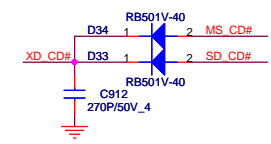
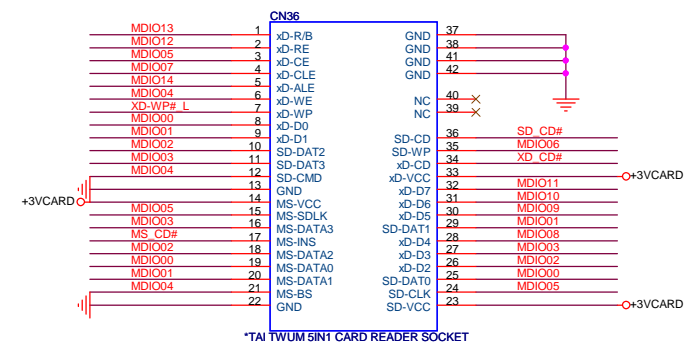
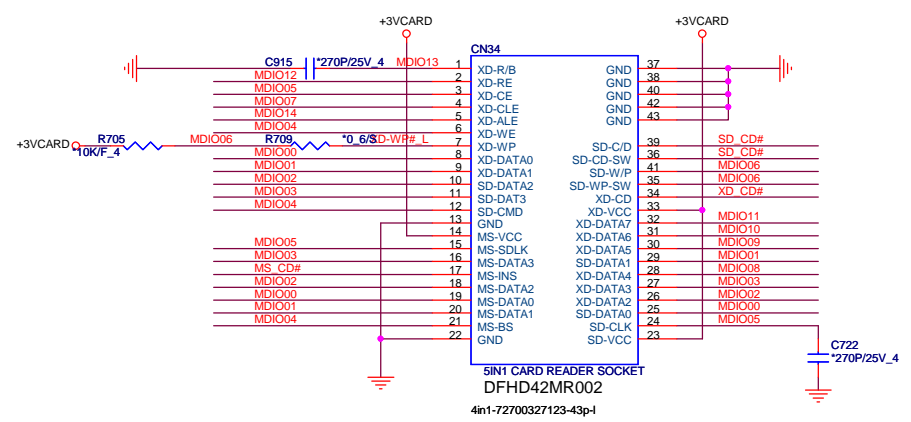


JMB 380 Note:

SD/MMC	MS	XD
MDIO0	SD DAT0	MS D0
MDIO1	SD DAT1	MS D1
MDIO2	SD DAT2	MS D2
MDIO3	SD DAT3	MS D3
MDIO4	SD CMD	MS BS
MDIO5	SD CLK	MS SCLK
MDIO6	SD WP	MS CE#
MDIO7	SD CLE	XD CLE
MDIO8	SD DAT4	XD D4
MDIO9	SD DAT5	XD D5
MDIO10	SD DAT6	XD D6
MDIO11	SD DAT7	XD D7
MDIO12	SD RE#	XD RE#
MDIO13	SD R/B#	XD R/B#
MDIO14	SD ALE	XD ALE
CR1 LEDN	SD1 LED#	MS1 LED#
CR1_PCTLN	SD1 PCTL#	MS1 PCTL#
CR1 CD0	SD1 CD#	MS1 CD#
CR1 CD1	SD1 CD#	MS1 CD#

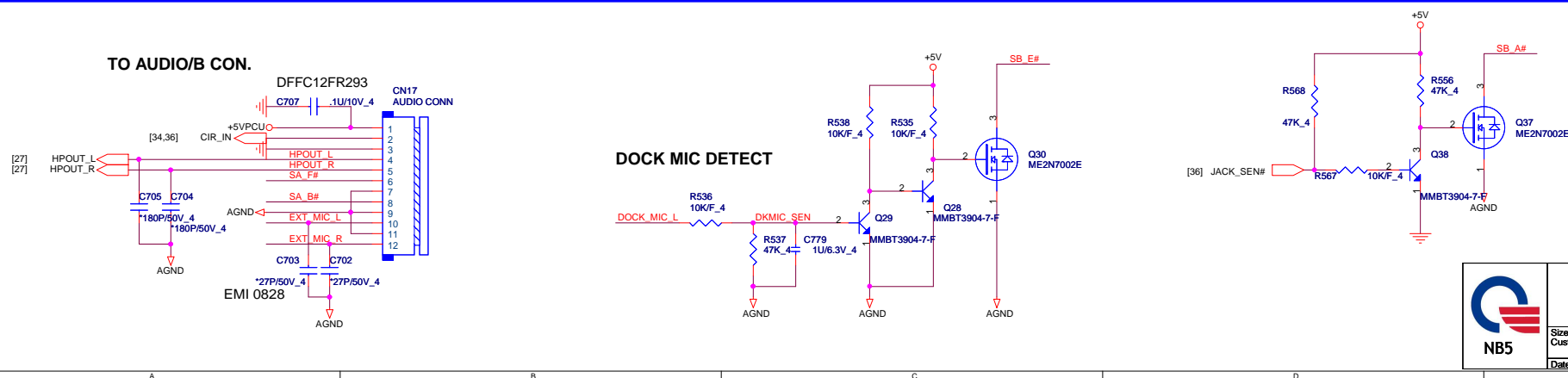
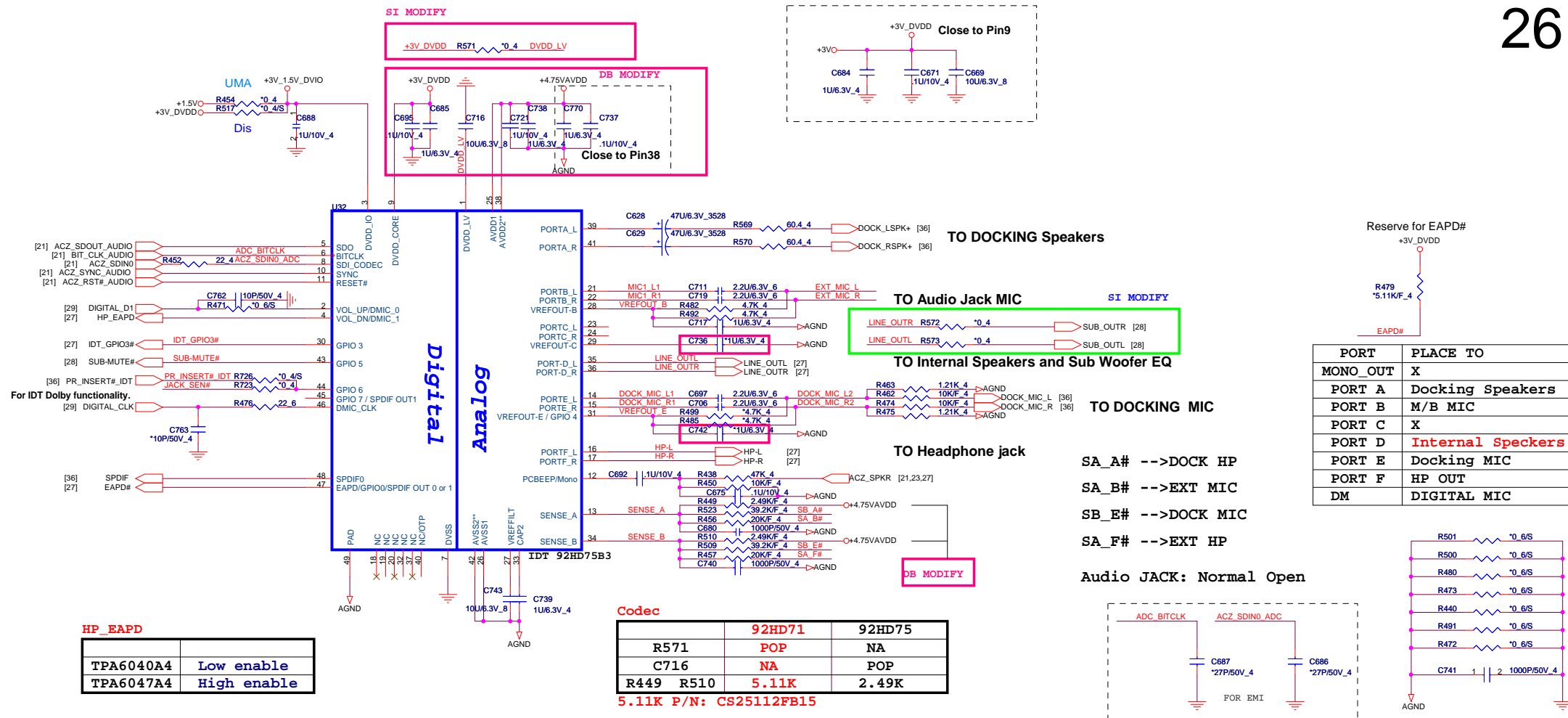
5 IN1 CARD READER

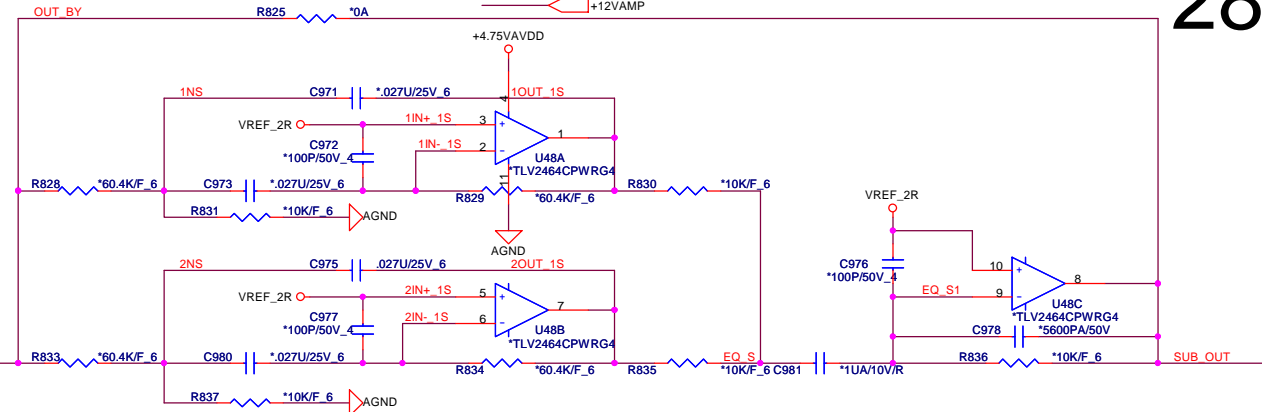
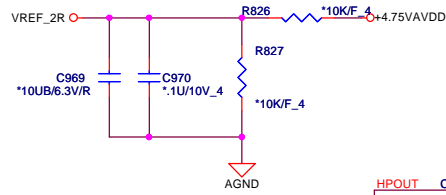
XD, MMC/SD, MS/MSP



PROJECT : UT3/5
Quanta Computer Inc.

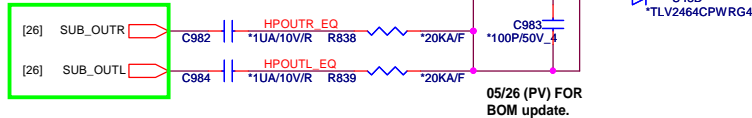
Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET & HOLE	PV
Date: Monday, October 20, 2008	Sheet 25 of 43	



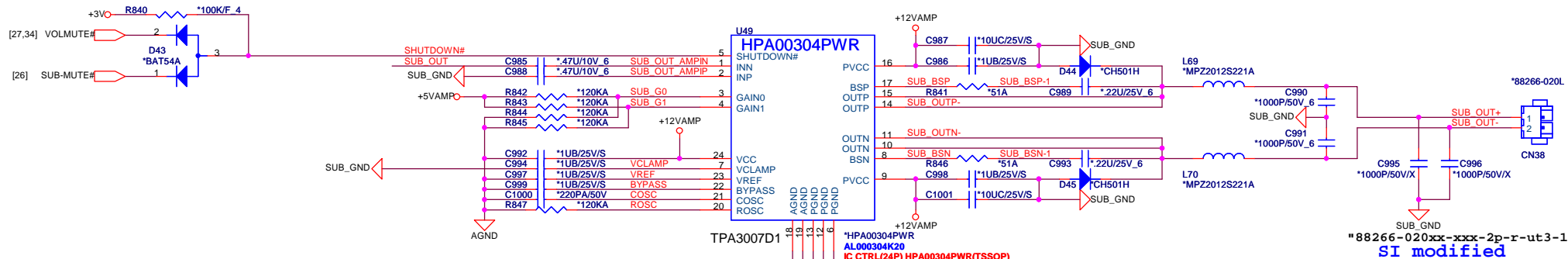


Change 4EQ to 2EQ

SI MODIFY

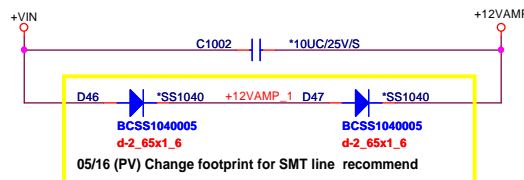


MODEL	UT5
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6

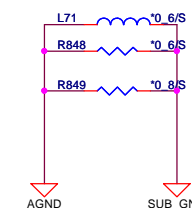


SI modified

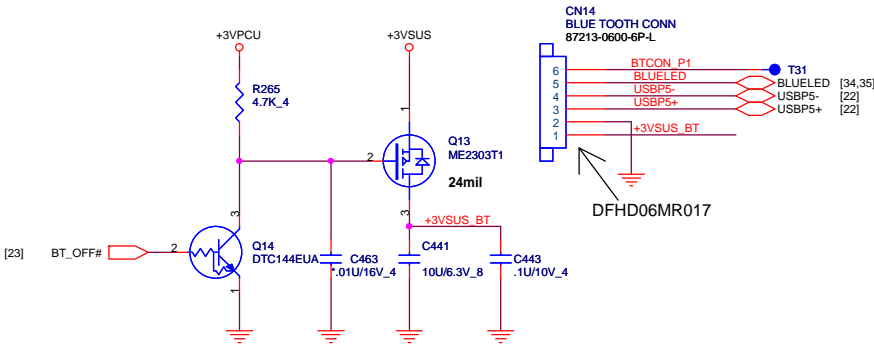
Sub-Woofer power



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

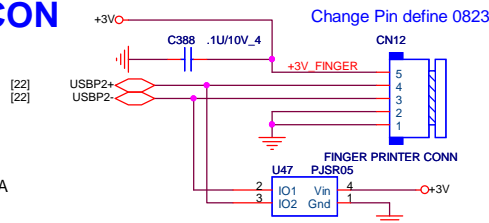


BLUETOOTH

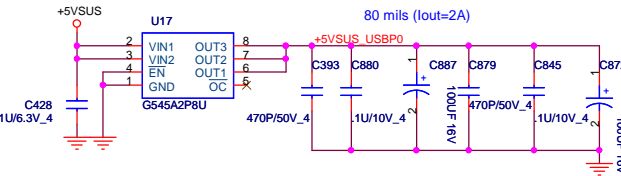


USB fingerprint CON

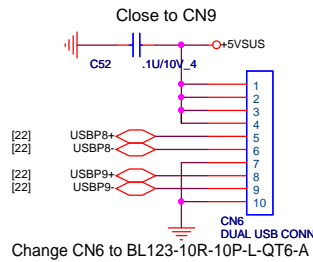
1. ESD GND
 2. SYSTEM GND
 3. USB-
 4. USB+
 5. USB PWR(+3V)
- Change CN12 to BL123-05R-5P-L-QT6-A
Add U47 for Finger print USB signal



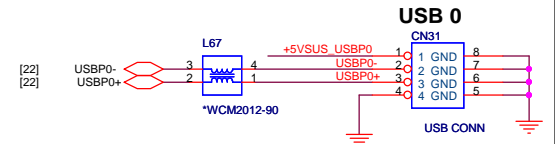
LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



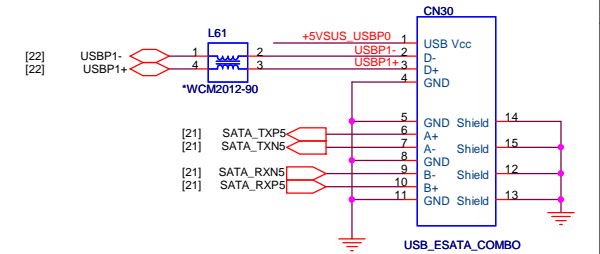
29



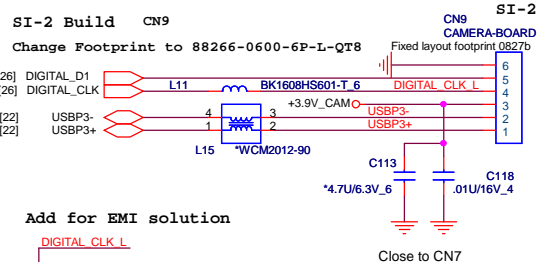
SI modified

usb-020173mr004s51-4p-r-h-ut3

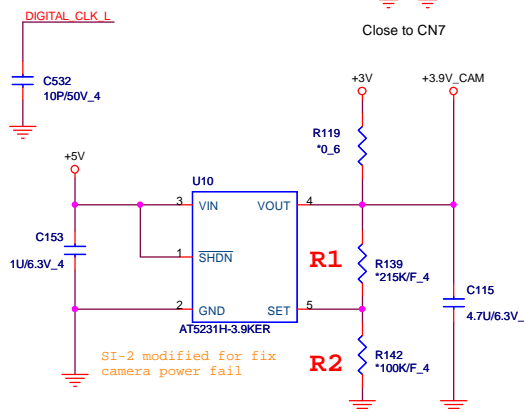
USB & ESATA



USB CAMERA /DIGITAL MIC CONNECT

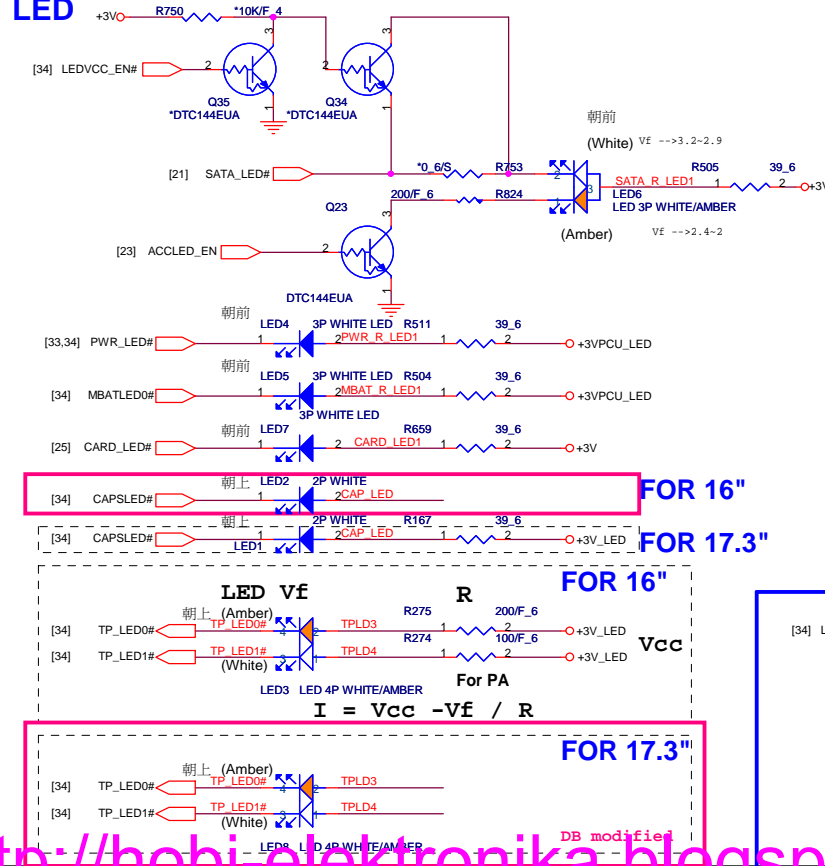


Add for EMI solution



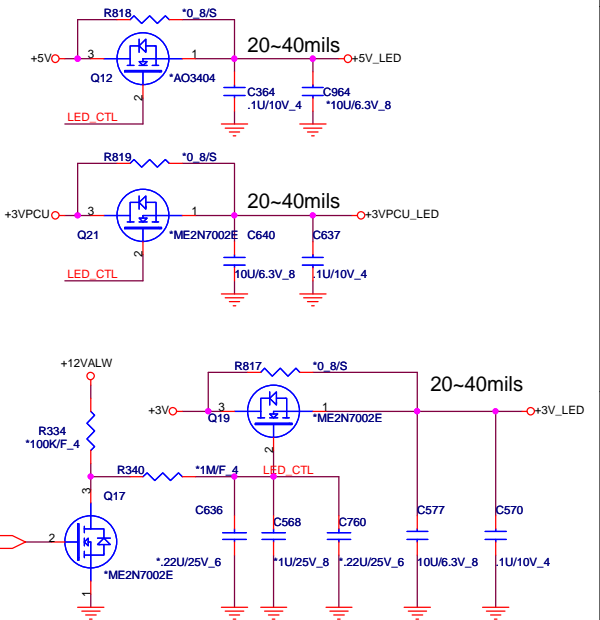
$$V_{out} = 1.25(1 + R1/R2)$$

LED



LED PWR CONTROL

Change Q12 to AO3404 as LED current limited



PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/TS/ESATA/USB	PV
Date: Monday, October 20, 2008	Sheet 29 of 43	

E : Stuffed for 8101E/8102E(10/100)

Stuffed for 8102E

Stuffed for RTL8111C and nostuff 8102E

Stuffed for 8102E/RTL8111C

Stuffed for RTL8111C(10/100/1000)

```
Isolate pull low:
1.Can only disable RTL8111C.
2.RTL8101E can't disable
```

Swap PCIE from Port 6 to PCIE Port 1

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)

Stuffed for RTL8101E

Add C898,C899,C900,C902 as HP request

RJ45



Size Custom	Document Number RTE111C/8101E/RJ45	Re F
Date: Monday, October 20, 2008	Sheet 30 of 43	

<http://hobi-elektronika.blogspot.com>

T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

LANVCC
1.2W
364mA

Power trace Layout 寬度> 30mil

C454 .1U/10V_4 C475 .1U/10V_4 C477 .1U/10V_4 C399 .1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

+3V_A_LAN

C401 .1U/10V_4 C434 .1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)

+CTRL18 will become to switch power phase

**L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%**

placement close to lan chipset

Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

+CTRL18

SI Build

L65 4.7UH_2016

C884 4.7U/6.3V_6

For 8102E

C931 10U/6.3V_8

C930 10U/6.3V_8

C881 4.7U/6.3V_6

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

C876 4.7U/6.3V_6

C878 .1U/10V_4

Remove R250,L63,L66 -->For 8102E

STUFF 100 ohm BEAD

R250 100 ohm

+LAN_A1.8

C422 Change to 1u for 8102E

C421 .1U/10V_4

C422 1U/6.3V_4

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

Only For 8111C application

C422 change to 1uf

+CTRL15

For 8102E

C474 .1U/10V_4 C479 .1U/10V_4 C459 .1U/10V_4 C456 .1U/10V_4 C472 .1U/10V_4 C461 .1U/10V_4 C476 .1U/10V_4 C415 .1U/10V_4 C478 .1U/10V_4 C400 .1U/10V_4

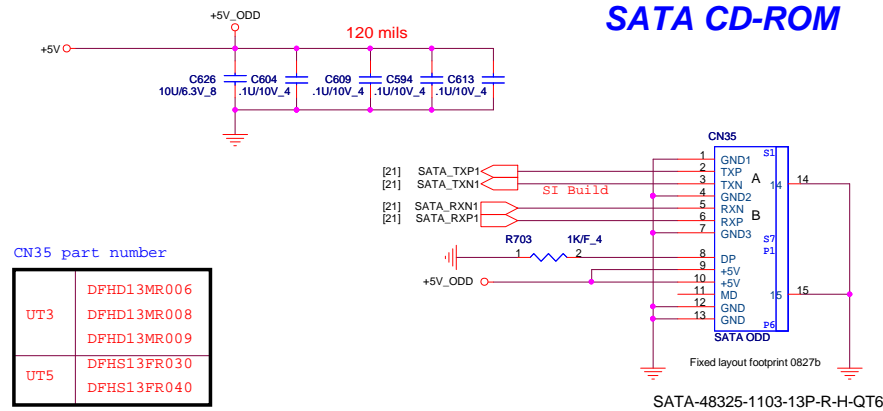
these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 38, 41, 43, 49, 52 and 58.placement close lan chip



PROJECT : UT3/5
Quanta Computer Inc.

Size A3	Document Number	Rev PV
Date: Monday, October 20, 2008	LAN Power	
Sheet 31	of 43	

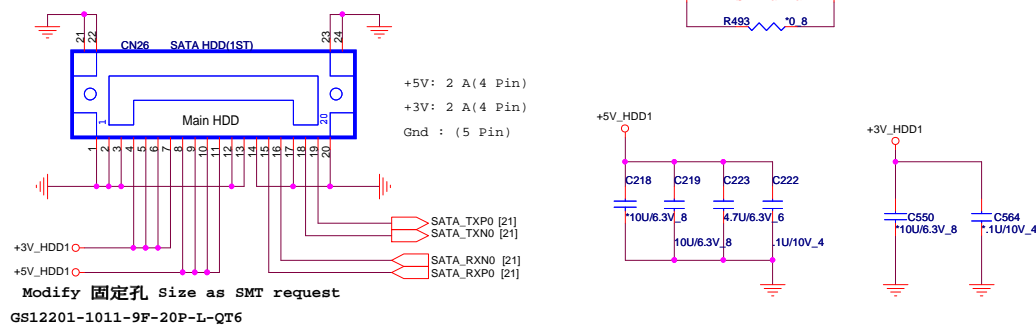
SATA CD-ROM



SATA HDD CONNECTOR

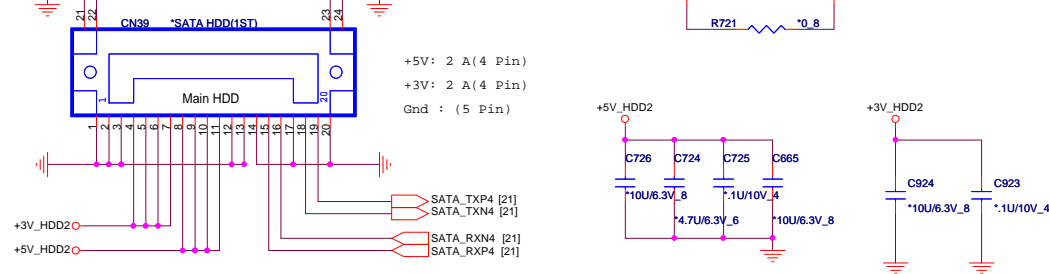
DFHD20MR005

DC Current rating: 0.5 A



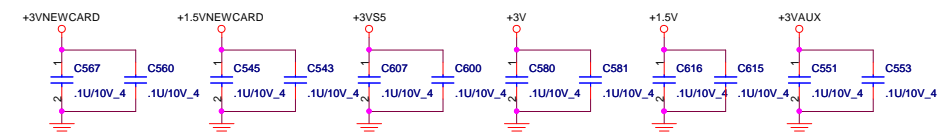
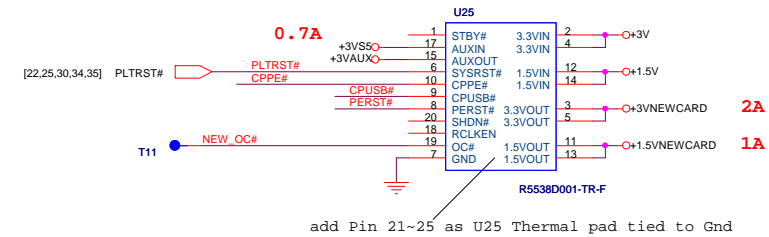
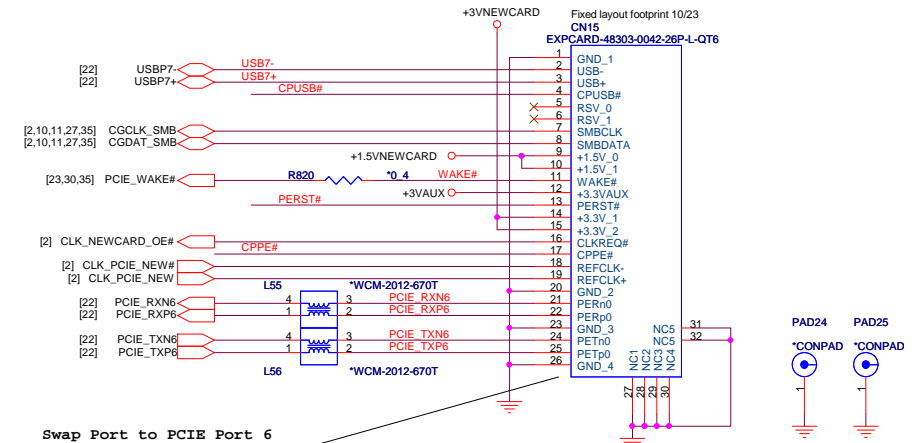
SATA_2 CONNECTOR

DC Current rating: 0.5 A



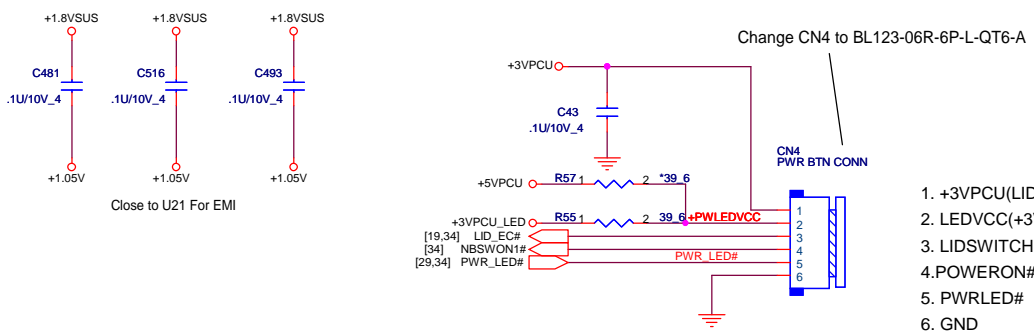
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



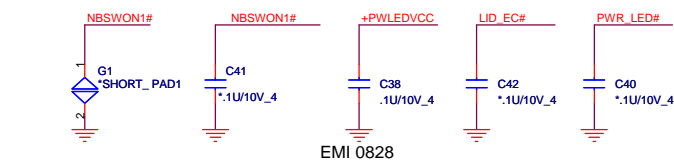
	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

NB5	PROJECT : UT3/5 Quanta Computer Inc.		
	Size Custom	Document Number ODD/HDD/NEW CARD	Rev PV
	Date: Monday, October 20, 2008	Sheet 32 of 43	

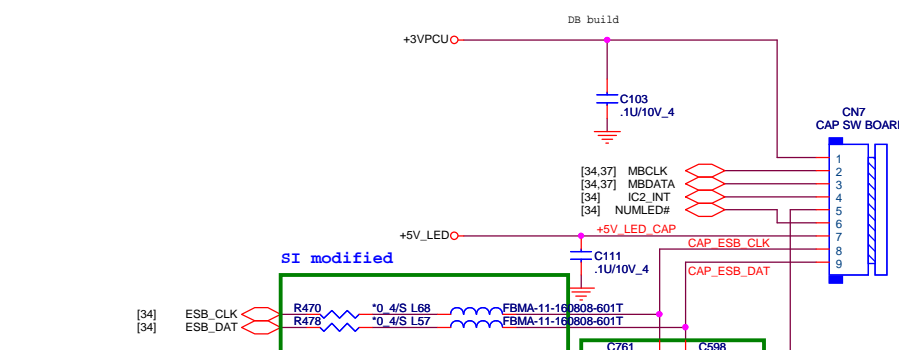


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

POWER BOTTOM CONNECT

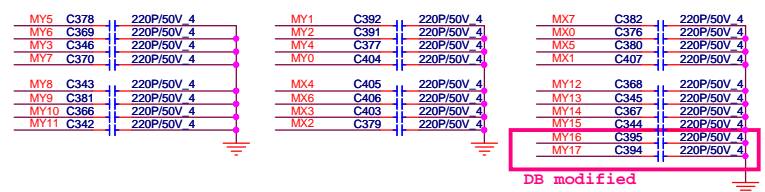
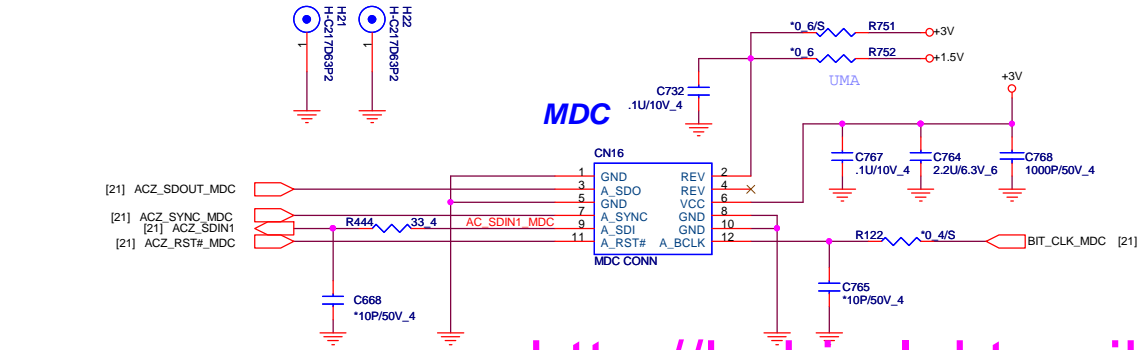


POWER SW CONNECT

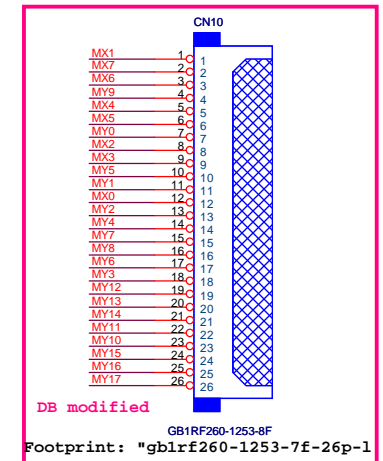
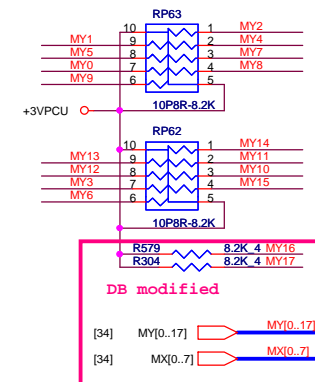


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

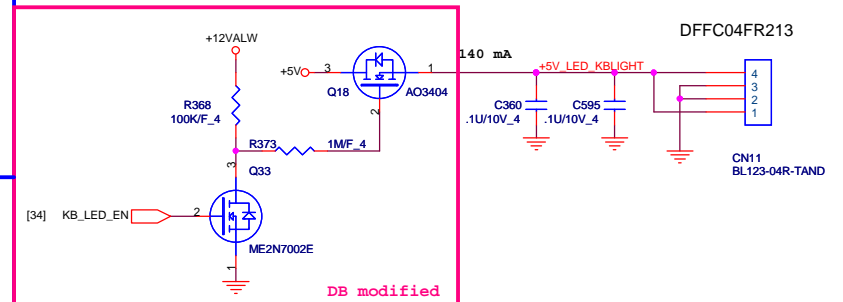
Modem CONN

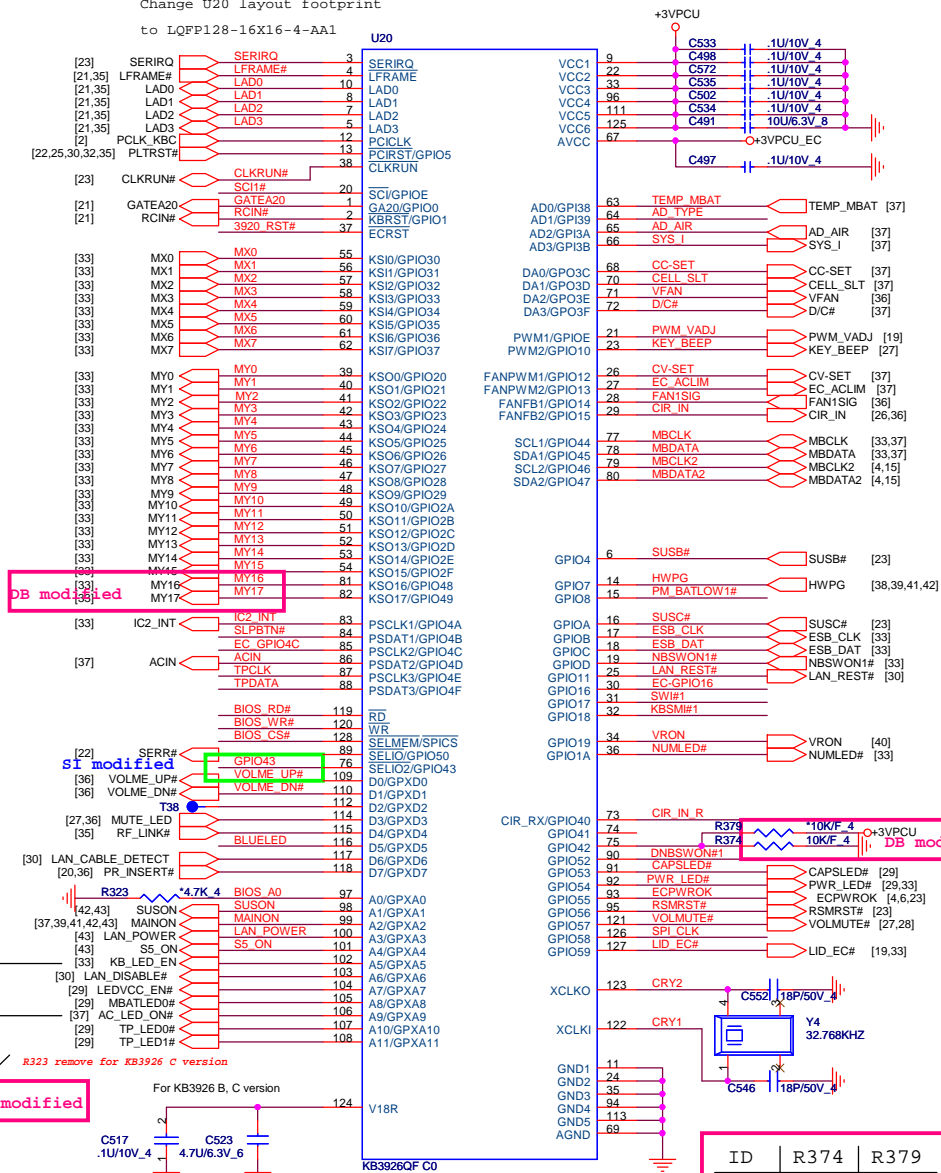


KEYBOARD PULL-UP



clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

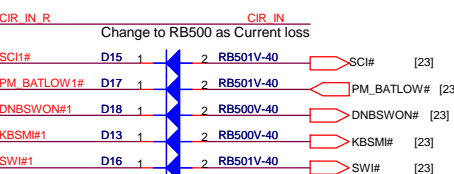
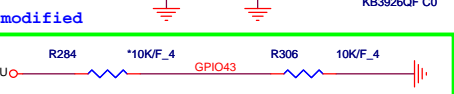




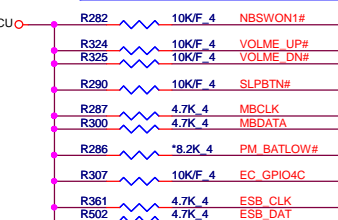
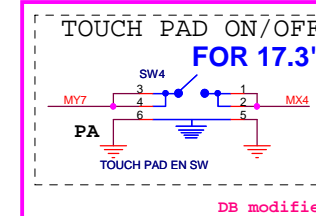
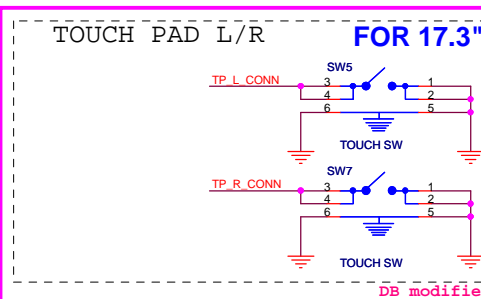
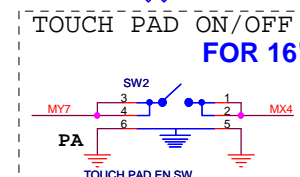
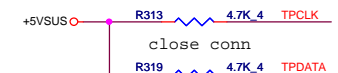
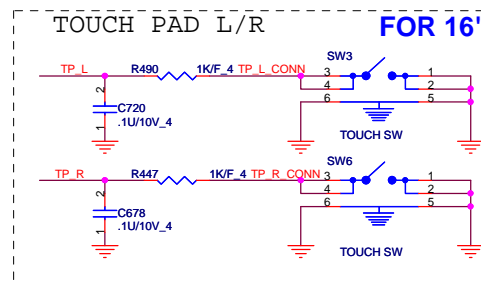
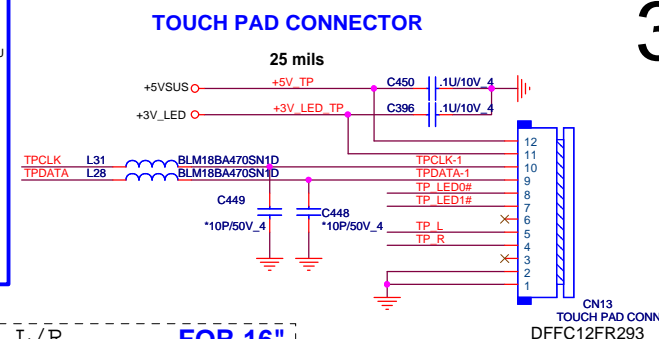
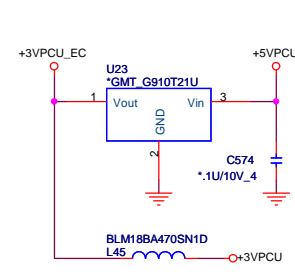
ID	R374	R379
UT3	10K	N/A
UT5	N/A	10K

Hi ==> 120W

Low ==> 65W/90W



Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM

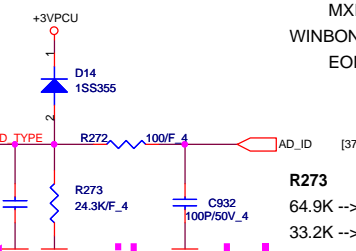


Socket: DG008000031

MXIC AKE38FP0Z00

WINBOND AKE38ZP0N01

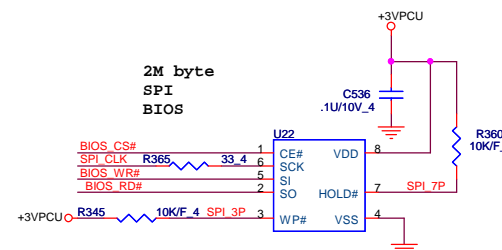
EON AKE38ZA0Q00



R273

64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13

Change to 1SS355 as Current Los



PROJECT : UT3/5
Quanta Computer Inc.

Size Custom	Document Number KB3926/ROM/TP
----------------	---

Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCI-E-AS0B223-S40N-7F-52P-QT6 as ME drawing

only resever Qtr6 not support IAMT

[23] CL_RST#1 R49 0.4 CL_RST#1 R
[23] CL_DATA1 R53 0.4 CL_DATA1 R
[23] CL_CLK1 R56 0.4 CL_CLK1 R

[22] PCIE_TXP0 PCIE_TXP0
[22] PCIE_TXN0 PCIE_TXN0

[22] PCIE_RXP0 PCIE_RXP0
[22] PCIE_RXN0 PCIE_RXN0

[2] PCLK_DEBUG PLTRST#

[2] CLK_PCIE_WLAN CLK_PCIE_WLAN
[2] CLK_PCIE_WLAN# CLK_PCIE_WLAN#

T13 MV modified
[21] BT_COMBO_EN# R59 0.4 CLK_MINI_OE#
BT_DATA, BT_CHCLK, CLKREQ#
internal pull-DOWN 100k
ohm

MINICAR_PME#

CN23

51 Reserved +3.3V
49 Reserved GND
47 Reserved +1.5V
46 LED_WPAN#
43 Reserved LED_WLAN#
42 Reserved LED_WWAN#
40 X
37 Reserved USB_D+
36 GND USB_D-
35 PETP0 GND
34 PETN0
33 SMB_DATA
32 SMB_CLK
31 GND
29 GND +1.5V
28 PERP0 GND
27 PERN0
26 +3.3Vaux
25 PERST#
24 W_DISABLE#
23 GND
22 Reserved
21 GND
20 Reserved
19 GND
18 GND
17
16
15 GND
14 REFCLK+
13 REFCLK-
12 GND
11 GND
10 CLKREQ#
9 BT_CHCLK +1.5V
8 BT_DATA
7 WAKE# +3.3V
6
5
4
3
2

52 Reserved +3.3V
50 GND
48 Reserved +1.5V
46 LED_WPAN#
44 LED_WLAN#
42 Reserved LED_WWAN#
40 X
37 Reserved USB_D+
36 GND USB_D-
35 PETP0 GND
34 PETN0
33 SMB_DATA
32 SMB_CLK
31 GND
29 GND +1.5V
28 PERP0 GND
27 PERN0
26 +3.3Vaux
25 PERST#
24 W_DISABLE#
23 GND
22 Reserved
21 GND
20 Reserved
19 GND
18 GND
17
16
15 GND
14 REFCLK+
13 REFCLK-
12 GND
11 GND
10 CLKREQ#
9 BT_CHCLK +1.5V
8 BT_DATA
7 WAKE# +3.3V
6
5
4
3
2

MINI_PCIE_H=4.0

MIPCI-A50B223-S40N-7F-52P-QT6

R47 0.4 BLUED LED [29,34]
RF_LINK# [34]
R45 10K/F 0 +3V
USBP10+ [22]
USBP10- [22]
CGDAT_SMB [2,10,11,27,32]
CGCLK_SMB [2,10,11,27,32]

PLTRST# [22,25,30,32,34]
MINIRF_OFF# [23]
RF_OFF#

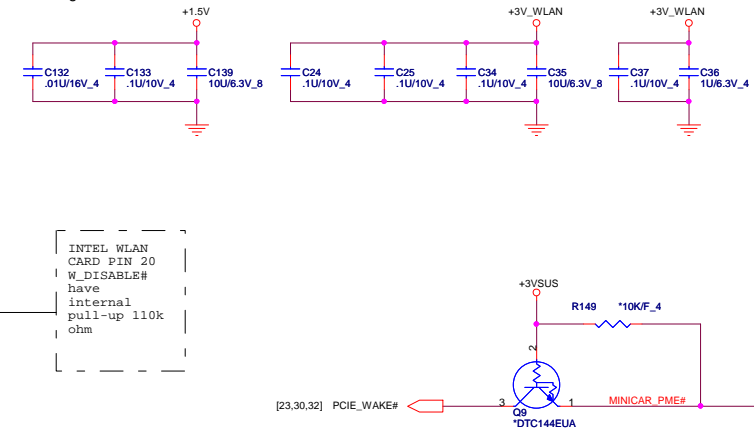
R50 0.4/S

LAD0 [21,34]
LAD1 [21,34]
LAD2 [21,34]
LAD3 [21,34]
LFRAME# [21,34]

R74 0.4 C71 33P/50V_4

for EMI request

Change Library to MIPCI-C-1775861-52P-LDV



Change Library to MIPCI-C-1775861-52P-LDV-QT6 12/11

Mini PCI-E Card 3
TV Tuner

+3V_TVC

Change Library to MIPCI-E-P04-FJ504-170-52P-QT6 12/10

CN37

51 COMP VIDEO IN +3.3Vaux 52
49 Therm Trip out GND 50
47 AUD_R_IN +1.5V 48
45 AUD_L_IN NC 46
43 GND NC 44
41 GND NC 42
39 +3.3Vaux GND 40
37 GND NC(USB_D+) 38
35 GND NC(USB_D-) 36
33 PETp0 GND 34
31 PETn0 NC(SMB_DATA) 32
29 GND NC(SMB_CLK) 30
27 GND +1.5V 28
25 PERP0 GND 26
23 PERn0 NC(+3.3Vaux) 24
21 S-Video Y/in PERST# 22
19 S-Video C/in GND 20
17 GND NC 18
15 GND NC 16
13 REFCLK+ NC 14
11 REFCLK- NC 12
9 GND NC 10
7 CLKREQ# NC 8
5 NC +1.5V 6
3 NC GND 4
1 NC +3.3Vaux 2

MINIPCI-E H=7.0

WWAN -- have 2.8A 7W power consumption
power pin 24,39,41
GND pin 37,43
need to be careful power rail

USBP11+ [22]
USBP11- [22]

CGDAT SMB
CGCLK SMB

R719 0.6/S
R720 0.6

+3V
+3VSUS

TV tuner card

	Peak	Normal
+3.3Vaux:	2750mA	1100mA
+1.5V:	500mA	375mA


+3V_TVC

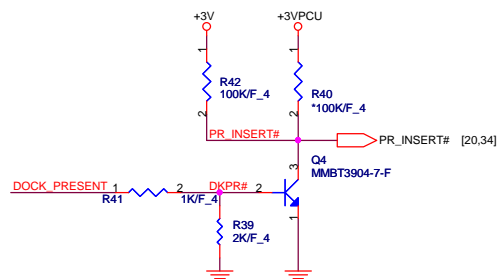
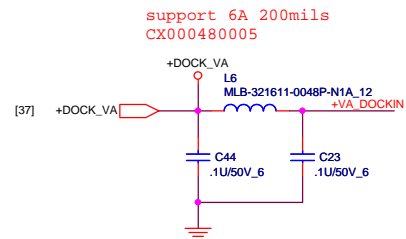
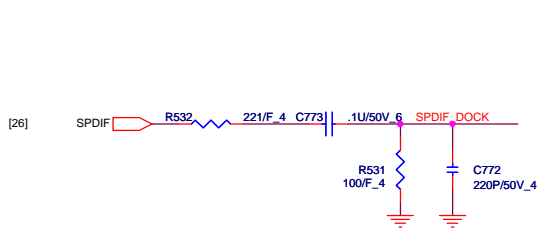
+1.5V

C921 .1U/10V_4
C922 .1U/10V_4
C708 .1U/10V_4
C709 10U/6.3V_8
C917 .01U/16V_4
C919 .1U/10V_4
C920 10U/6.3V_8

PROJECT : UT3/5
Quanta Computer Inc.

Size Custom
Document Number
MINI PCI-E CONN Y3 & HOLE

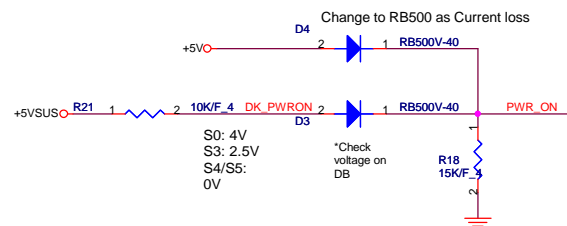
 NB5	PROJECT : UT3/5 Quanta Computer Inc.		
	Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev PV
	Date: Monday, October 20, 2008	Sheet 35 of 43	



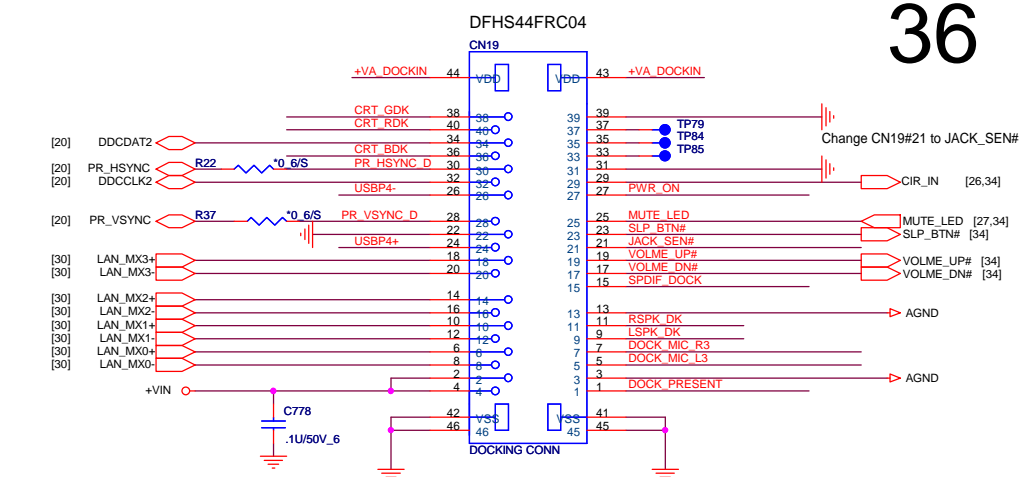
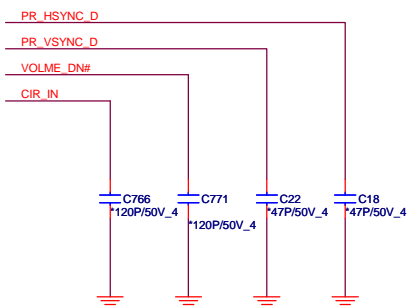
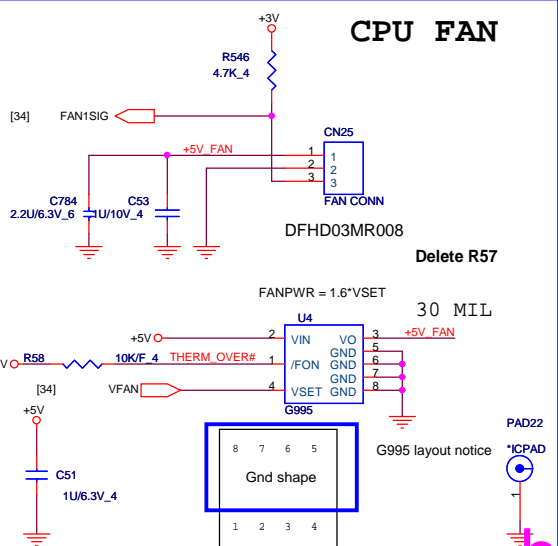
For IDT Dolby functionality.

DB modified

[26] PR_INSERT#_IDT < PR_INSERT#_IDT R730 *0.4/S PR_INSERT#

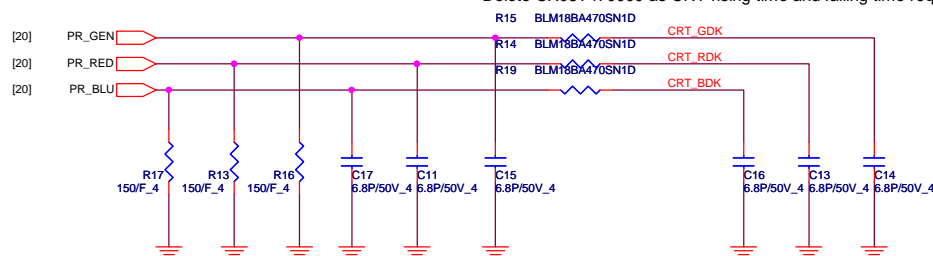


CPU FAN

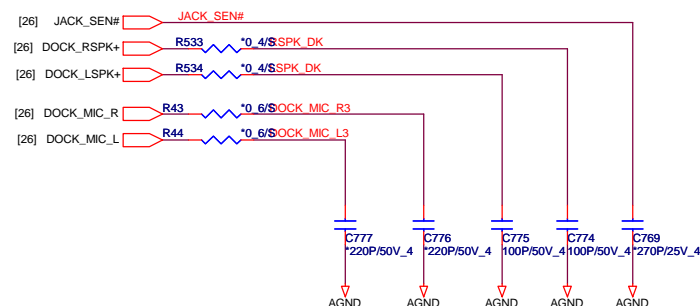


R13,R16,R17 Change to install

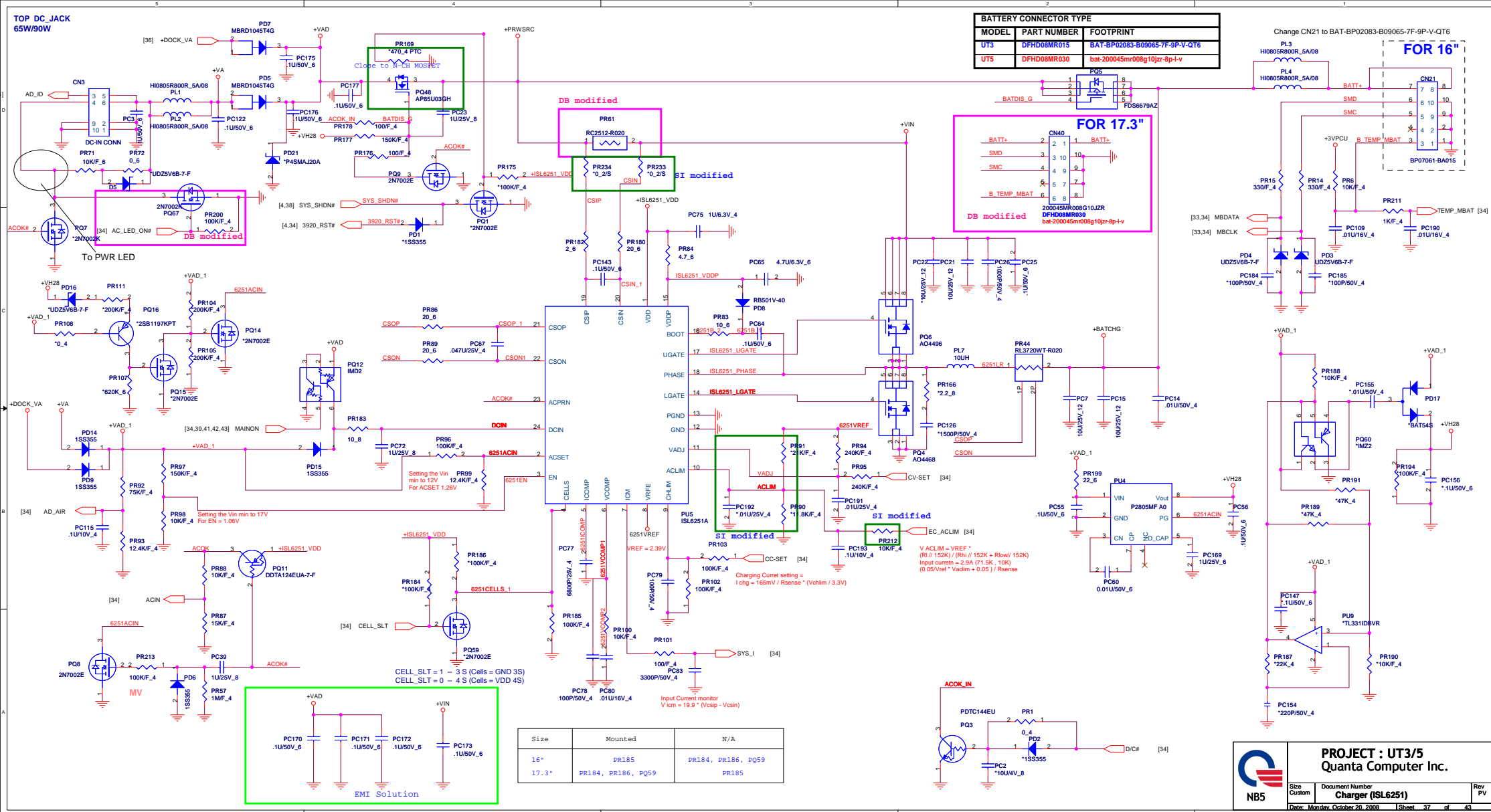
Delete CX08T470000 as CRT rising time and falling time request

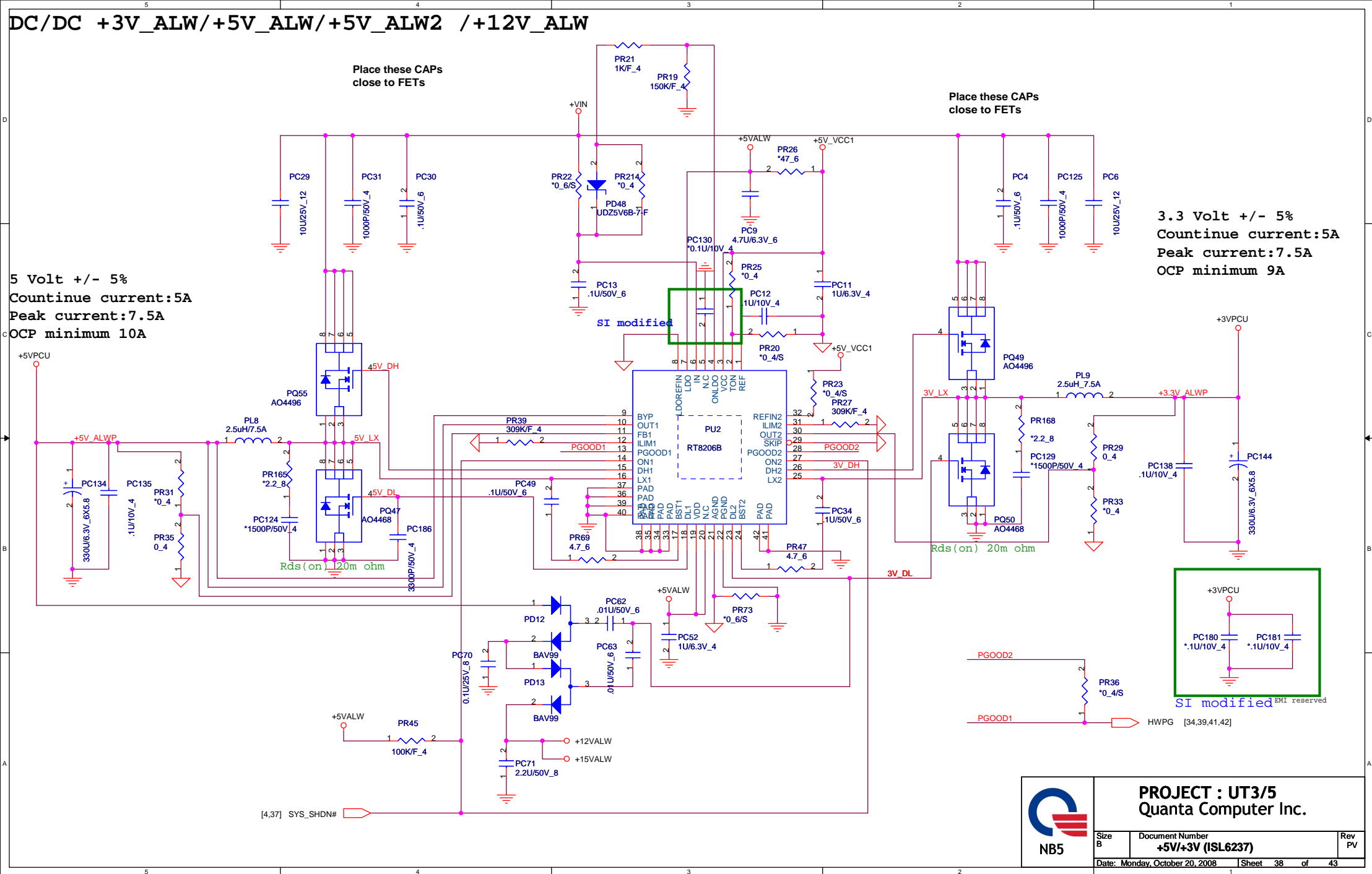


Add Loss net(GND Net)



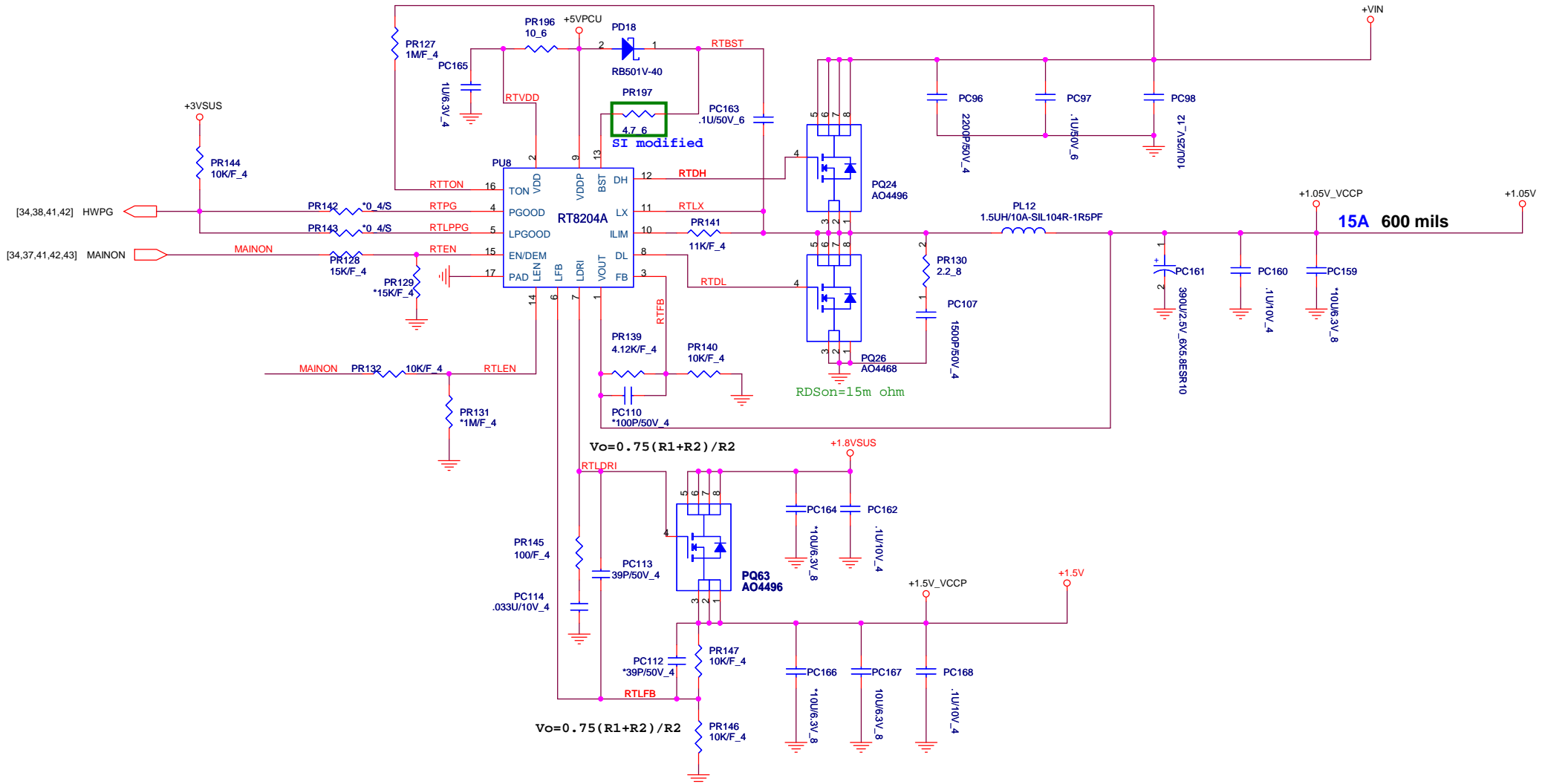
Change to Analog Gnd






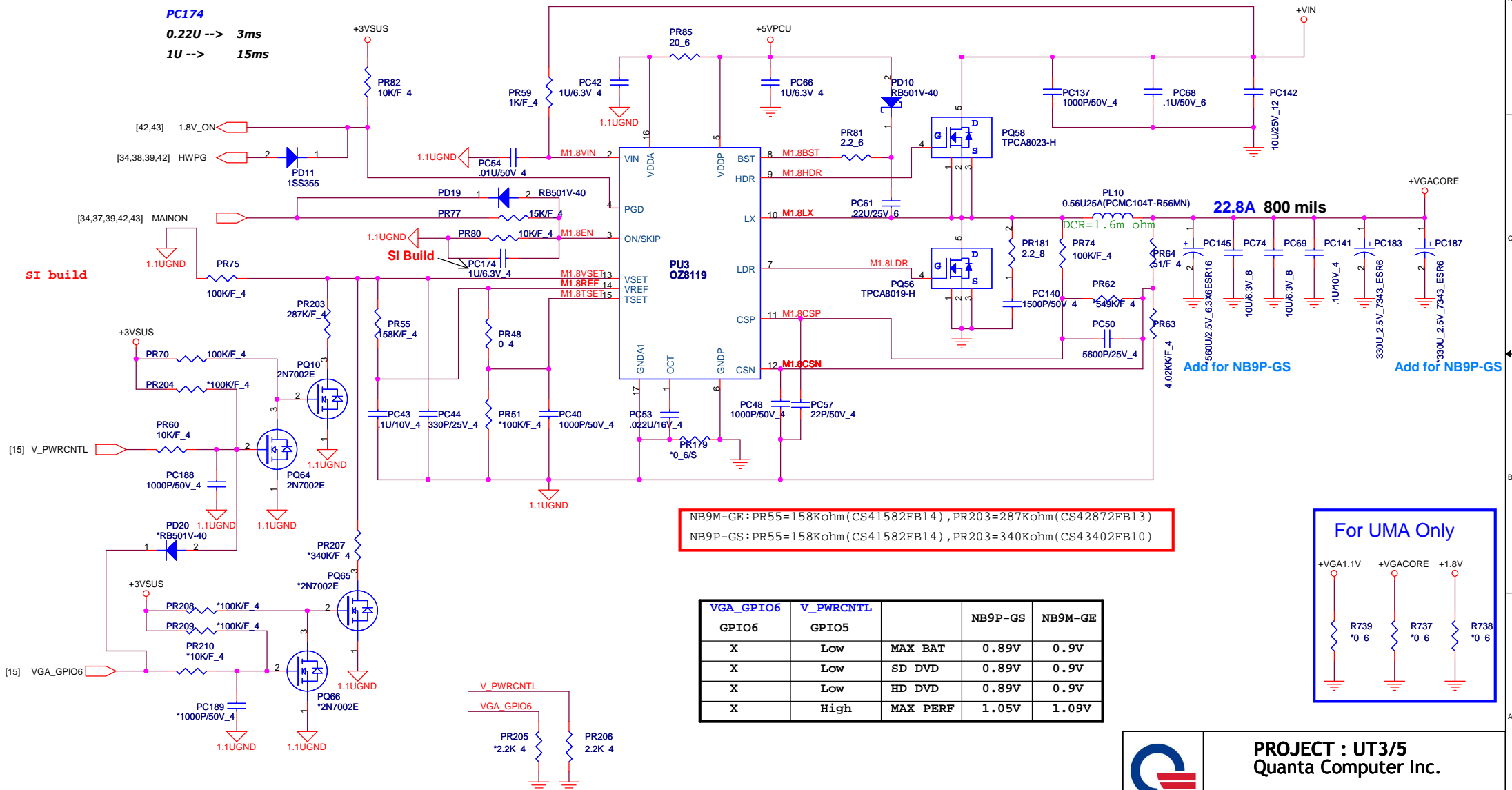
VCCP1.05V & +1.5V

+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

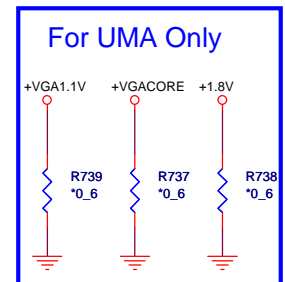


			PROJECT : UT3/5 Quanta Computer Inc.		
Size B	Document Number +1.05V/+1.5V (RT8204)				Rev PV
Date: Monday, October 20, 2008			Sheet 39 of 43		

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A

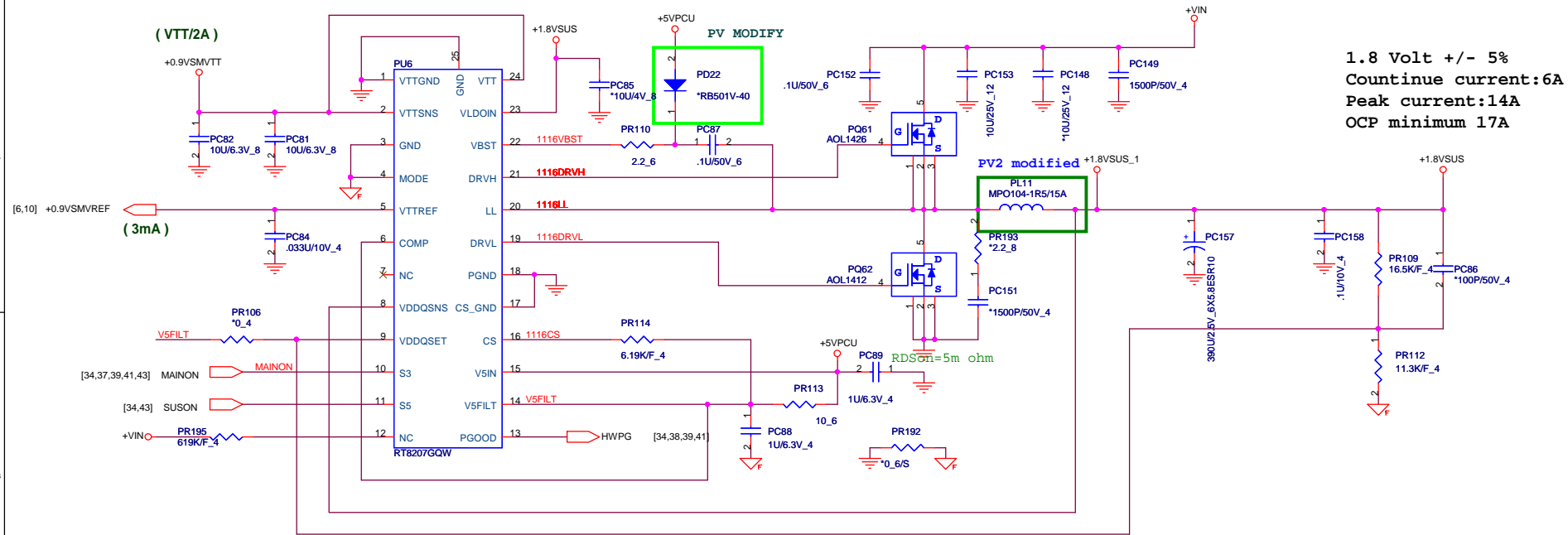


VGA_GPIO6	V_PWCNTL			
GPIO6	GPIO5		NB9P-GS	NB9M-G
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V



PROJECT : UT3/5
Quanta Computer Inc.

Size B	Document Number VGA Core OZ8119	Rev PV
Date: Monday, October 20, 2008		Sheet 41 of 43



For Discrete Only

