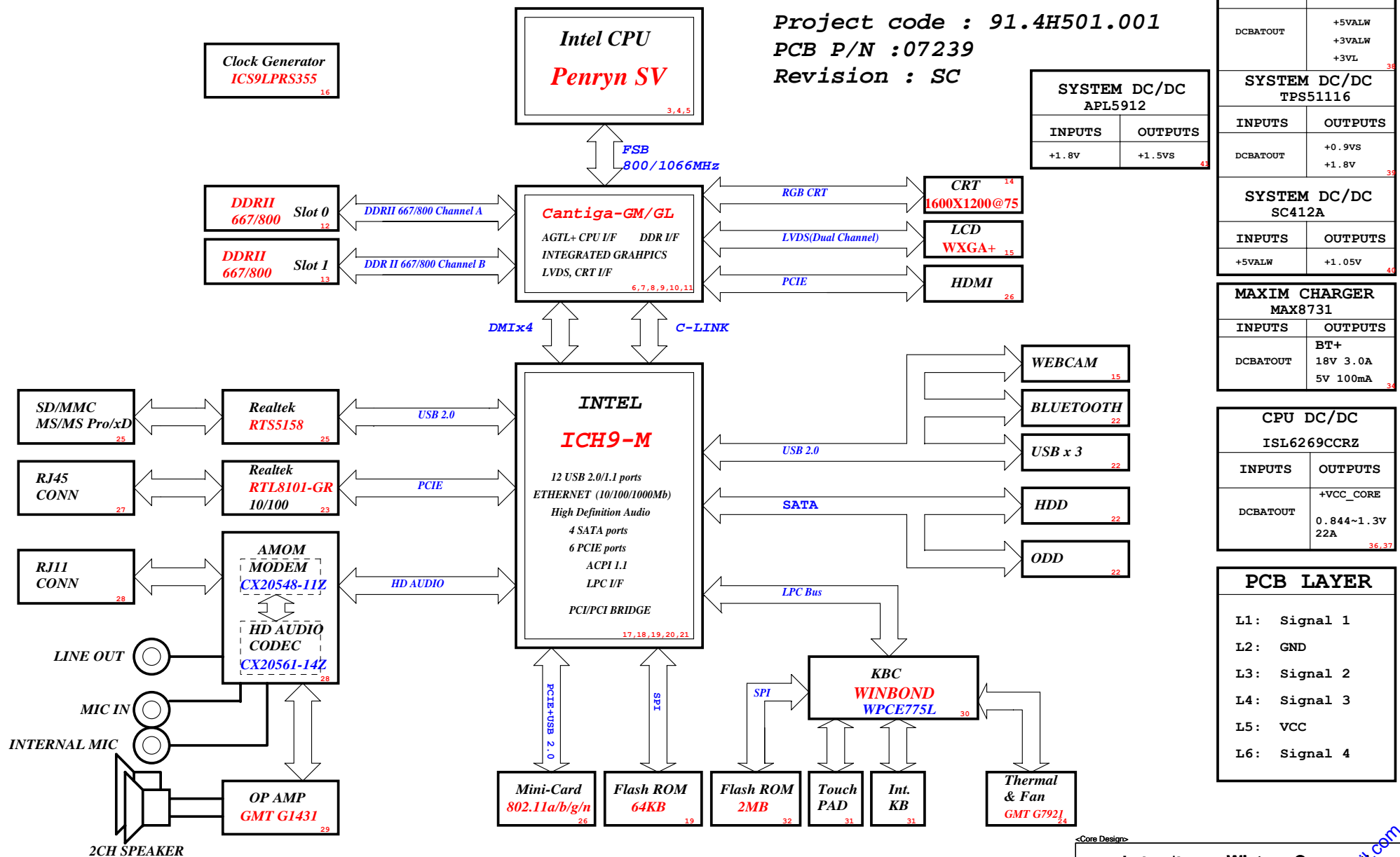


Warrior Intel UMA Block Diagram



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title _____

Block Diagram

Size A3	Document Number	Rev
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Date: Friday, January 04, 2008 Sheet 1 of 42

SEMIOTIC	1	100%	1	100%
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

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ICH9 Integrated pull-up
and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIOT20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

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Cantiga chipset and ICH9M I/O controller
Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG6 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default)
CFG9	PCIe Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

1

PCIE Routing

page 19

LANE1	LAN
LANE2	MiniCard WLAN

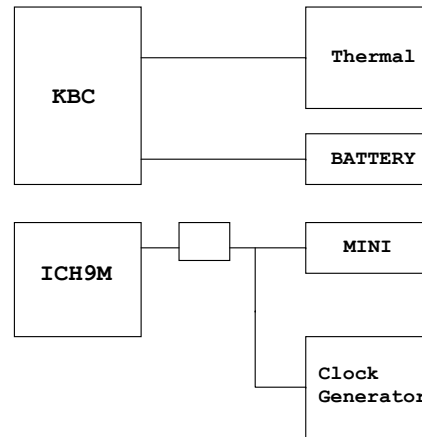
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USB Table

page 19

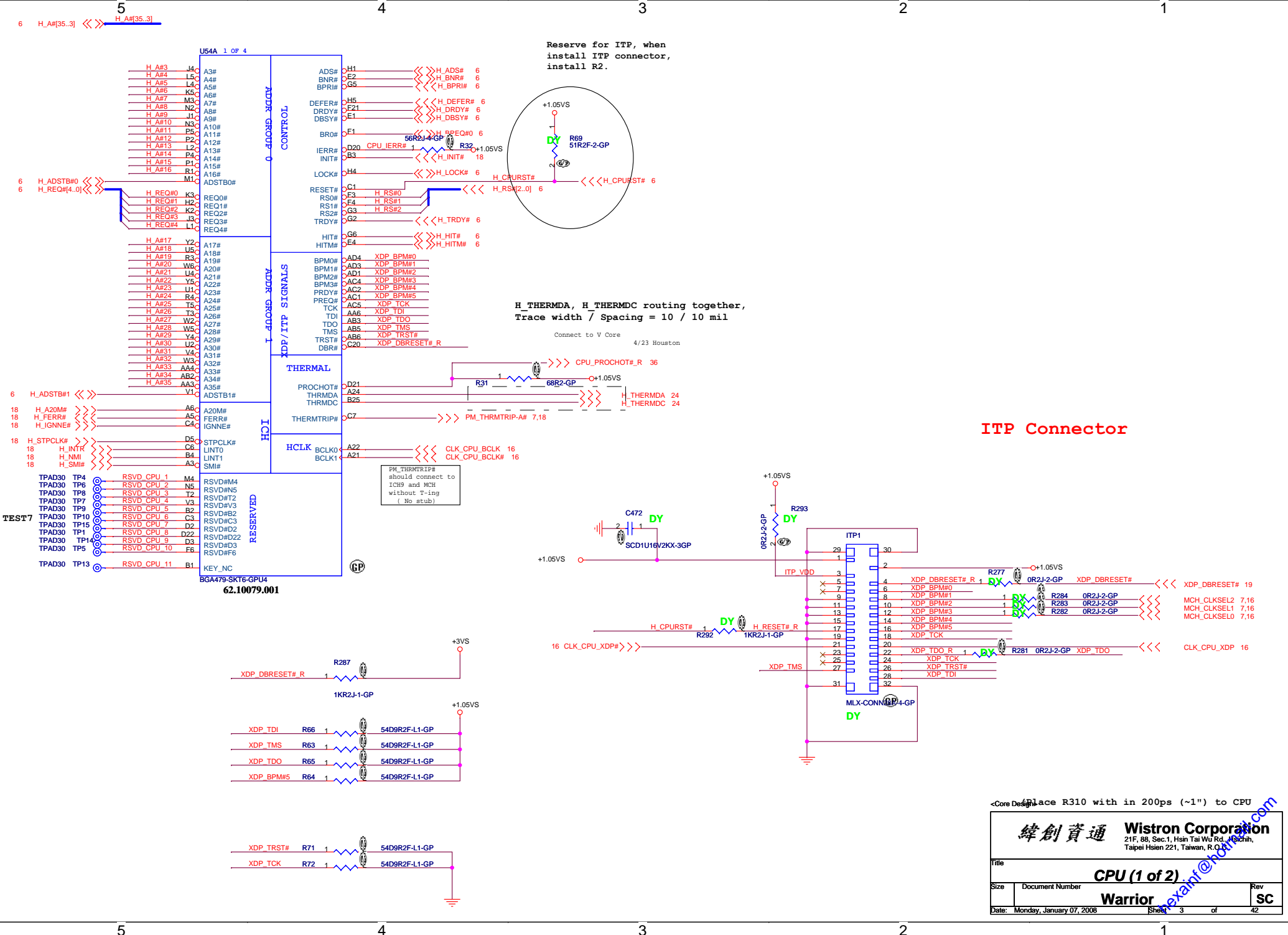
USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

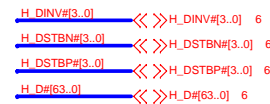
SMBus



<Core Design>

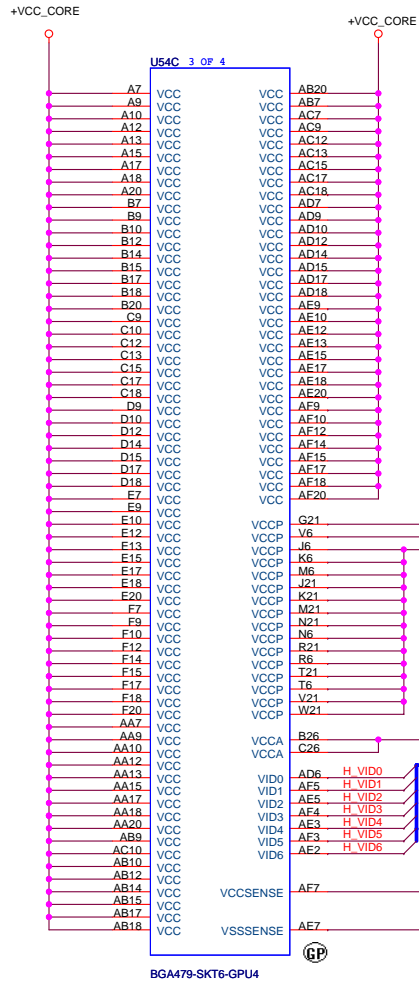
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Table of Content			
Size A3	Document Number	Warrior	Rev SC
Date: Friday, January 04, 2008	Sheet	2 of	42



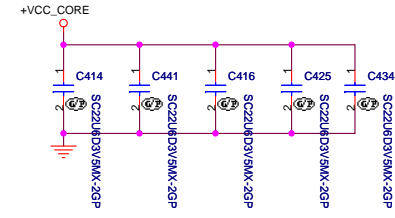


Layout Note:
Comp0, 2 connect with $Z_0=27.4$ ohm, make
trace length shorter than $0.5''$.
Comp1, 3 connect with $Z_0=55$ ohm, make
trace length shorter than $0.5''$.

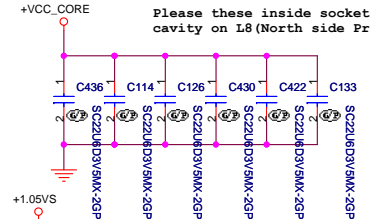
Please these inside socket cavity on L8(North side Secondary)



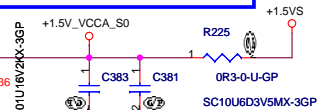
Please these inside socket cavity on L8(South side Secondary)



Please these inside socket cavity on L8(North side Primary)



layout note: "1D5V VCCA_S0" as short as possible



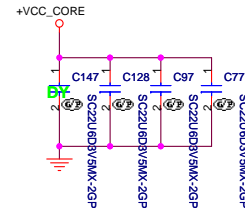
Layout Note:
Place as close as possible to the CPU VCCA pin.

Layout Note:
VCCS and VSSS lines should be of equal length.

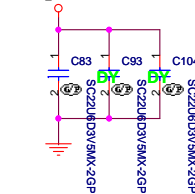
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCS and VSSS at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(North side Secondary)

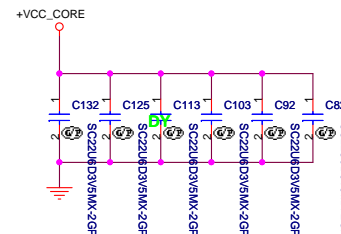


+VCC_CORE

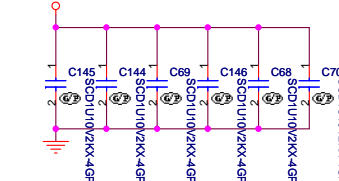


Please these outside socket cavity on L8(South side Secondary)

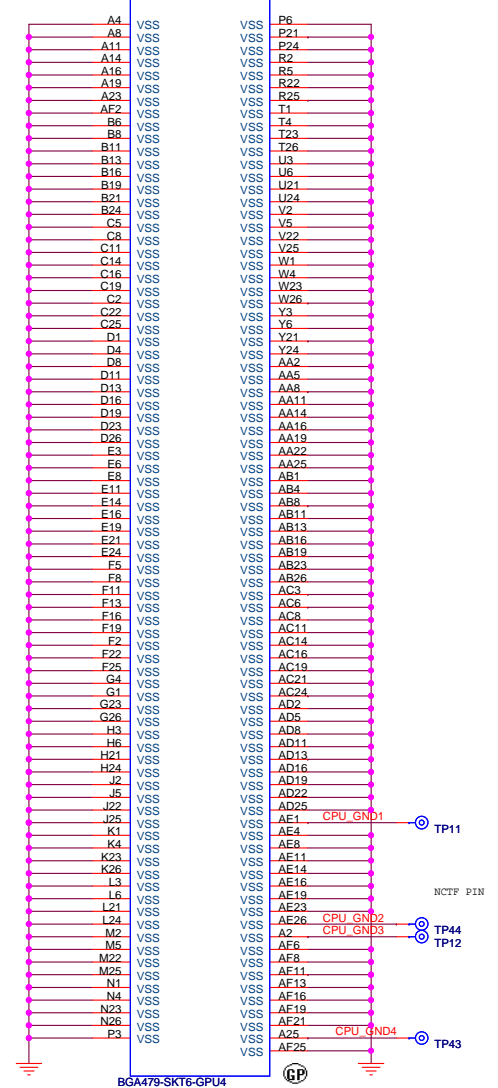
Please these inside socket cavity on L8(South side Primary)



+1.05VS

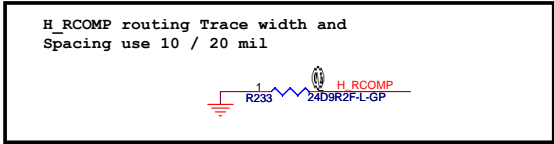
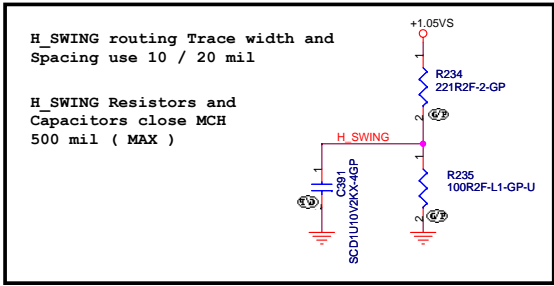


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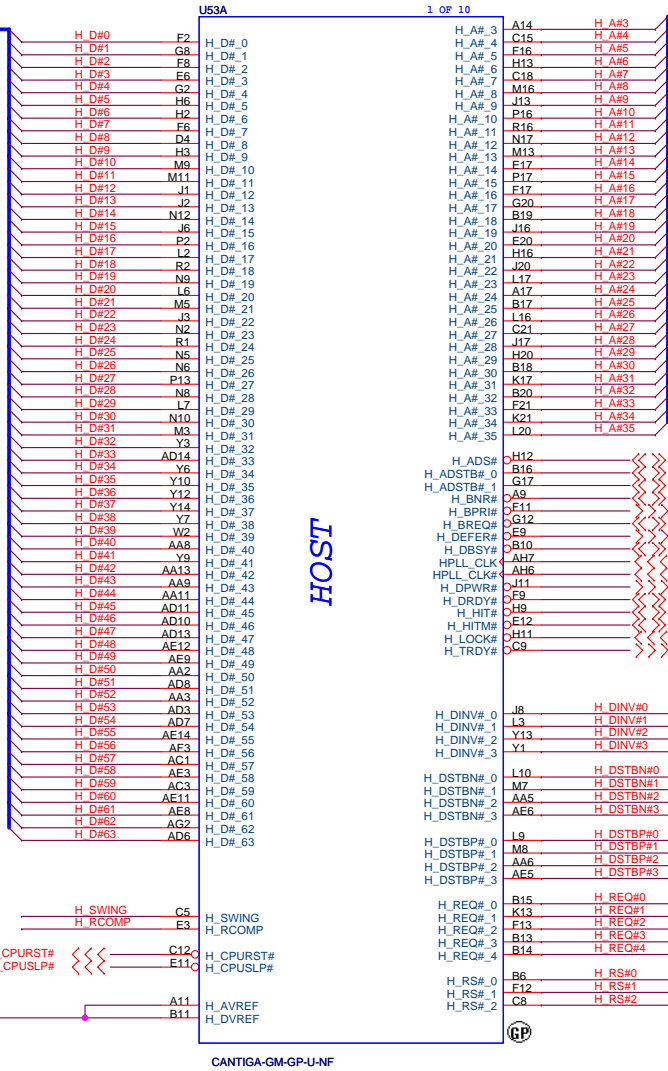
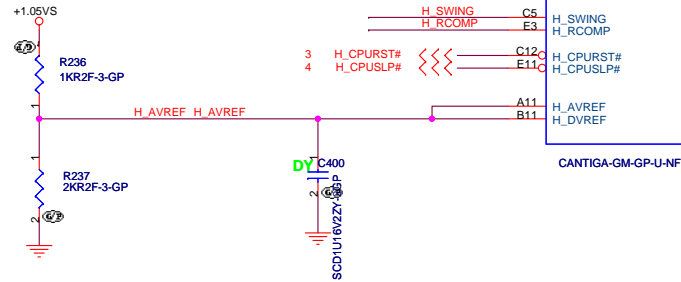


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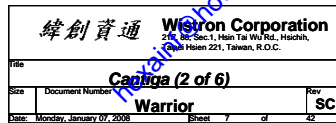
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Size	Document Number	Rev
Warrior		SC
Date: Monday, January 07, 2008	Sheet	of 42

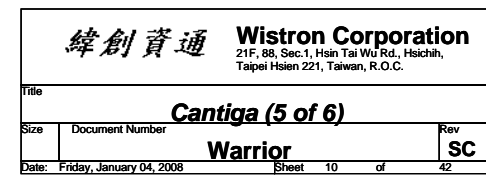


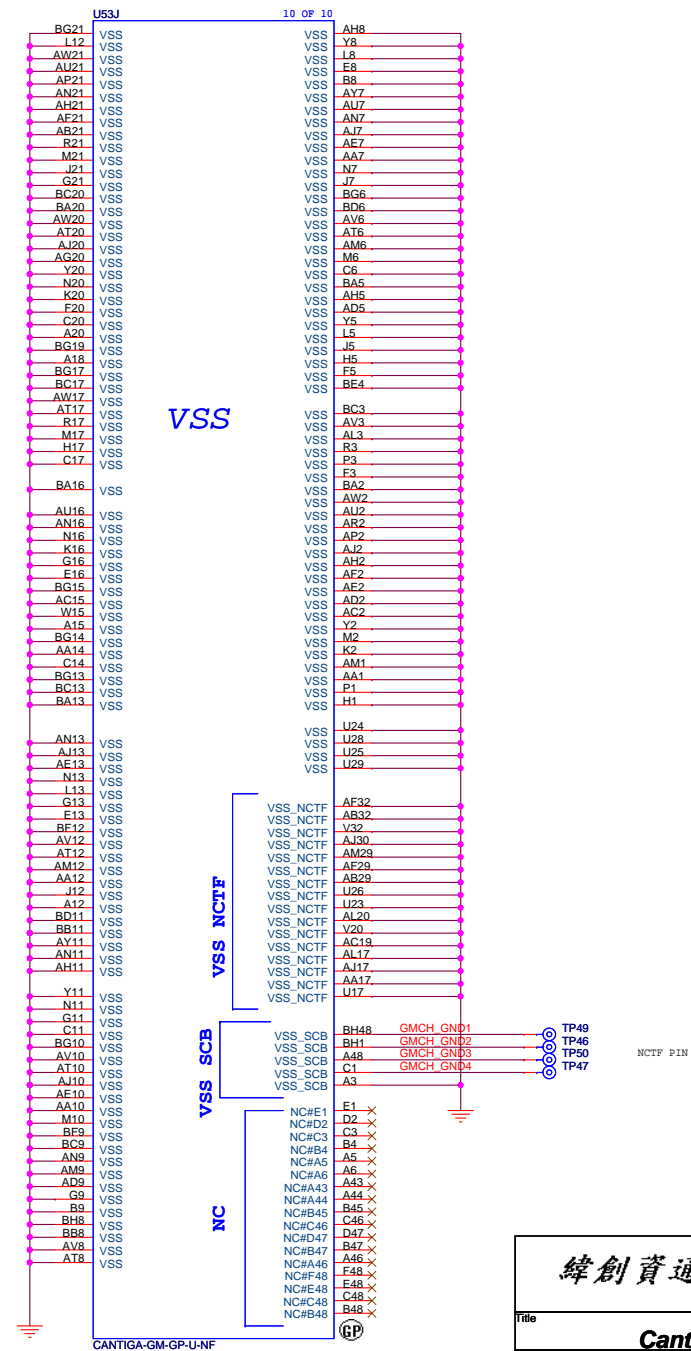
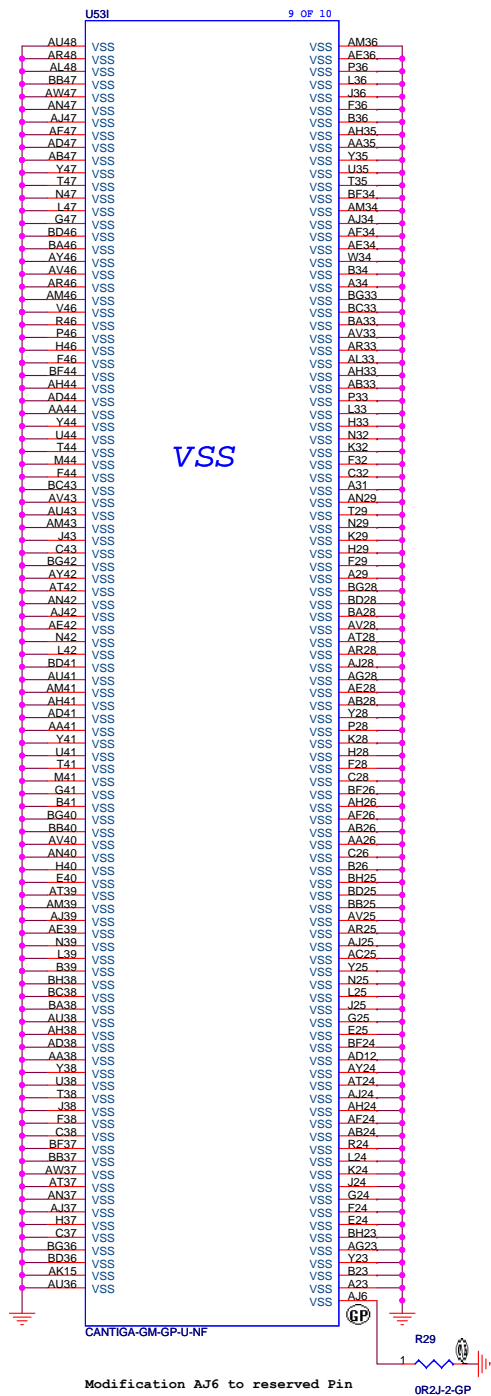
Place them near to the chip (< 0.5")



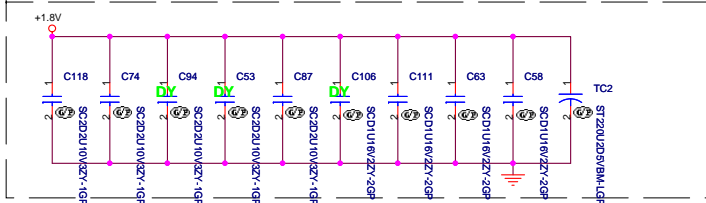
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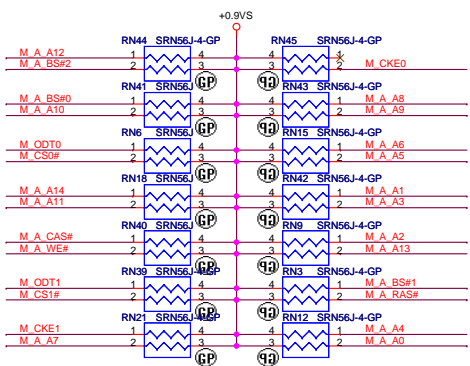
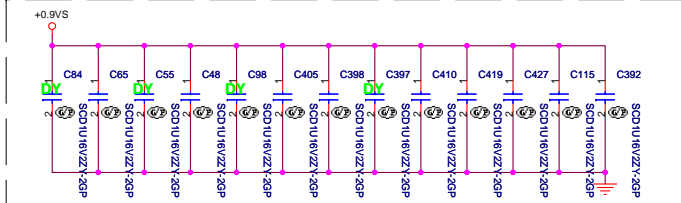




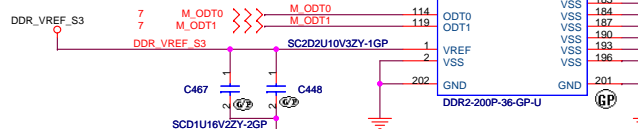
Layout Note:
Place near DM1



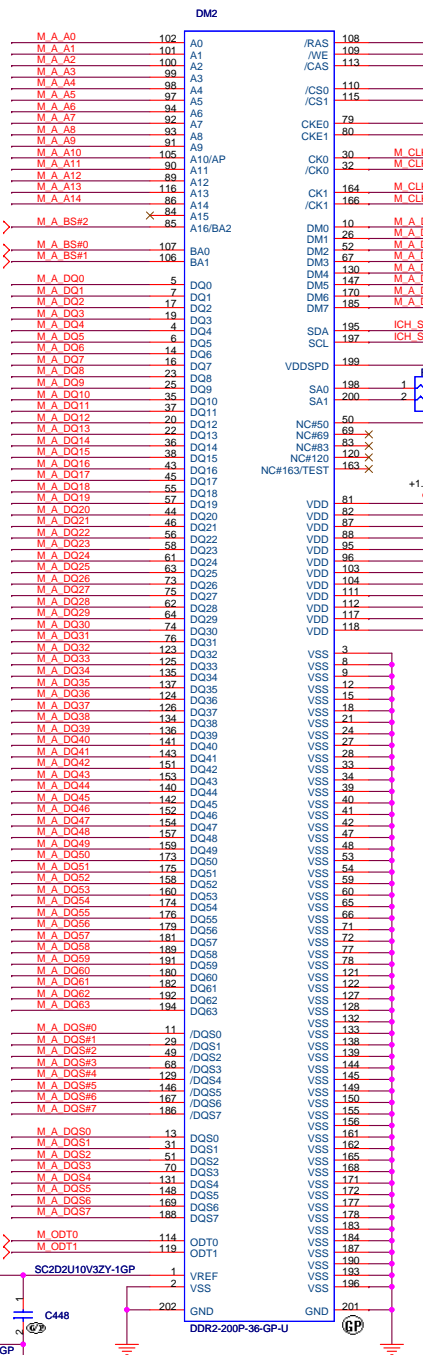
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

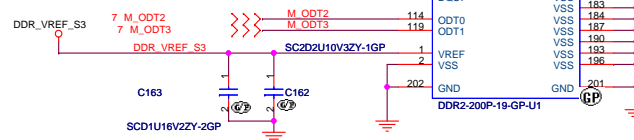
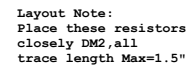
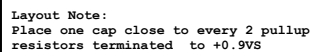
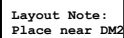


Layout Note:
Place these resistors
closely DM1, all
trace length Max=1.5"



DM2 use 62.10017.E11





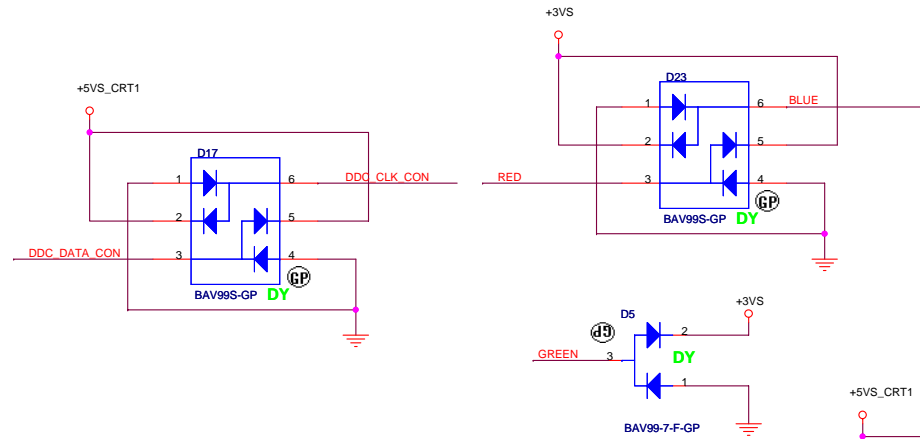
DM1 use 62.10017.B51



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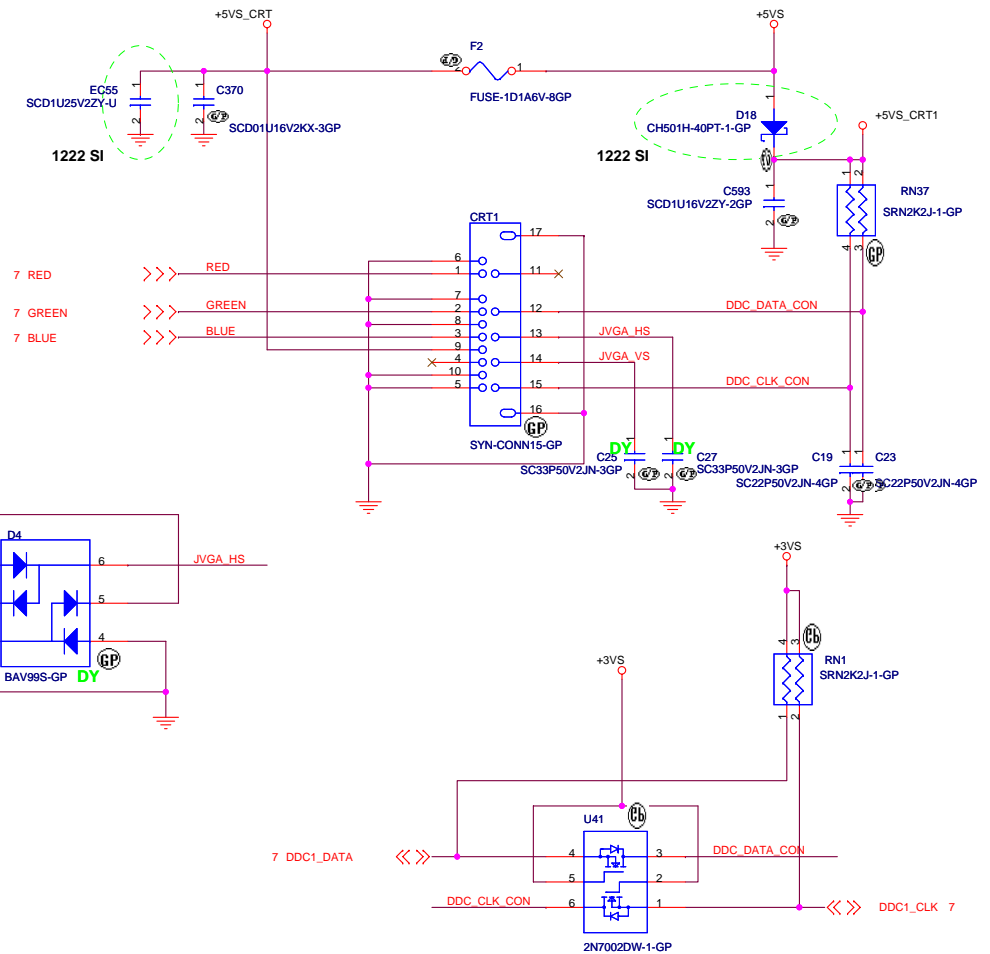
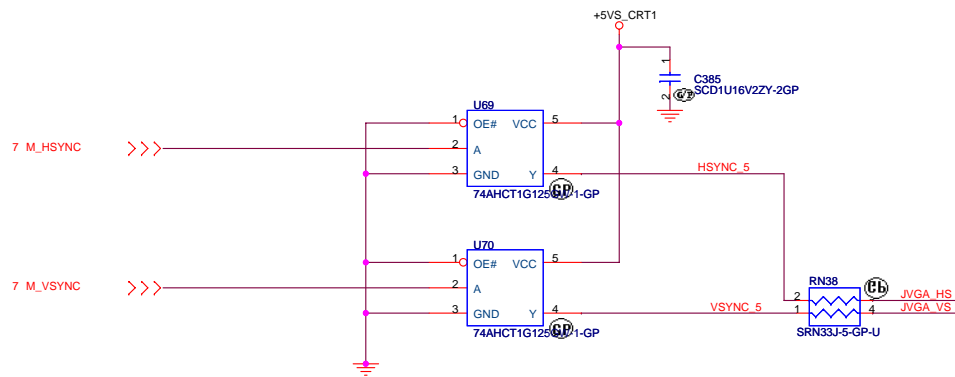
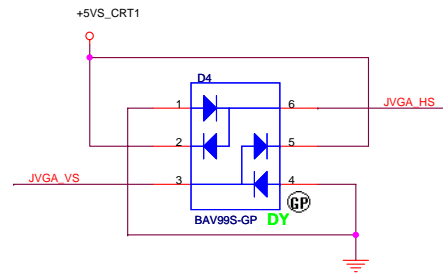
SO

CRT I/F & CONNECTOR



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



5V @ ext. CRT side

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CRT Connector

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Document Number

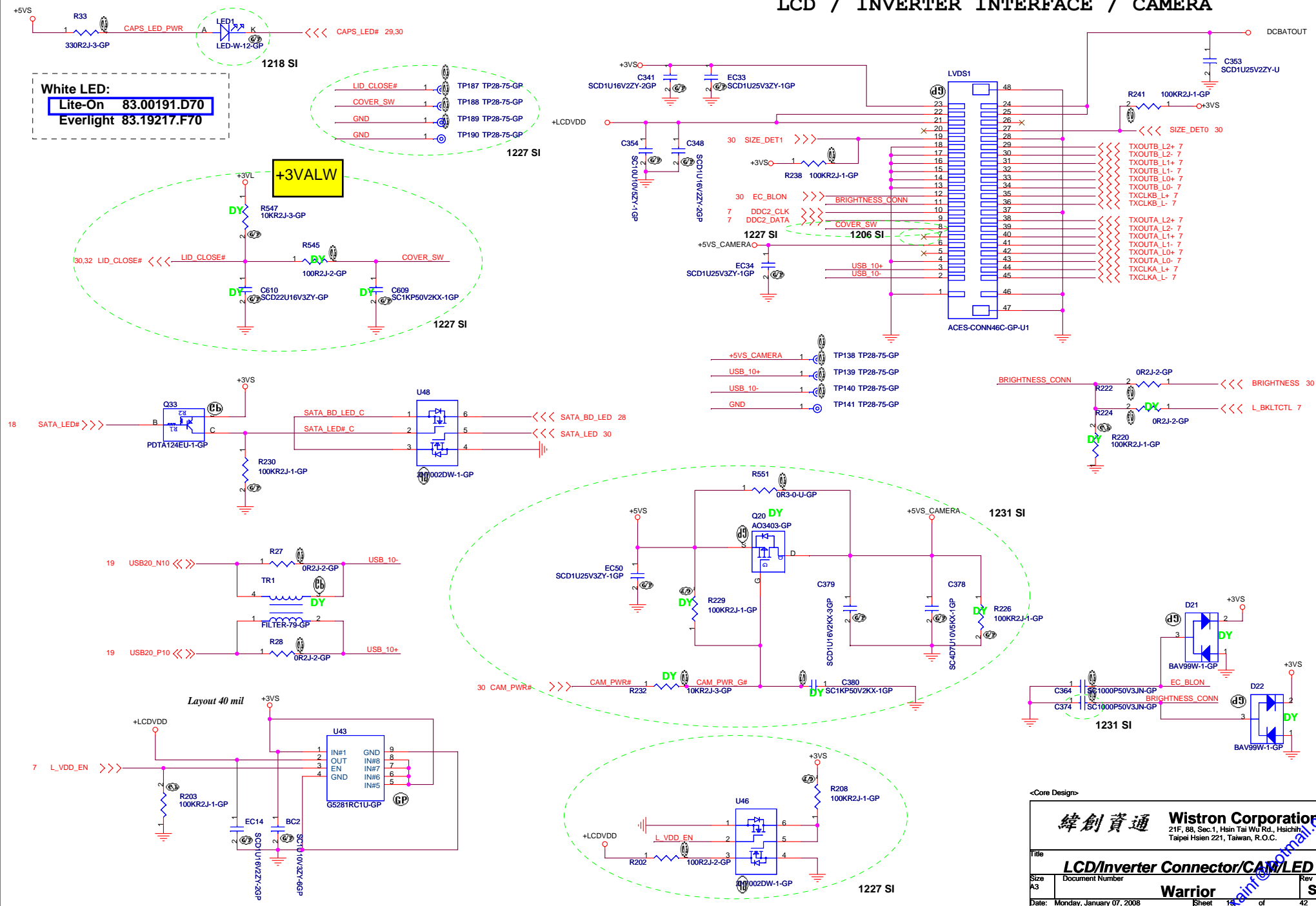
Warrior

Rev
SC

Date: Monday, January 07, 2008

Sheet 14 of 42

LCD / INVERTER INTERFACE / CAMERA

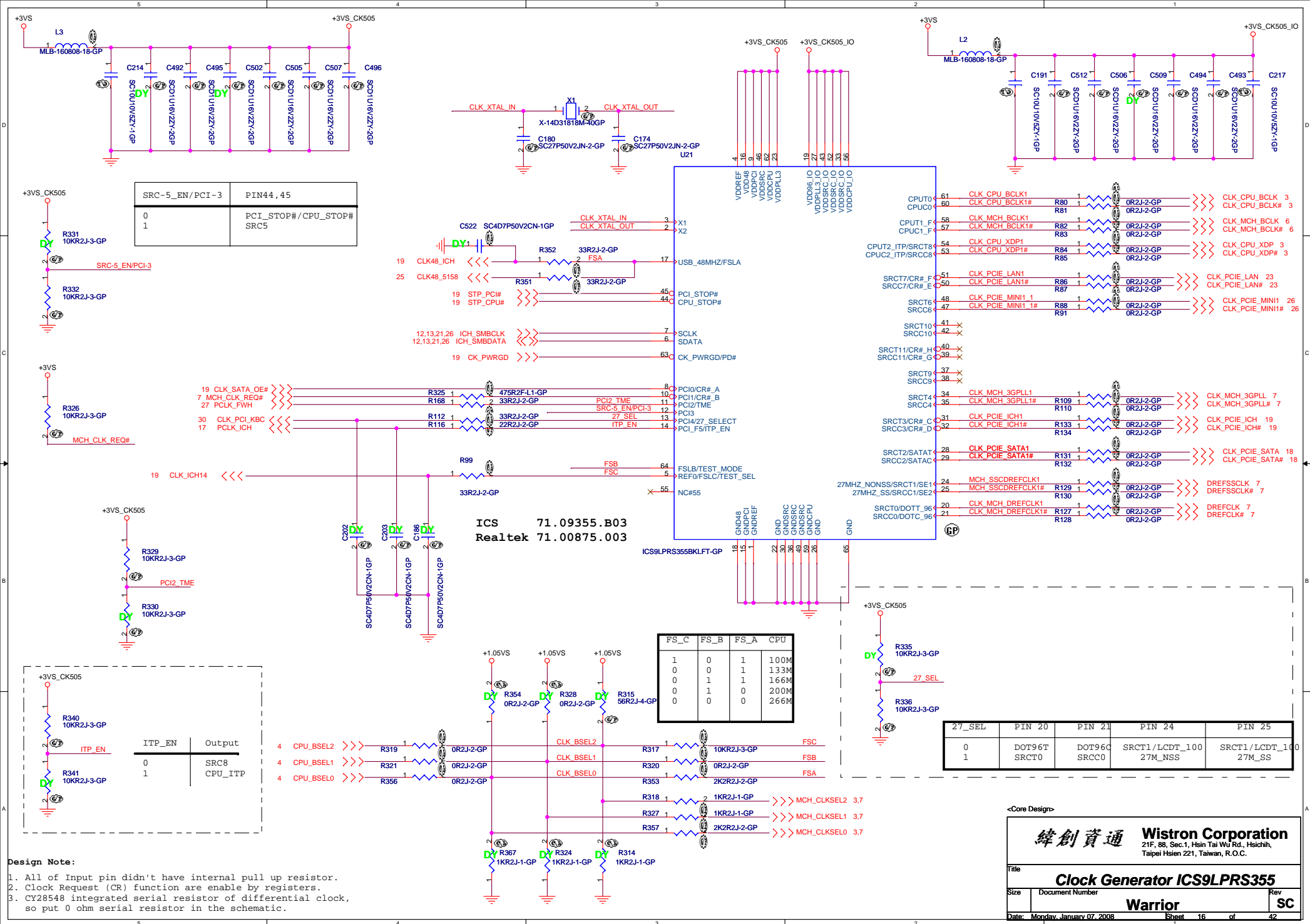


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Size A3	Document Number		Rev
	Warrior		SC
Date: Monday, January 07, 2008	Sheet 18	of 42	

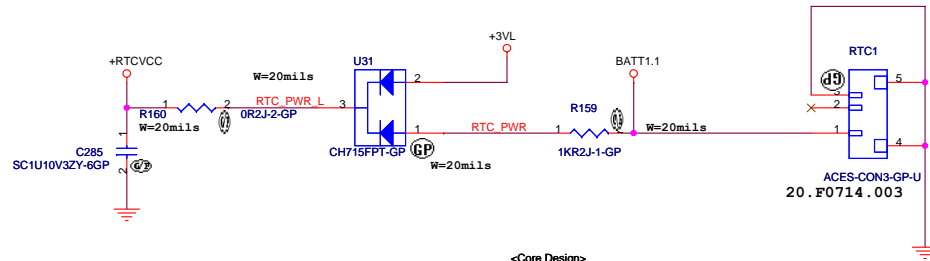
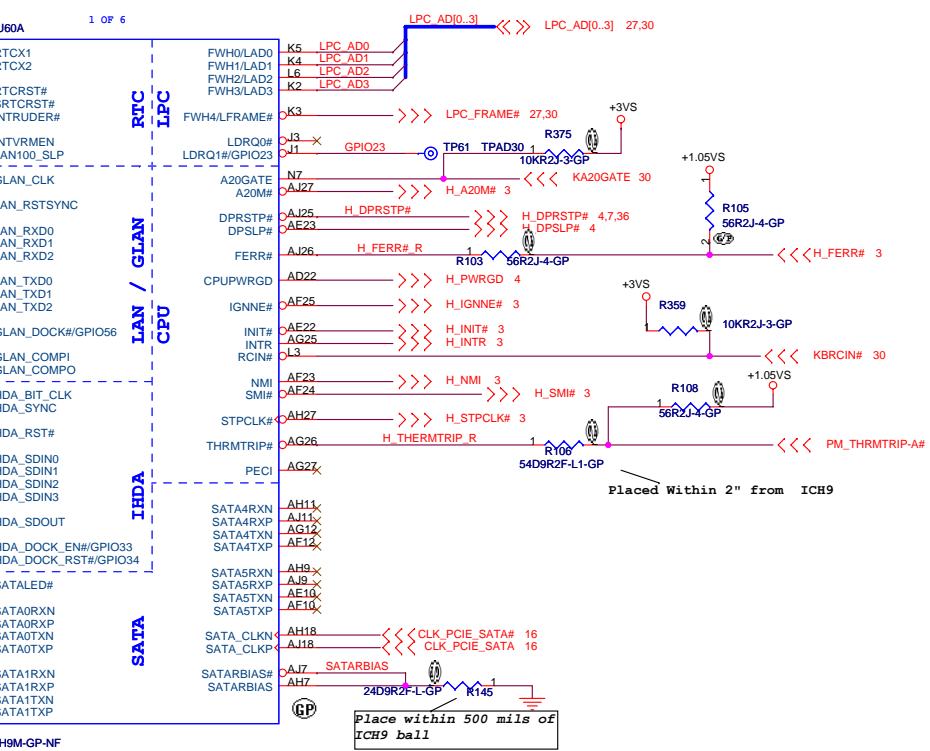
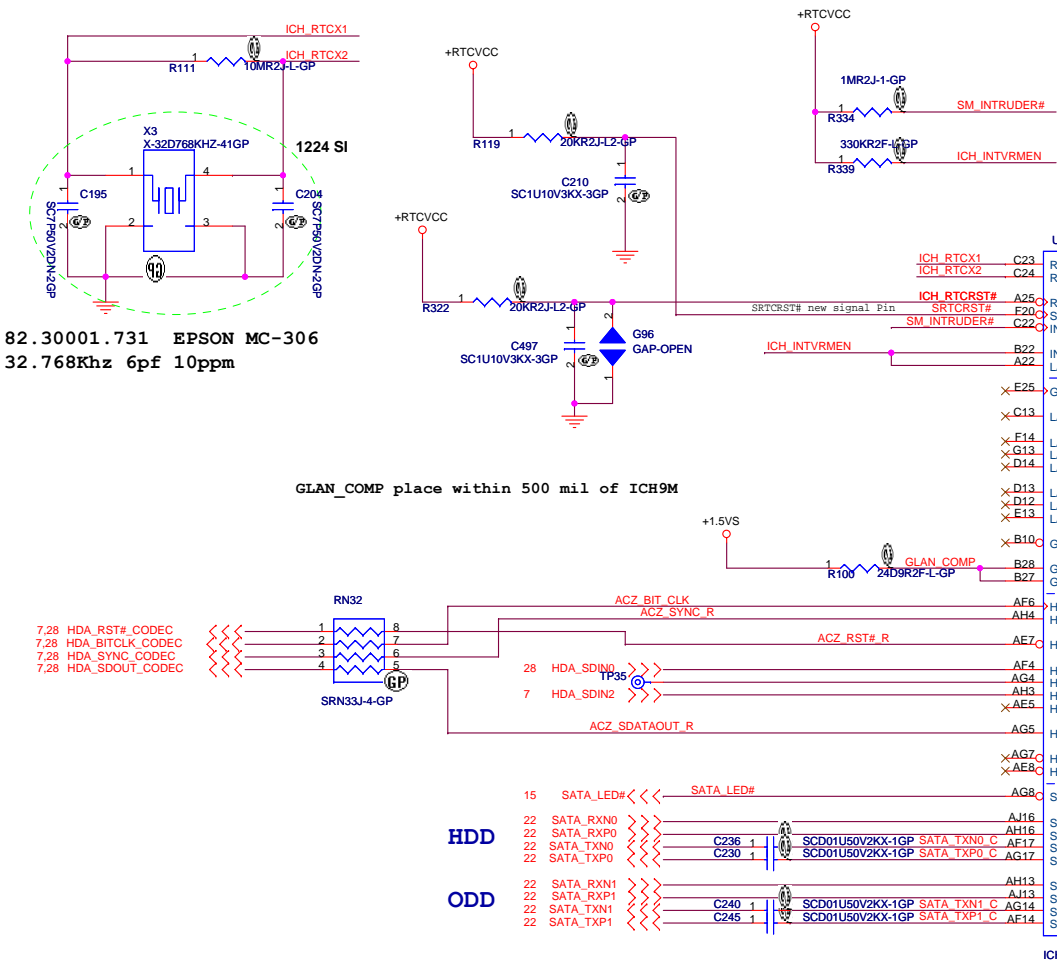


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Title			
Clock Generator ICS9LPRS355			
Size	Document Number		Rev
	Warrior		SC
Date:	Monday, January 07, 2008	Sheet 16 of	A2

82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm



Integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

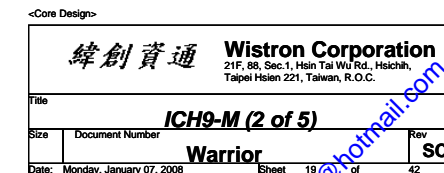
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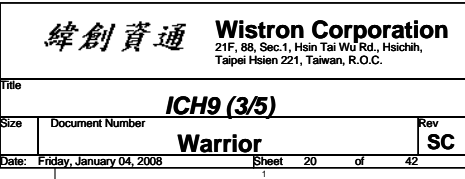
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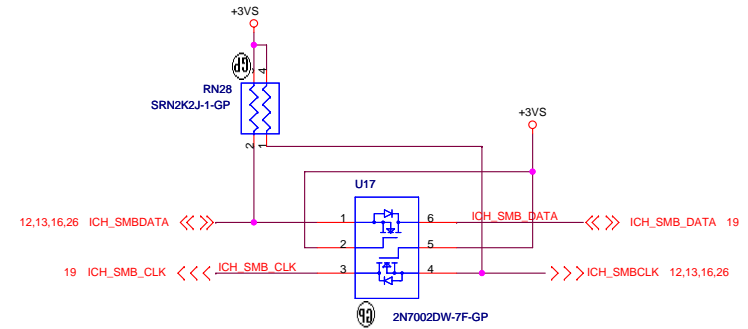
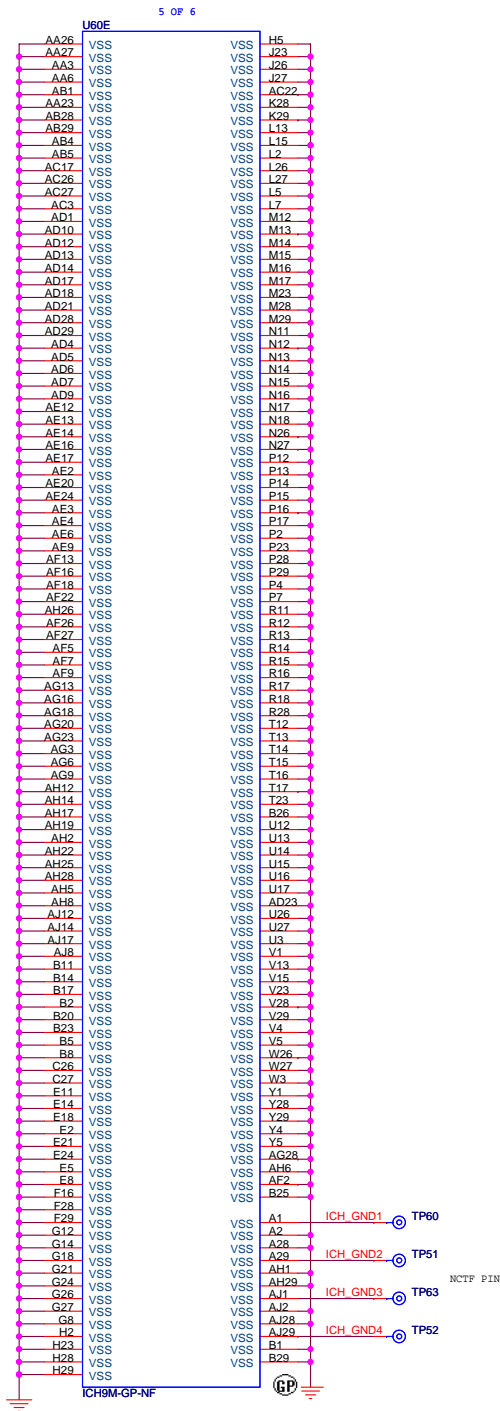
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Date: Monday, January 07, 2008 Sheet: 18 of 42



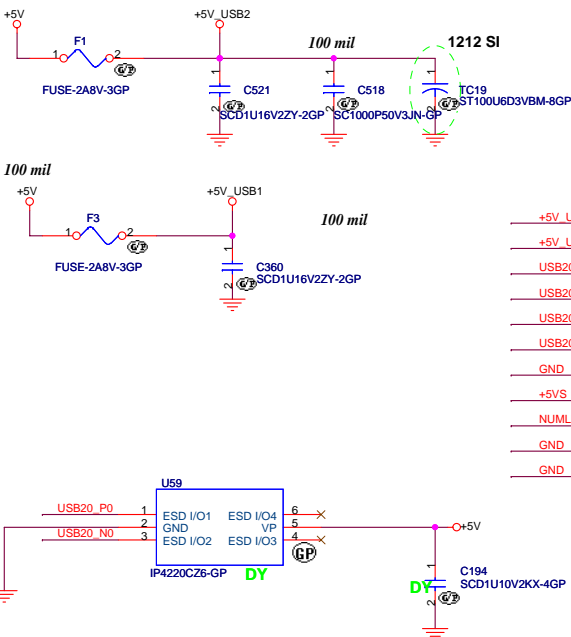




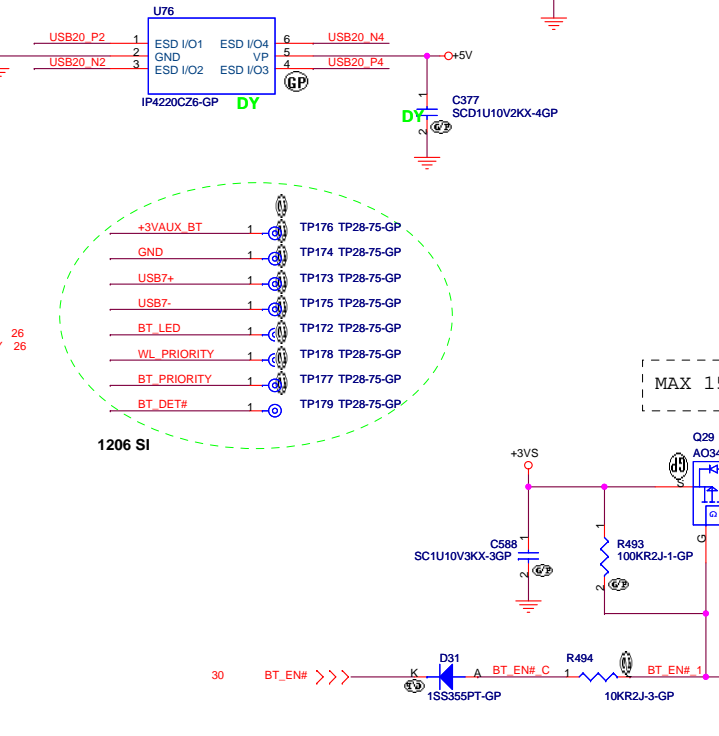
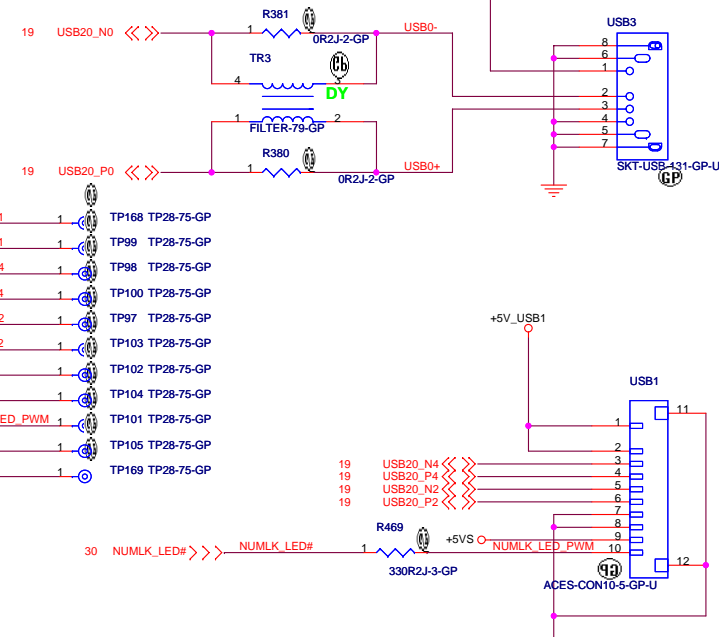
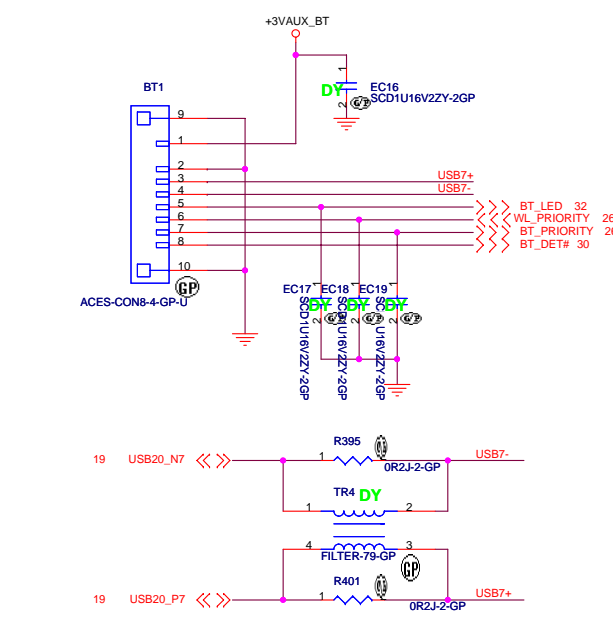
SMBUS

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Size	Document Number: Warrior Date: Monday, January 07, 2008
Rev	SC Sheet 21 of 42

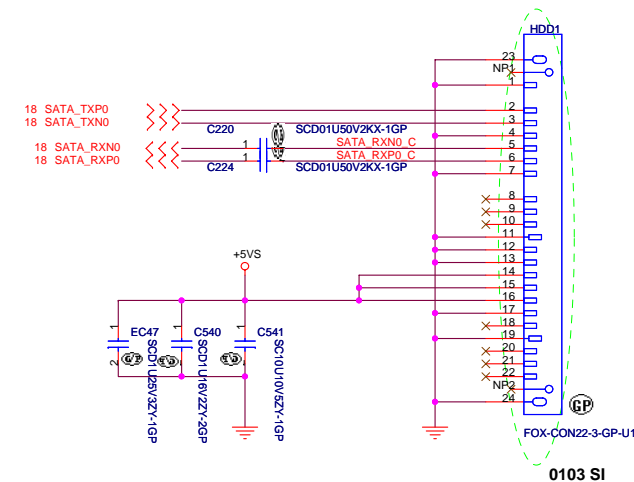
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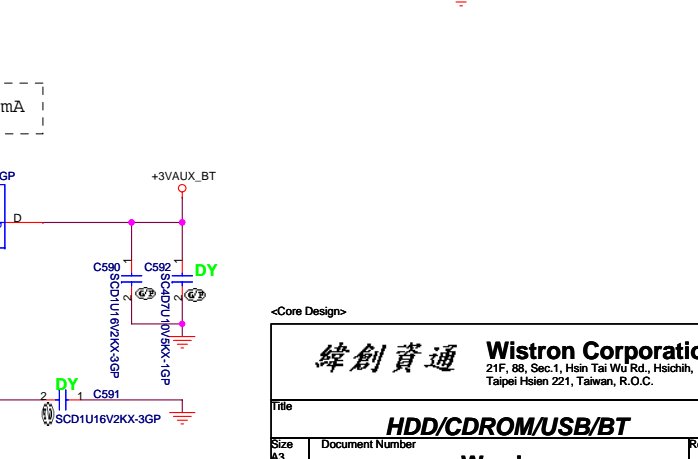
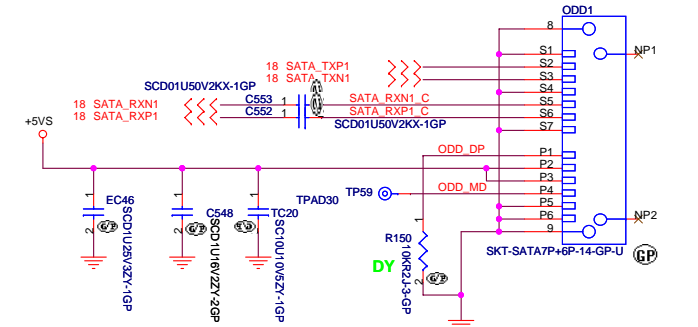
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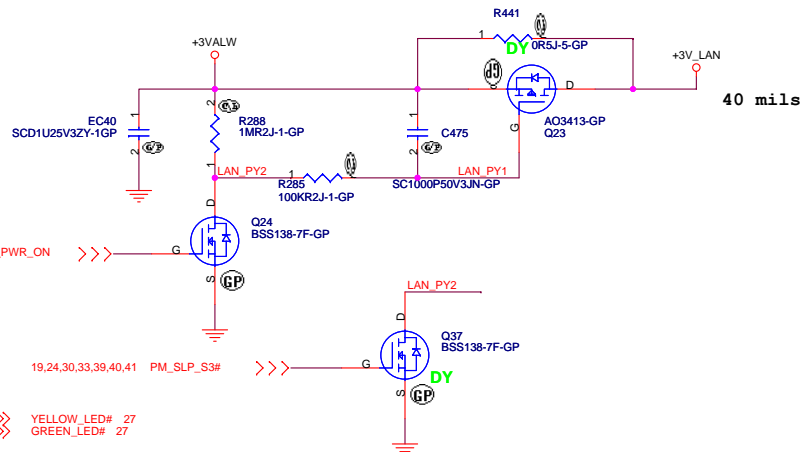
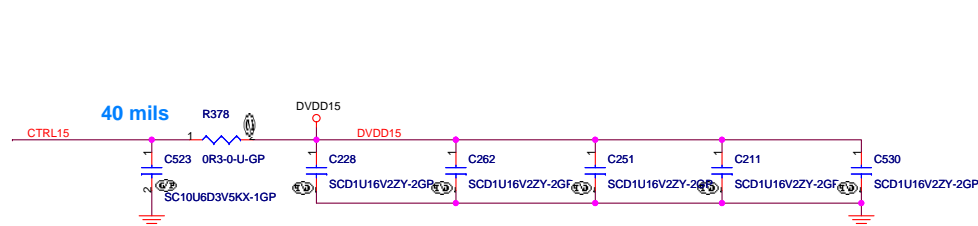
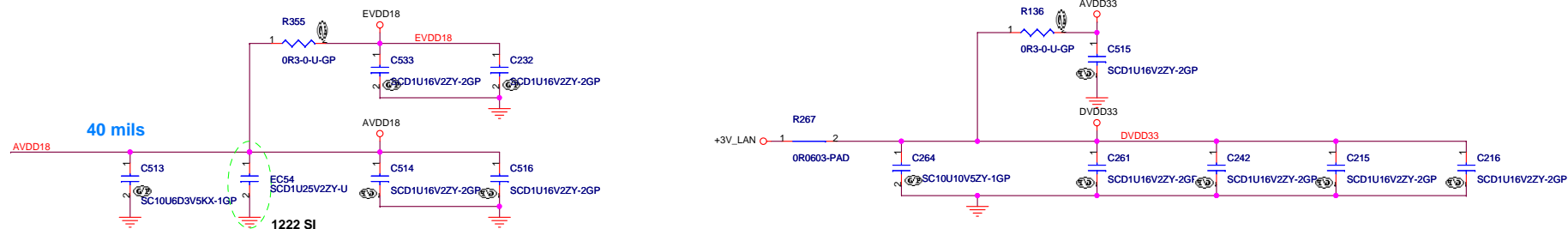


SATA HD Connector

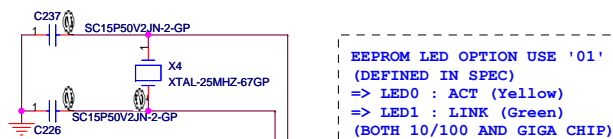


ODD Connector

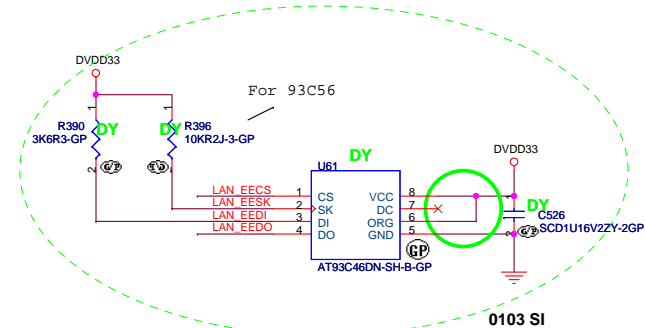
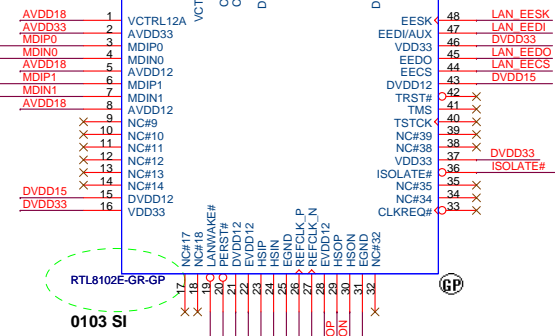
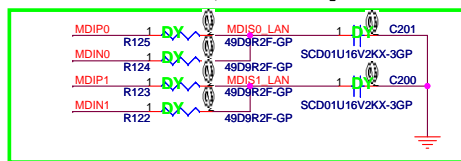




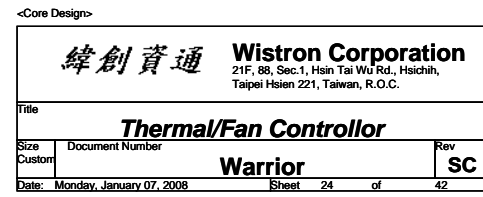
R548 should be 2.49K 1% ohm for 8102E,
R548 should be 2K 1% for 8101E.



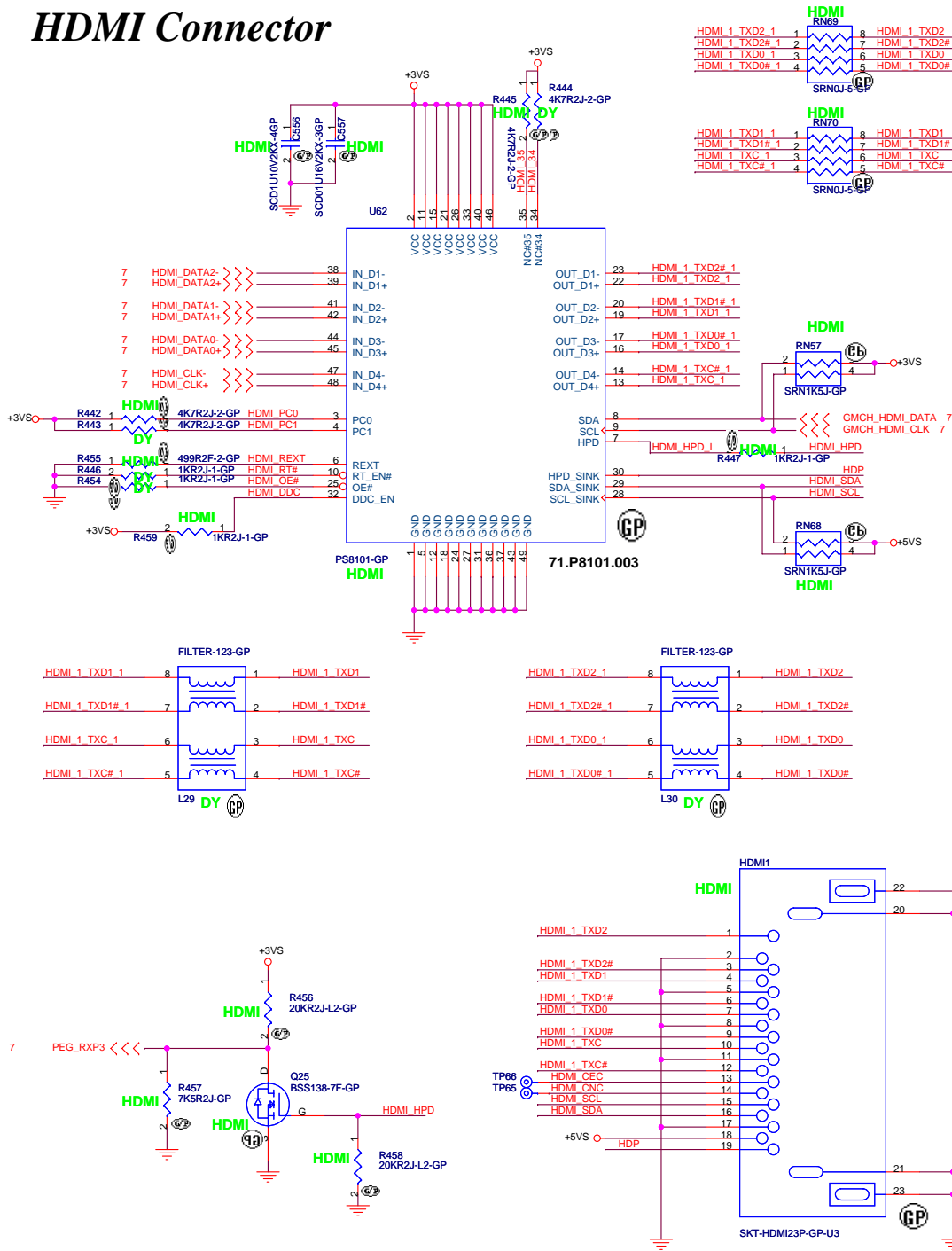
8101E use this circuit, 8102E dummy this circuit



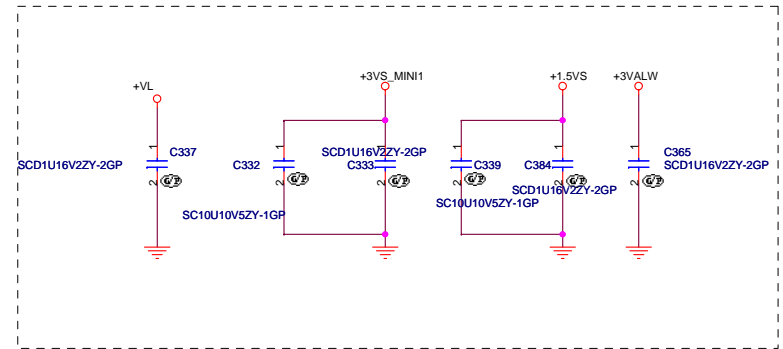
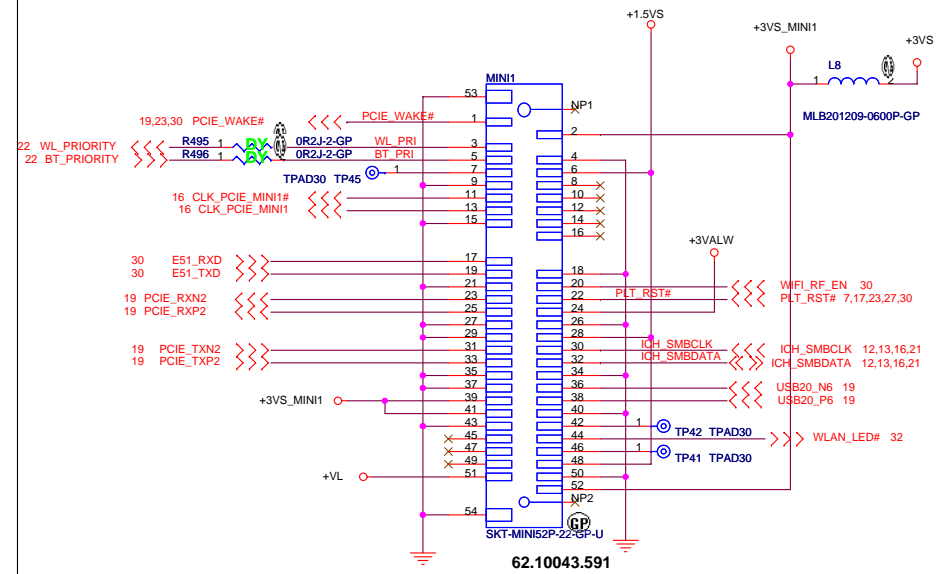
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緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Neihu, Taipei Hsien 221, Taiwan, R.O.C.		
Title	RTL8101E	
Size	Document Number	Rev
A3		SC
Date: Monday, January 07, 2008	Sheet 23	of 42



HDMI Connector



Mini Card Connector1(802.11a/b/g)



&ltCore Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number

MINI CARD/HDMI CONN.

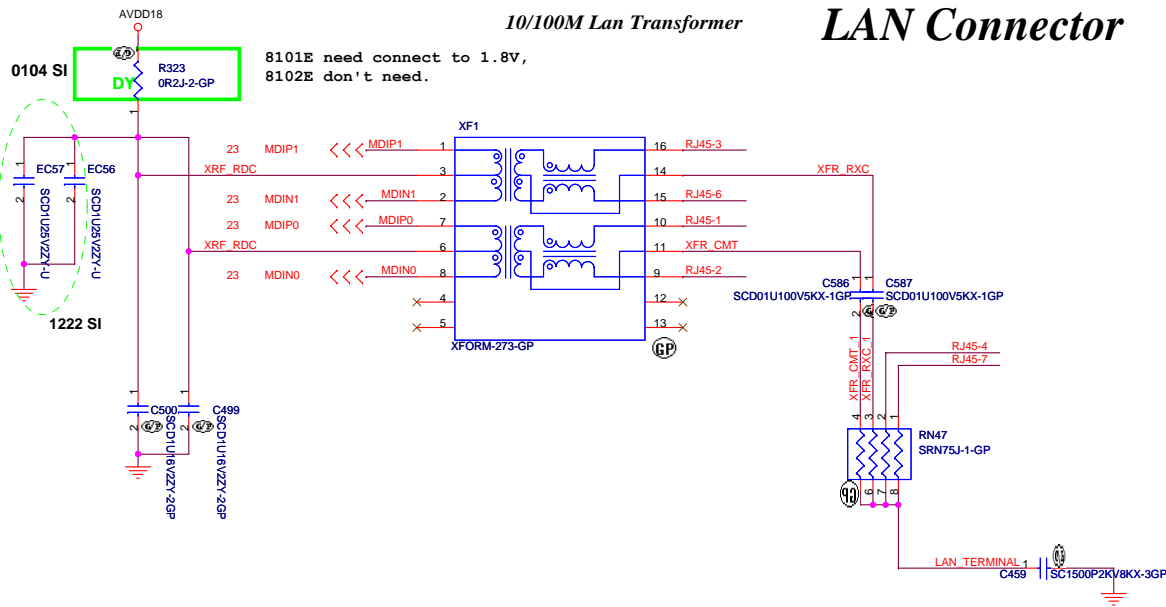
Warrior

Rev
SC

Date: Monday, January 07, 2008

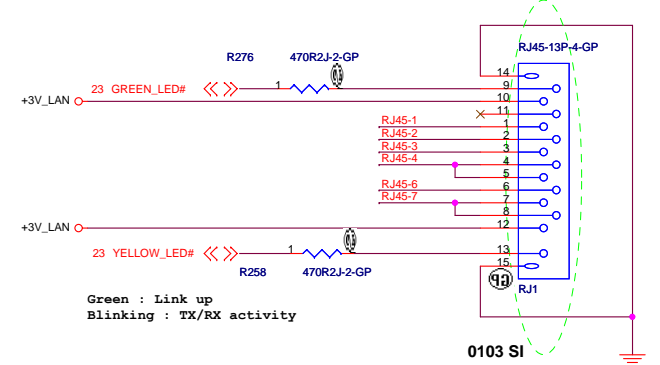
Sheet 26 of

42



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:

Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

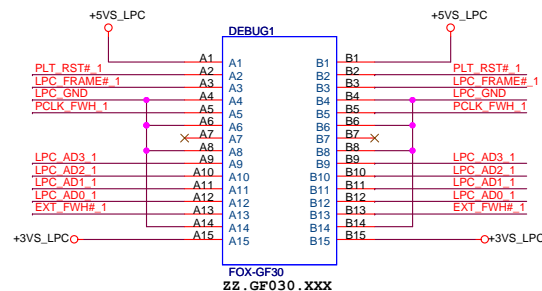
Golden Finger for Debug Board

TOP VIEW (A)

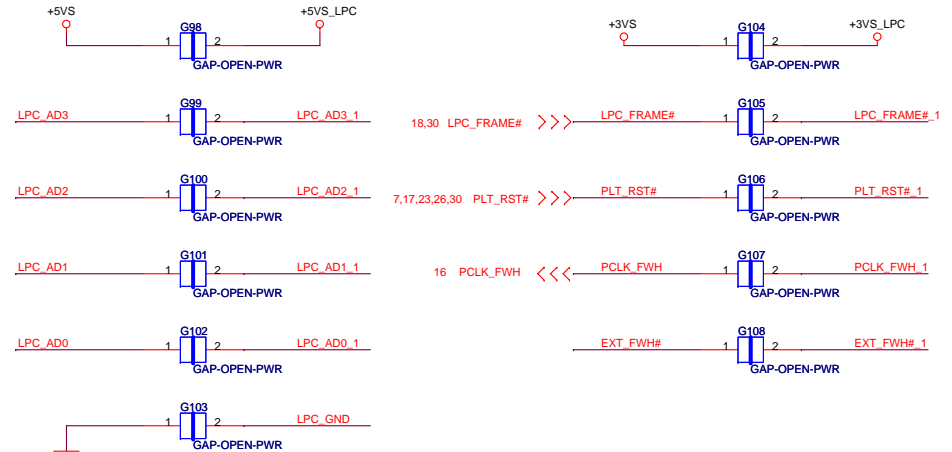
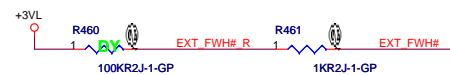
A15 (B1)
A14 (B2)
:
:
:
A2 (B14)
A1 (B15)

BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Please put near board edge.



<Core Design>

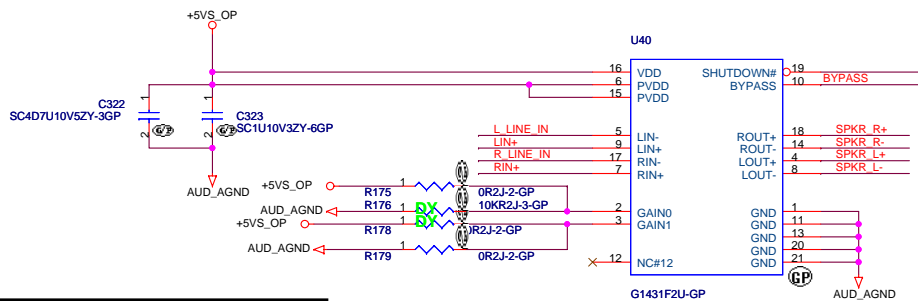
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Taipei Hsien 221, Taiwan, R.O.C.

Title
Size A3 Document Number
Date: Monday, January 07, 2008

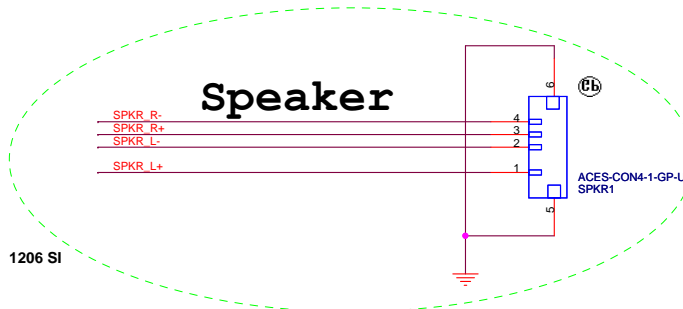
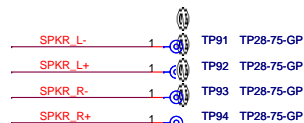
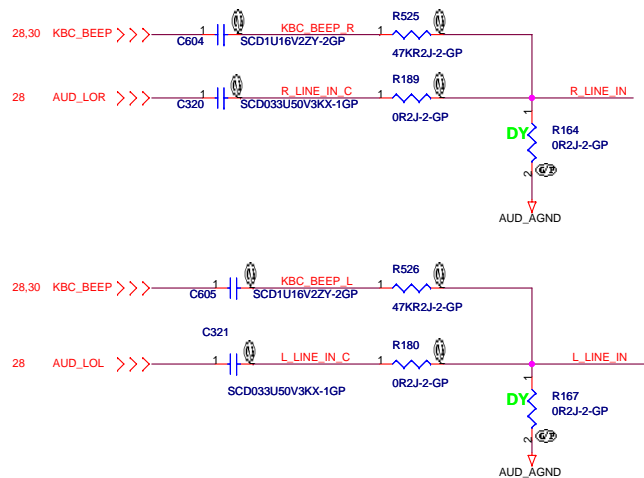
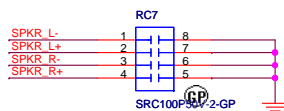
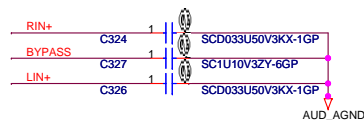
LAN CONN/Debug

Warrior

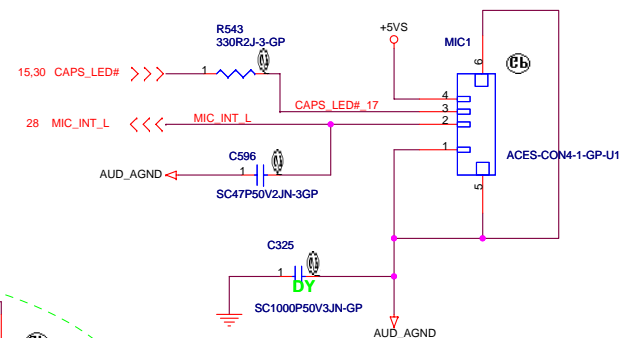
Rev SC



GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



MIC



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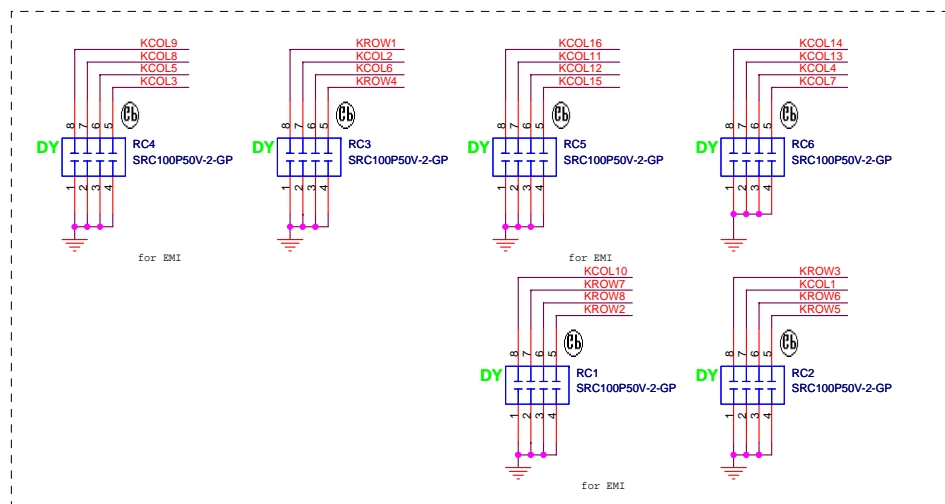
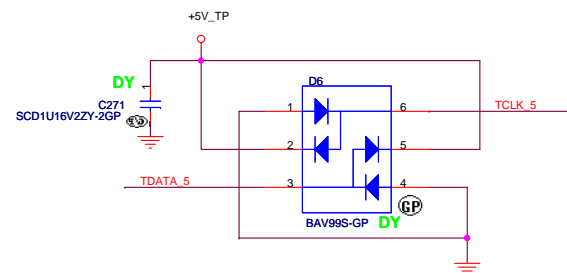
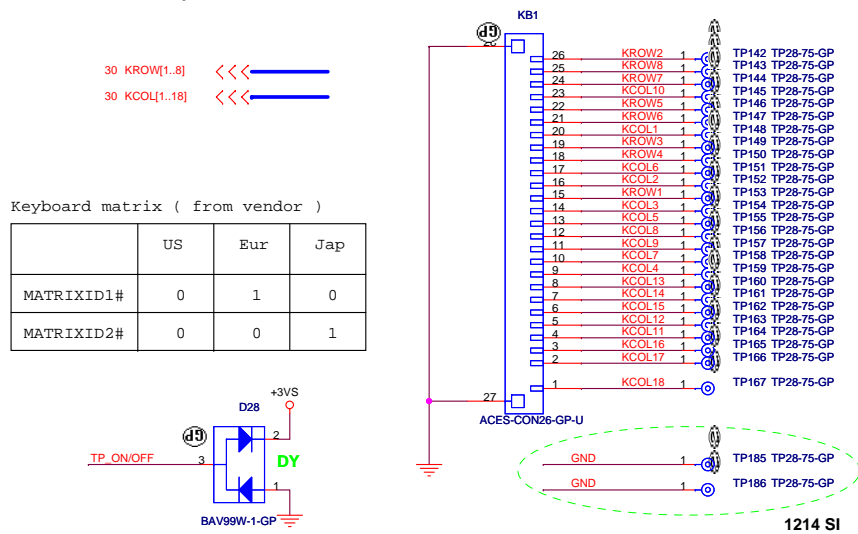
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP/SPEAKER**

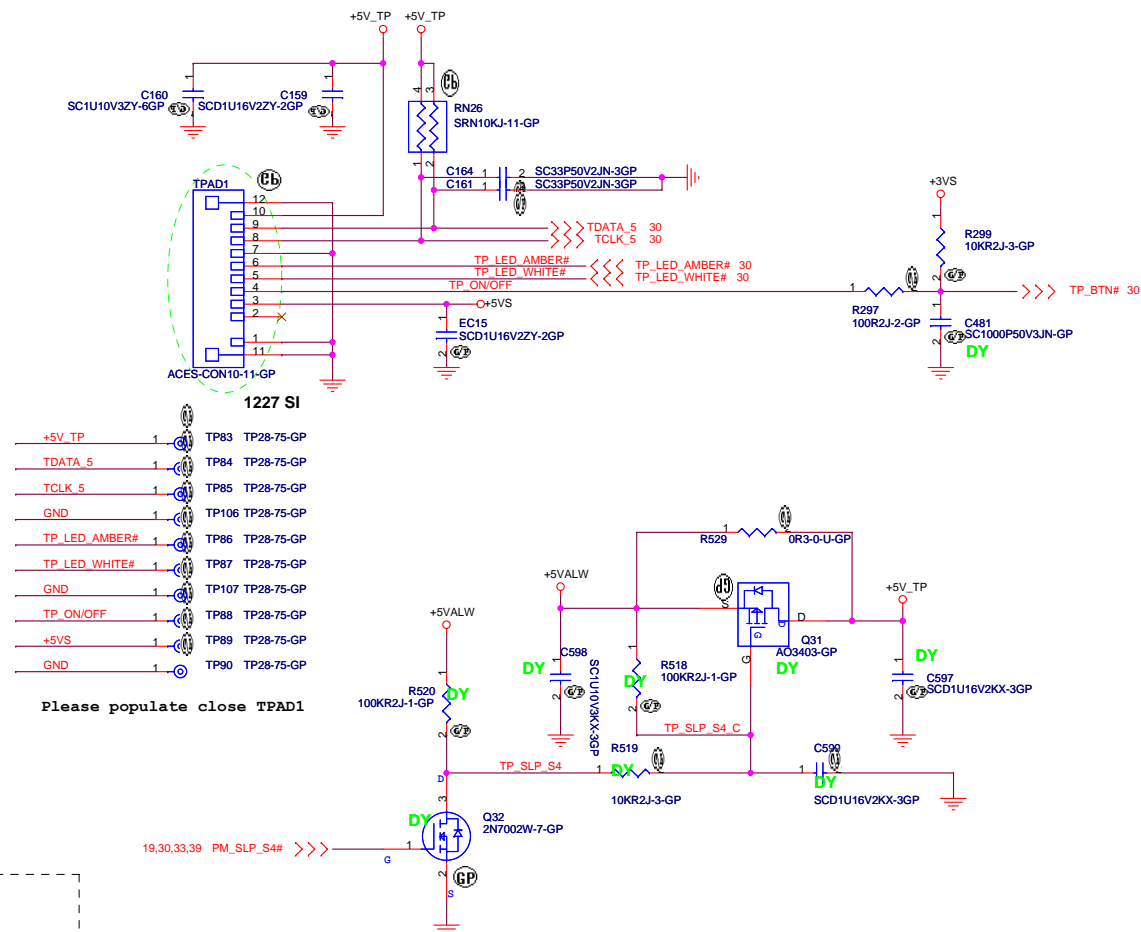
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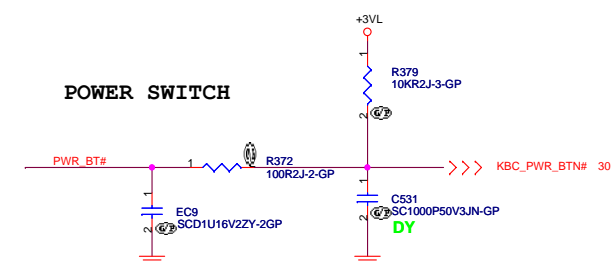
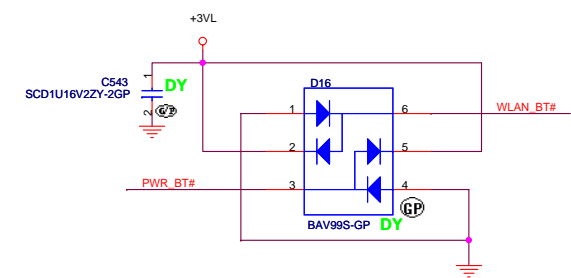
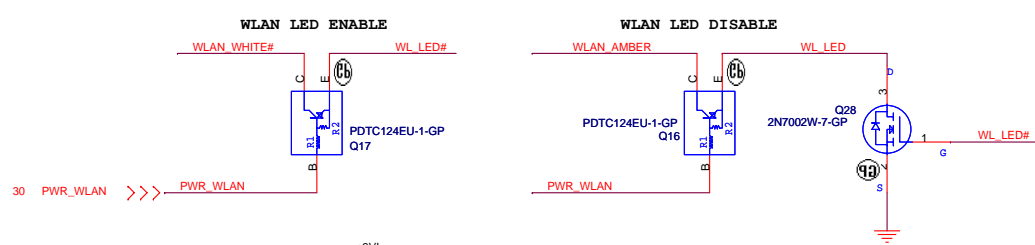
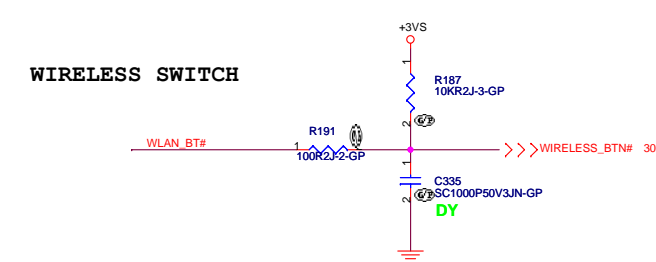
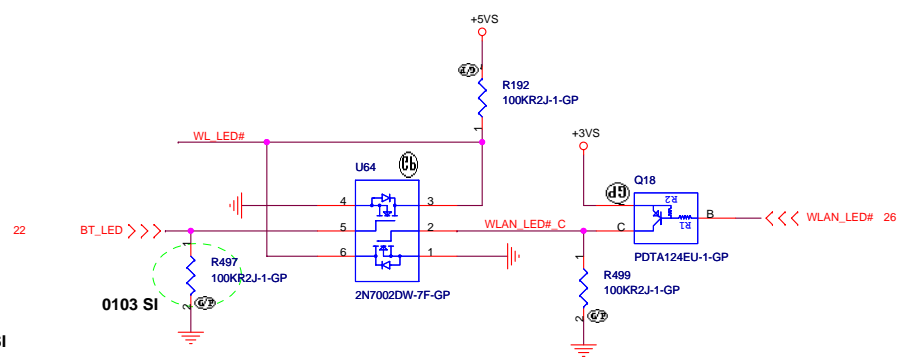
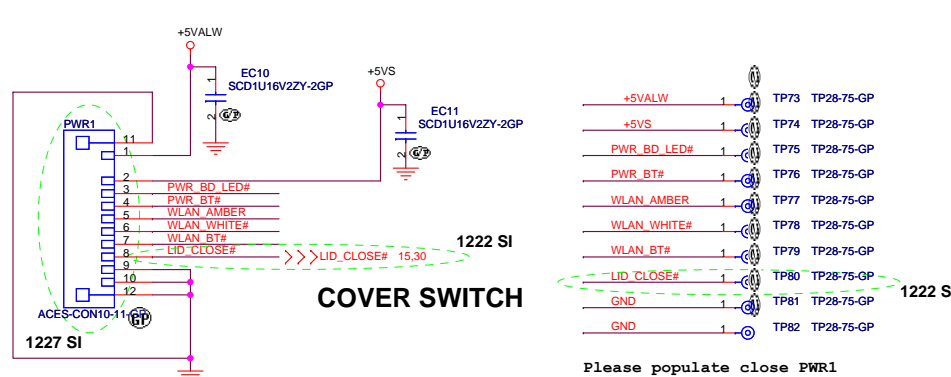
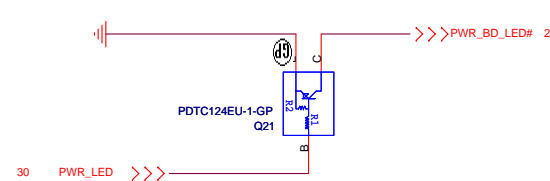
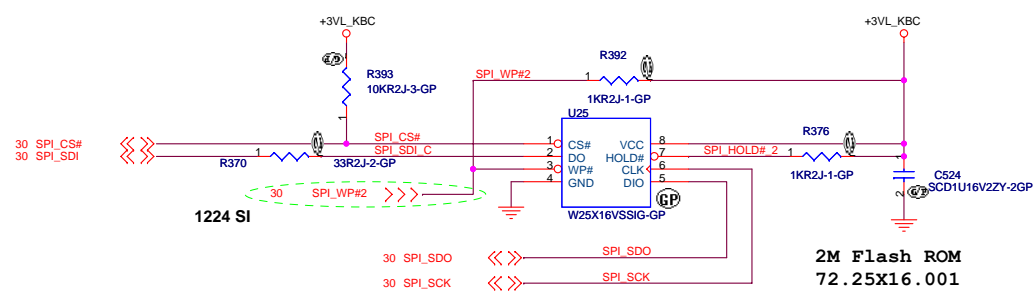
Date: Monday, January 07, 2008 Sheet: 29 of 42

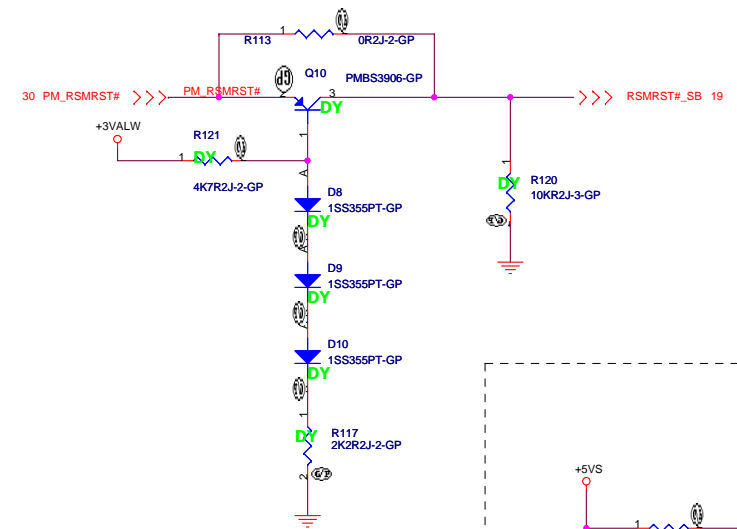
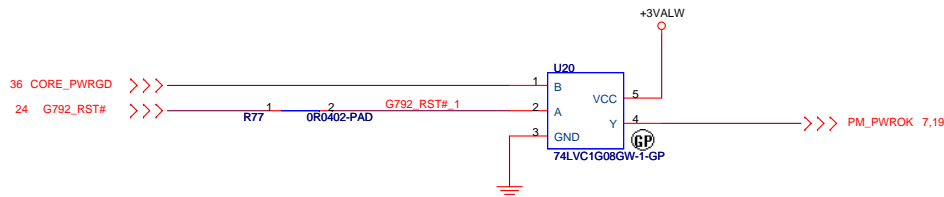
Internal KeyBoard Connector



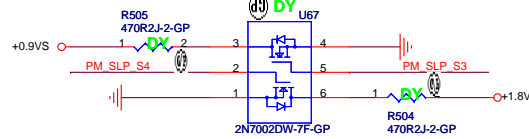
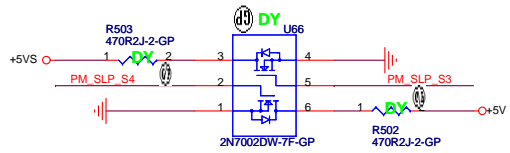
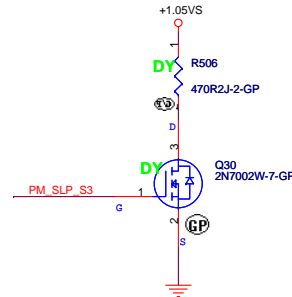
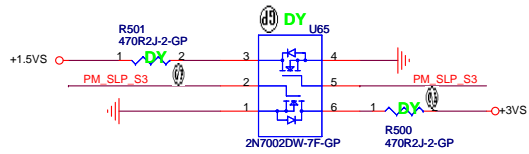
TouchPad Connector







Discharge Circuit

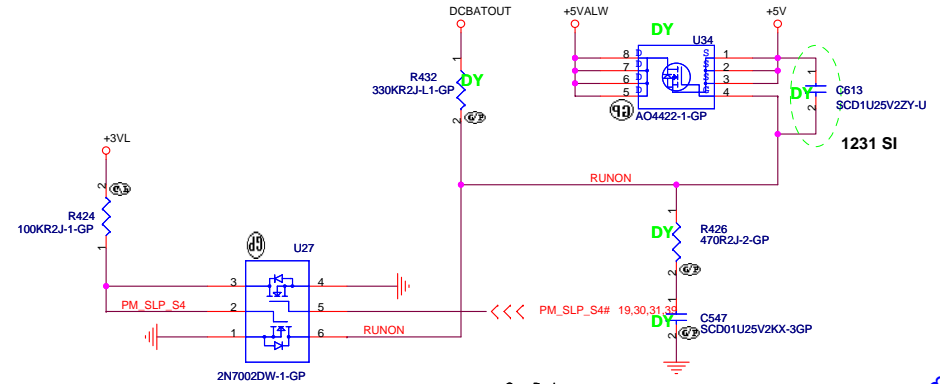
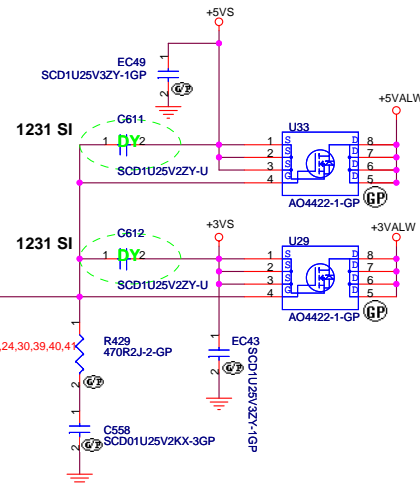
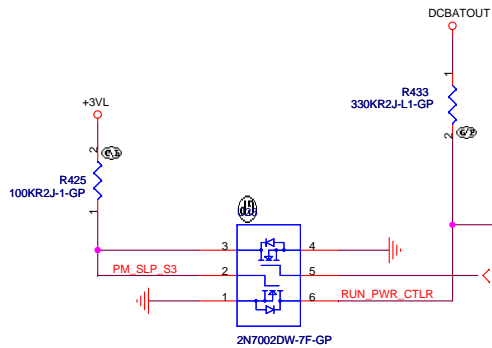


Populate close U34

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

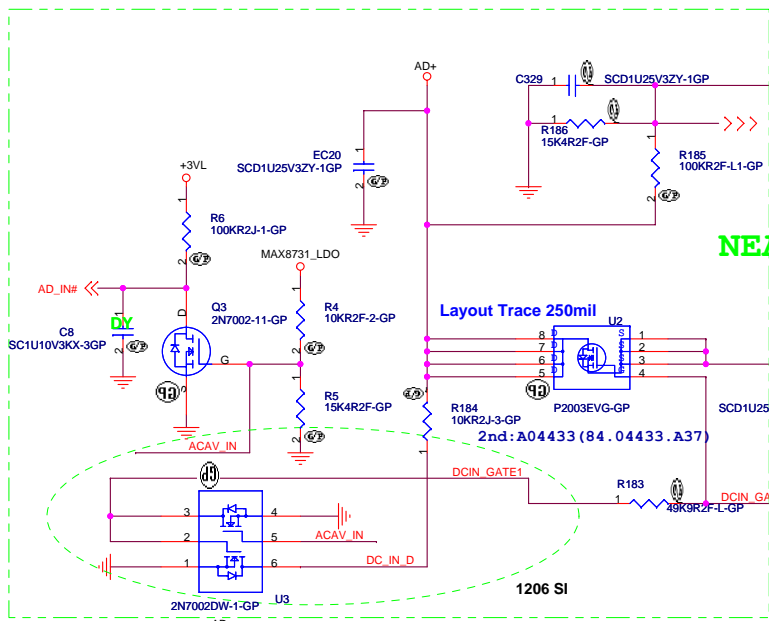
+5VALW to +5V Transfer

Run Power



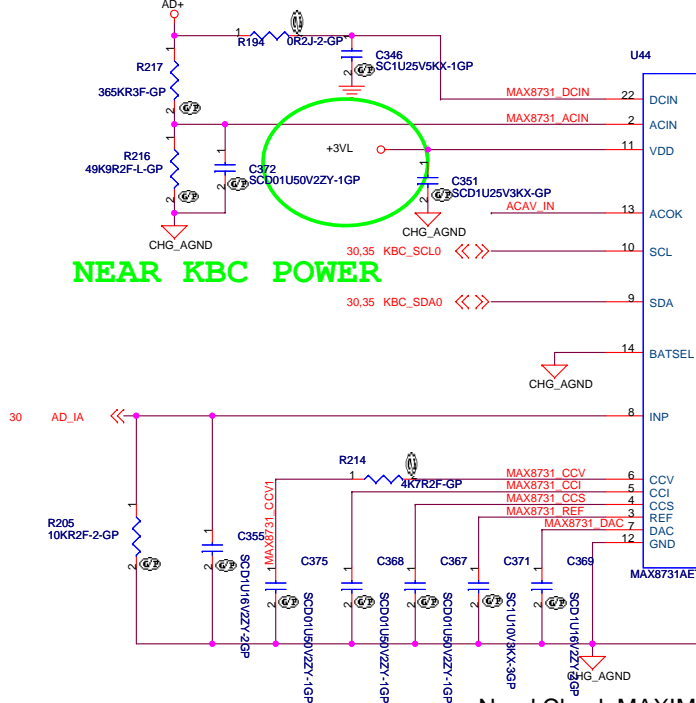
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Size A3	Document Number	Rev
	Warrior	SC
Date: Monday, January 07, 2008	Sheet 33 of 42	

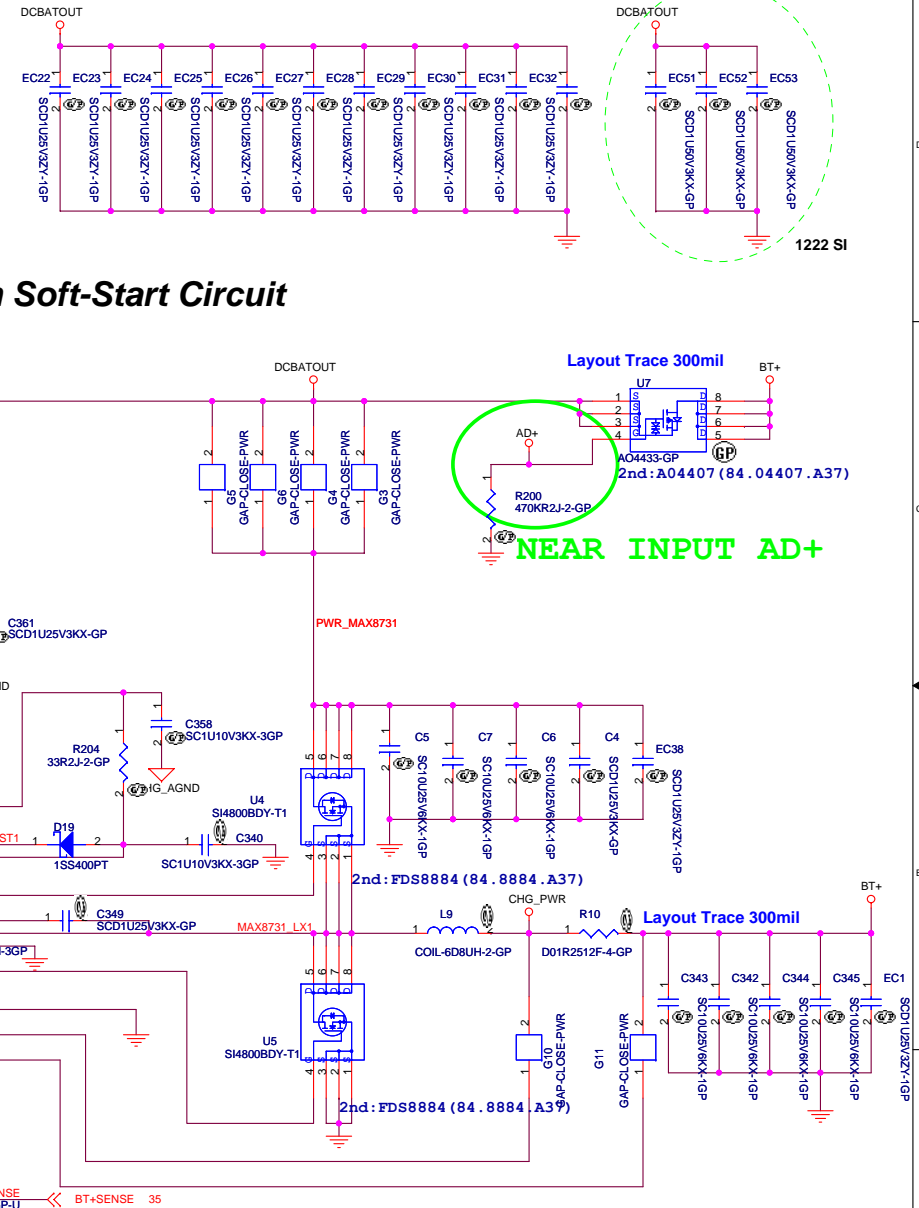


AIRLINE_VOLT 30
AD<17V, disable
charger function

Adaptor In Soft-Start Circuit



Need Check MAXIM Sming Use MAX8731 or MAX8731A



<Core Design>

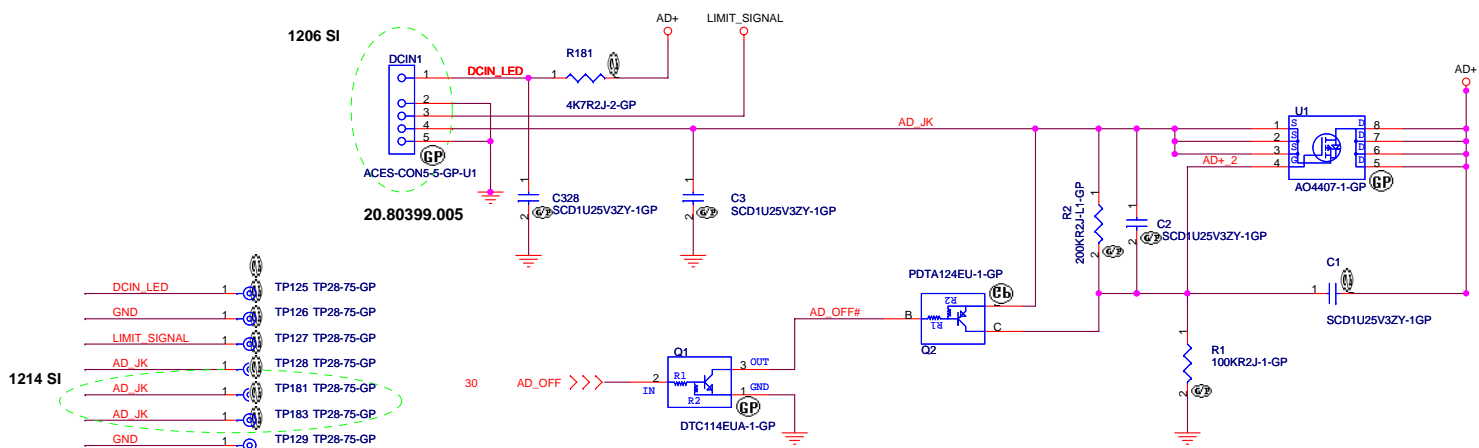
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File: **CHARGER MAX8731ETI**

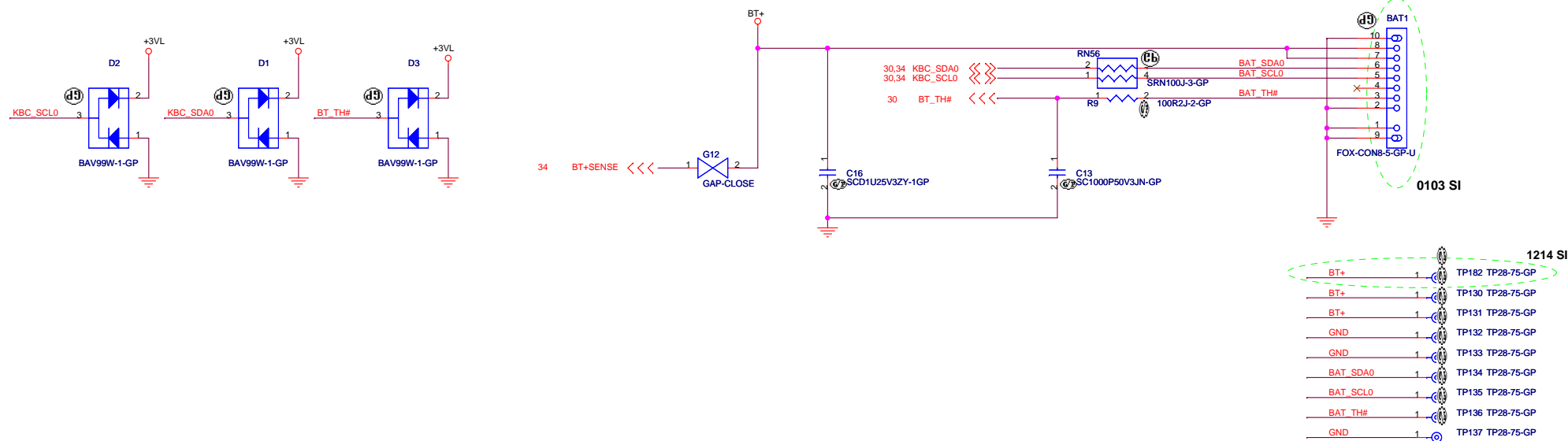
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Date: Monday, January 07, 2008 Sheet 34 of 42

Adaptor in to generate DCBATOUT



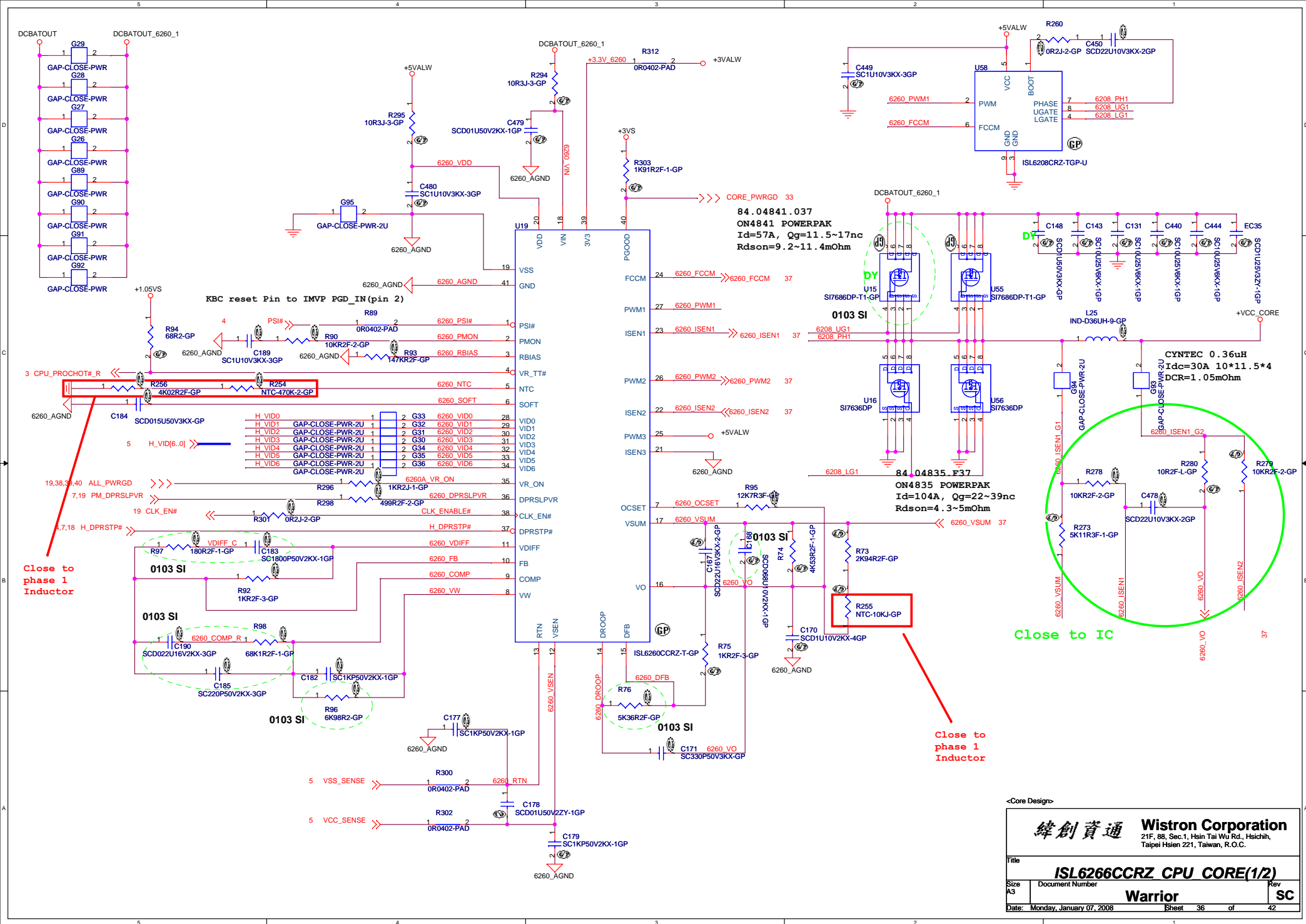
BATTERY CONNECTOR



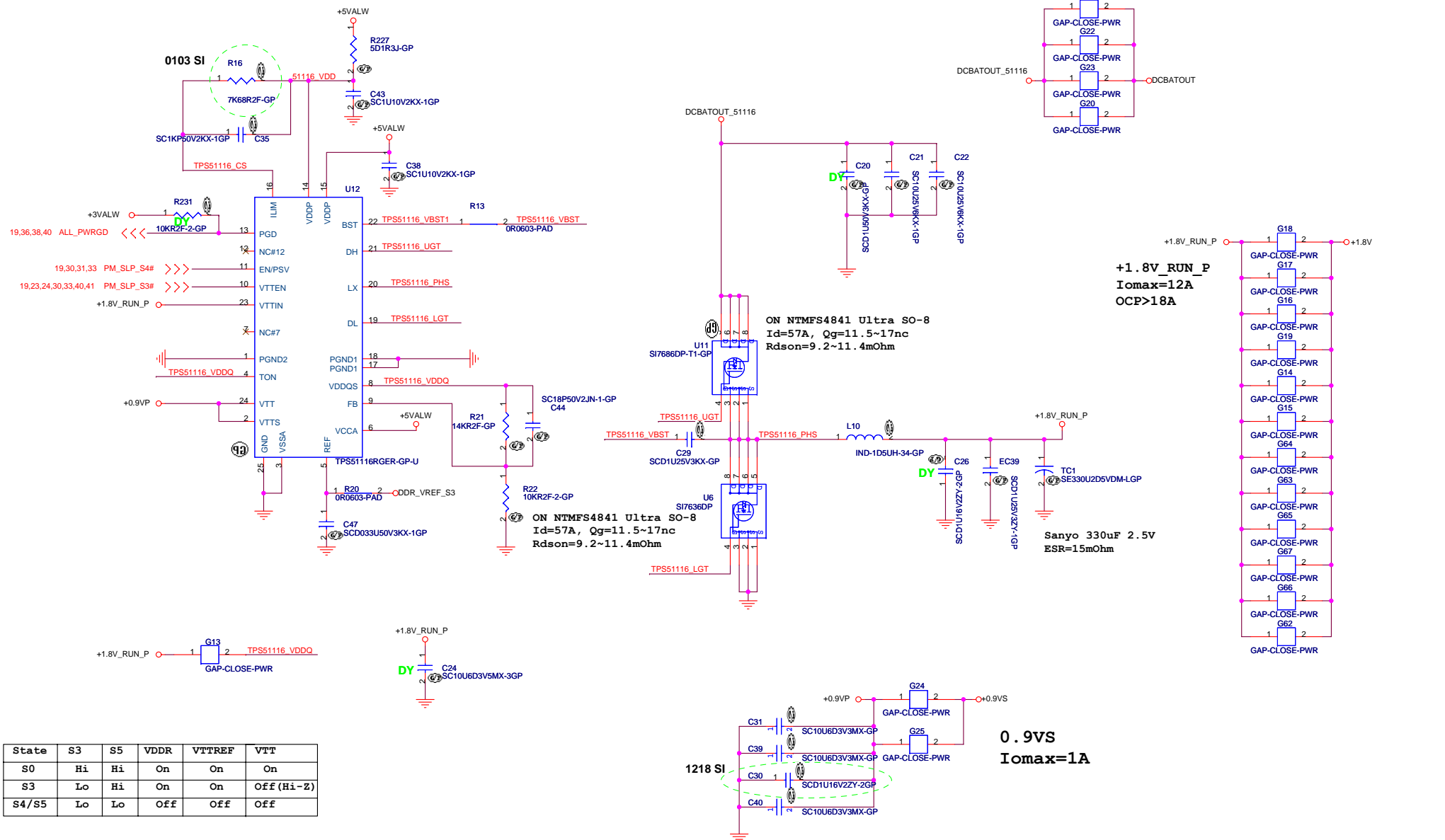
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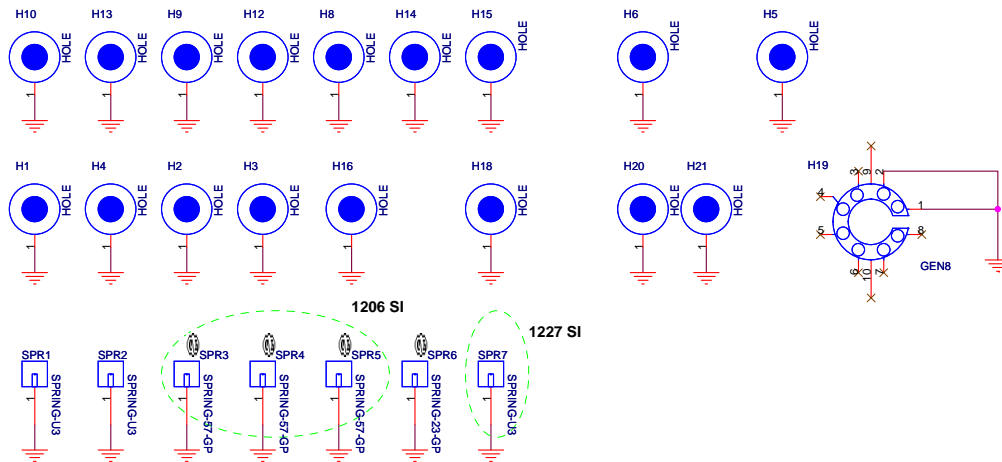
Title AD/BATT CONN
Size A3 Document Number Warrior Rev SC
Date: Monday, January 07, 2008 Sheet 35 of 42



TI TPS51116 for 1D8V and 0D9V







SPR1-2: 34.40U07.001
 SPR3-5: 34.42T14.002
 SPR6 : 34.39S07.003
 SPR7 : 34.40U07.001

<Core Design>

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Title	MISC
Size A3	Document Number
Date: Monday, January 07, 2008	Rev SC
Sheet 42 of 42	