A.2 MOS transistor in weak and strong inversion

In this section I will treat briefly the operation of the MOS transistor: 1) in weak inversion; 2) in strong inversion.

A.2.1 Weak inversion

The transistor works in weak inversion region if the following condition are satisfied:

$$V_G - nV_S < V_{TH0}$$

The last condition may be expressed in current I_{DS} term as follows:

$$I_{DS} < I_s$$

where the current I_s is equivalent to the drain-source current when the gate-source voltage is equal to V_{TH0}. The current I_{DS} in weak inversion region is given by [111] [81]:

$$I_{DS} = I_s e^{(\frac{V_G - nV_S - V_{THO}}{nV_t})}(1 + e^{\frac{-V_{DS}}{V_t}})$$

If $V_{DS} >> V_t$, the transistor works in saturation region and then the last equation becomes:

$$I_{DS} = I_s e^{(\frac{V_G - nV_S - V_{THO}}{nV_t})}$$

From the last equation one notes that if $V_G - nV_S < V_{TH0}$ the current $I_{DS} < I_s$.

A.2.2 Strong inversion

If $V_G - nV_S > V_{TH0}$ or $I_{DS} > I_s$ the last equation is not valid, because the transistor works in strong inversion, and as a conseguence there is another relation.

If $V_{DS} < V_G - nV_s - V_{TH0}$ the transistor is in lineare region. The current is given by [111]:

$$I_{DS} = \frac{\beta}{n}(V_G - nV_S - V_{THO} - \frac{V_{DS}}{2})V_{DS}$$

If $V_{DS} > V_G - nV_s - V_{TH0}$ the transistor is in saturation region. The current is given by:

$$I_{DS} = \frac{\beta}{2n}(V_G - nV_S - V_{THO})^2(1 + \lambda V_{DS})$$

Where λ is the channel width modulation parameter.

Finally, if the current I_{DS} is not greater enough than I_s or is not lower enough than I_s, the transistor is in moderate inversion [97] and as a conseguence I can not use the precedent equations (see next paragraph).

A.2.3 Unique model of the MOSFET transistor

[111] has proposed a unique model of the MOS transistor where it is valid for strong inversion and weak inversion and it has a good precision for moderate inversion. The equation is given by:

$$I_{DS} = I_s \ln^2(1 + e^{\frac{V_G - nV_s - V_{TH}}{2nV_T}})$$

If $V_G - nV_s << V_{TH}$ then the last equation can be approximated as follows:

$$I_{DS} = I_s e^{\frac{V_G - nV_s - V_{TH}}{nV_T}}$$

Else if $V_G - nV_s >> V_{TH}$ then:

$$I_{DS} = I_s(\frac{V_G - nV_s - V_{TH}}{2nV_T})^2$$

A.3 Design rules for circuits operate in weak or strong inversions

To design a transistor that works in weak o strong inversion, I have to design its dimensions in a way that the current I_{DS} must be sufficiently greater or lower than the specific current of the transistor I_s.

Eq. 60 may be rewritten as follows:

$$I_s = 2n\mu C_{ox} V_t^2 \frac{W}{L} = A\frac{W}{L} \tag{61}$$

where $A = 2n\mu C_{ox} V_t^2$ is the specific current when (W/L)=1. I_s dipends linearly on (W/L). For n-channel transistor, I_s is given by:

$$I_{sn} = 2n\mu_n C_{ox} V_t^2 \frac{W_n}{L_n} = A_n \frac{W_n}{L_n}$$

For p-channel transistor, I_s is given by:

$$I_{sp} = 2n\mu_p C_{ox} V_t^2 \frac{W_p}{L_p} = A_p \frac{W_p}{L_p}$$

where μ_n is the n-channel transistor mobility, μ_p is the p-channel transistor mobility, C_{ox} is the oxide capacitor, W_n and L_n are the width and the lenght of n-channel transistor, W_p and L_p are the width and the lenght of p-channel transistor. The values of A_n and A_p dipend on the type of technology: using the technology *ES2 CMOS 1.0 μm* ($ECPD10$ process), A_n=185nA, A_p=53nA; using *ES2 CMOS 0.7 μm* ($ECPD07$ process), A_n=235nA, A_p=82nA.

The ratio A_{np} between A_n and A_p is equal to the ratio between μ_n and μ_p. The ratio is used to simplify the design, or rather a n-channel transistor designed (dimensions calculated), one can multiply the dimensions of n-channel transistor by the ratio A_{np} to obtain the dimensions of the p-channel transistor. A_{np} is given by:

$$A_{np} = \frac{A_n}{A_p} = \frac{\mu_n}{\mu_p}$$

Using the technology *ES2 CMOS 1.0 μm* ($ECPD10$ process), A_{np}=3.49, and using *ES2 CMOS 0.7 μm* ($ECPD07$ process), A_{np}=2.865.

Approximately, if the current I_{DS} is greater than I_s, the transistor works in strong inversion and vice versa, if the current I_{DS} is lower than I_s, the transistor works in weak inversion. But really, there is a region, the moderate inversion region, which is the region that we aren't sure that the transistor works in weak or strong inversion. For that to be sure, one can use a factor of security FS greater than 1; if the current I_{DS} is greater than (FS I_s), we are sure that the transistor works in strong inversion, on the contrary if it is lower than (I_s/FS) the transistor works in weak inversion.

From equations point of view, I_{DS} is given by:

$$\begin{cases} I_{DS} \leq \frac{I_s}{FS} & \text{the transistor is biased in weak inversion} \\ \frac{I_s}{FS} \leq I_{DS} \leq FS \times I_s & \text{the transistor is biased in moderate inversion} \\ I_{DS} \geq FS \times I_s & \text{the transistor is biased in strong inversion} \end{cases}$$

W/L may be expressed as a function of I_{DS} (assuming that the current is constant) as follows:

$$\begin{cases} \frac{W}{L} \geq FS \times \frac{I_{DS}}{A} & \text{the transistor is biased in weak inversion} \\ FS \times \frac{I_{DS}}{A} \leq \frac{W}{L} \leq \frac{I_{DS}}{FS \times A} & \text{the transistor is biased in weak inversion} \\ \frac{W}{L} \leq \frac{I_{DS}}{FS \times A} & \text{the transistor is biased in weak inversion} \end{cases}$$

If the current I_{DS} varies in the range $[0, I_{max}]$, the following rules must be satisfied: 1) in weak inversion, the transistor is designed using the maximum current I_{max}; 2) in strong inversion, the transistor is designed using the minimum current (minimum current =0), but because it is not possible to design with 0 minimum current, one can take a small percentage of the maximum current as minimum current αI_{max} (e.g. $\alpha = 0.1$). At this point W/L is given by:

$$\begin{cases} \frac{W}{L} \geq \frac{FS \times I_{max}}{A} & \text{weak inversion} \\ \frac{W}{L} \leq \frac{\alpha I_{max}}{FS \times A} & \text{strong inversion} \end{cases} \tag{62}$$

In Fig. 89 one can see the three regions of operation [32]. Given the current of the transistor I_{DS} and the operation region, one can calculate from the figure the ratio W/L.

Please note that, to obtain dimension ratio $\frac{W}{L} \approx 1$ (that is to say that the transistor it is not very wide and not very long), it is needed to design it in a way that, in strong inversion the current I_{DS} must be in the range of micro ampere (μA) and, in weak inversion, I_{DS} in the range of (nA). On the contrary, a transistor works in weak inversion with a current I_{DS} in μA range, it must have a W very wide, vice versa a transistor works in strong inversion with a current I_{DS} in nA range, it must have a L very long. Note that if the channel lenght L increases the operating frequency of the transistor decreases.

In table 14 [32], the dimensions of n-channel transistor are calculated with respect to the current, assuming $FS = 10$ and using the parameters of *ES2 CMOS 0.7μm*. For a p-channel transistor the values of the table must be multiplied by A_{np}.

For example, for a n-channel transistor: 1) for a current of 25nA the transistor has W/L of 0.01 (strong inversion) and 1 (weak inversion); 2) for a current of $2\mu A$ the transistor has ratio of 0.85 (strong inversion) and 85 (weak inversion). For a p-channel transistor, the above results must be multiplied by A_{np}.

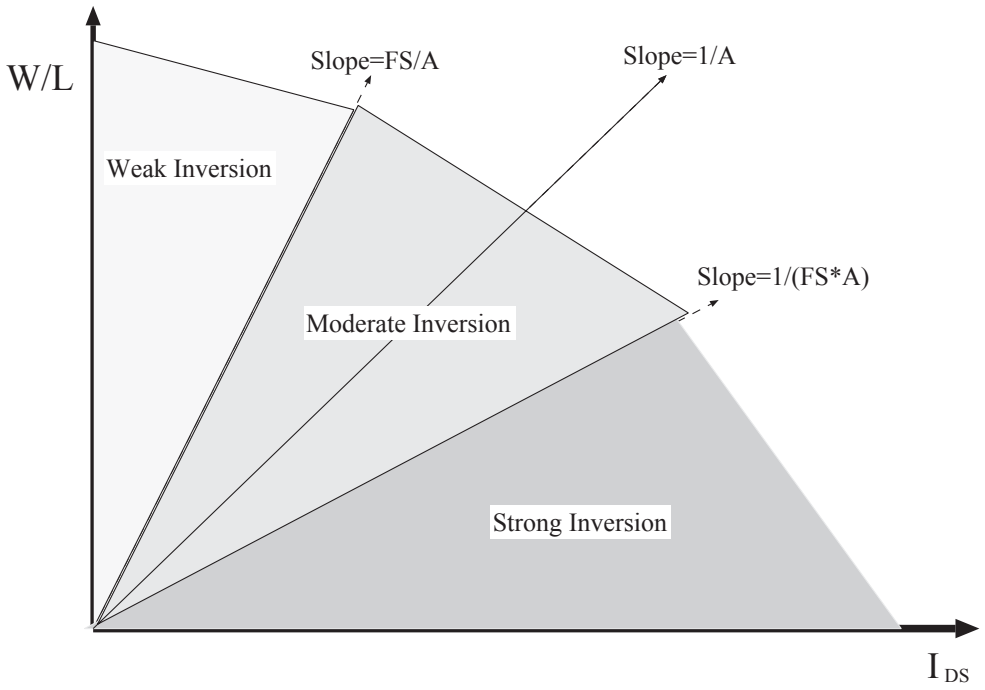

Figure 89: The relation between the dimension ratio of a transistor $\frac{W}{L}$ and the current I_{DS}.

I_{DS} in μA	0.025	0.05	0.1	0.25	0.5	1	2	4	5	10
W/L weak inversion	1.06	2.127	4.25	10.6	21.3	42.5	85	170	212	425
W/L mederate inversion	0.106	0.2127	0.425	1.06	2.13	4.25	8.5	17.0	21.2	42.5
W/L strong inversion	0.0106	0.02127	0.0425	0.106	0.213	0.425	0.85	1.70	2.12	4.25

Table 14: The computation of the transistor dimensions in function of the drain source current.