# BIPOLAR AND MOS ANALOG INTEGRATED CIRCUIT DESIGN

**ALAN B. GREBENE**

*MICRO-LINEAR CORPORATION*
*SUNNYVALE, CALIFORNIA*

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converter in a feedback path (see Figs. 15.14 and 15.15). In such a case, potential nonmonotonic behavior of the D/A converter can result in missing codes at the digital output. The missing codes are most likely to occur at the so-called major carry points in the transfer characteristics, where the MSB or the next significant bit is changing sign.

The gain and offset errors can be trimmed externally. However, linearity and differential nonlinearity errors cannot be eliminated by adjustment. They can be minimized by improving the matching and tracking of circuit components, or by the proper choice of the circuit configuration.

## 15.2. INTEGRATING-TYPE A/D CONVERTERS

Integrating A/D converters perform the A/D conversion in an indirect manner. The analog input is first converted to a timing pulse whose duration is proportional to the analog voltage $V_A$. The duration of the timing pulse is then measured in a digital format by counting the number of cycles of a stable reference frequency (i.e., the clock signal) between the beginning and the end of the timing pulse. Because of this basic principle of operation, such converters are often called *indirect* or *pulse-width-modulating* converters.

Figure 15.8 shows an illustrative example of a simple integrating A/D converter system. The operation of the converter is as follows. Before the start of

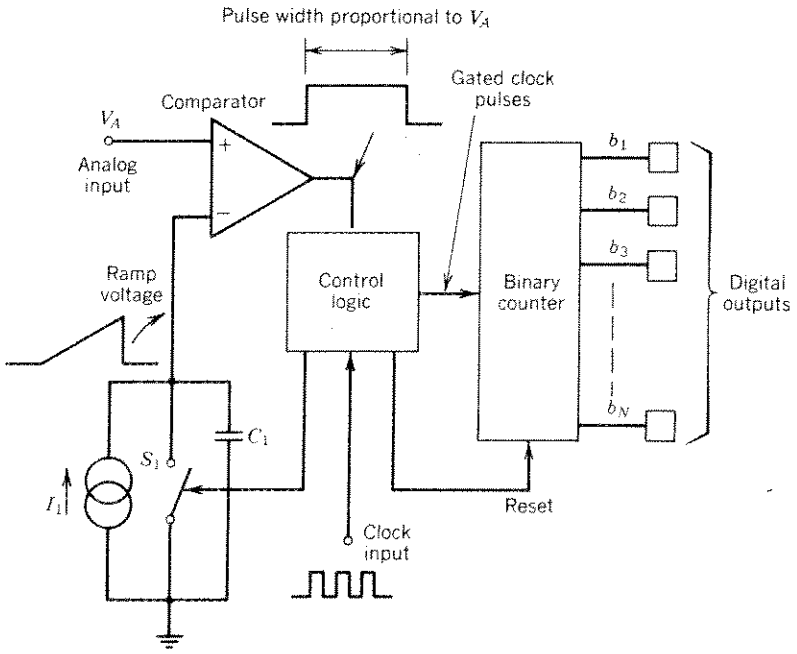


**FIGURE 15.8.** Block diagram of simple integrating A/D converter.

the conversion cycle, the counter is reset to zero and the switch $S_1$ is closed. When the conversion cycle is started, the switch $S_1$ is opened, and the current source $I_1$ generates a linearly rising ramp voltage across the integrating capacitor $C_1$. During this time, the counter starts counting the input clock cycles. When the linear ramp across $C_1$ reaches the level of the analog input $V_A$, the comparator changes state, stops the counter, and ends the conversion cycle. The final count in the counter is then the digital equivalent of the analog signal $V_A$. For example, if it takes a total count $N_T$ to reach the full-scale output $V_{FS}$, then the count $n$ in the counter when the ramp reaches $V_A$ is

$$n = N_T \frac{V_A}{V_{FS}} \tag{15.10}$$

For $N$-bit resolution, $N_T = 2^N$, and the accumulated count $n$ in the counter is

$$n = \frac{2^N}{V_{FS}} V_A \tag{15.11}$$

The accumulated count $n$ in the counter is quantized in increments of unit clock cycles. Therefore, each additional clock cycle corresponds to 1 LSB increment in $V_A$. The accumulated count is normally displayed as the digital states of the $N$-stage binary counter. The first counter stage output which changes state with every clock input corresponds to the LSB, and the last counter stage which changes state with every $2^{N-1}$ clock cycles corresponds to the MSB output.

Although the simple counter circuit of Figure 15.8 illustrates the basic principle of operation of integrating A/D converters, it is seldom used in practice because of inaccuracies associated with the initial ramp startup point, as well as with the control of the absolute values of $I_1$ and $C_1$. Some of these errors can be eliminated to a large degree by using more complex circuit techniques. Two such circuit techniques used for this purpose are the *single-slope* and the *dual-slope* integration methods.

### Single-Slope A/D Converters

The single-slope converter is essentially identical to the basic circuit of Figure 15.8, except that the ramp voltage does not start exactly at zero, but at a slightly lower voltage level. Figure 15.9 shows the functional block diagram and the timing waveforms associated with a typical single-slope converter system. Prior to the start of the conversion cycle, the switch $S_1$ across the integrating operational amplifier $A_1$ is closed, and the integrator output is clamped to a negative voltage $-V_1$ at a level slightly below zero. At the start of the conversion cycle, $S_1$ is opened, and the integrator output ramps in the positive direction with a slope equal to $1/R_1C_1$. When this ramp reaches zero, Comparator 1 changes state and gates the clock signal into the counter. The clock pulses are counted, and the count is accumulated in the counter until the ramp level reaches the analog

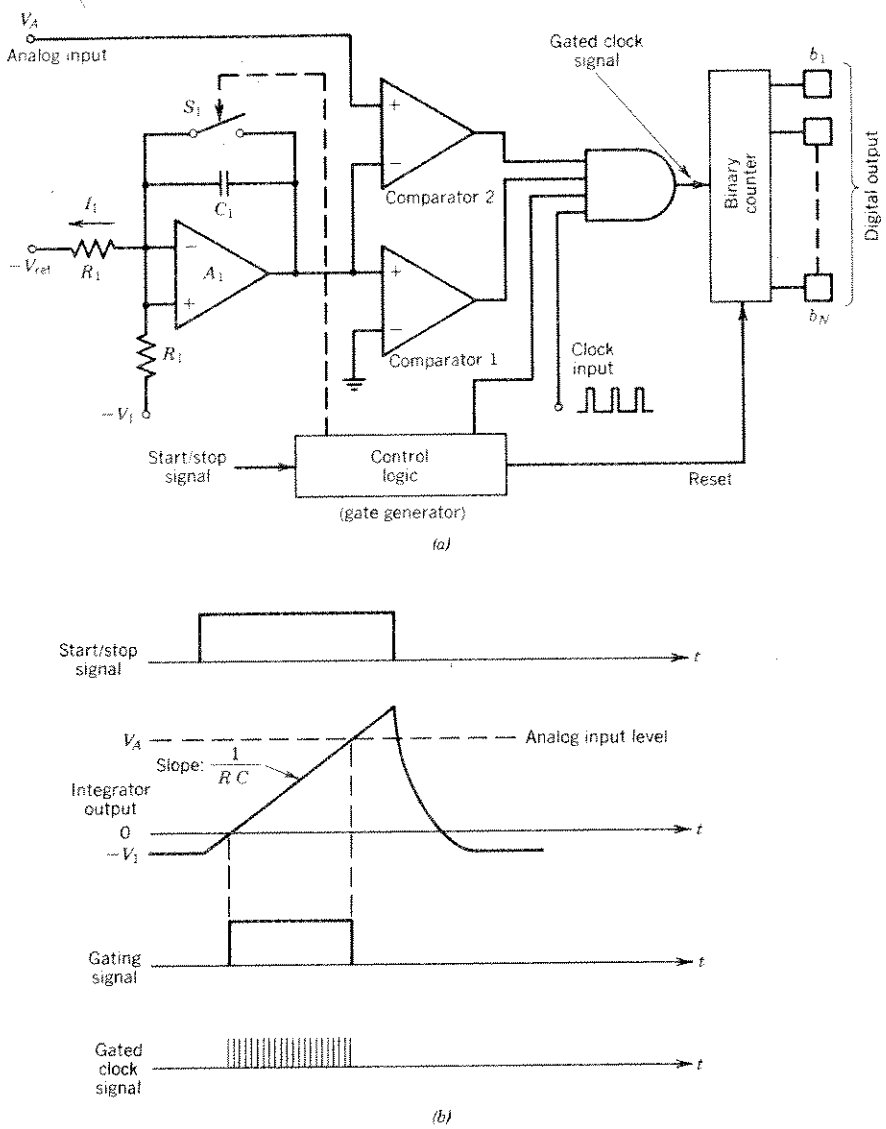


**FIGURE 15.9.** *Ramp-pick-off* or single-slope-type integrating A/D converter. (*a*) Basic block diagram. (*b*) Timing waveforms.

input level $V_A$. At that point, Comparator 2 changes state and gates off, the clock signal going into the counter. The accumulated count $n$ in the counter is the digital equivalent of the analog signal $V_A$, as given by Eq. (15.11).

The single-ramp converter has one basic drawback. Assuming that the comparator, the integrator, and the voltage reference characteristics are ideal, the

system accuracy depends strongly on the absolute value of the $R_1C_1$ product which determines the scale-factor accuracy and stability. This is inherent in all single-slope-type converters, and can be avoided by using the dual-slope conversion techniques described in the next section.

## Dual-Slope A/D Converters

The dual-slope-type converter is one of the most popular types of integrating A/D converters. It eliminates most of the error sources and component tolerance requirements associated with the single-slope circuits. Figure 15.10 shows the functional block diagram of a dual-slope converter. The system operates by integrating the unknown analog signal $V_A$ for a fixed period of time (i.e., for a fixed count). The resulting integrator output level is then returned to zero, by integrating a known reference voltage of opposite polarity. The length of time required for the integrator output to return to zero, as measured by the number of clock cycles gated into a counter, is proportional to the value of the input signal, averaged over the integration period.

With reference to the block diagram of Figure 15.10, the principle of operation can be illustrated as follows. Prior to the start of conversion, the switch $S_2$ is closed, the integrator output voltage $V_X$ is clamped to ground, and $S_1$ is connected to the analog voltage $-V_A$. For illustrative purposes, the analog input is assumed to be negative and varying between zero and $-V_{FS}$. At the start of

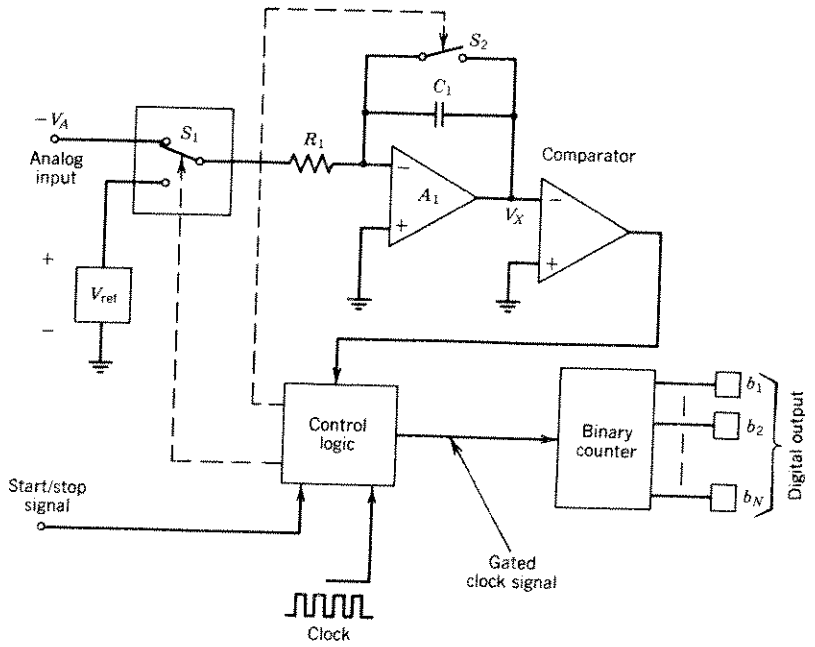


**FIGURE 15.10.** Block diagram of dual-slope A/D converter.

the first phase of the conversion cycle, the switch $S_2$ is opened, and the input signal is integrated for a predetermined time period, normally equal to $2^N$ clock cycles. During this time period, the integrator output voltage $V_X$ ramps up with the slope,

$$\left(\frac{dV_X}{dt}\right)_{\text{phase I}} = \frac{+V_A}{R_1C_1} \tag{15.12}$$

At the end of $2^N$ clock cycles, the counter is reset to zero, switch $S_1$ is connected to $V_{\text{ref}}$, and the integrator output ramps down with the slope

$$\left(\frac{dV_X}{dt}\right)_{\text{phase II}} = \frac{-V_{\text{ref}}}{R_1C_1} \tag{15.13}$$

During this phase, the clock cycles are accumulated in the counter until the ramp reaches back to zero, and the comparator changes state to stop the conversion. Then the count $n$ stored in the counter during this reference integration phase is the digital equivalent of the analog voltage

$$n = -V_A\frac{2^N}{V_{\text{ref}}} \tag{15.14}$$

Figure 15.11 shows the integrator output waveforms during the two phases of the converter operation for various values of analog input voltage. Note that the signal integration phase is associated with a fixed count and variable ramp slope depending on the value of the analog input. The reference integration phase is associated with a fixed ramp slope, but a variable count $n$. Since all ramp-down integration paths have the same slope during phase II, longer ramp-up signals due to large values of analog input take proportionally longer to return to zero during the ramp-down phase. Thus, the duration of the ramp-down phase, and the count accumulation during it, are both proportional to the value of the analog input.

The dual-slope conversion technique has some unique advantages for high-resolution converter design. Some of these are the following:

1. The conversion accuracy is independent of both the value of the integrator time constant (i.e., the $RC$ product) and the clock frequency, since these parameters affect the ramp-up and ramp-down times equally, as long as their values remain stable during the integration cycle. In this manner, long-term drifts due to time or temperature effects are largely avoided.
2. The linearity is excellent, determined primarily by the quality of the integrator ramp waveform. Differential nonlinearity is virtually eliminated since the analog function and the ramp waveform remain continuous during the conversion process. The only contribution to differential nonlinearity is the clock jitter during the counting interval.

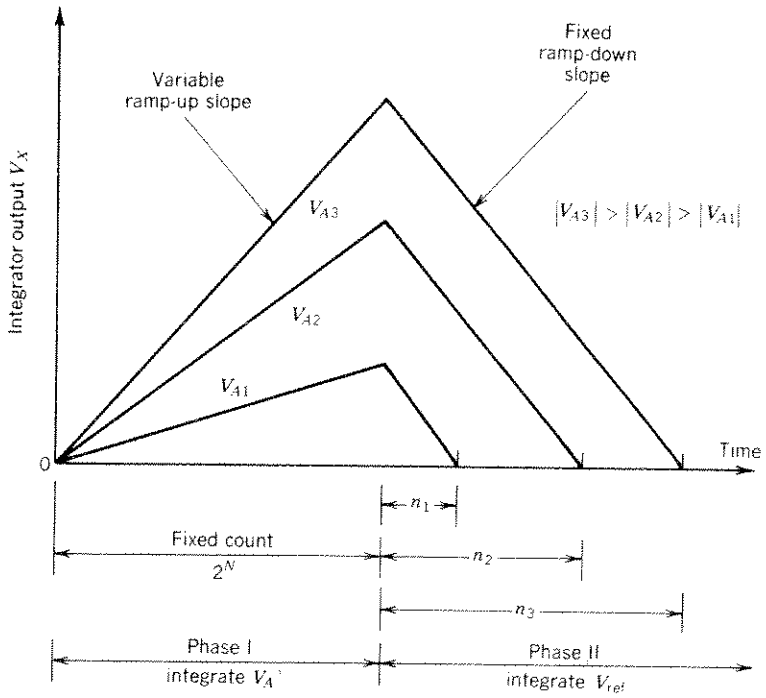


**FIGURE 15.11.** Integrator output waveforms in dual-slope A/D converter.

3. The power-line noise rejection characteristics are excellent. One of the limitations to high resolution in line-operated instruments is the presence of noise at the power-line frequency or its integer multiples. This noise normally appears superimposed on the input signal, and has zero average value. During the conversion process, the input signal is integrated for a fixed period of time (i.e., for the duration of phase I of Fig. 15.11). If this period is made equal to the period of the power-line signal (i.e., 16.67 msec for 60-Hz line) or its integer multiples, then the power-line noise is greatly attenuated during the integration process. In practical designs, power-line noise can be attenuated by as much as 70 dB using this technique.[7]

Because of the advantages listed above, the dual-slope conversion technique has become one of the most commonly used high-resolution A/D conversion methods for low-speed converter applications. Using auto-zero techniques (see Figs. 7.46 and 7.47) to reduce operational amplifier and comparator offsets to well below 1 mV, it is possible to build monolithic A/D converters in the 12- to 14-bit resolution and linearity range. At present, a number of monolithic A/D converter products are available which use the dual-slope technique or its derivatives[7,8] which are fabricated with CMOS technology.

## Charge-Balancing Converters

Although the charge-balancing A/D converter belongs to the family of integrating converters, its basic principle of operation is quite different from that of single- or dual-slope-type converters. It operates on the principle of balancing or "canceling" a charge applied to the input terminal of an integrator by generating an equal amount of charge of opposite polarity which is supplied in discrete *quantum* packets.

The principle of operation of a charge-balancing A/D converter is conceptually very similar to the case of the voltage-to-frequency (V/F) converter configurations discussed in Chapter 11 (see Fig. 11.55). First, an analog signal is converted to a periodic pulse train whose pulse-width is fixed and whose repetition rate is proportional to the analog signal. Next, the number of such pulses per unit of time interval are counted by a binary counter to form a digital output.

Figure 15.12 shows the conceptual block diagram of a charge-balancing A/D converter. Prior to the start of the conversion cycle, the switch $S_2$ is closed, and $S_1$ is switched to ground. During the conversion cycle, $S_2$ is opened, and the integrator starts generating a negative-going ramp whose slope is proportional to the input current, $I_1(=V_A/R_1)$. When the negative ramp at the integrator output (node $B$) causes the comparator to change state, the switch $S_1$ is activated for a time duration of $t_1$ corresponding to one-half clock cycle, and an amount of charge $Q_0$ is extracted from the integrator summing node (node $A$), where

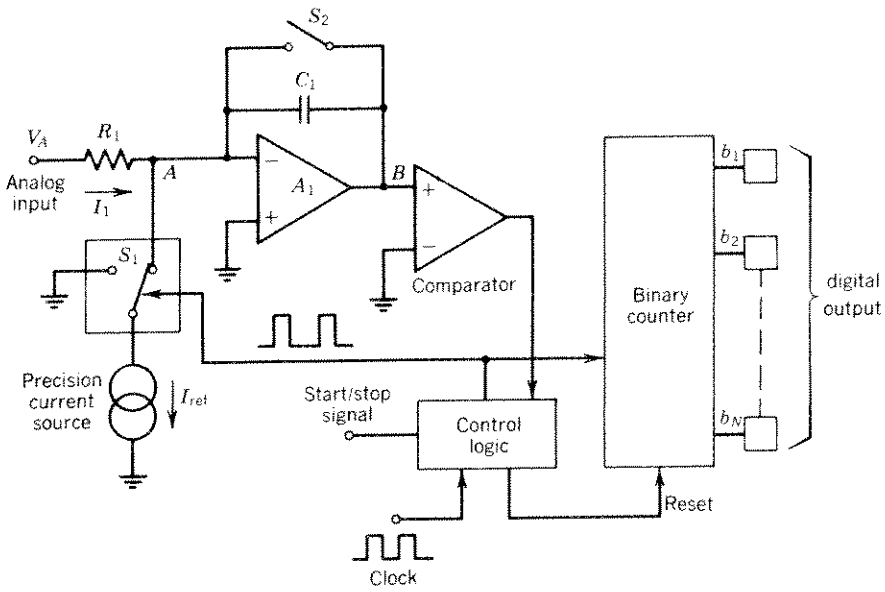


**FIGURE 15.12.** Block diagram of charge-balancing A/D converter.

$$Q_0 = I_{\text{ref}} t_1 \tag{15.15}$$

This charge packet momentarily subtracts from the analog input current $I_1$ and causes the integrator output to ramp up again. In this manner, the integrator output is constantly forced down with a steady input current $I_1$, and is intermittently forced up with the internal current $I_{\text{ref}}$ applied for discrete intervals of duration $t_1$. At the equilibrium condition, the net charge accumulated at node $A$ is identically equal to zero. Over a conversion period of $N_t$ clock cycles, the total charge $Q_{\text{in}}$ supplied by the current $I_1$ is

$$Q_{\text{in}} = I_1 N_t 2t_1 = \frac{V_A}{R_1} 2N_t t_1 \tag{15.16}$$

During the same time interval, a charge $Q_{\text{out}}$ is extracted from the same node by $n$ pulses of the intermittent current source $I_{\text{ref}}$, where

$$Q_{\text{out}} = nQ_0 = I_{\text{ref}} nt_1 \tag{15.17}$$

Equating the net input charge to the outgoing charge, from Eqs. (15.16) and (15.17), one obtains

$$n = \frac{V_A}{R_1 I_{\text{ref}}} 2N_t \tag{15.18}$$

Setting $I_{\text{ref}} R_1$ equal to $V_{\text{FS}}/2$, and choosing the total number of clock pulses $N_t$ available during the conversion step equal to $2^N$ for $N$-bit resolution, one can rewrite Eq. (15.18) as

$$n = \frac{2^N}{V_{\text{FS}}} V_A \tag{15.19}$$

which is of the same form as Eq. (15.11). Then, accumulating the total count $n$ of the clock cycles which activate the switch $S_1$ in the binary counter, one obtains the digital equivalent of the analog input. Note that each unit packet of charge $Q_0$, delivered from the reference current source, corresponds to 1 LSB increment of the digital output.

To control the accuracy of the charge packet $Q_0$, symmetrical clock pulses with 50% duty cycle are required. In practice, this is achieved by dividing down the clock frequency by an $R$–$S$ flip-flop.

Figure 15.13 illustrates a practical method of implementing the switching current reference of Figure 15.12, using a voltage follower and resistor $R_2$, which is switched between $-V_{\text{ref}}$ and ground. Equating the incoming and outgoing charge at the integrator input node, under equilibrium conditions, the number of charge packets $n$ can be expressed as

$$n = \frac{2R_2}{R_1} \frac{2^N}{V_{\text{ref}}} V_A \tag{15.20}$$

Setting the full-scale output $V_{\text{FS}}$ to be equal to

$$V_{\text{FS}} = V_{\text{ref}} \frac{R_1}{2R_2} \tag{15.21}$$

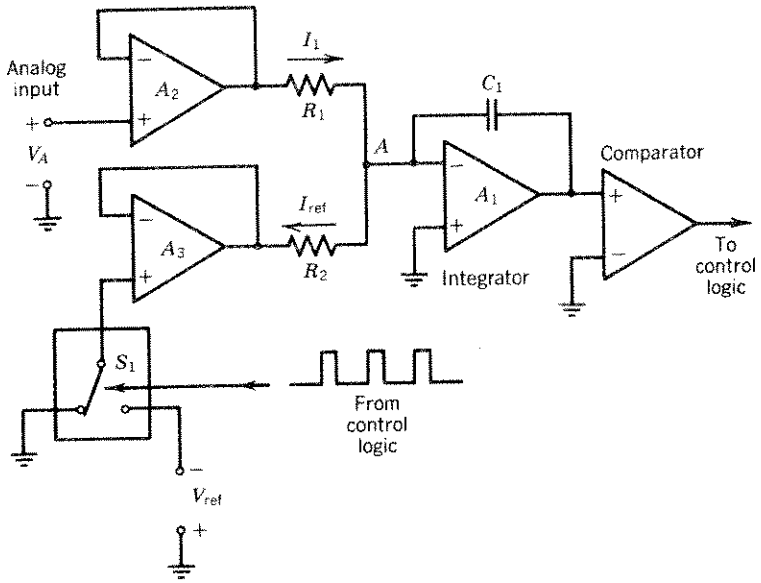


**FIGURE 15.13.** Method of implementing the switching current reference of Figure 15.12.

Eq. (15.20) becomes the same as Eq. (15.19). Note that since $R_1$ and $R_2$ appear as a ratio in the transfer function, only their matching and tracking is critical.

The basic circuit configuration of Figure 15.13 is particularly suited to circuit design with CMOS technology, using internal offset correction (i.e., auto-zero techniques) to eliminate operational amplifier and comparator offsets.[9]

The charge-balancing A/D conversion technique has some of the advantages of the dual-slope conversion. The dependence on absolute values of $R$ and $C$ is avoided, and due to a fixed-interval integration process, the effects of periodic power-line noise can be significantly reduced. However, the charge-balance conversion technique is inherently slower and requires careful control of clock signal symmetry. Therefore, it does not lend itself to the same degree of precision as the dual-slope technique.

### Error Sources in Integrating A/D Converters

Major error sources in integrating A/D converters are the offset voltages associated with the detection and integration circuitry, nonlinearity of the integrator output, and comparator response time. In addition to these inherent errors, other error sources, such as the stability and accuracy of the voltage reference and the external $R$ and $C$ components for the integrator section also affect the accuracy of conversion.

The effect of the reference voltage inaccuracy is an additive error term, present in every A/D and D/A converter. The effect of external $R$ and $C$ values on circuit accuracy can be greatly reduced by using self-compensating tech-

niques, such as the dual-slope conversion. In this discussion, we will briefly examine the effects and magnitudes of the remaining error sources, which are inherent to the integrating-type A/D converter operation.

**Offset Errors.** The offset voltages of operational amplifier and comparator circuits would appear superimposed on the analog signal input, and thus cause errors in the detected or integrated voltage levels. In MOS designs where offset voltage levels are in the range of ±10–±30 mV, these errors would correspond to approximately 0.3% of $V_{FS}$ for a 10-V full-scale signal. This would correspond to greater than $\pm\frac{1}{2}$ LSB error for 8-bit or higher resolution levels. Fortunately, in MOS technology where sampling switches and high-impedance levels are available, one can use self-correcting sample-and-hold techniques (i.e., so-called auto-zero methods) to reduce the apparent level of these offsets to approximately 1 mV (see Figs. 7.46 and 7.47). Thus, using auto-zero techniques, offset errors can be maintained to within ±0.01% of $V_{FS}$, which is suitable for 12- to 14-bit resolution.

**Integrator Linearity Error.** The nonlinearity in the integrator output is primarily due to the finite open-loop gain $A_o$ of the integrating operational amplifier. The error voltage $\Delta V_I$ between the ideal and the actual integrator outputs can be approximated as[10]

$$\Delta V_I = (V_{out})_{ideal} - (V_{out})_{actual} \approx V_{FS}\frac{t_I}{2A_oR_1C_1} \tag{15.22}$$

where $t_I$ is the total integration time, and $R_1$ and $C_1$ are the integrator time constants. Normally, $(R_1C_1)$ product is set equal to $t_I$, resulting in

$$\Delta V_I = \frac{V_{FS}}{2A_o} \tag{15.23}$$

To keep the linearity error under $\pm\frac{1}{2}$ LSB in a 12-bit integrating converter, a ramp nonlinearity of less than 0.01% of $V_{FS}$ is required. Equation (15.23) implies that under such circumstances, the minimum operational amplifier gain $A_o$ must be in excess of 5000 (i.e., ≈74 dB).

**Comparator Response Time Errors.** The comparator section must have enough gain to switch fully with an input level of 1 LSB. For a 12-bit converter with $V_{FS}$ = 10 V, this implies that the comparator must fully switch with ±2.5 mV input differential, and that such switching must be accomplished within one clock cycle. Any finite delay $t_d$ in comparator switching causes a resolution error $\epsilon_d$ in units of LSB,

$$\epsilon_d = \frac{t_d}{T_{ck}} \quad \text{LSB} \tag{15.24}$$

where $T_{ck}$ is the period of the clock frequency. Typical CMOS comparator stages have response times of approximately 0.5–1 μsec, with 2.5-mV input drive.

Thus, from Eq. (15.24), to maintain 12-bit resolution, the maximum allowable clock rate must be limited to under 1 MHz.

### Characteristics and Applications

From the previous discussions, the basic characteristics of integrating A/D converters can be summarized as follows:

1. *Low Conversion Rate.* A total of $2^N$ clock cycles would be required for a full-scale conversion. For a 10-bit converter operating with 1-MHz clock frequency, this would result in a conversion time of approximately 1 msec, or a rate of about 1000 conversions per second.
2. *No Missing Codes.* Since all clock cycles are accumulated in the counter during the conversion process, all digital codes between zero and full scale will be present at the output.
3. *High Linearity.* Linearity is primarily determined by the linearity of the ramp signal. By proper design, the ramp nonlinearity error can be reduced to less than 0.01%.
4. *High Resolution.* Within the limits of ramp linearity and comparator-sensing capability, the resolution can be increased by increasing the total clock cycles $N_T$. Since the maximum clock frequency is fixed by the comparator response time and the control logic capability, the only way to increase $N_T$ is by increasing the ramp time, which decreases the conversion rate. Thus, in general, the conversion rate varies inversely with the resolution.
5. *Noise Rejection.* Integrating converters have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integral multiple of the conversion rate. For example, 60- and 120-Hz power-line noise can be greatly attenuated by choosing the conversion rate to be 30 and 60 conversions per second, respectively.

Because of these characteristics, integrating A/D converters are primarily suited for high-accuracy and low-speed measurements of slowly varying signals. Their prime areas of application are in digital panel meters and multimeters, as well as in remote-area data-acquisition and monitoring systems. In digital panel-meter applications, the counter outputs are normally brought out in binary-coded decimal (BCD) format, rather than as a simple binary code, so that they can directly interface with numerical displays.

The circuit configuration of integrating A/D converters is best suited to the fabrication with CMOS process technology. This is because the high-impedance nature of CMOS devices and the availability of analog switches greatly simplify the system architecture and permit on-chip offset correction and sample-and-hold capability. The design of digital control logic and the counter circuitry is also simplified by using CMOS technology, due to the high functional density

of MOS devices on the IC chip. An important added benefit of the use of CMOS technology is the significant reduction in power dissipation. As a result, almost all of the commercially available integrating-type A/D converters are fabricated with CMOS technology.

## 15.3. DIGITAL-RAMP-TYPE A/D CONVERTERS

Digital-ramp-type A/D converters operate by using a combination of a binary counter and a D/A converter in a feedback loop around a voltage comparator. The binary counter and D/A converter combination is used to generate a digital ramp or staircase output, which is compared to the level of the analog input signal. There are two main classes of digital-ramp-type converters: (1) tracking or servo type converters; and (2) staircase converters. The principles of operation of both converter types are very similar; they only differ in circuit complexity.

### Tracking Converter

Figure 15.14 shows the functional block diagram of a tracking or servo type A/D converter. It operates with a clock signal which is counted by the binary up-down counter. Whether the counter is counting up or down is set by the polarity of the control input from the voltage comparator. The binary outputs of the counter drive a D/A converter whose analog output $V_O$ is connected to one of the comparator inputs. At the start of the initial conversion cycle, the system counts

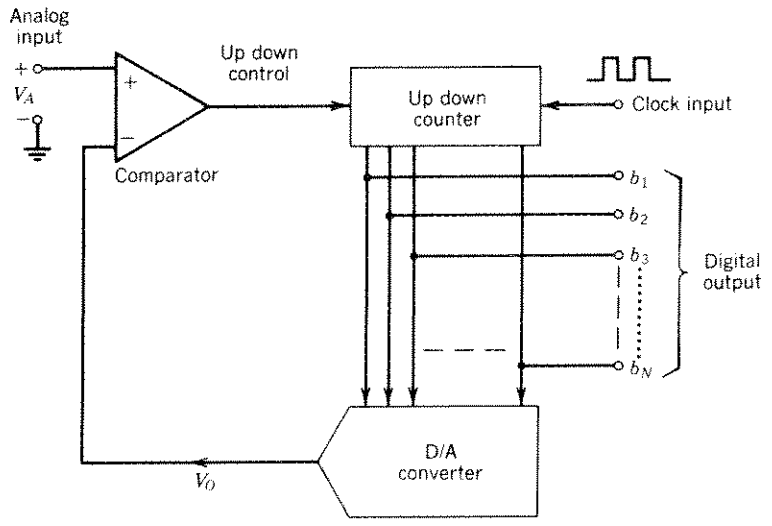


**FIGURE 15.14.** Functional block diagram of tracking A/D converter.

the clock pulses. At the output of the D/A converter, the binary count is converted to a staircase output, corresponding to the uniformly increasing sequence of binary codes. This analog level $V_O$ is continuously compared with the analog input level. When it reaches the analog input level $V_A$, the comparator changes state and stops the count. The counter output code necessary to set $V_O = V_A$ is the digital word corresponding to the analog input $V_A$. When the next cycle of A/D conversion is initiated, the counter does not start from zero. Instead, it retains the previous count and starts incrementing or decrementing the count, based on the polarity of the error signal from the comparator. The conversion is again completed when $V_O$ reaches $V_A$ and causes the comparator to change state.

For full-scale digital output this type of converter is quite slow, since $2^N - 1$ clock cycles need to be counted. However, it has a very rapid small-signal response. For example, if the input varies only a small amount, the output can follow it within a few clock cycles. The term *tracking* or *servo* type converter stems from this property. Note that in Figure 15.14, the reference voltage $V_{ref}$ is not shown separately, but is assumed to be an integral part of the D/A converter.

### Staircase Converter

This is a simplified version of the tracking converter. Instead of an up–down counter, a simple one-directional binary counter is used. In each conversion step, the counter is reset to zero and starts counting the clock pulses. This creates a staircase output from the D/A converter. The count is stopped when the D/A converter output equals the analog input, and the last count present in the counter corresponds to the digital word for the analog input. Unlike the tracking converter, the staircase-type A/D converter resets itself to zero after every conversion step. Thus, it does not have the rapid small-signal response properties of a tracking converter. However, since only unidirectional count is used, the counter circuitry is somewhat simplified.

## 15.4. SUCCESSIVE-APPROXIMATION A/D CONVERTERS

The successive-approximation converter is a feedback system which operates on a trial-and-error technique to approximate an analog input with a corresponding digital code. The system is comprised of a so-called successive-approximation register (SAR) and a D/A converter in feedback around a voltage comparator, as shown in the functional block diagram of Figure 15.15. With reference to the block diagram, the operation of the circuit can be described as follows. Prior to the start of the conversion process, the $N$-bit shift register and the holding register which form the successive-approximation register section are cleared. In the first step of conversion, a 1 is inserted as a trial bit for the MSB in the holding register, with the rest of the bits remaining at 0. If the resulting analog output