Design of MOS Amplifiers Using gm/ID Methodology

Ashutosh Tiwari

Outline

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- Why gm/Id Methodology
- Performance Metrics
- Generation Of Performance Curves
- Implementation And Design examples

Introduction

- Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive (Vov) as the key parameter
- Micropower design techniques, on the other hand, exploit weak inversion models.
- This methodology is based on a unified synthesis methodology in all the regions of operation of MOS transistor.

Introduction

- The method exploits the transconductance over dc drain current ratio (gm/Id) relationship versus the normalized current [Id/(W/L)].

Why gm/Id Methodology

Consider a simple common source amplifier, the power and bandwidth are given by following equations:

$$\boxed{P = \frac{1}{2}\frac{V_{DD}}{R_L} \cdot A_{DC} \cdot V_{OV}}$$

$$\boxed{\omega_{-3dB} = \frac{3}{2}\frac{R_L}{R_i} \cdot \frac{1}{A_{DC}} \cdot \frac{\mu}{L^2} \cdot V_{OV}}$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox} V_{OV}}$$

With gm and L fixed, smaller Vov translates into a bigger (wider) device, and thus larger Cgs. So we conclude from this that the Vov is not a good design parameter

Why gm/Id Methodology

The choice of gm/Id is based on its relevance for the three following reasons:

1. It is strongly related to the performances of analog circuits.
2. It gives an indication of device operating region.
3. It provides a tool for calculating the transistors dimensions.

How gm/Id is an indicator of the mode of operation?

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{\partial(\ln I_D)}{\partial V_G} = \frac{\partial\left\{\ln\left[\frac{I_D}{\left(\frac{W}{L}\right)}\right]\right\}}{\partial V_G}$$

This derivative is maximum in weak inversion region. The gm/Id ratio decreases as the operating point moves toward strong inversion.

What we really want from MOS transistor

– Large gm without investing much current

– Large gm without having large Cgs

To quantify how good of a job our transistor does, we can therefore define the following "figures of merit”:

Performance Metrics of Interest:

- Transit Frequency: (or Unity Gain Frequency)

$$\omega_T = \frac{g_m}{C_{gs}}$$

It is the maximum frequency beyond which MOS transistor will not act as amplifier.

- Intrinsic Gain:

$$g_m r_o$$

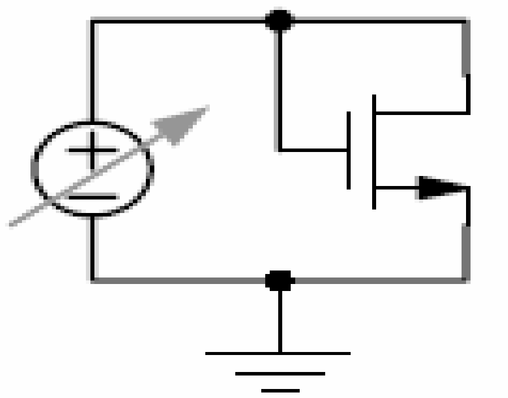
- Trans-conductor Efficiency: (Should be high)

  It is the efficiency of the MOS transistor to translate given current into an equivalent transconductance.

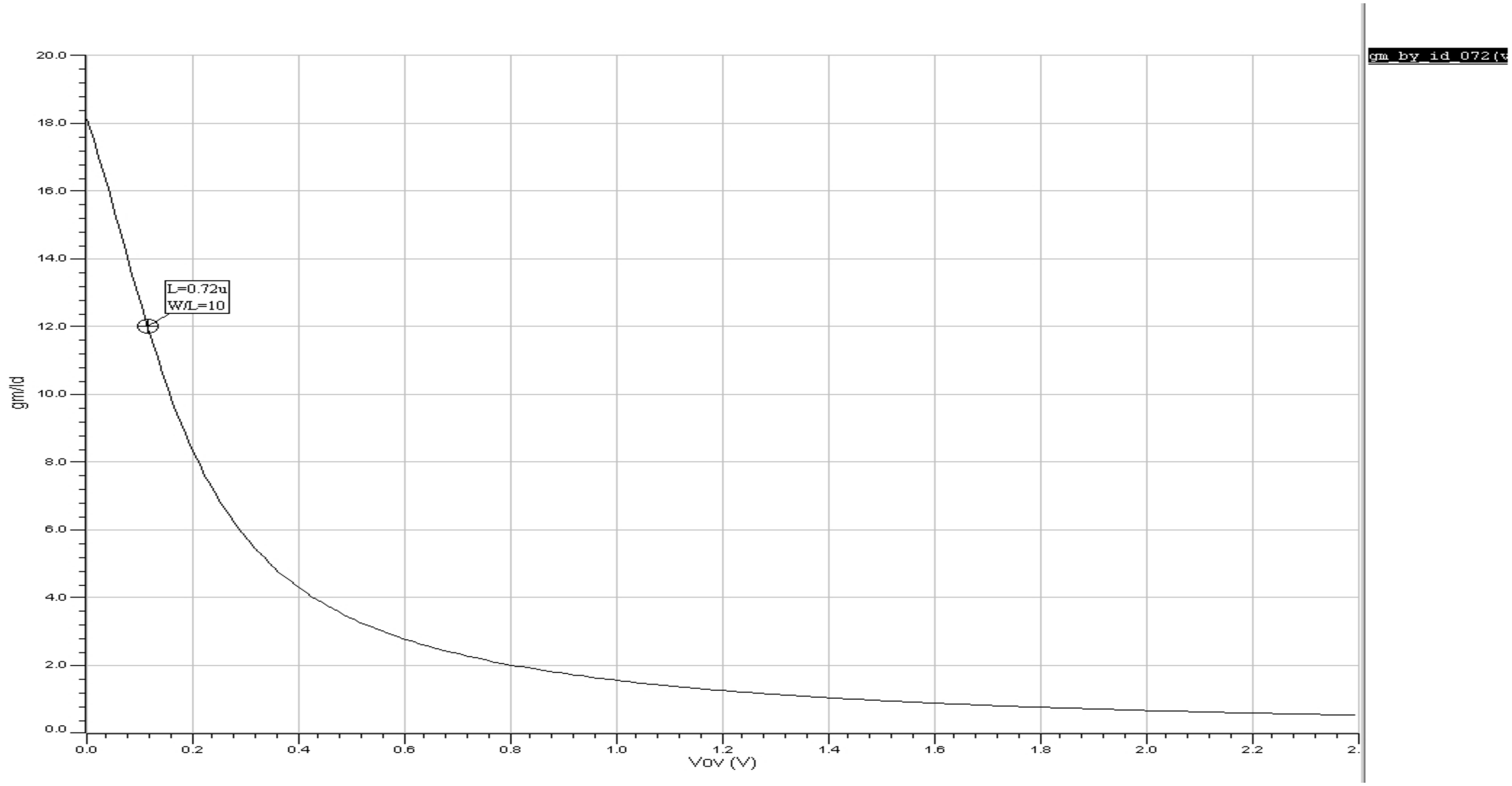
$$\frac{g_m}{I_D}$$

Generation of Performance Curves

gm/ID Simulation



gm/ID Vs Vov curve



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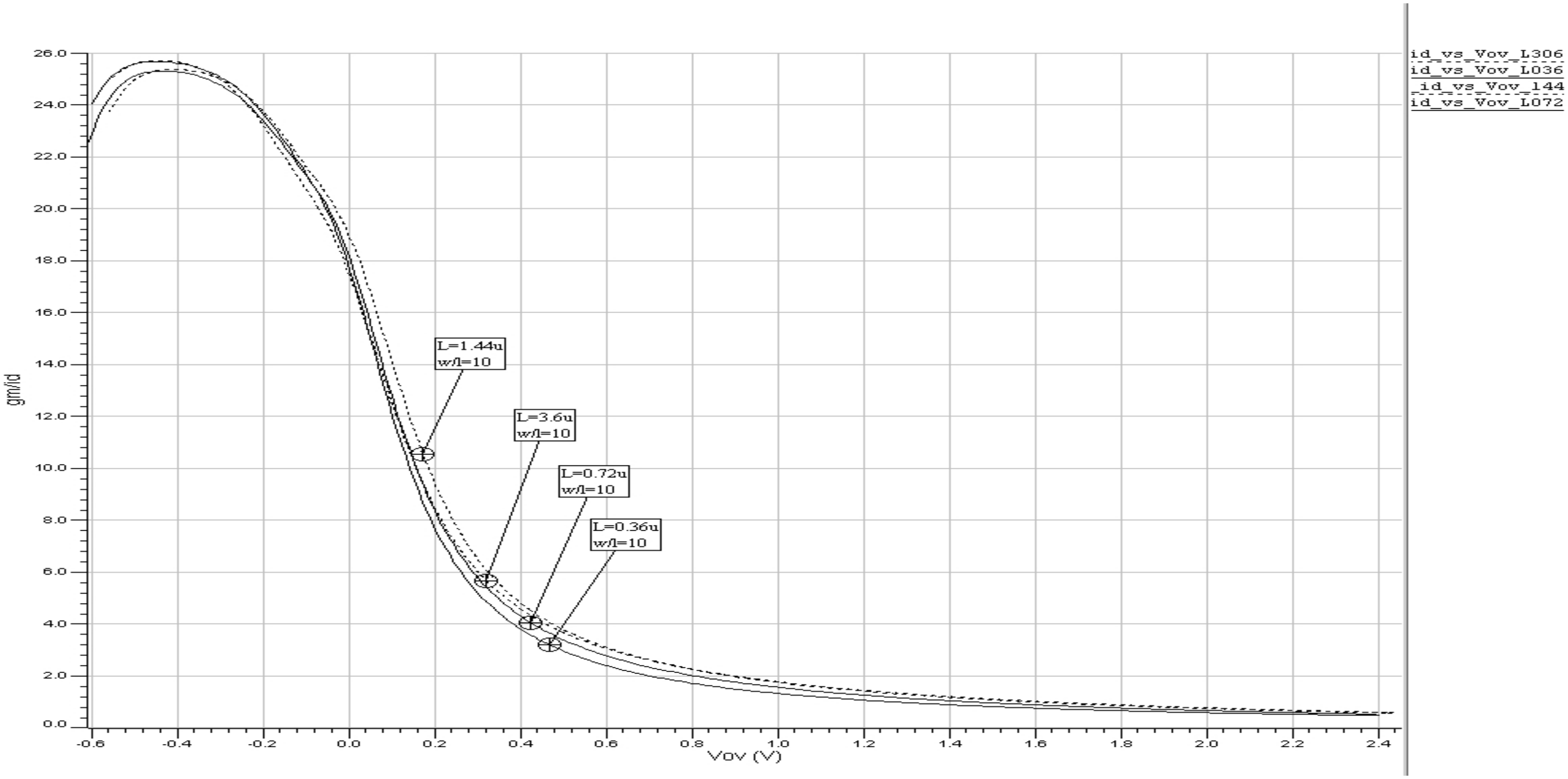

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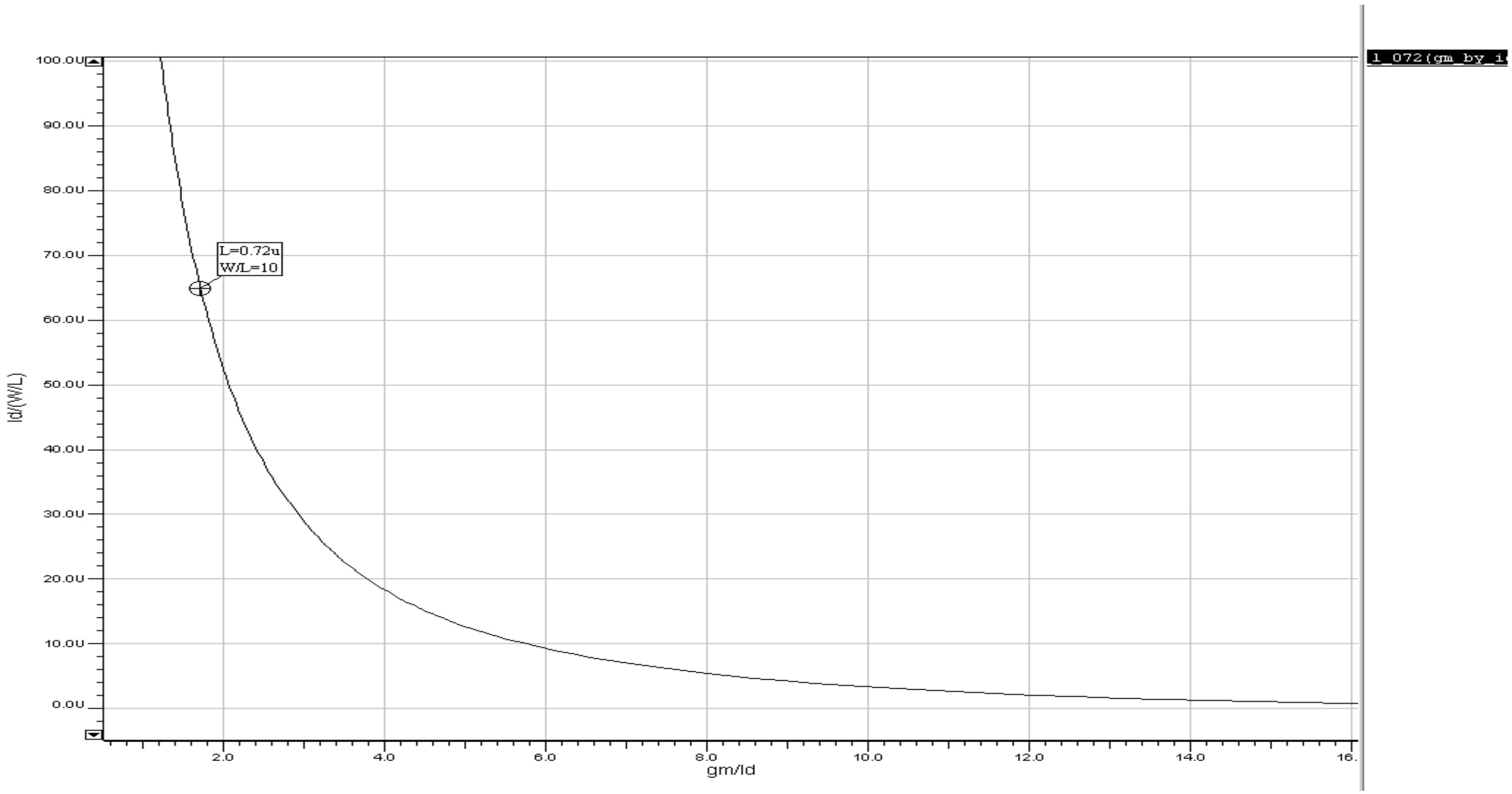
ID/(W/L) Vs gm/ID curve



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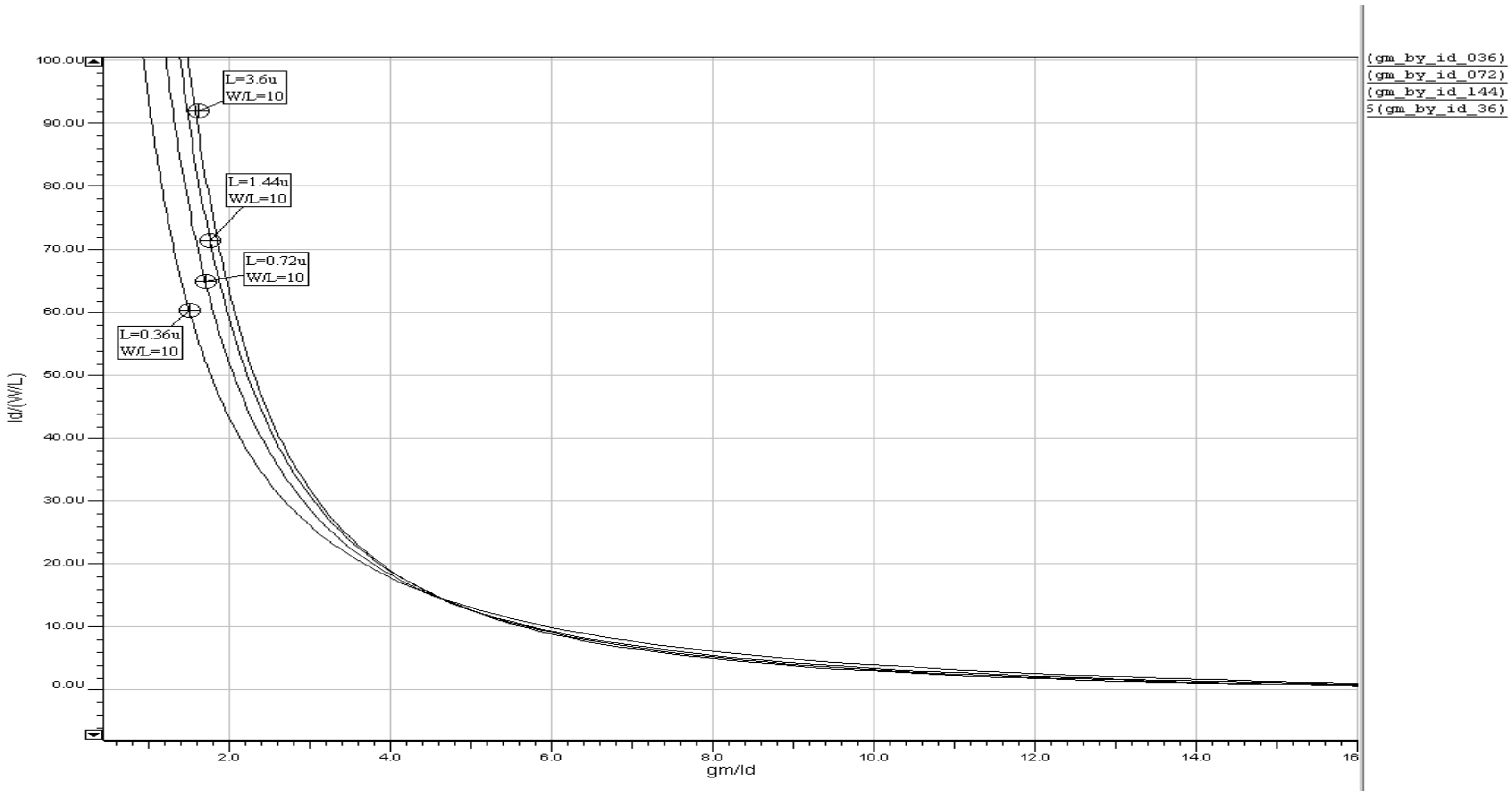
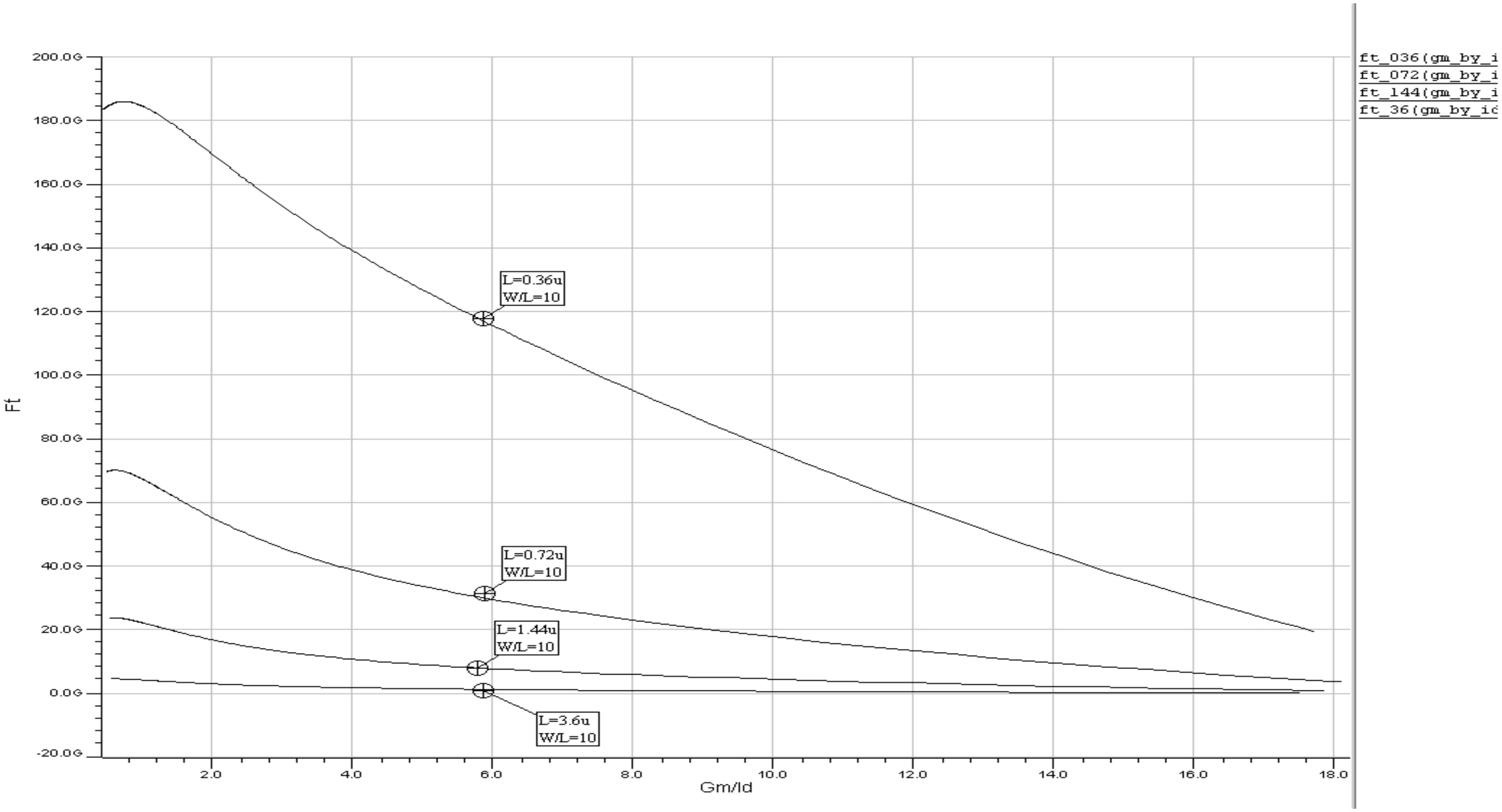

L=3.6u
W/L=10
L=1.44u
W/L=10
L=0.72u
W/L=10
L=0.36u
W/L=10
(gm_by_id_036)
(gm_by_id_072)
(gm_by_id_144)
5(gm_by_id_36)
Id/(W/L)
gm/Id
100.0U
90.0U
80.0U
70.0U
60.0U
50.0U
40.0U
30.0U
20.0U
10.0U
0.0U
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16

ft Simulation



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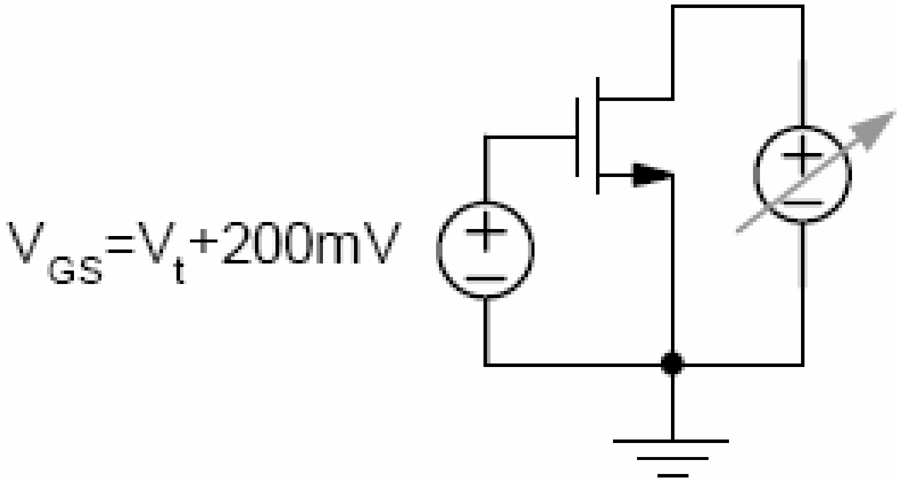
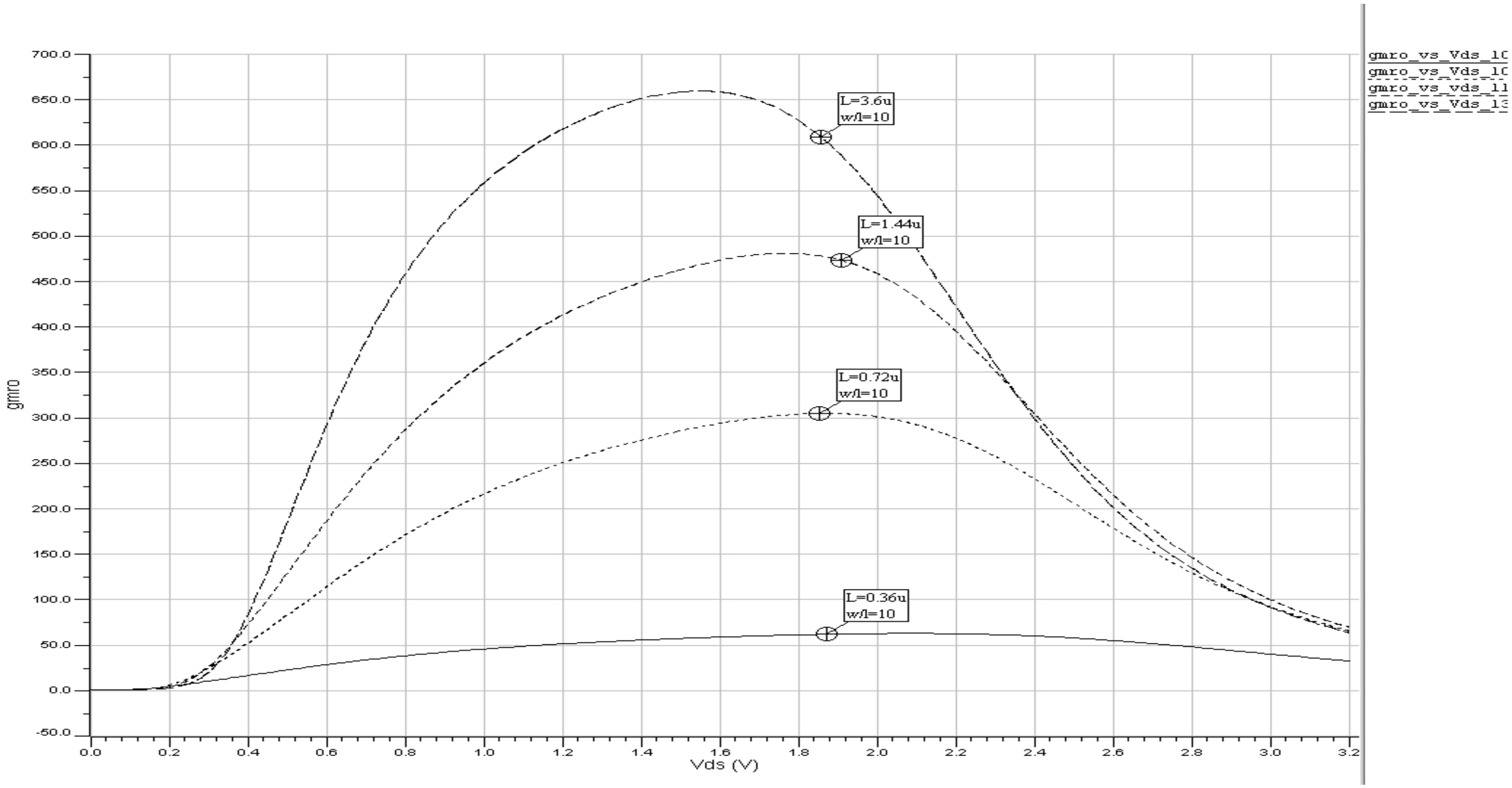
Intrinsic Gain Simulation



Gm×ro Vs Vds Curve



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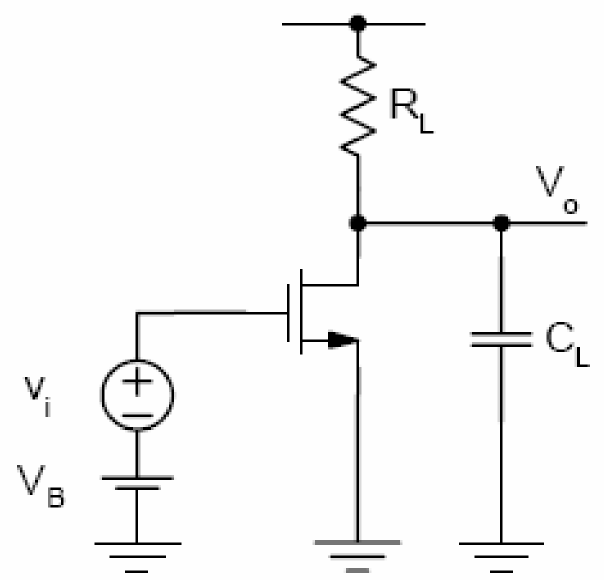
Design Example:



Given specifications

– DC gain=-2, ID ≤ 1mA, f-3dB=100MHz, CL=10pF

Solution:

– From the given specifications, we can find gm and RL as follows:

$$f_{-3dB} = \frac{1}{2\pi} \frac{1}{R_L C_L} \quad \Rightarrow \quad R_L = \frac{1}{2\pi} \frac{1}{100MHz \cdot 10pF} = 159\Omega$$

$$A_{DC} = -g_m R_L = -2 \quad \Rightarrow \quad g_m = \frac{2}{159\Omega} = 12.6mS$$

- With the maximum available current, we have 1mA

  $gm/ID = 6.3\ V^{-1}$

- From the current density chart, we can find out ID/(W/L) for the corresponding gm/ID.

  ID/(W/L) = ? 10μA

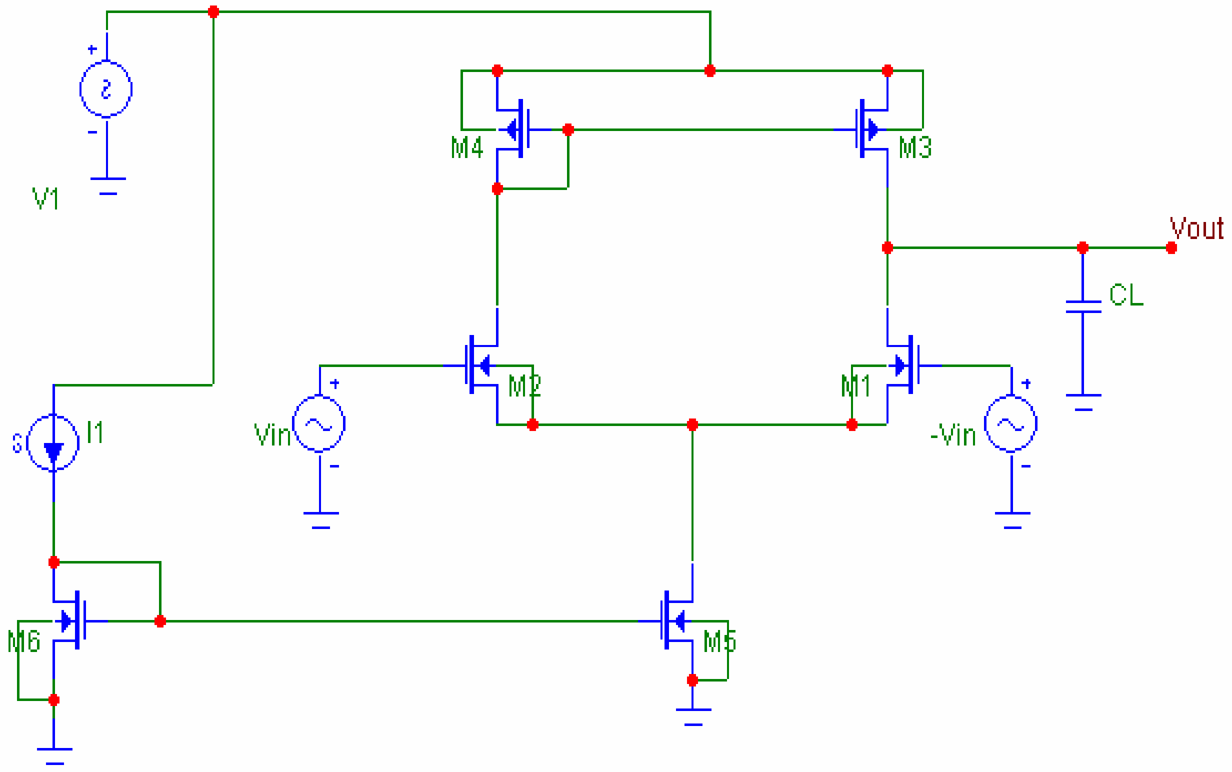
- Get Vov corresponding to gm/ID from gm/ID Vs Vov chart

  Vov $\cong$? 0.3V

  From this we get the device W as

  W=ID*L

Design Example:
Differential Amplifier (Single Ended Output)



Thank You

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References

- D. Flandre, A. Viviani, J.-P. Eggermont, P. Jespers, "Improved synthesis of regulated-cascode gain-boosting CMOS stage using symbolic analysis and gm/ID methodology", *IEEE Journal of Solid-State Circuits* (Special Issue on 22nd ESSCIRC conference), 32 (1997) 1006-1012.
- Silveira F., Flandre D., Jespers P.G.A. *A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-ion- insulator micropower OTA*. IEEE Journal of Solid State Circuits. Vol. 31, pg 1314-1319, Sept. 1996.