MOS-AK workshop
13 Dec. 2008

Sizing CMOS circuits by means of the g_m/I_D methodology and a compact model.

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sizing....

find D.C. currents and transistor sizes meeting :

- a prescribed gain-bandwidth product
- minimal power consumption
- minimal area
- large gain
- ….

low- voltage, low-power MOS circuits

Outline

Sizing...

- the Intrinsic Gain Stage (I.G.S.)

  g_m/I_D semi-empirical methodology

  g_m/I_D compact model methodology

  L-V, L-P, short channel I.G.S.

- the Miller Op. Amp.

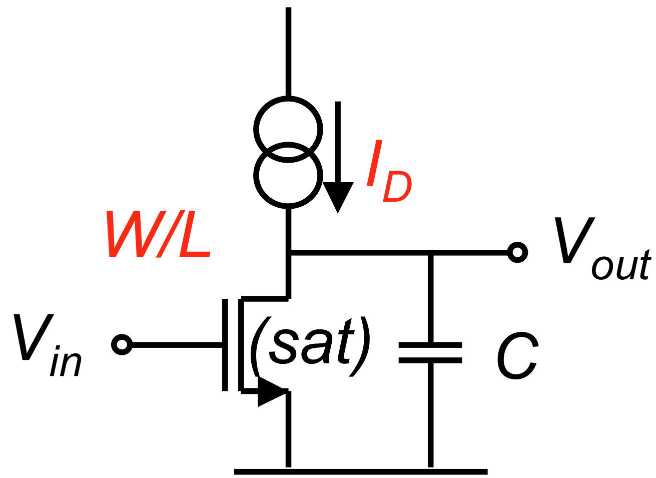
Conclusion

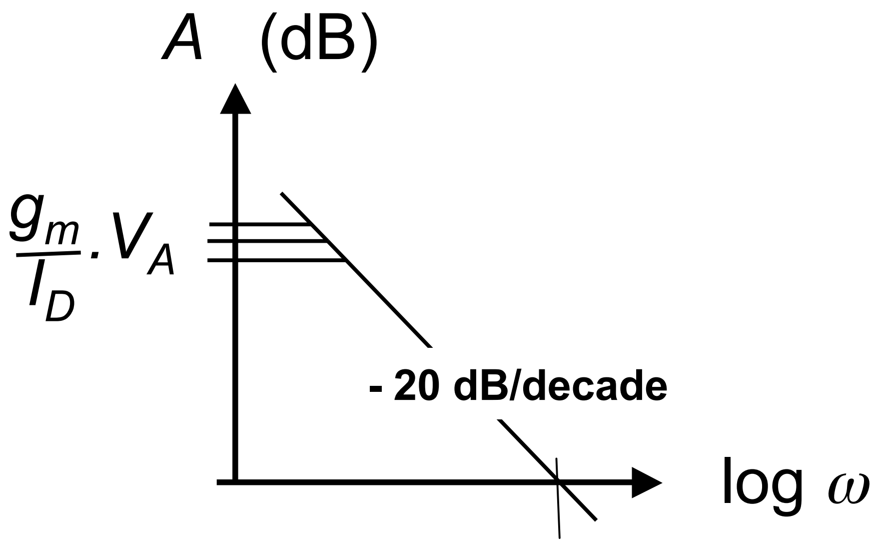
The Intrinsic Gain Stage (I.G.S.)

gain-bandwidth sizing:

find I_D and W/L
achieving ω_T

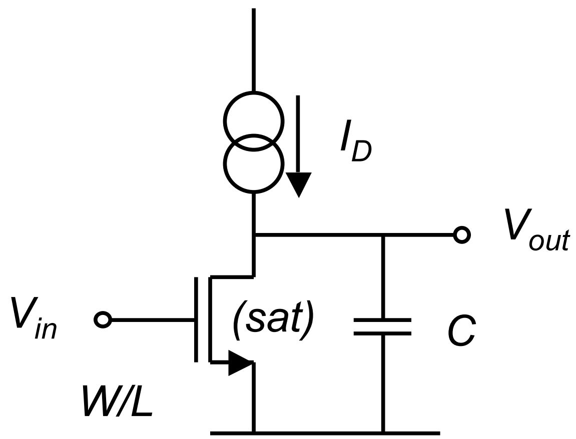
$$g_m = \omega_T . C$$





$$\omega_T = \frac{g_m}{C}$$

1) *(strong inversion)*



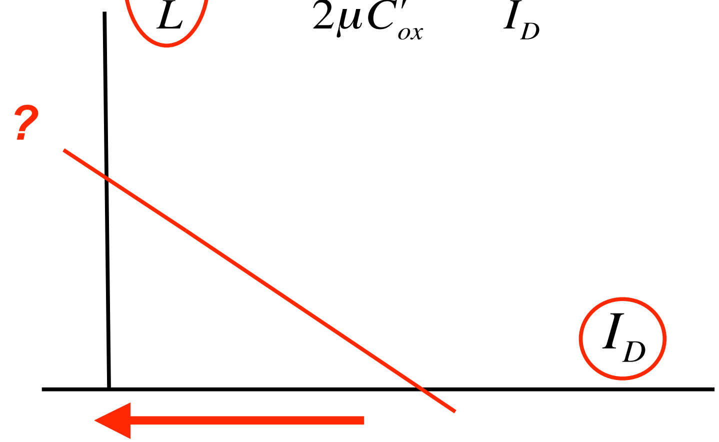
$$\beta = \mu C'_{ox}\frac{W}{L}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \sqrt{\frac{2\beta I_D}{n}}$$

$$g_m = \omega_T C$$

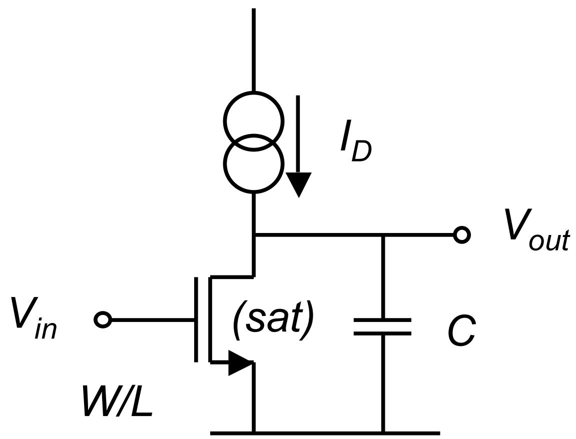
$$\frac{W}{L} = \frac{n\left(\omega_T C\right)^2}{2\mu C'_{ox}}\cdot\frac{1}{I_D}$$

$$A = \frac{g_m}{I_D}V_A = \sqrt{\frac{2\beta}{nI_D}}V_A$$



power decreases, gain increases

2) *weak inversion)*



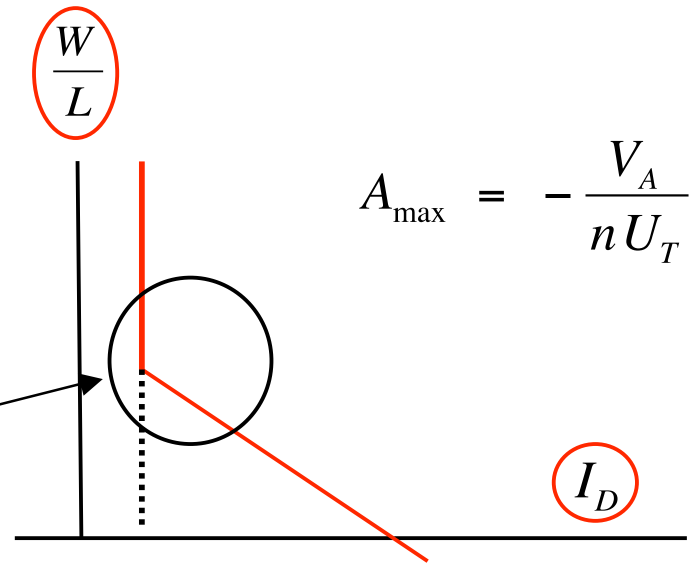
$$I_D = I_o \exp\left(\frac{V_G}{nU_T}\right)$$

$$g_m = \frac{I_D}{nU_T}$$

$$g_m = \omega_T C$$

$$A_{\max} = -\frac{V_A}{nU_T}$$

sizing in moderate inversion?



$$I_D = n\,U_T \omega_T C$$

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  - g_m/I_D compact model methodology
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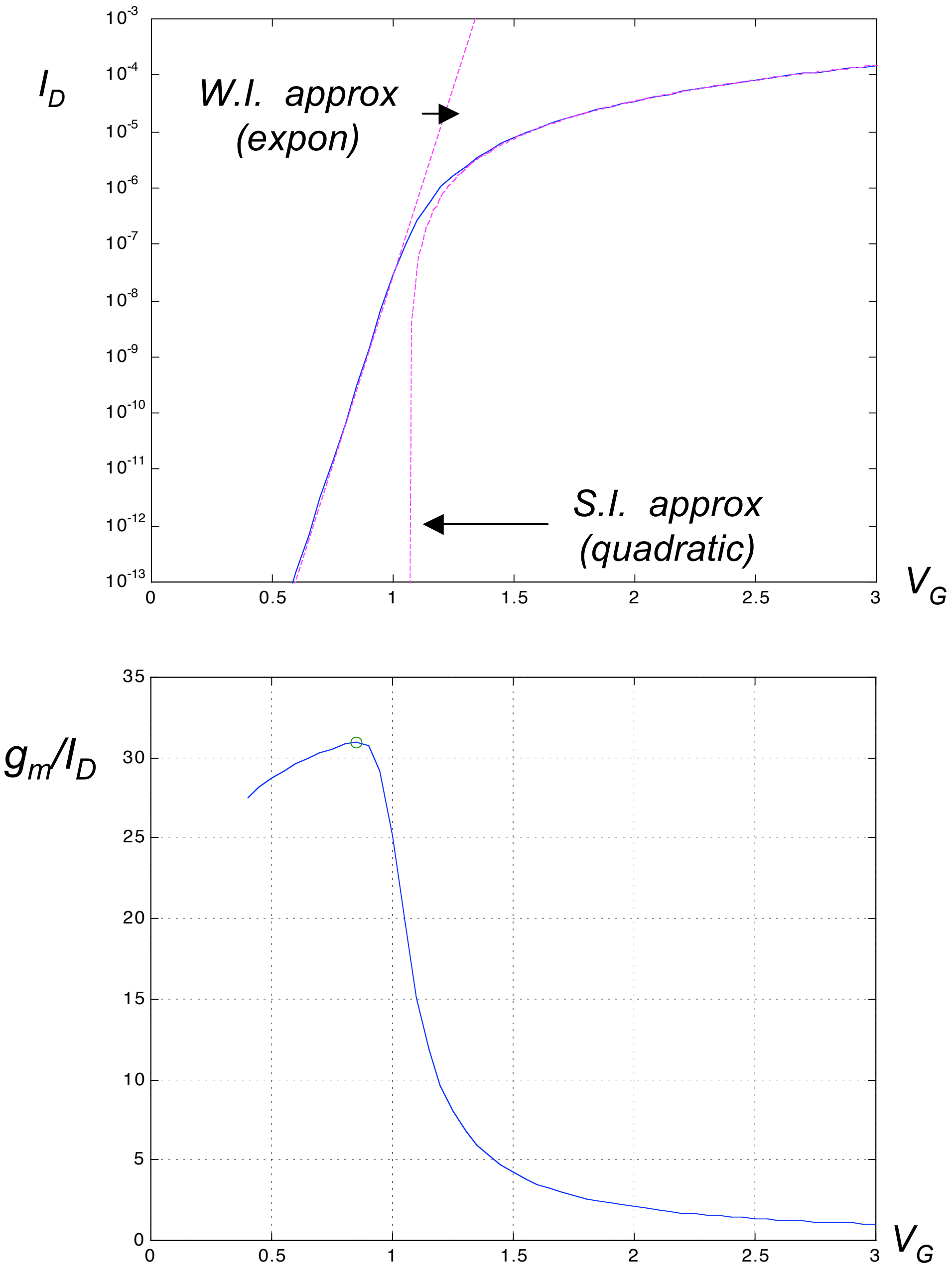
- the Miller Op. Amp.

Conclusion

what does g_m/I_D represent ?

$$\left(\frac{g_m}{I_D}\right) = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\log(I_D)$$



why g_m/I_D?

- g_m/I_D does not depend on the transistor width

  g_m and I_D are proportional to W

- g_m/I_D bridges a small signal and a large signal quantity

$$g_m \quad \Leftrightarrow \quad I_D$$

- g_m/I_D controls gain, power consumption ...

$$A = \frac{g_m}{I_D} V_A$$

The g_m/I_D sizing methodology (semi-empirical)

- **measurements**
- **reconstructed data (BSIM, PSP...)**
- **model E.K.V...**

W_{ref}

$$g_m = \omega_T C$$

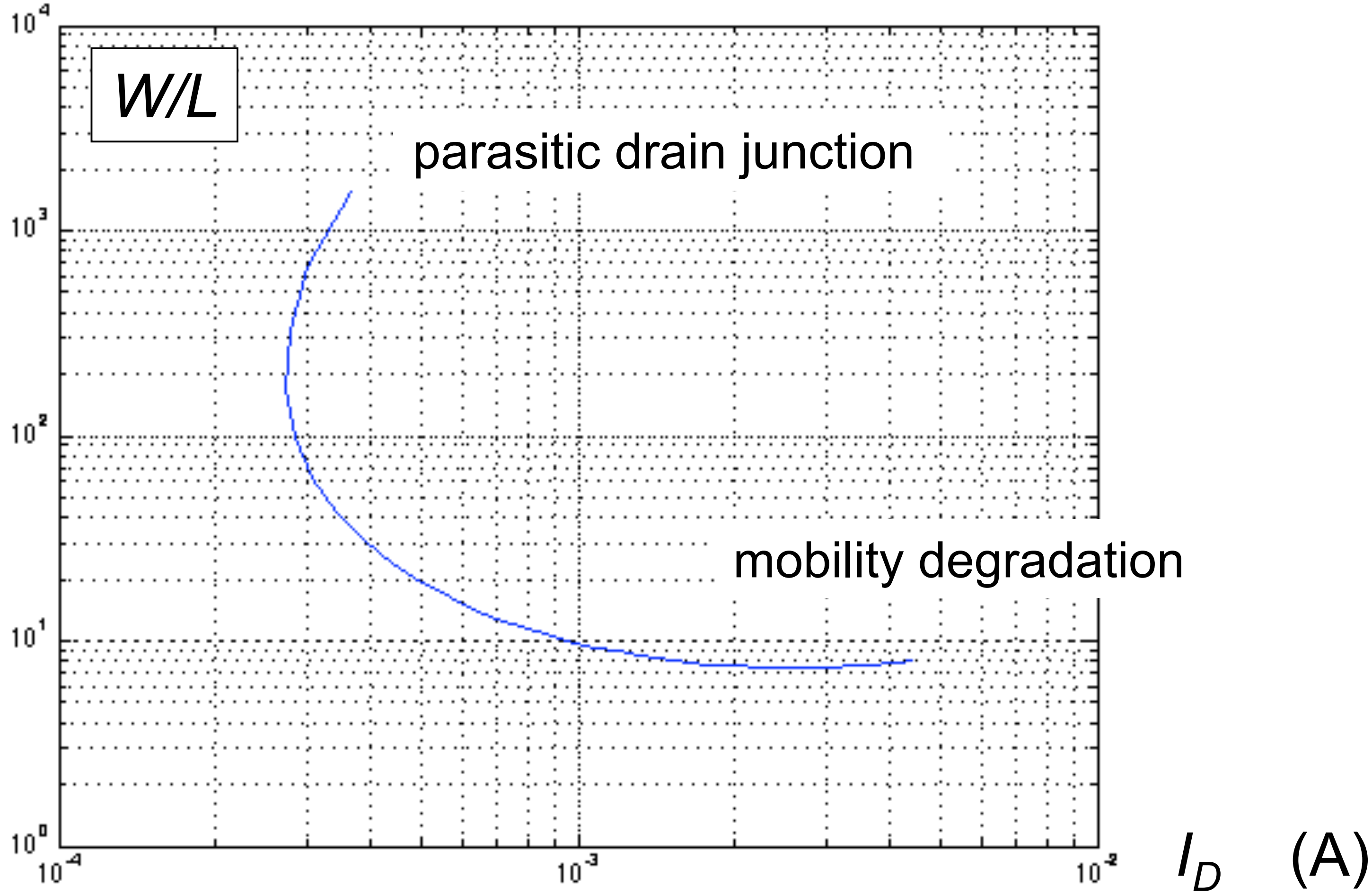
$$\frac{\partial}{\partial V_{GS}} \log\left(I_{Dref}\left(V_{GS}\right)\right)$$

monitors the mode of operation of the MOS transistor

$$I_D\left(V_{GS}\right) = \frac{g_m}{\left(\frac{g_m}{I_D}\right)}$$

$$W\left(V_{GS}\right) = \frac{I_D\left(V_{GS}\right)}{I_{D\,ref}\left(V_{GS}\right)}\left(W\right)_{ref}$$

Example



f_T = 1 GHz; C_o = 1 pf; L = 120 nm; V_S = 0; V_{DS} = 0.6 V; Wmax = 1 µm;

First paper

A g_m/I_D Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA

F. Silveira, D. Flandre, P.G.A. Jespers

IEEE JOURNAL OF SOLID STATE CIRCUITS, VOL. 31, NO. 9, SEPTEMBER 1996
p. 1314 ...

Outline

Sizing...

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Conclusion

The ACM and EKV compact models

+ *continuous model (saturation, weak to strong inversion)*
+ *few parameters:*
  - n *subthreshold slope factor*
  - I_{Su} *unary specific current*
  - V_{To} *threshold voltage*

- *uniformly doped substrate, no mobility degradation,*
- *gradual channel approximation (1D)*

A.C.M.

- An MOS transistor model for analog circuit design
  Ana I. Cunha, M.C. Schneider, C. G. Montoro.
  IEEE JSSC,vol 33,n°10,oct, 1998.

E.K.V.

- An analytical MOS transistor model valid in all regions of operation and dedicated to Low-Voltage and Low-current applications.
  Chr. C.Enz, F. Krummenacher, E. A. Vittoz.
  Analog Integrated Circuits and Signal Processing, Kluwer Ac. Publ. 1995.

The compact model (1)

drain current normalization

normalized drain current
$$i = \frac{I_D}{I_S}$$

specific current

$$\overbrace{\underbrace{2nU_T^2\mu C'_{ox}}_{I_{Su}}\frac{W}{L}}$$

EKV

$$\frac{1}{2}nU_T^2\mu C'_{ox}\frac{W}{L}$$

ACM

unary specific current ($W = L$)

The compact model (2)

norm. drain current (*saturation*)

$$i = q^2 + q$$

normalized mobile charge density

$$q = -\frac{Q_i'}{2nU_T C_{ox}'}$$

channel voltage

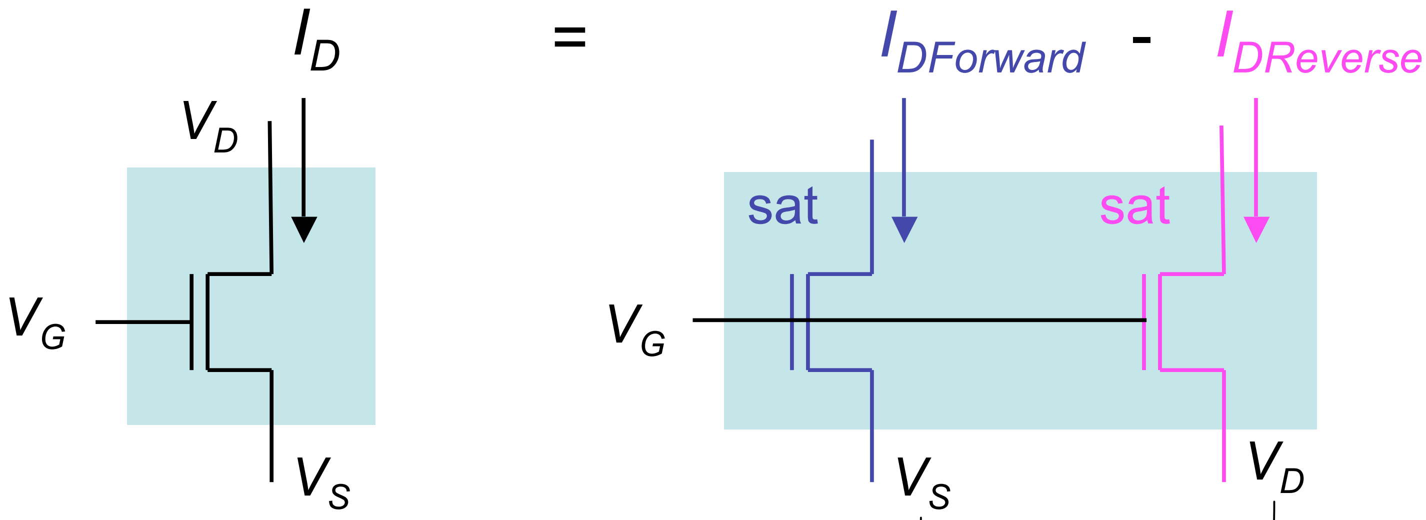
$$V_P - V = U_T\left[2(q-1) + \log(q)\right]$$

pinch - off voltage

gate voltage

$$V_P = \frac{V_G - V_{To}}{n}$$

The compact model (3)



$$V_P - V_S = U_T\left[2(q_F - 1) + \log(q_F)\right]$$

$$V_P - V_D = U_T\left[2(q_R - 1) + \log(q_R)\right]$$

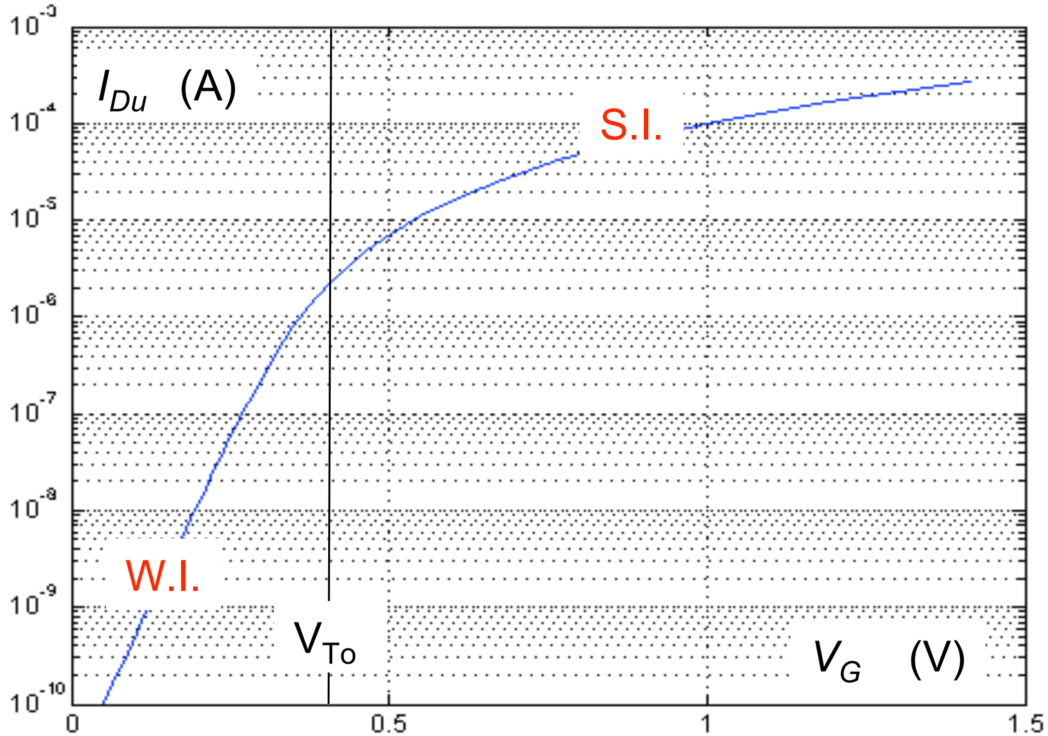
$$i = q_F^2 + q_F - \left(q_R^2 + q_R\right)$$

example : $I_{Du}(V_G)$ of grounded source ($V_S = 0$ V) saturated ($q \Rightarrow q_F$) transistor

parametric method

$$q_F \begin{cases} i = q_F^2 + q_F & \Longrightarrow \quad I_{Du} = i\,I_{Su} \\ V_P = U_T\left(2\left(q_F - 1\right) + \log q_F\right) & \Longrightarrow \quad V_G = nV_P + V_{To} \end{cases}$$

```
% data
UT  = .026;
n   = 1.2;
Isu  = 1e-6;
VTo = 0.4;

% compute
qF  = logspace(-4,1.2,50);
i   = qF.^2 + qF;
ID  = i*Isu;
VP = UT*(2*(qF-1) + log(qF));
VG = n*VP + VTo;

% plot
semilogy(VG,ID); grid
```



g_m/I_D of the saturated transistor

$$\frac{g_m}{I_D} = \frac{d\log(i)}{dV_G} \quad \begin{cases} d\log(i) = \dfrac{di}{i} = \dfrac{2q_F+1}{i}\,dq_F \\ and \\ dV_G = n\,dV_P = nU_T\left(2+\dfrac{1}{q_F}\right)dq_F = nU_T\,\dfrac{2q_F+1}{q_F}\,dq_F \end{cases}$$

$$\frac{g_m}{I_D} = \frac{1}{nU_T}\,\frac{q_F}{i} = \frac{1}{nU_T}\,\frac{1}{q_F+1}$$

sizing the Intrinsic Gain Stage by means of the E.K.V. model

E.K.V. param

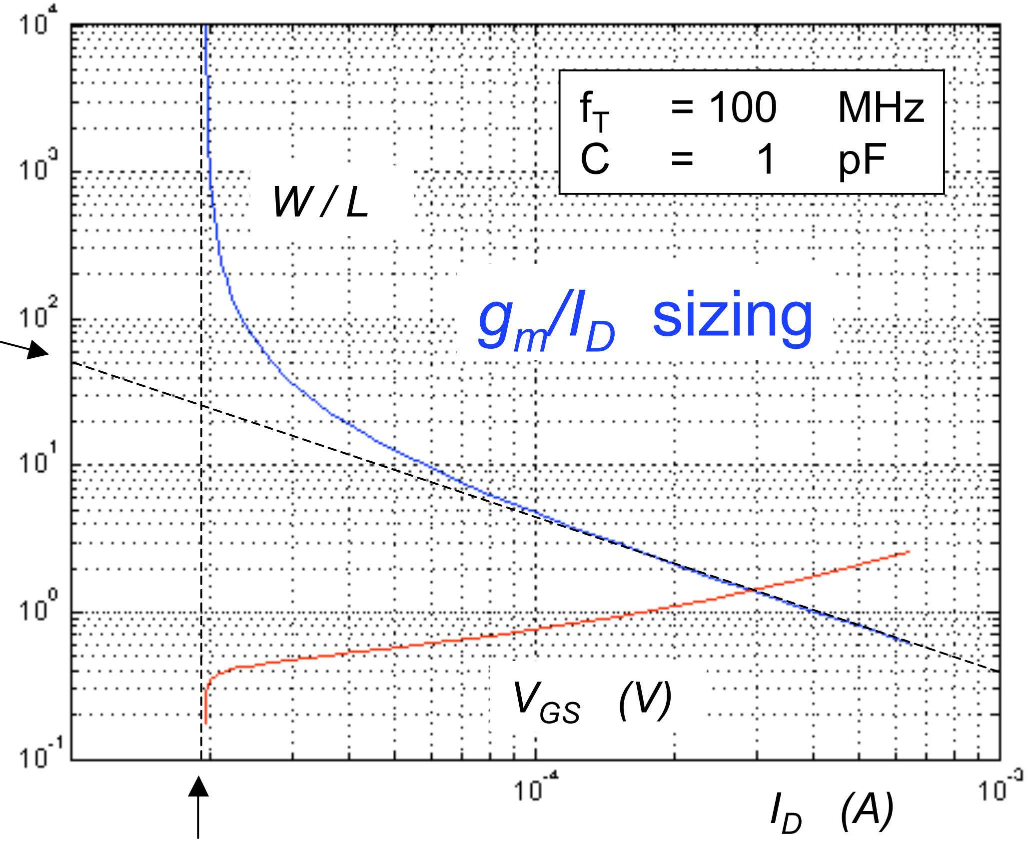
g_m/I_D sizing

```
% data
fT     = 1e8;
C      = 1e-12;
n      = 1.2;
Isu    = 1e-6;
VTo    = 0.4;

% compute
UT     = .026;
ωT     = 2*pi*fT;
gm     = ωT*C;
qF     = logspace(-4,1.5,50);
gmoverID = 1./(n*UT*(1+qF));
ID     = gm./gmoverID;
IDu    = Isu*(qF.^2 + qF);
WsL    = ID./IDu;
VP     = UT*(2*(qF+1) + log(qF));
VG     = n*VP + VTo;

% plot
loglog(ID,WsL,'b',ID,VG,'r');
```

specs

sizing the Intrinsic Gain Stage by means of the E.K.V. model

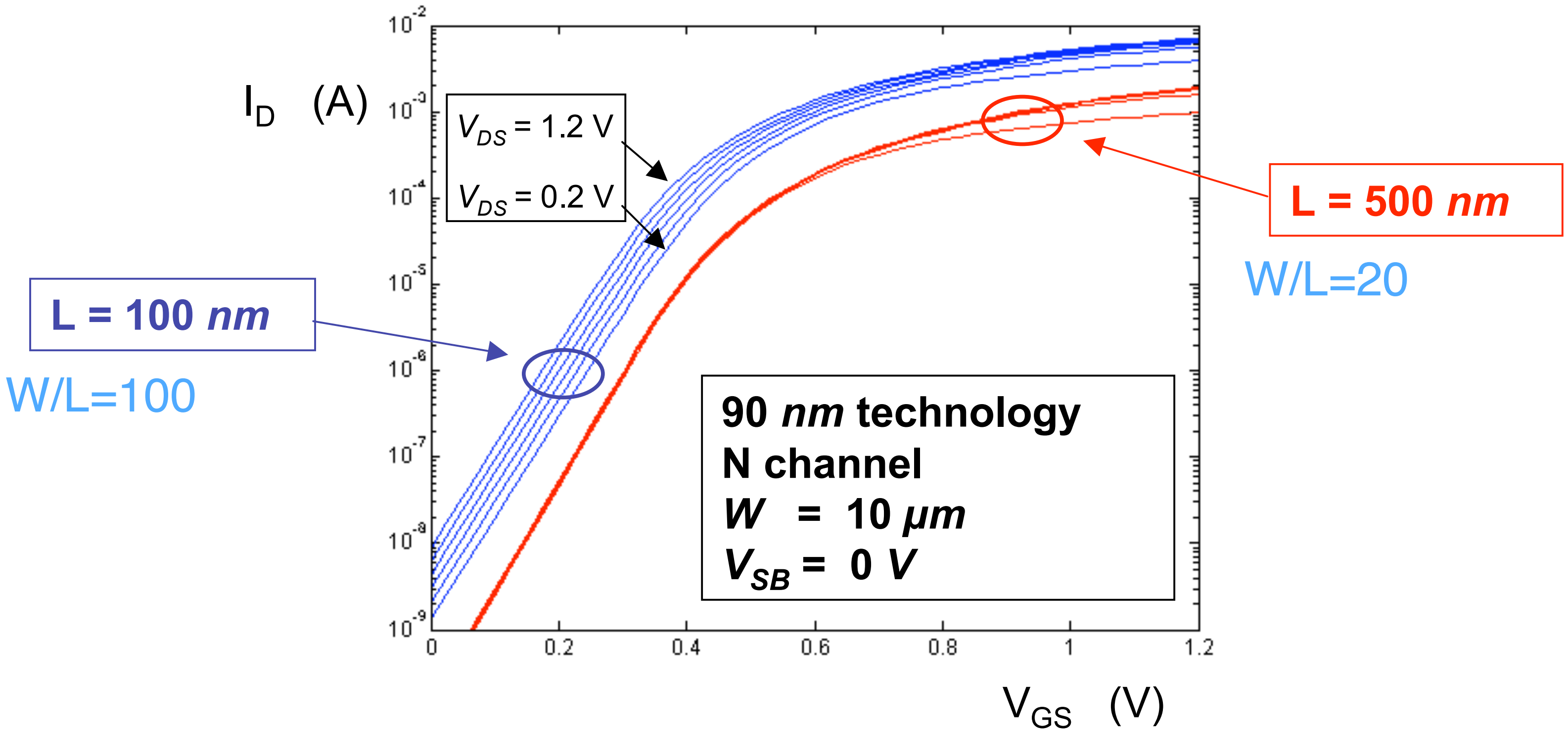
strong inversion approx.



weak inversion approx.

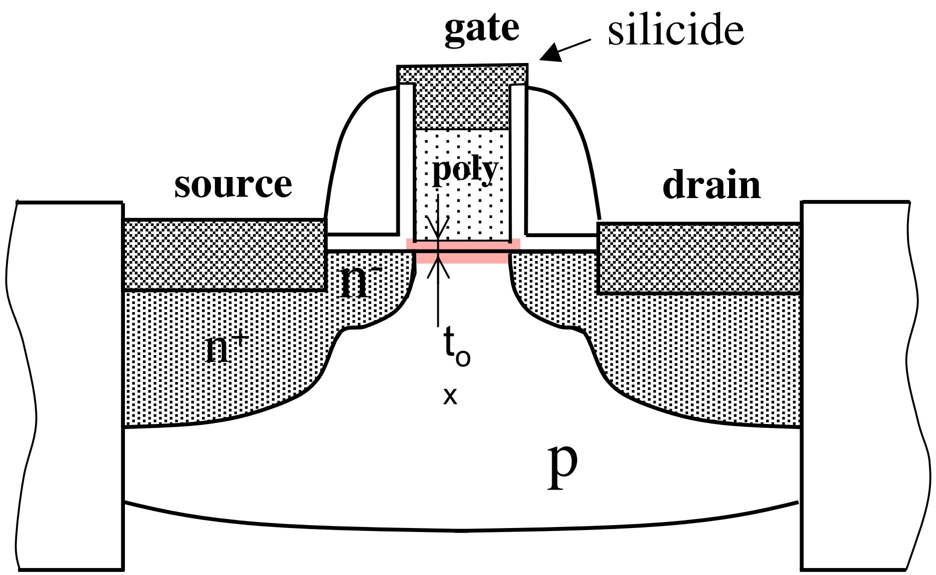
- The basic EKV / ACM model does not apply to short channel devices!

- Real $I_D(V_{GS})$ characteristics however look very similar.



- The spatial distribution of electrical fields in the substrate boils down to a 2D problem controlled mainly by L, V_{SB}, V_{DS}, little by V_{GS}.
- The inversion layer confines to a 1D problem controlled by V_{GS} and L, V_{SB}, V_{DS}.

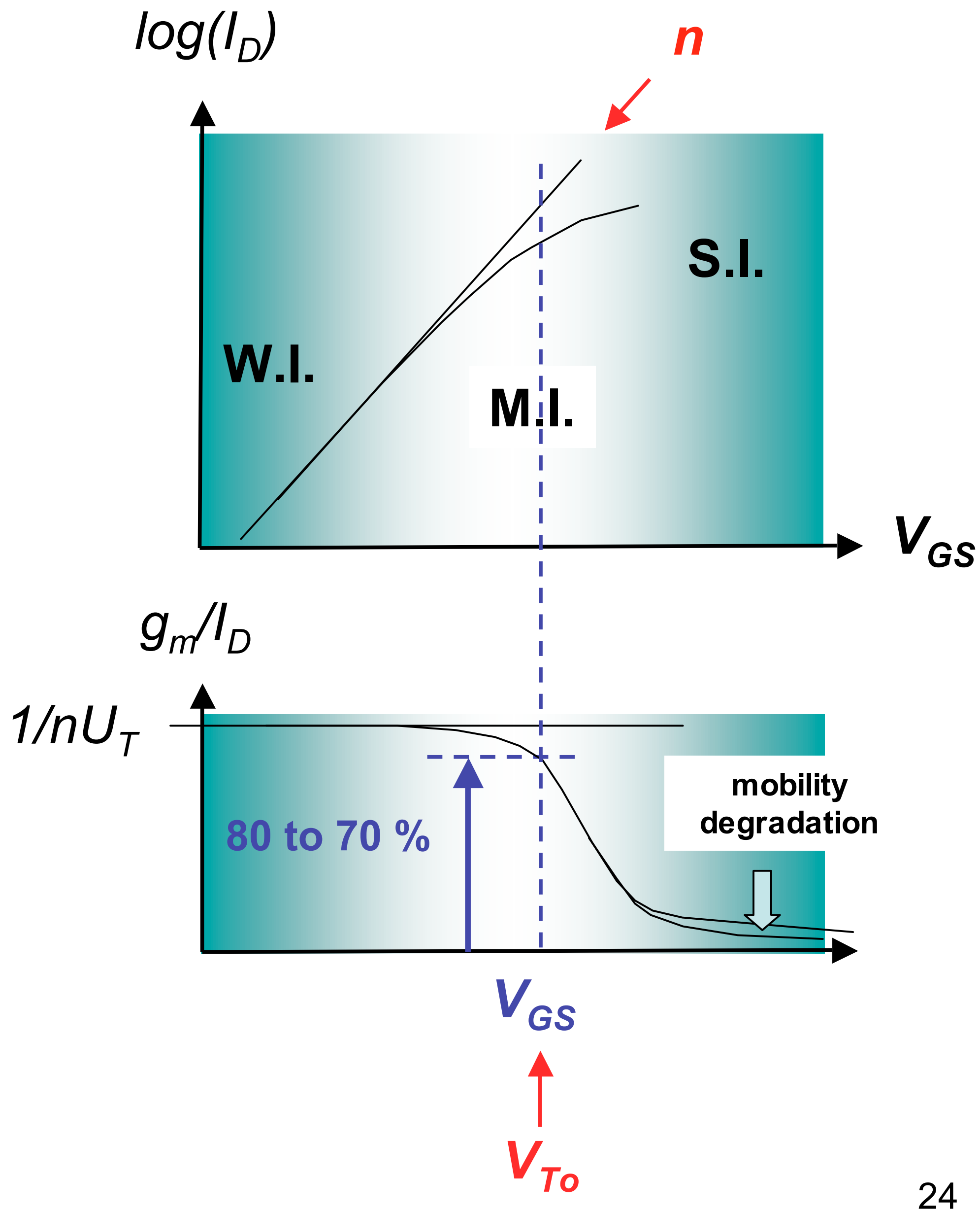
- Is it possible to model $I_D(V_G)$ characteristics by means of the EKV / ACM model with parameters that are functions of L, V_S and V_D?



E.K.V. Identification

to be performed in the
common source configuration

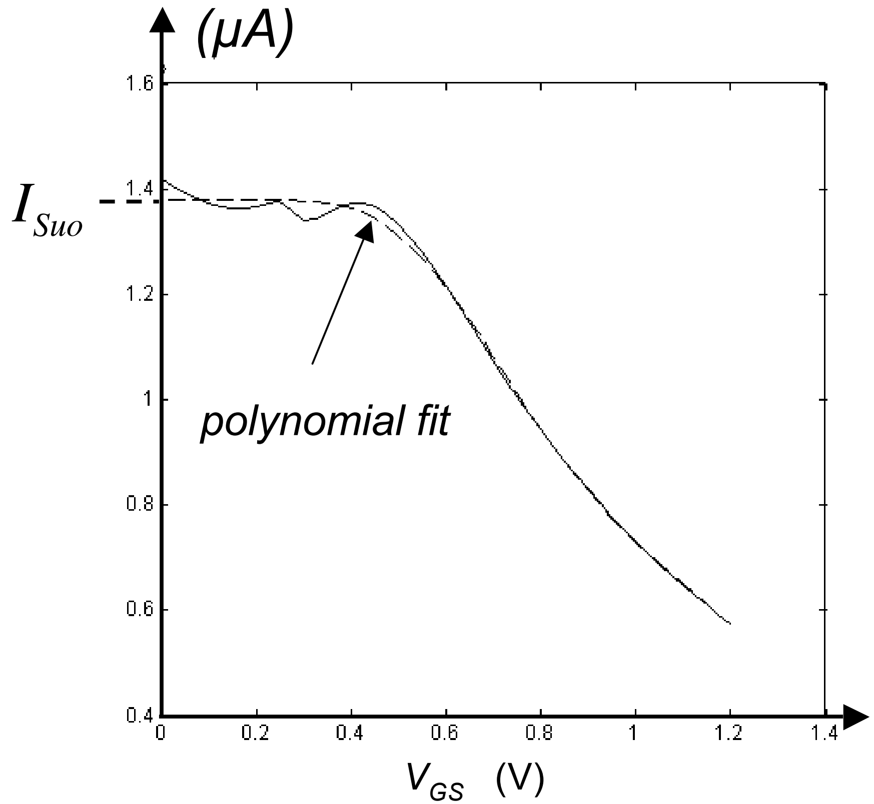
For L, V_S and V_{DS}



I_{su} (specific current)

$$\frac{I_{Du}(V_{GS})}{i} = I_{Su}(V_{GS})$$

$$\frac{V_{GS} - \boxed{V_{To}}}{\boxed{n}} = V_P \rightarrow q$$

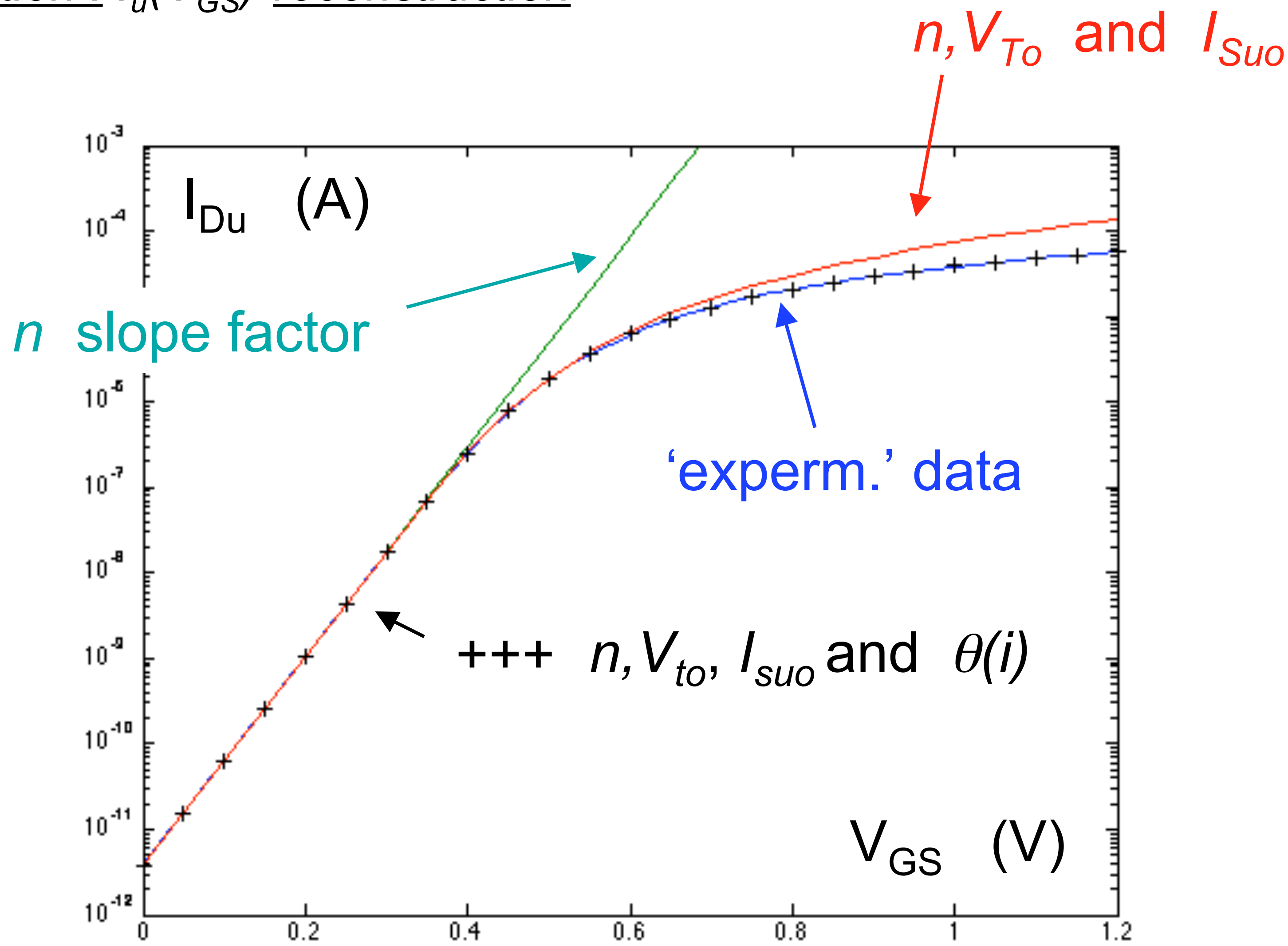


$$I_{Su} = \underbrace{2nU_T^2\,\mu_o C'_{ox}}_{\boxed{I_{Suo}}}\boxed{\theta(i)}$$

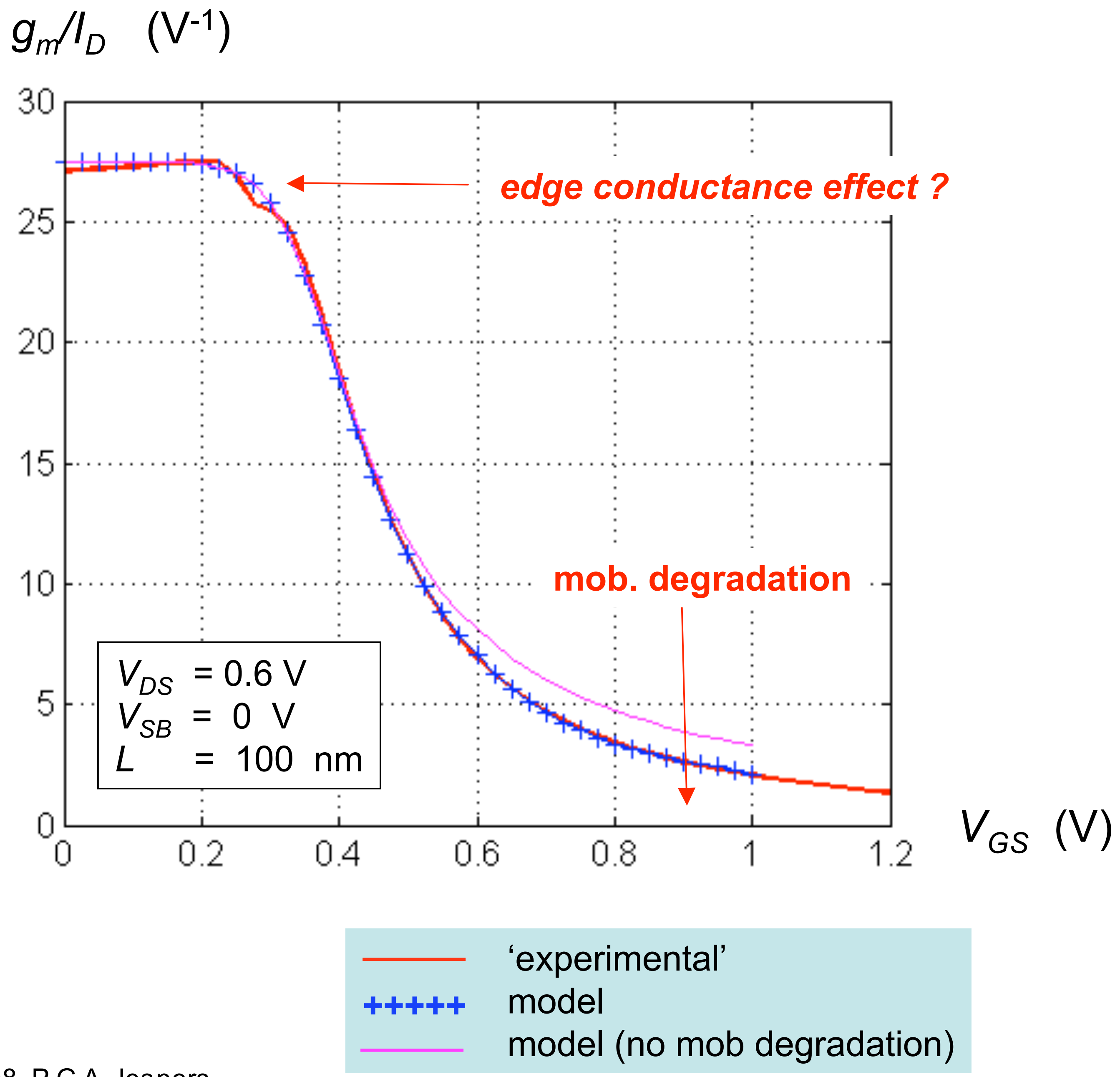
mobility degradation factor

For L, V_S and V_{DS}

Verification : $I_u(V_{GS})$ reconstruction



N-channel; L = 100 nm; V_{DS} = 0.6 V; V_{SB} = 0.6 V.



g_m/I_D (V^{-1})
30
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
1.2
V_{GS} (V)
edge conductance effect ?
mob. degradation
V_{DS} = 0.6 V
V_{SB} = 0 V
L = 100 nm
'experimental'
model
model (no mob degradation)

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Conclusion

$\frac{g_m}{I_D}$ does not depend on W

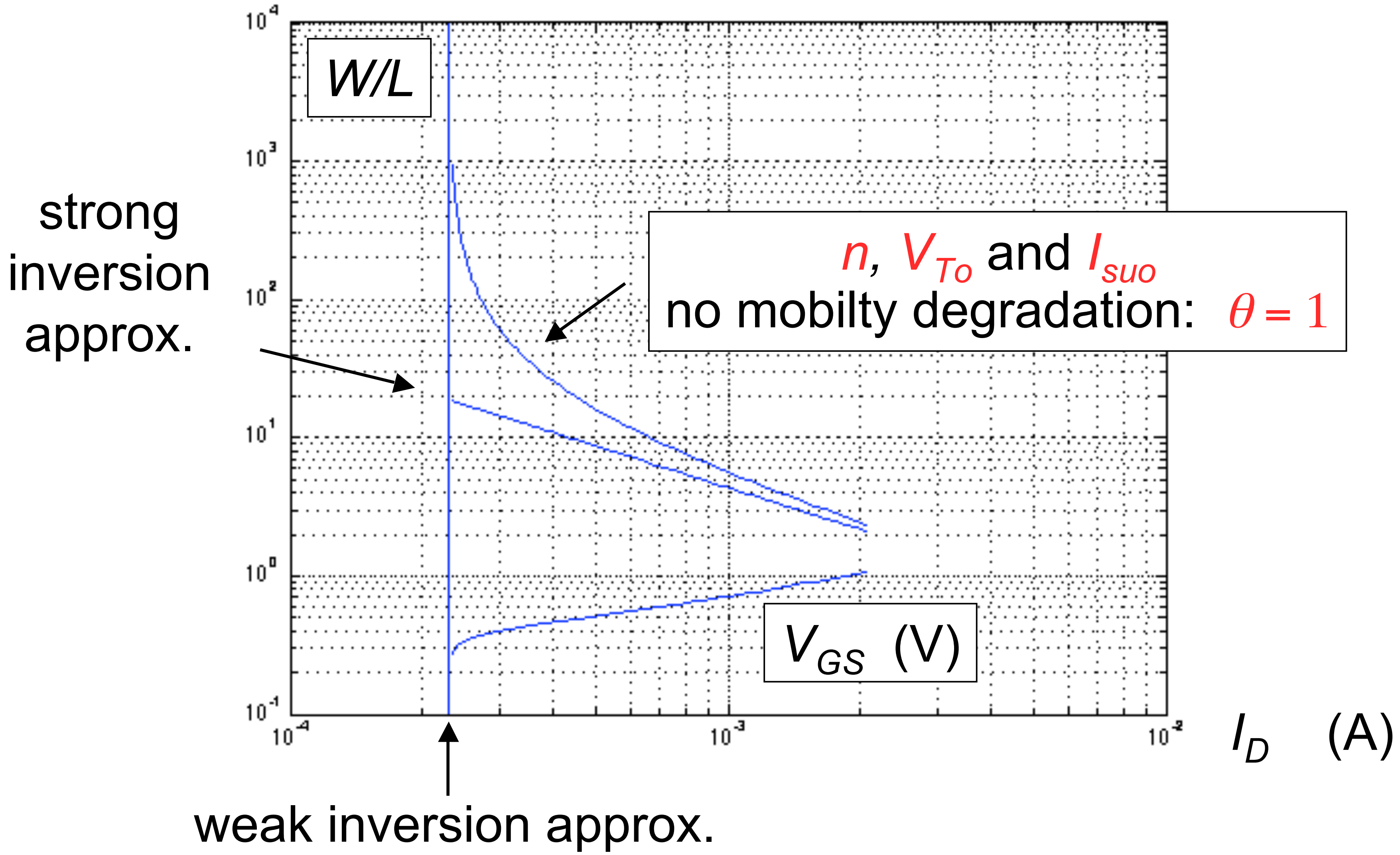
as long as $W >> W_{min}$

(true for most analogue circuits)

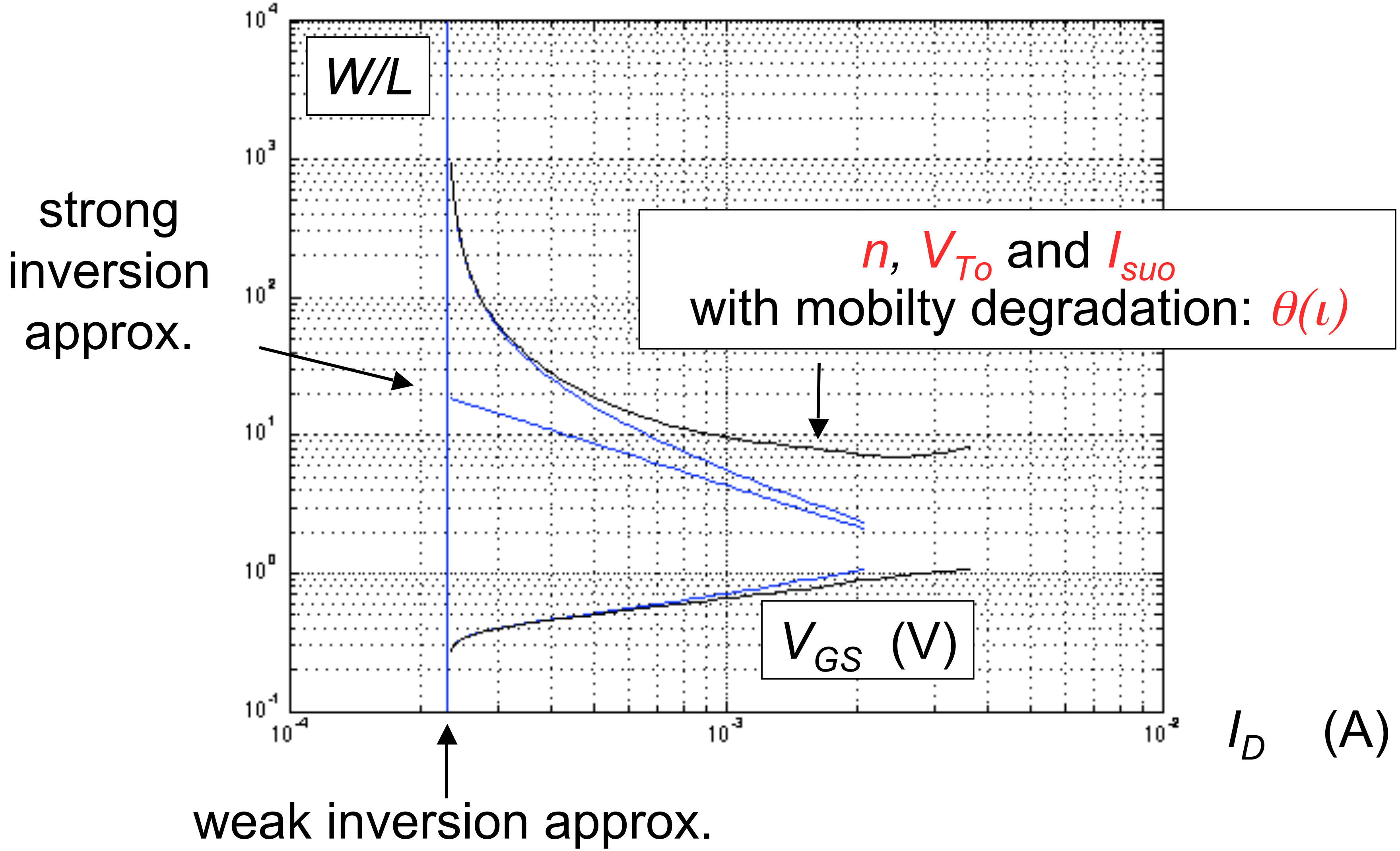
depends on L, V_{DS} and V_{SB} for

- V_T roll-off
- D.I.B.L.
- C.L.M.
- mobility degradation
- ....

f_T = 1 GHz; C_o = 1 pf; L = 120 nm; V_S = 0; V_{DS} = 0.6 V;

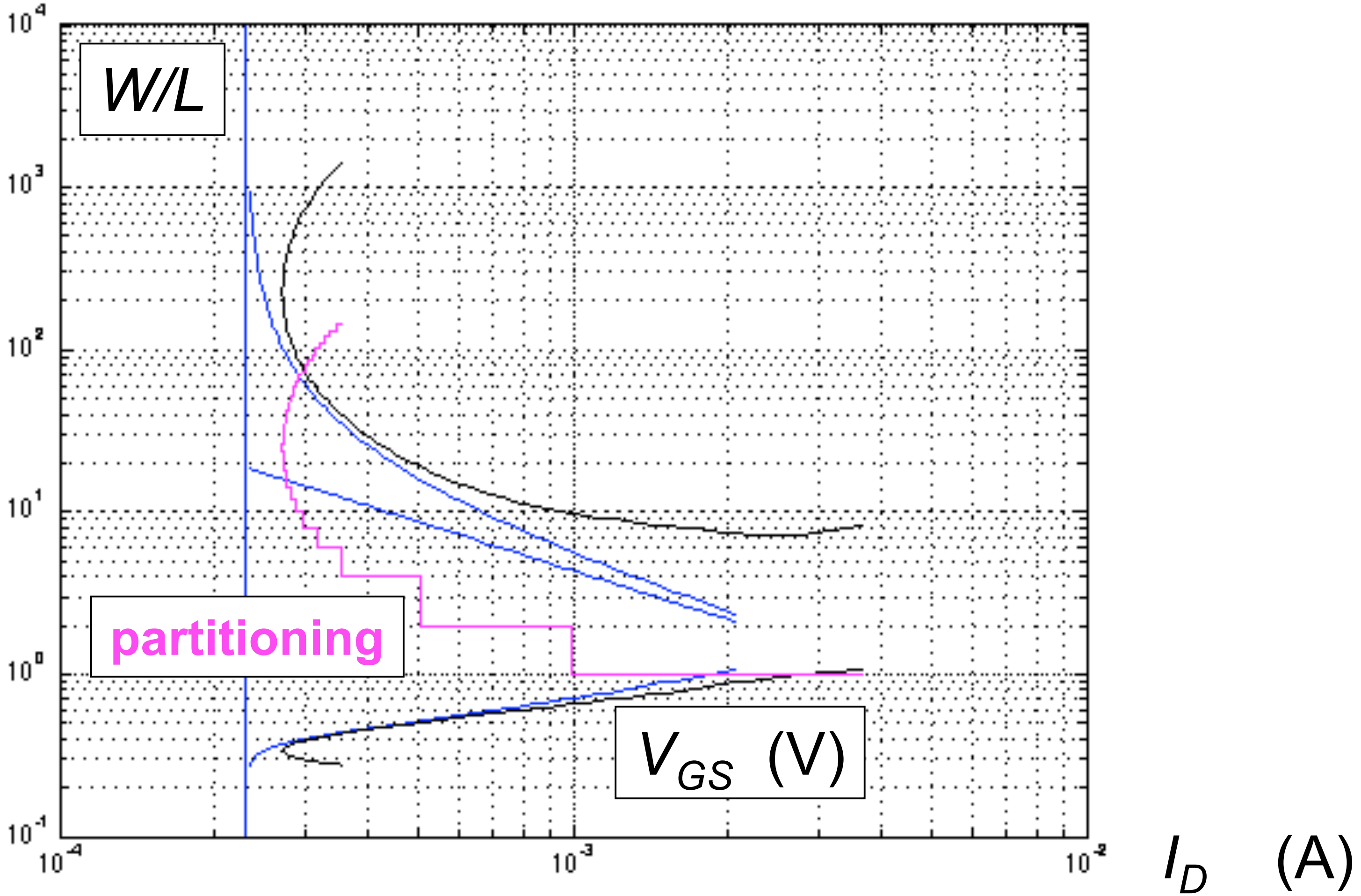


f_T = 1 GHz; C_o = 1 pf; L = 120 nm; V_S = 0; V_{DS} = 0.6 V;



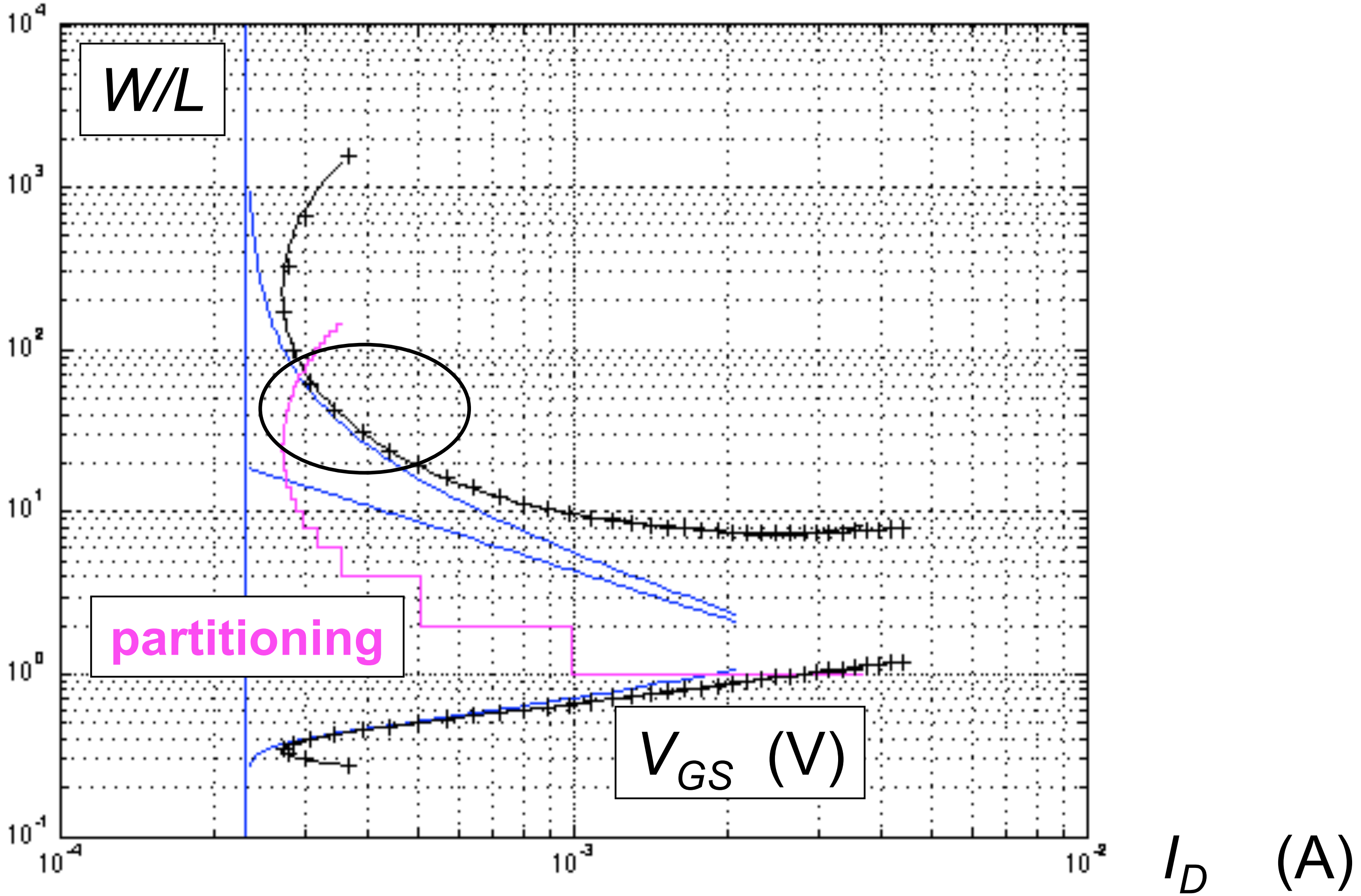
Add drain junction cap. to C_o

f_T = 1 GHz; C_o = 1 pf; L = 120 nm; V_S = 0; V_{DS} = 0.6 V; Wmax = 1 µm;



Comparison with semi-empirical method (+++)

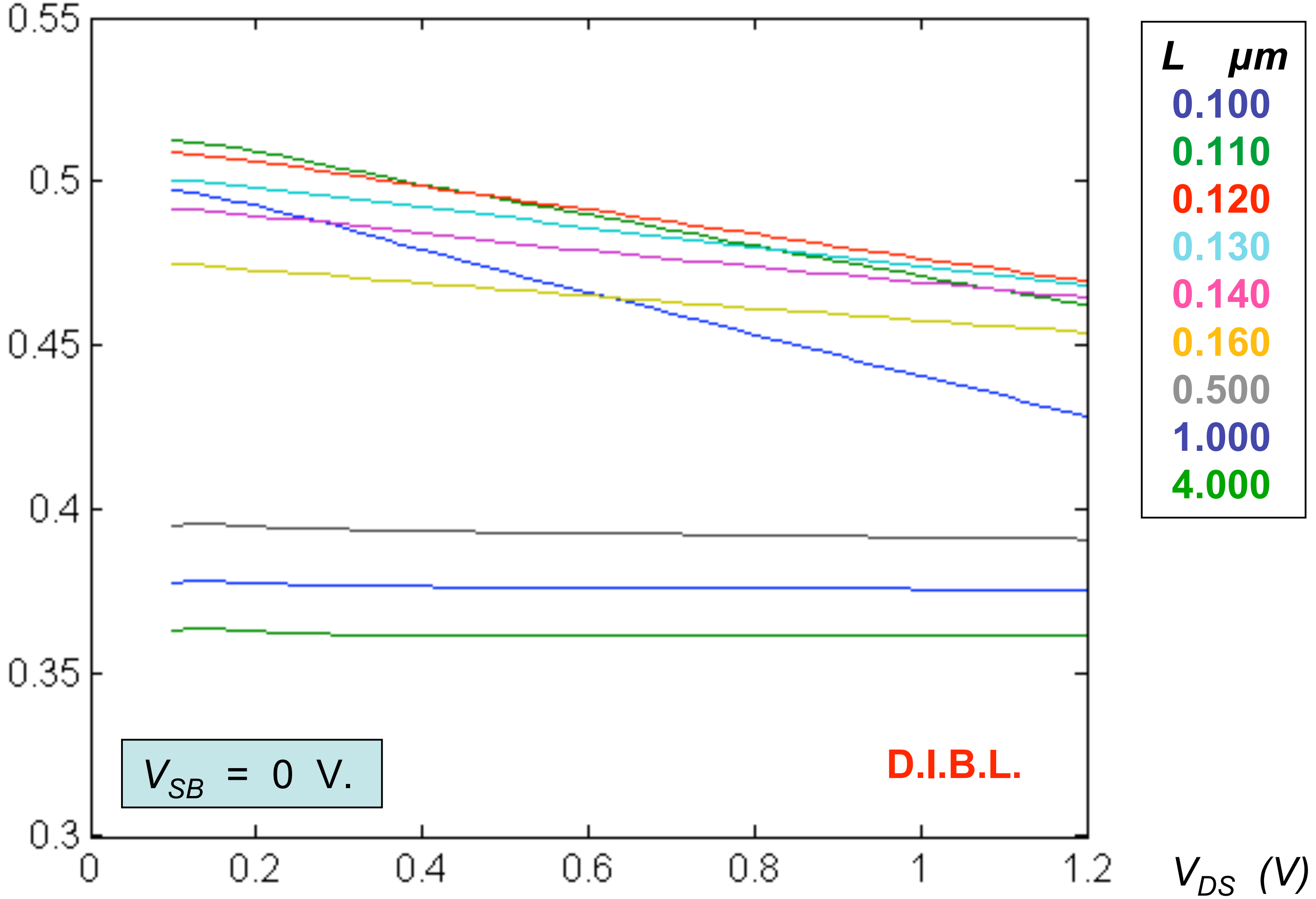
f_T = 1 GHz; C_o = 1 pf; L = 120 nm; V_S = 0; V_{DS} = 0.6 V; Wmax = 1 µm;



Param. dependence on V_{DS}

1) n small

2) V_{To} →

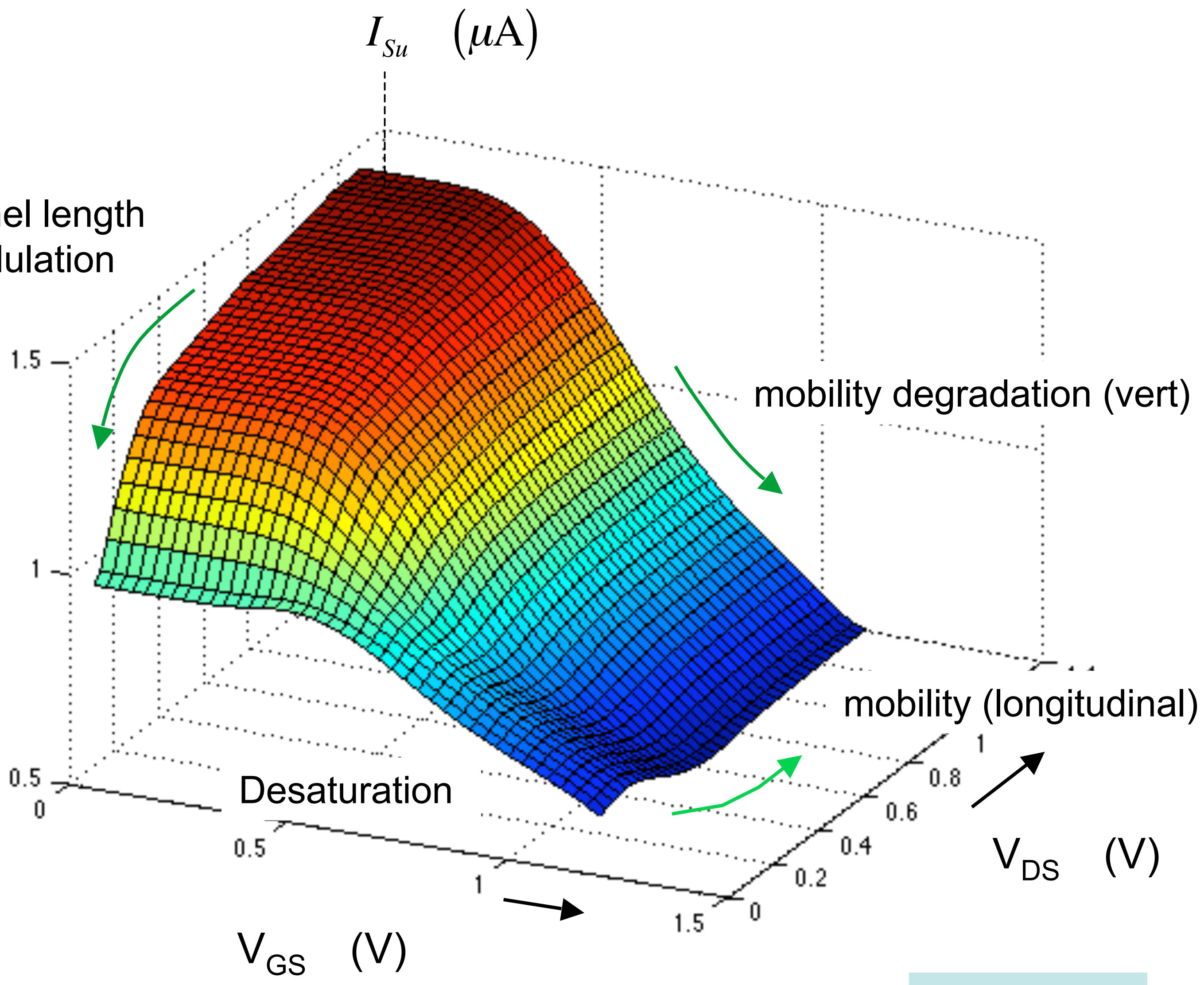


Param. dependence on V_{DS}

1) *n* small

2) V_{To}

3) I_{Su}



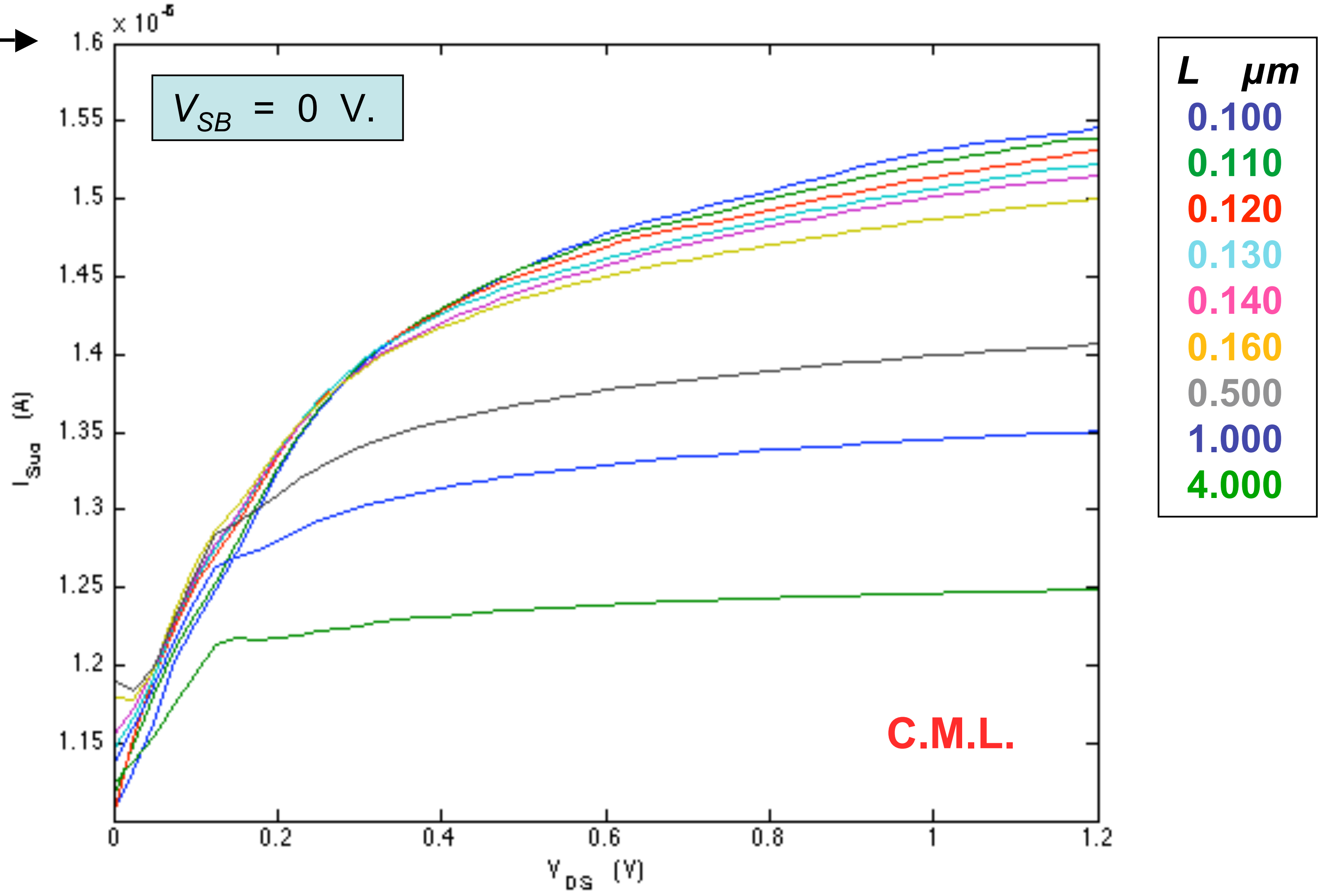
V_{SB} = 0 V.

Param. dependence on V_{DS}

1) n small

2) V_{To}

3) I_{Suo} →



$\underline{\text{Param. dependence on}}$ V_{DS}

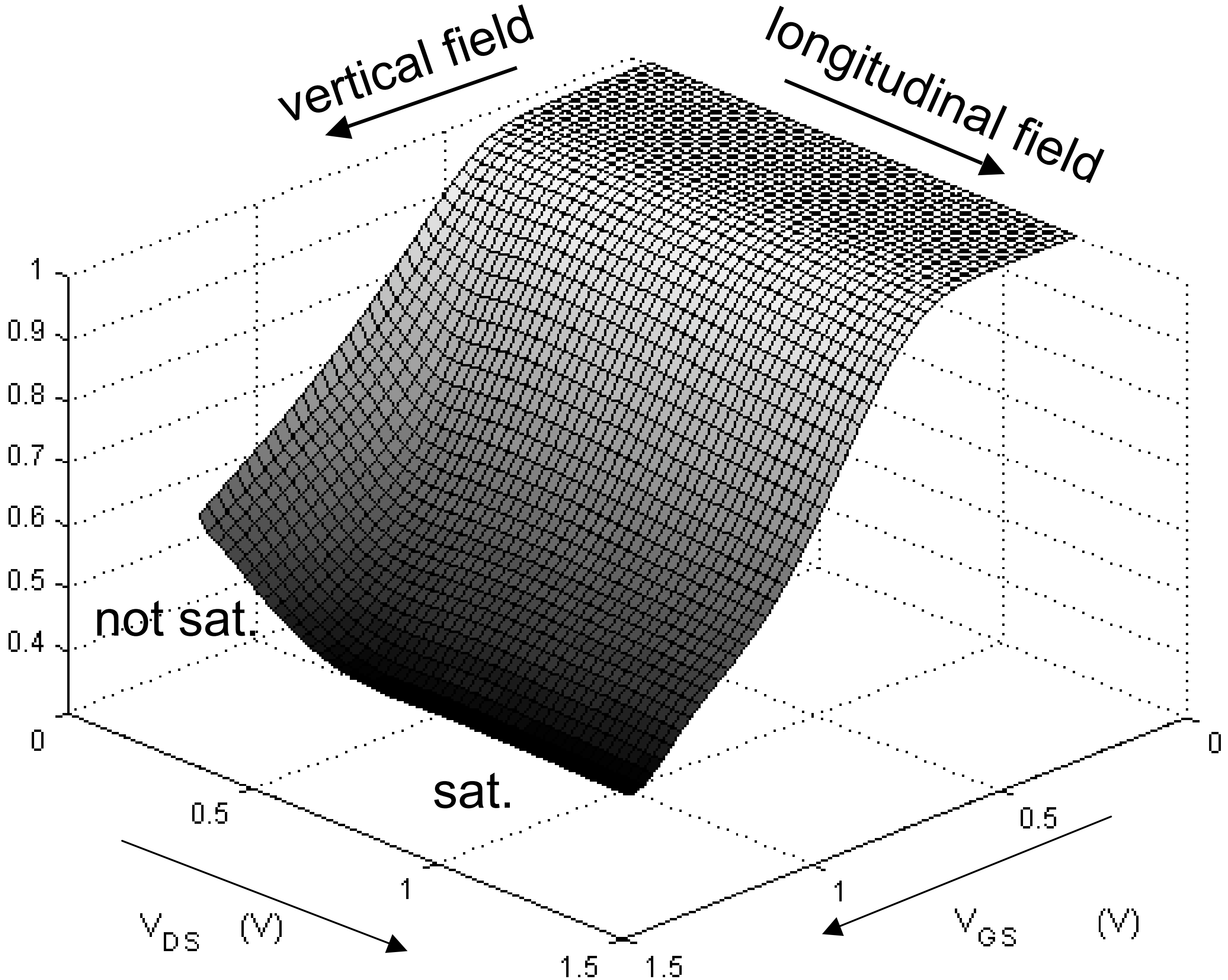
1) *n* small

2) V_{To}

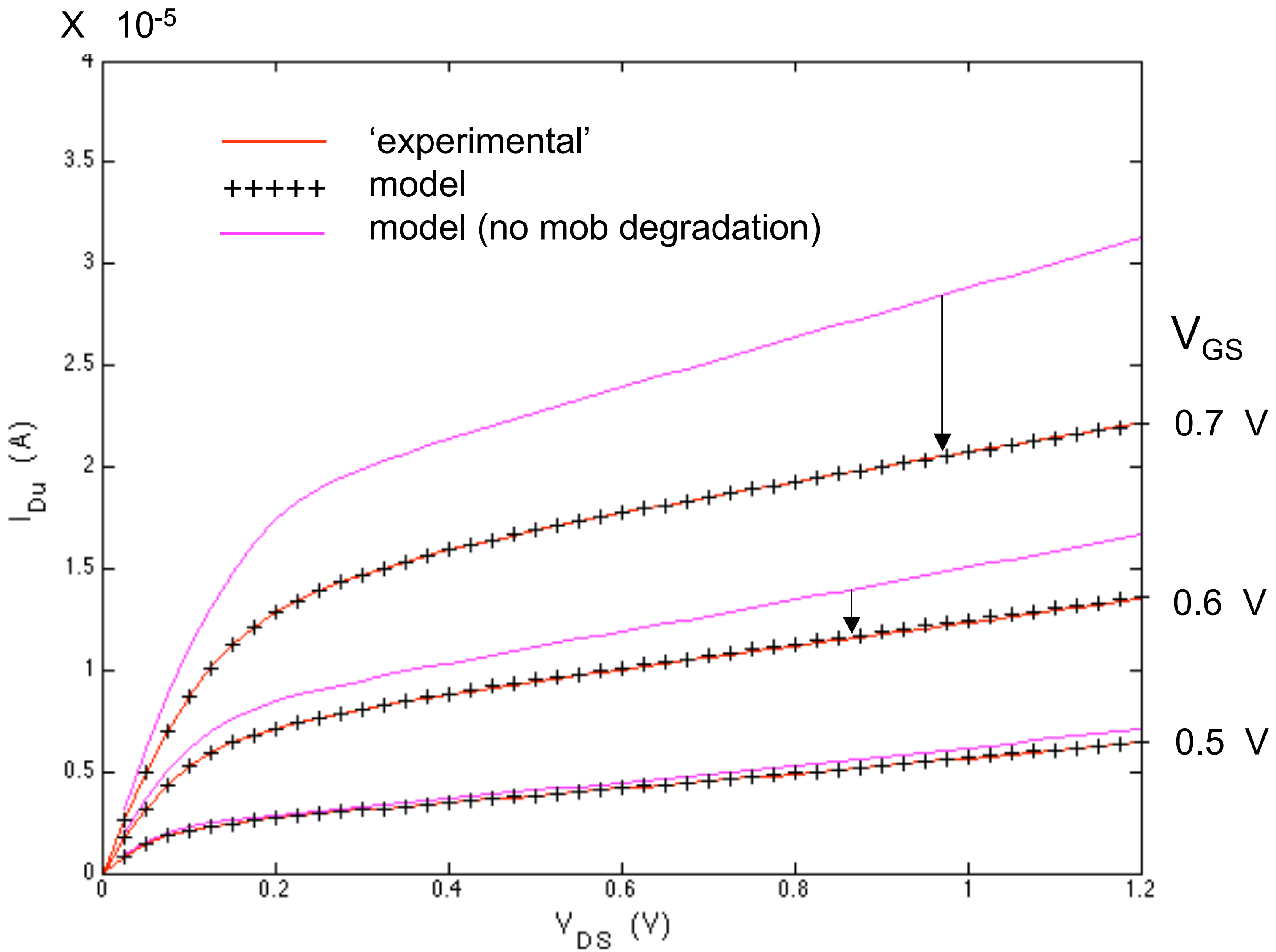
3) I_{suo}

4) $\theta(i)$ →

V_{SB} = 0 V.



Verification : $I_{Du}(V_{DS})$ reconstruction (S.I.)



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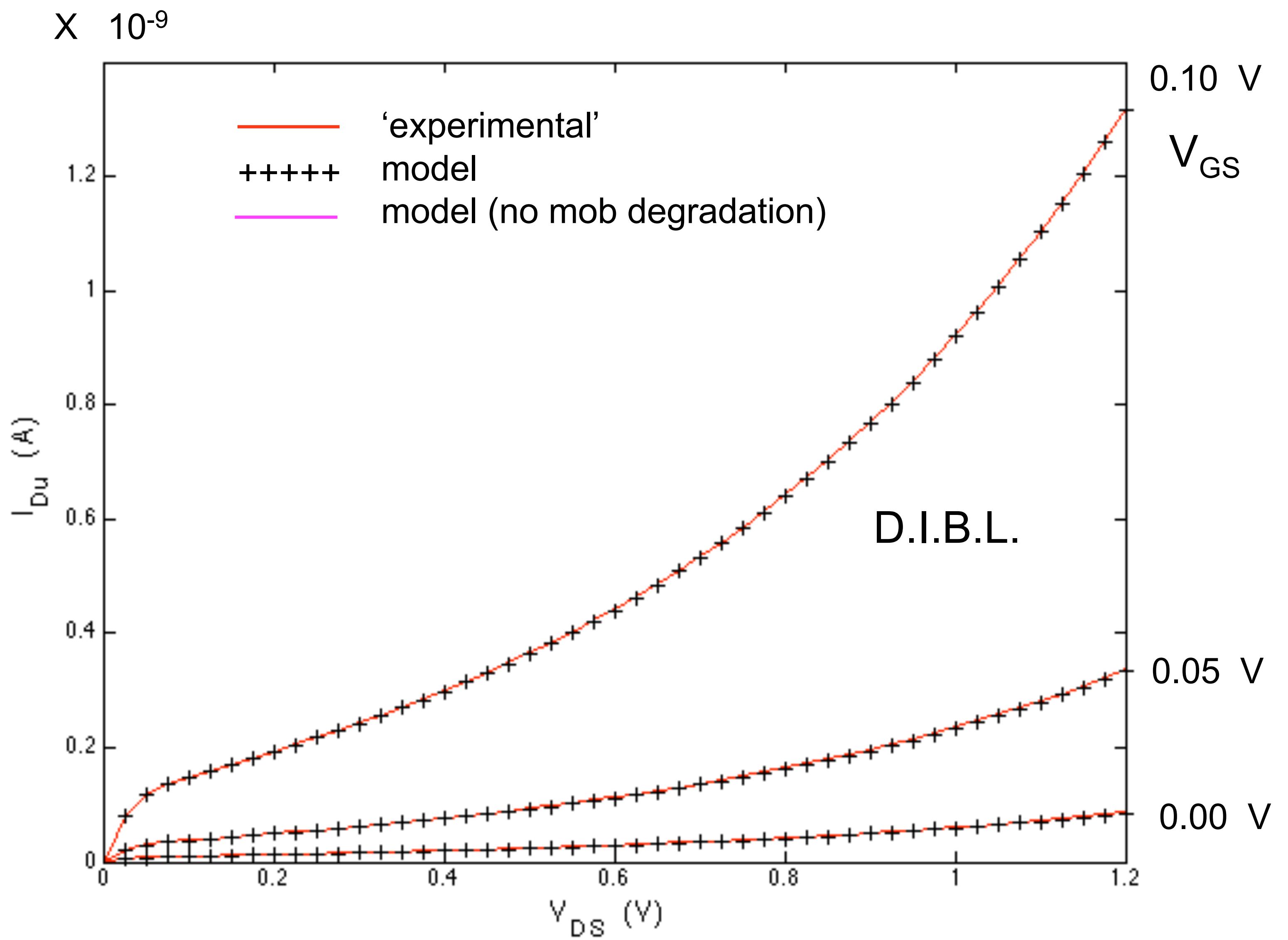

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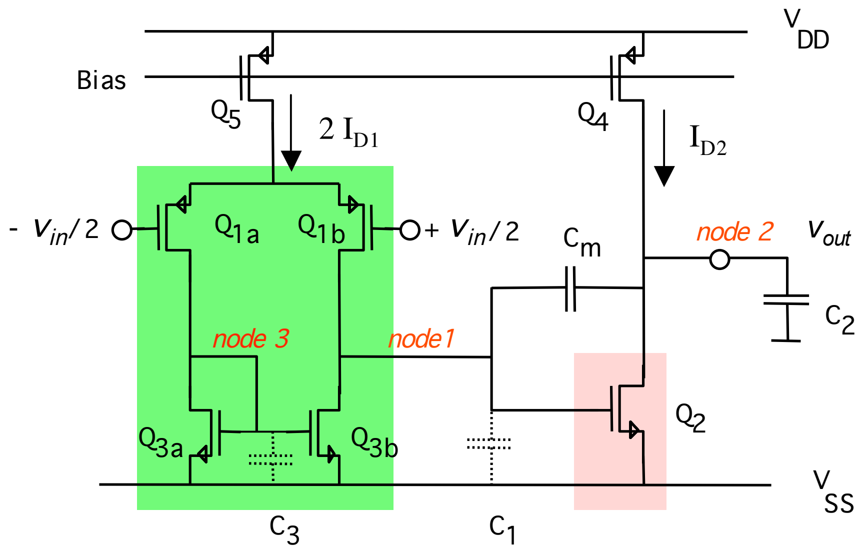
Conclusion

1) fix NDPole and Zero with respect to ω_T to meet phase margin



$$\omega_T = \frac{g_{m1}}{C_m}$$

$$z = \frac{g_{m2}}{C_m} = Z\omega_T$$

$$\omega_{ndp} = \frac{g_{m2}}{C_m}\frac{C_m^2}{(C_1+C_2)C_m + C_1C_2} = NDP\,\omega_T$$

e.g. $Z = 10$ and $NDP = 4\ldots 5$

for phase margin of approx. 60°

2) Size the ‘A’ transistors.

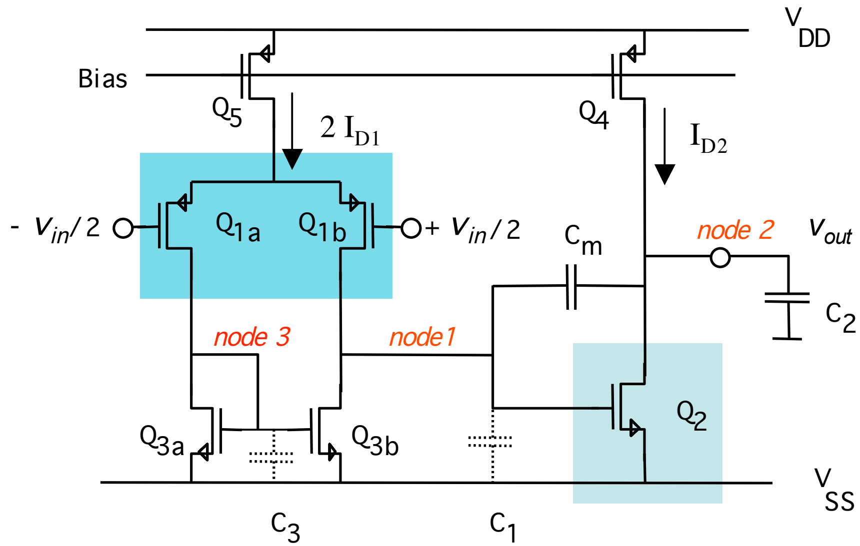
spec. initial guess

$$g_{m1} = \omega_T C_m$$

$$I_{D1} = \frac{g_{m1}}{\left(\frac{g_m}{I_D}\right)_1}$$

q_{F1}

$$\frac{W_1}{L_1} = \frac{I_{D1}}{I_{Du1}}$$



$$g_{m2} = Z\, g_{m1}$$

$$I_{D2} = \frac{g_{m2}}{\left(\frac{g_m}{I_D}\right)_2}$$

q_{F2}

$$\frac{W_2}{L_2} = \frac{I_{D2}}{I_{Du2}}$$

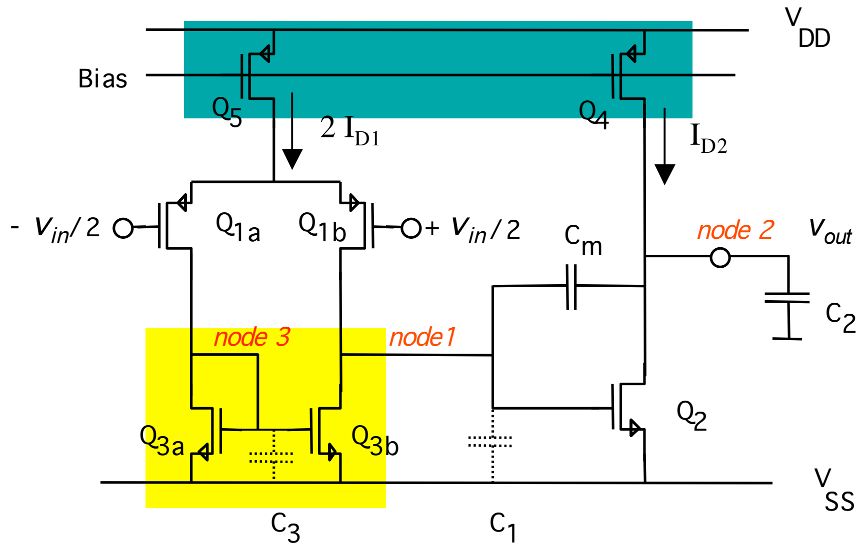
3) Size the 'B' transistors.

more constraints

- zero systematic offset

$$V_{G3} = V_{G2}$$

$$\left(\frac{W}{L}\right)_3 = \frac{I_{D1}}{I_{Du2}}$$



- choose bias so that Q4 and Q5 are in strong inversion

$$I_{Du4} = I_{Du5}$$

$$\left(\frac{W}{L}\right)_4 = \frac{I_{D2}}{I_{Du4}}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D1}}{I_{Du4}}$$

4) Estimate C_1, C_2, C_3 and compute C_m

Choose …

L_1	medium (voltage gain)
L_2	min. size
L_3	large for min 1/f noise (beware from doublet!)
L_4	matching + size
L_5	matching + common mode rejection

- the parasitic cap. are estimated knowing W's and L's + techno. data
- a new C_m is extracted from inverted NDP equation

$$C_m = 0.5\frac{NDP}{Z}\cdot\left[C_1 + C_2 + \sqrt{\left(C_1 + C_2\right) + 4\frac{Z}{NDP}C_1 C_2}\right]$$

reiterate until C_m gets constant

example

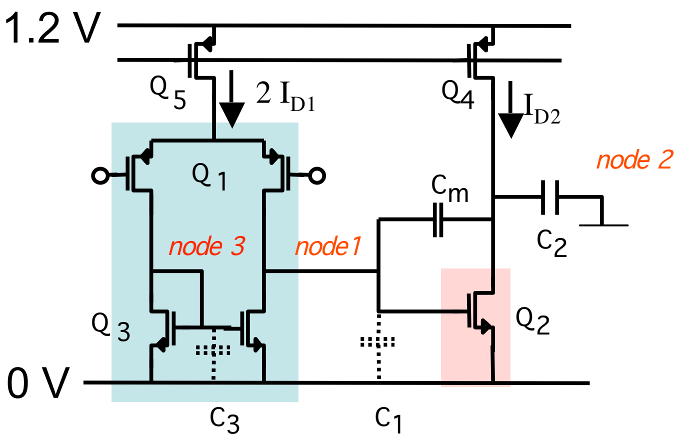
q_{F1}	= 0.0316 --> 3.16
q_{F2}	= 0.10 --> 2
q_{F4}	= 2,90

q_F exploration space

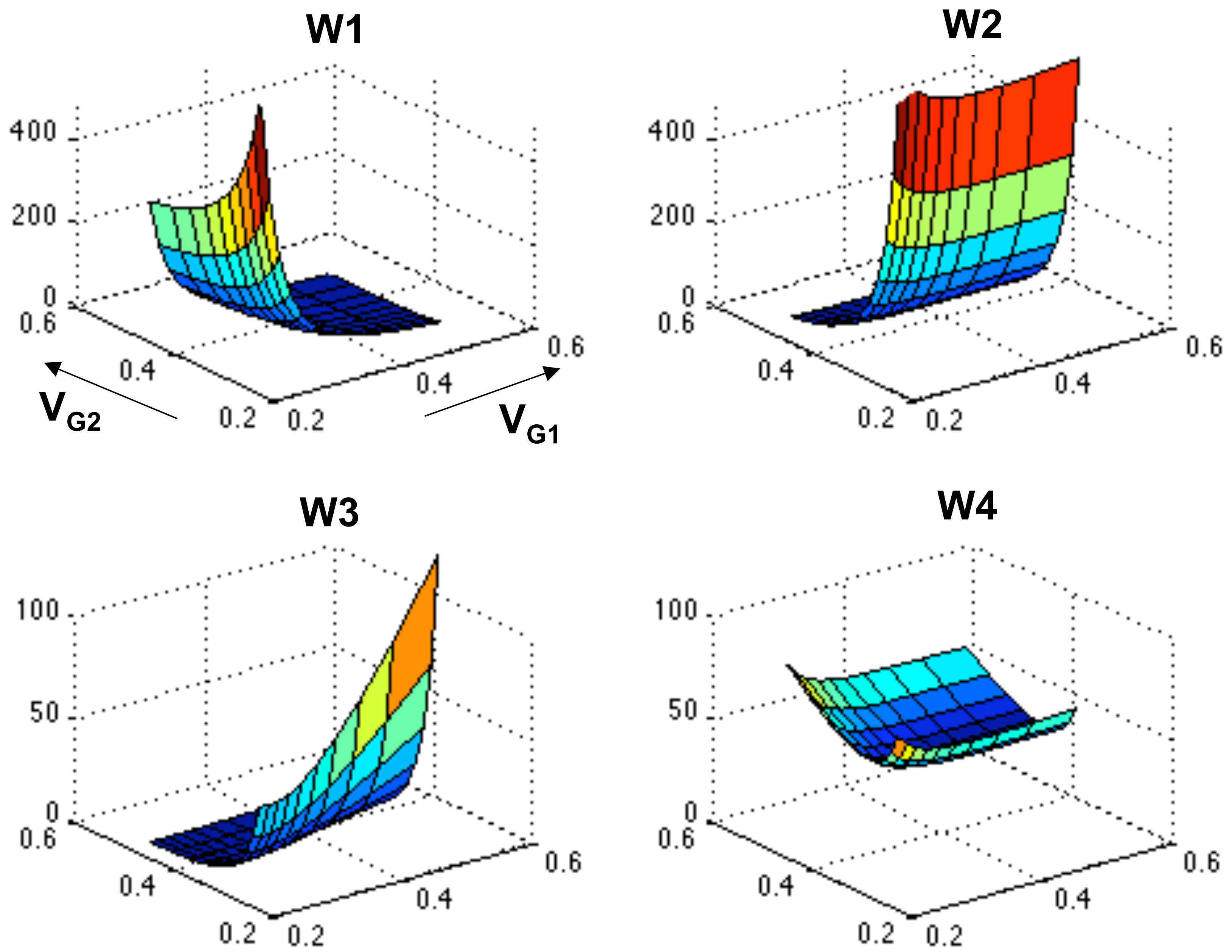
Spec: f_T = 50 MHz; C = 1 pF; VDD = 1.2 V;

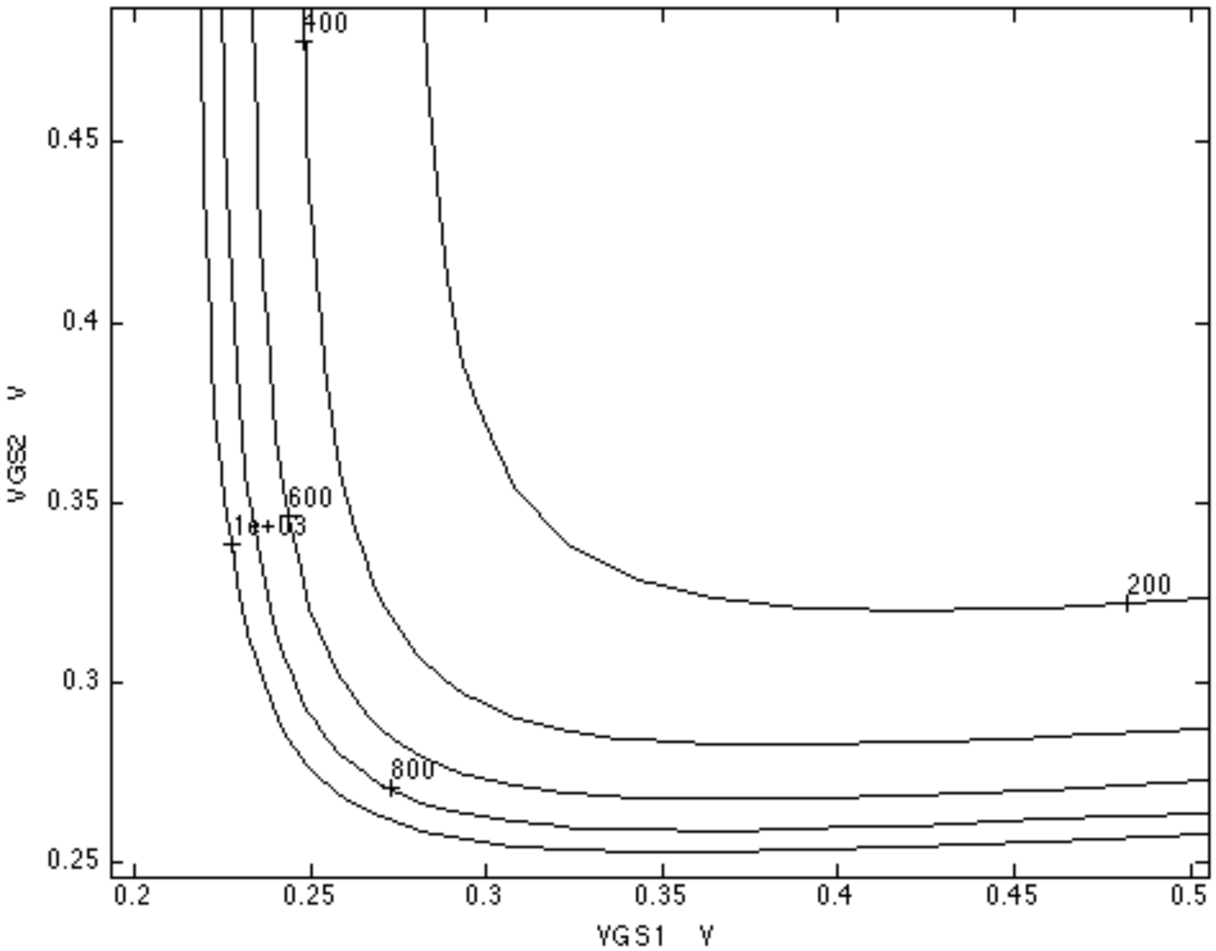
Z = 10
NDP = 4

phase margin

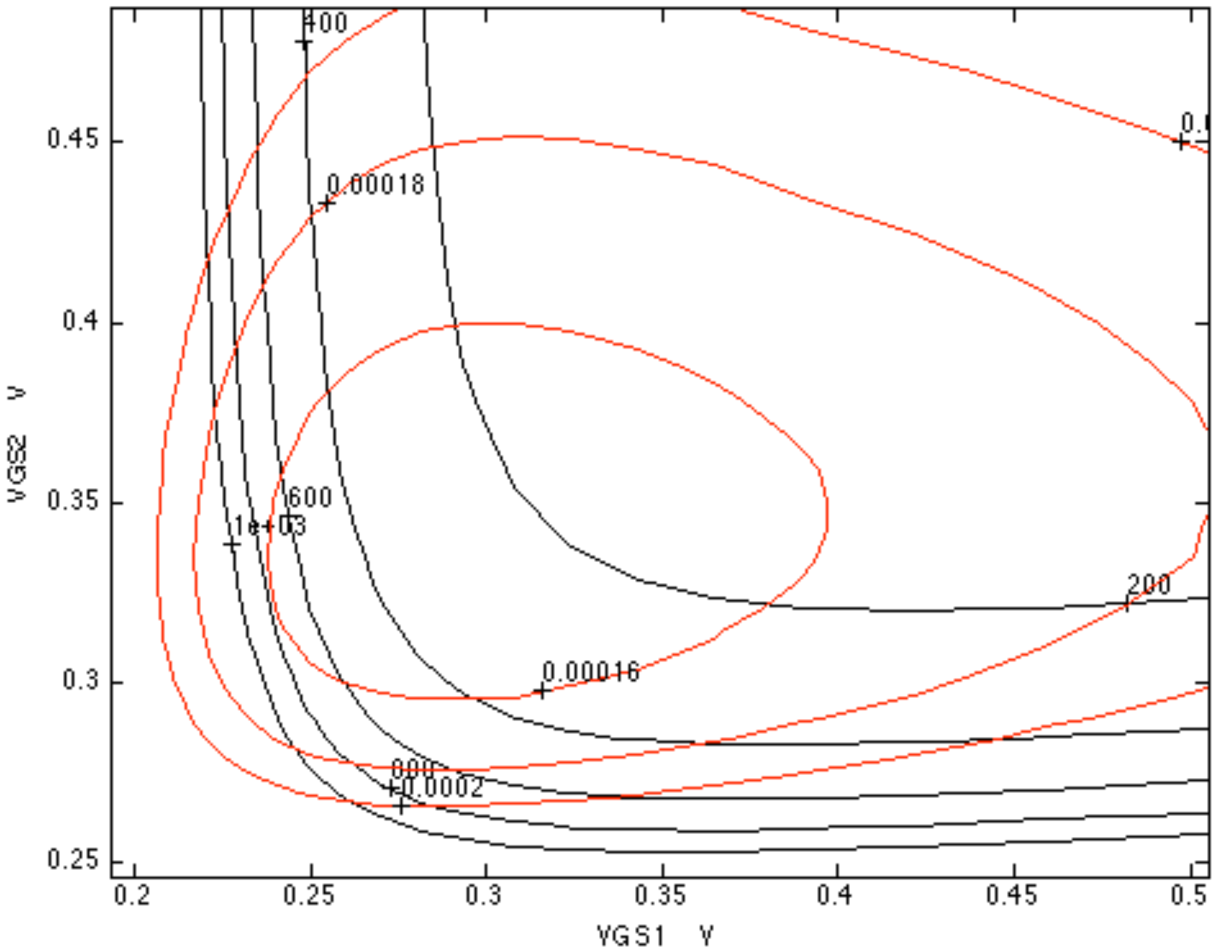


L1	= 1 µm
L2	= 0.5 µm
L3	= 1 µm
L4	= 0.5 µm
L5	= 1 µm

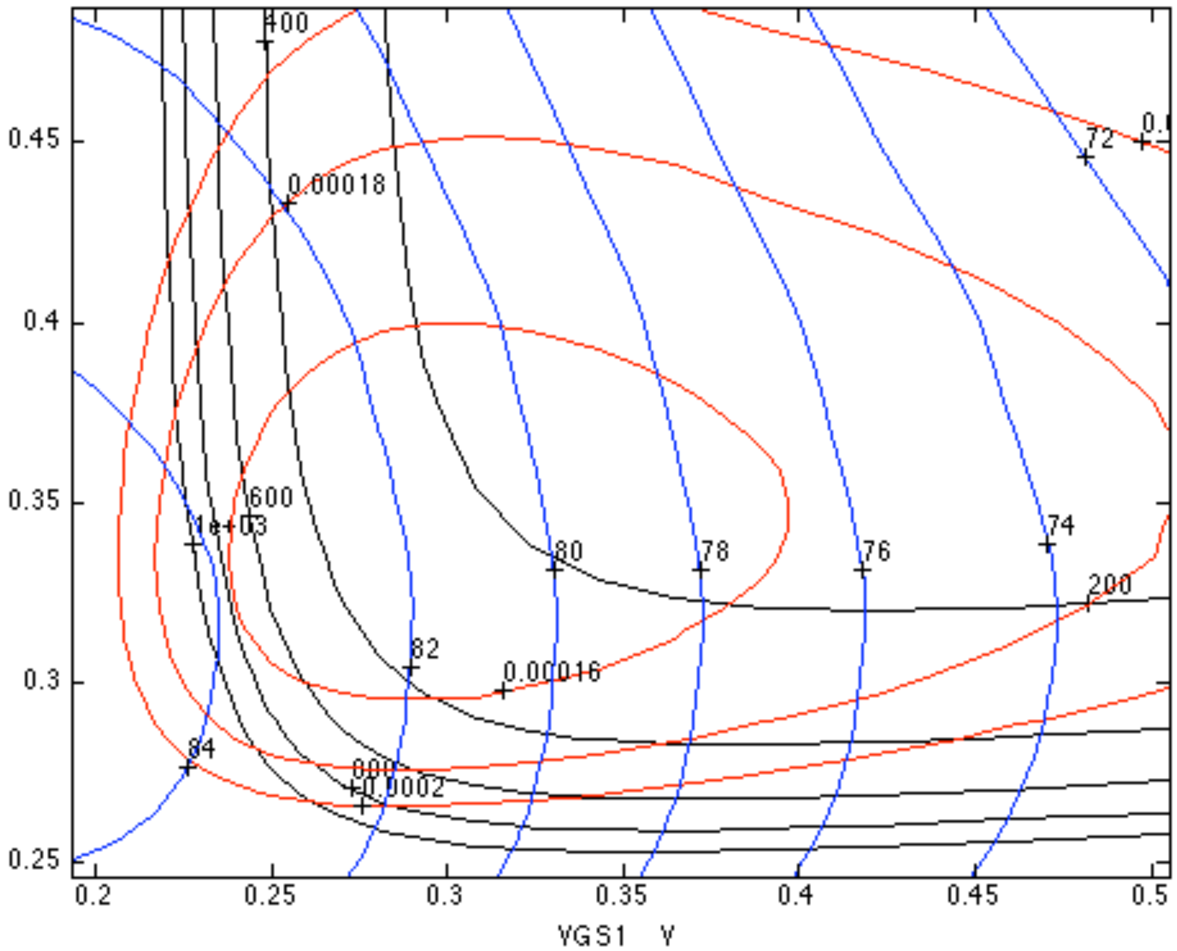

W1
W2
W3
W4
400
200
0
0.6
0.4
0.2
V_{G2}
V_{G1}
100
50



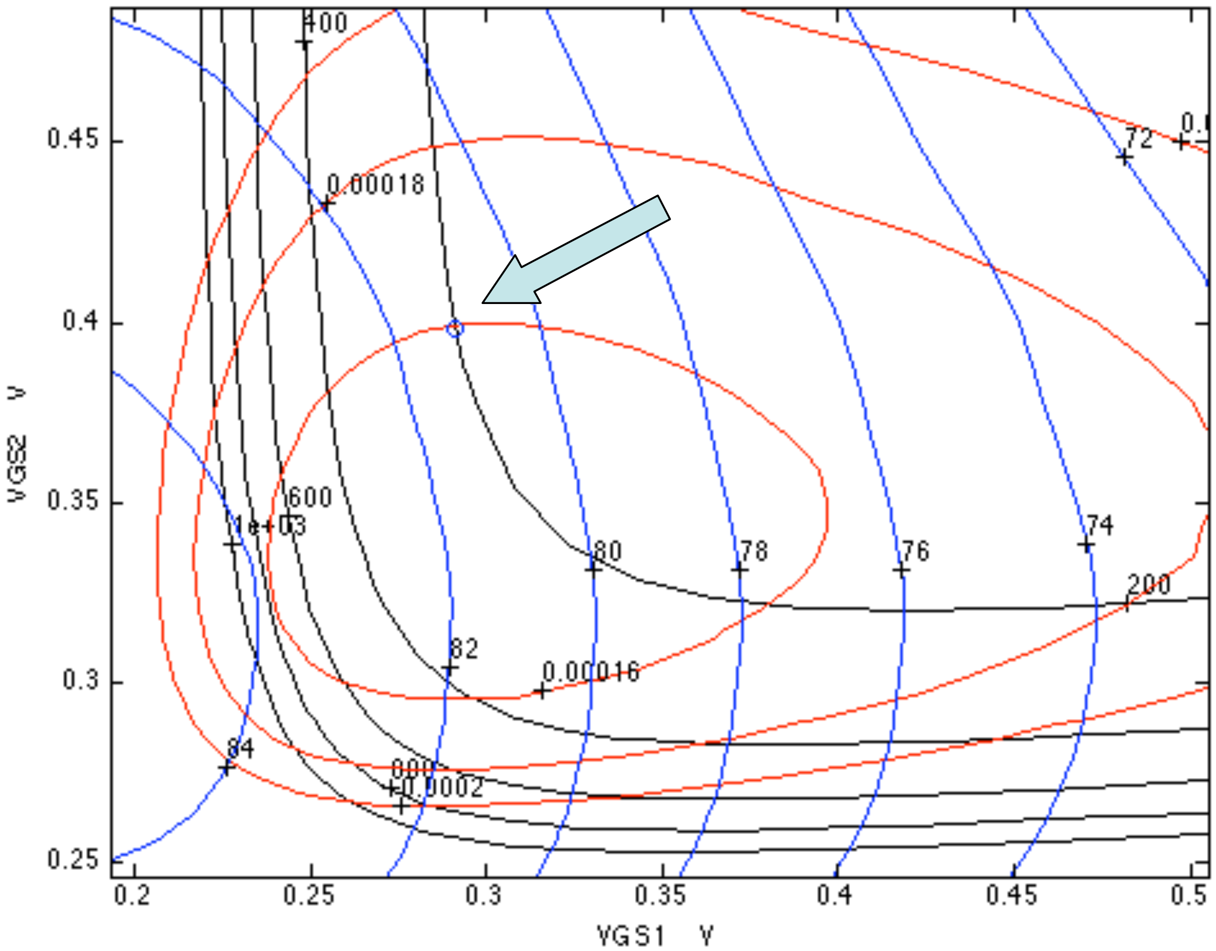
constant active area (μm^2) 47



constant supply (A)
constant active area (μm^2)



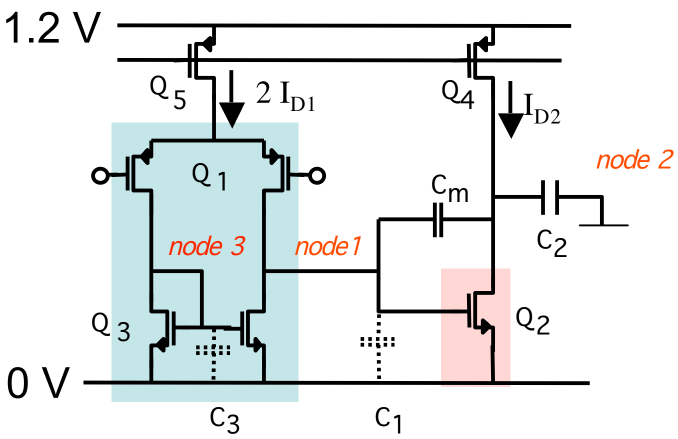
constant gain (dB)
constant supply (A)
constant active area (μm²)



constant gain (dB)
constant supply (A)
constant active area (µm²)

The selected point

	Q1	Q2	Q3	Q4	Q5
qF	0.433	1.065	1.236	2.90	2.90
VGS (V)	0.29	0.40	0.40	0.49	0.49
I (µA)	2 x 8.1	143.7	2 x 8.1		
W / L (µm)	67.3 / 1	47.5 / 0.5	2.23 / 1	57.83 / 0.5	7.69 / 1
gain (dB)	45.1	39.2			
	0.1965 C1 pF	1.0375 C2 pF	0.0576 C3 pF	0.6242 Cm pF	



gain = 81 dB
power consump. = 191 µW

Conclusion

g_m/I_D

- relates a small signal param. to a large signal quantity
- does not vary with transistor widths
- controls the mode of operation, power consump, gain ...

paves the way for sizing CMOS circuits

- semi-empirically

  (look-up tables : I_D, g_m, g_d, ..)
- by means of the E.K.V./A.C.M. model

  (parameters look-up tables or fitting functions)
  - simple expressions of I_D, g_m/I_D, g_d/I_D
  - q_F monitors mode of operation
  - increased physical insight

suitable for sub-micron low-voltage low-power circuits

g_m/I_D sizing methodology for low-power/voltage CMOS circuits

by P.G A. Jespers

to be published 2009 by Springer

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