Aim: Design of MOS amplifiers using gm/Id method

Q1. Characterization of MOS-T

Plot the following curves for NMOS

(a) gm/I_D vs Vov
(b) $I_D/(W/L)$ vs gm/I_D
(c) ft vs gm/I_D
(d) gm*ro vs V_{DS}

Q2. Design of Common Source amplifier with resistive load

(Take V_{DD}=3.0v and C_L= 25ff)

(a) Design for maximum gain
    $L = 2L_{min,}$ $I_D < 100uA$
(b) Design for maximum Bandwidth
    DC Gain = 2, $I_D < 100uA$

Do transient and ac simulation to get gain and -3dB frequency

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Theory: The methodology is intended for low-power analog and digital circuits where the weak as well as moderate inversion regions are often used because they provide a good compromise between speed and power consumption. The g_m/I_D ratio indeed is a universal characteristic of all transistors formed by the same process.

MOS transistors are either in strong inversion or in weak inversion. Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive (V_{OV}) as the key parameter, where $V_{OV} = V_{GS} - V_{T.}$

If we consider a simple common source amplifier, the power and bandwidth are given by following equations

$$P = \frac{1}{2}\frac{V_{DD}}{R_L} \cdot A_{DC} \cdot V_{OV}$$

$$\omega_{-3dB} = \frac{3}{2}\frac{R_L}{R_i} \cdot \frac{1}{A_{DC}} \cdot \frac{\mu}{L^2} \cdot V_{OV}$$

With the assumed fixed design specifications, and a given technology (, Lmin), both power and bandwidth of our circuit are completely determined by the choice of V_{OV}

Making V_{OV} small to save power also means that we lose bandwidth.

This makes intuitive sense since

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox} V_{OV}}$$

With gm and L fixed, smaller V_{OV} translates into a bigger (wider) device, and thus larger Cgs. So we conclude from this that the V_{OV} is not a good design parameter

What we really want from MOS transistor

– Large gm without investing much current

– Large gm without having large Cgs

To quantify how good of a job our transistor does, we can therefore define the following "figures of merit"

Performance Metrics of Interest:

- ***Transit Frequency:***

$$\omega_T = \frac{g_m}{C_{gs}}$$

- ***Trans-conductor Efficiency:***

$$\frac{g_m}{I_D}$$

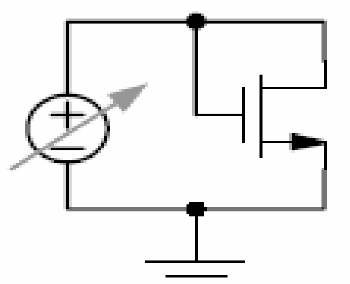
- ***Intrinsic Gain:***

$$g_m r_o$$

We find that V_{OV} is not "directly" related to performance metric. Hence, we switch towards a strategy called "gm/ID design methodology", in which gm/ID, rather than V_{OV} is used directly as a central design variable.

Generation of Performance Curves:

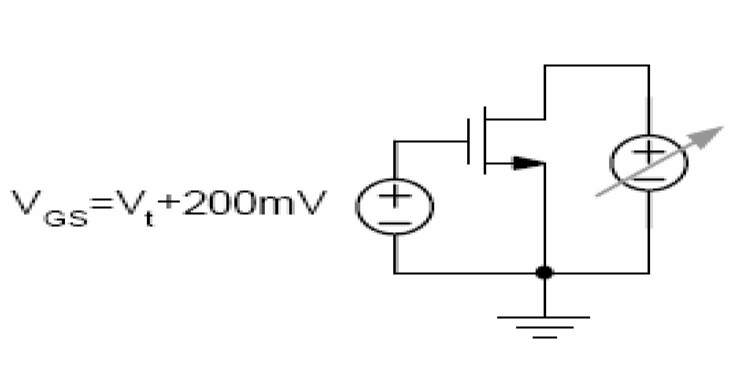
1. f_T Simulation:



Steps:

1) 1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2) Plot gate overdrive Vov = Vgs – Vt
3) Plot gm curve by taking derivative of I_D Vs Vgs
4) Divide gm curve by I_D curve to get gm/I_D.
5) Divide gm curve by Cgs to get f_T.
6) Plot (f_T Vs gm/I_D) transit frequency chart by taking F_T as Y-axis and gm/I_D as X-axis

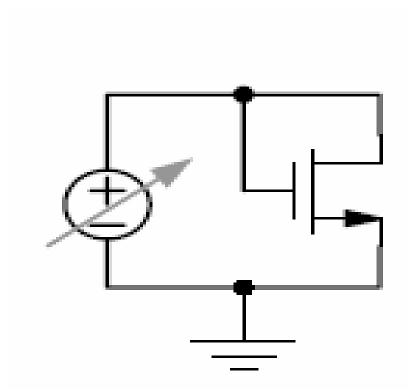
2. Intrinsic Gain Simulation:



Steps:

1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2. Get 1/ro curve by taking derivative of I_D Vs Vds.
3. To get ro plot, take the reciprocal of above curve. At very small value of Vds, gm is constant. Take that value as gmo. gmo can also be find out by dividing Id by (Vgs-Vt). Then plot gm = gmo*(1+λVds), where λ = 1/(ro*I_D)
4. Get gm*ro Vs Vds plot.

3. gm/ID Simulation:



Steps:

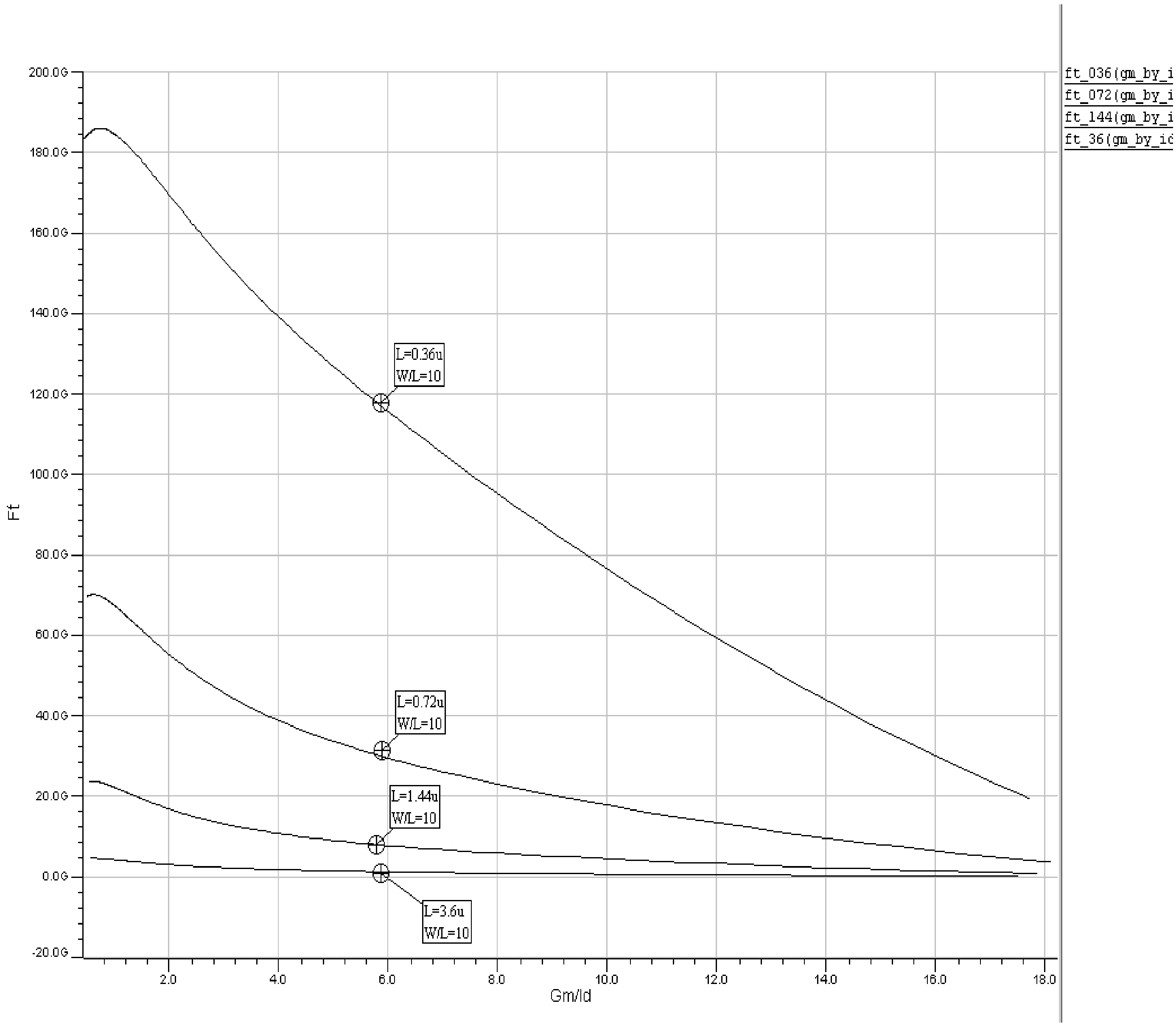
1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2. Find out gate overdrive Vov = Vgs – Vt. Vt can be seen in log files after running simulation after making the transistor in saturation.
3. Plot gm curve by taking derivative of I_D Vs Vgs.

4. Divide gm curve by I_D curve to get gm/I_D.
5. Divide I_D curve by W/L value to get I_D/W/L plot.
6. Setting gm/I_D as X-axis, plot I_D/W/L which is called current density plot.

Using the above method, gm/Id plots are generated for various Ls. This helps in design process.

1. Plots for F_T

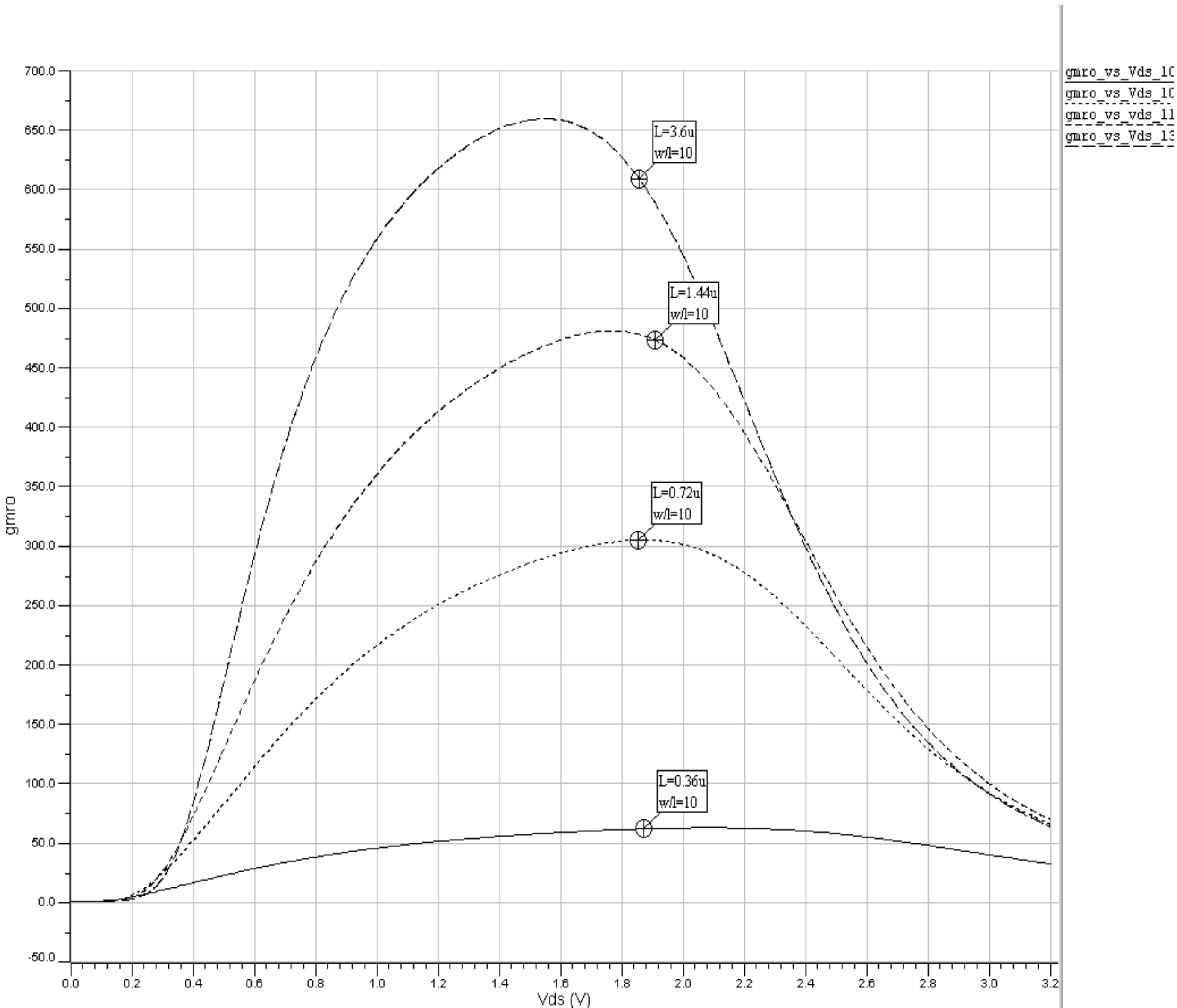
The following is the plot for F_T Vs gm/Id for four different L's



It had been stated earlier that the -3dB bandwidth is inversely proportional to L^2. Similar same effect can also be seen in case of F_T.

2. Plots for Intrinsic Gain

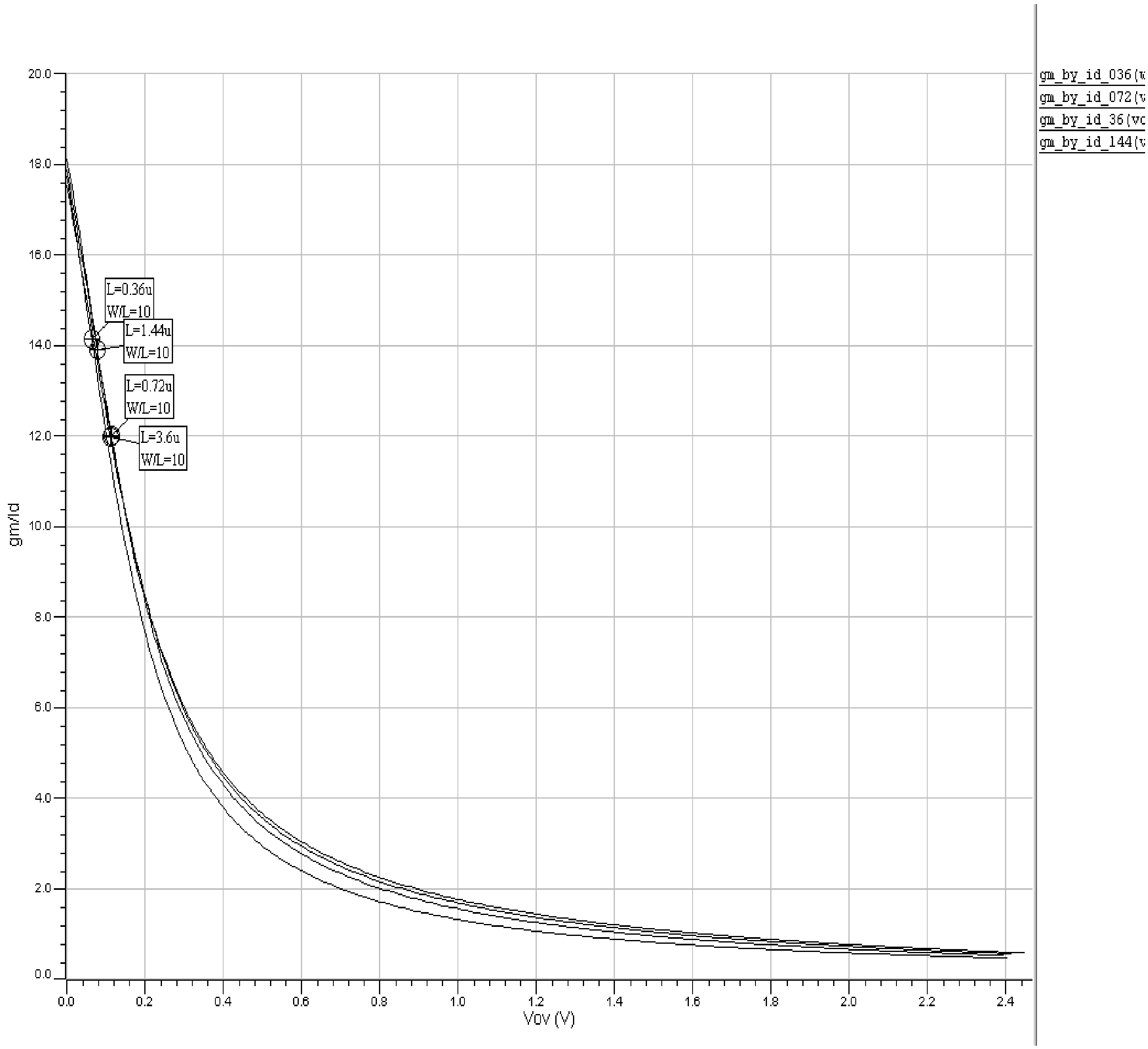
The plot for intrinsic gain ($gm*r_0$) has been given below.
Note how drastically the gain increases with increase in L.



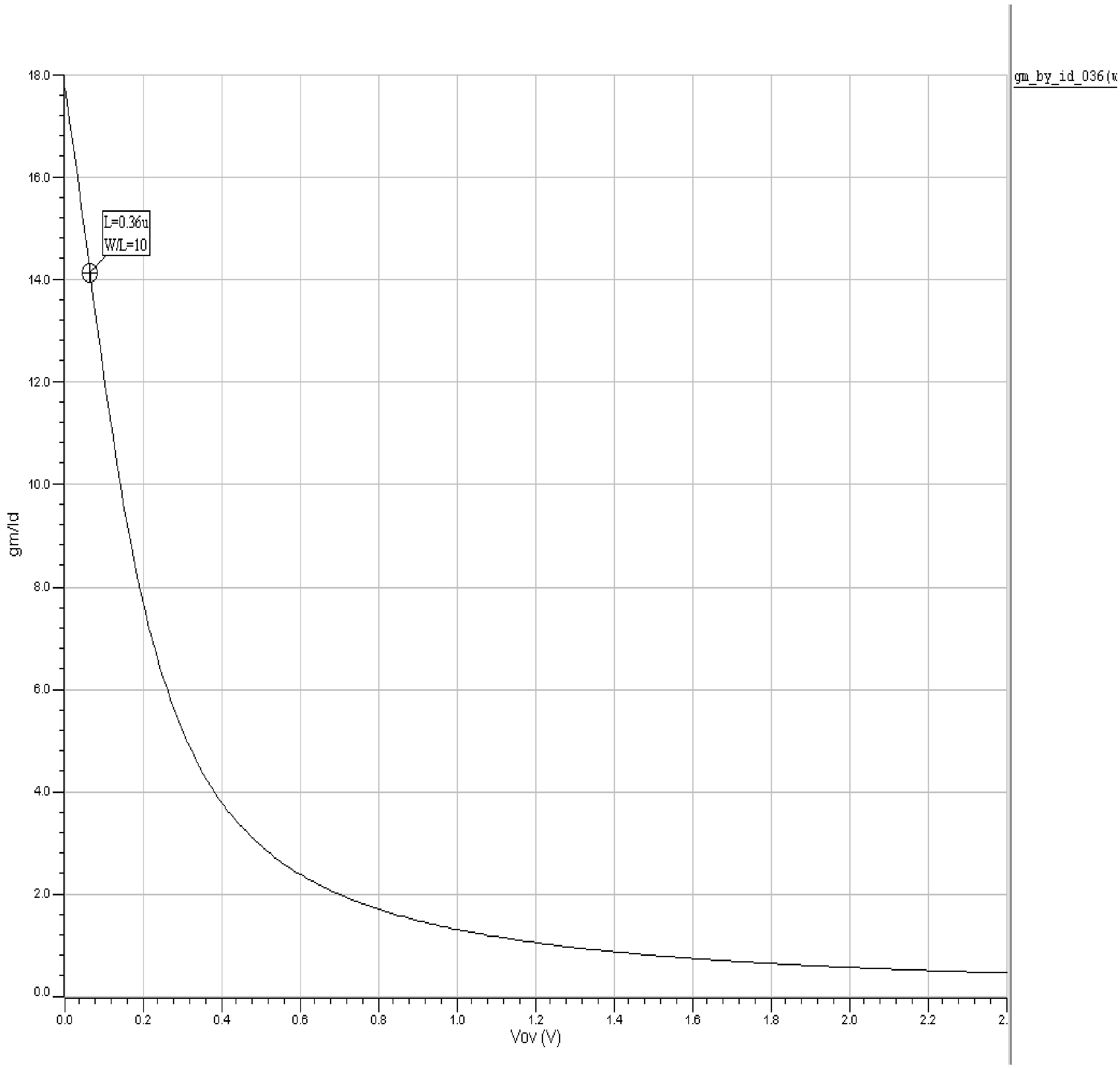
gm*r_0 Vs Vds

3. gm/Id Plots

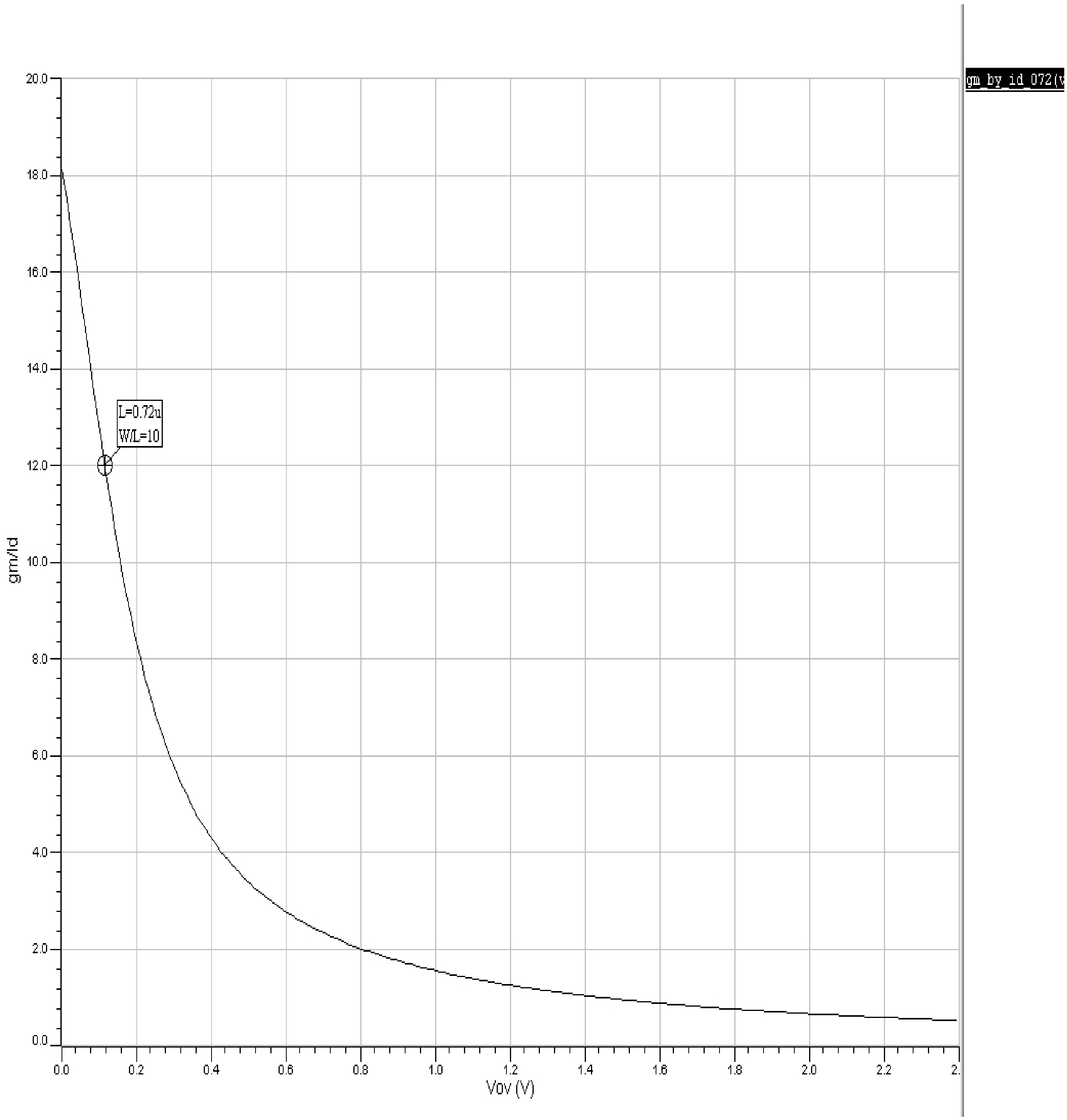
A comparative plot for gm/Id Vs Vov is given below:



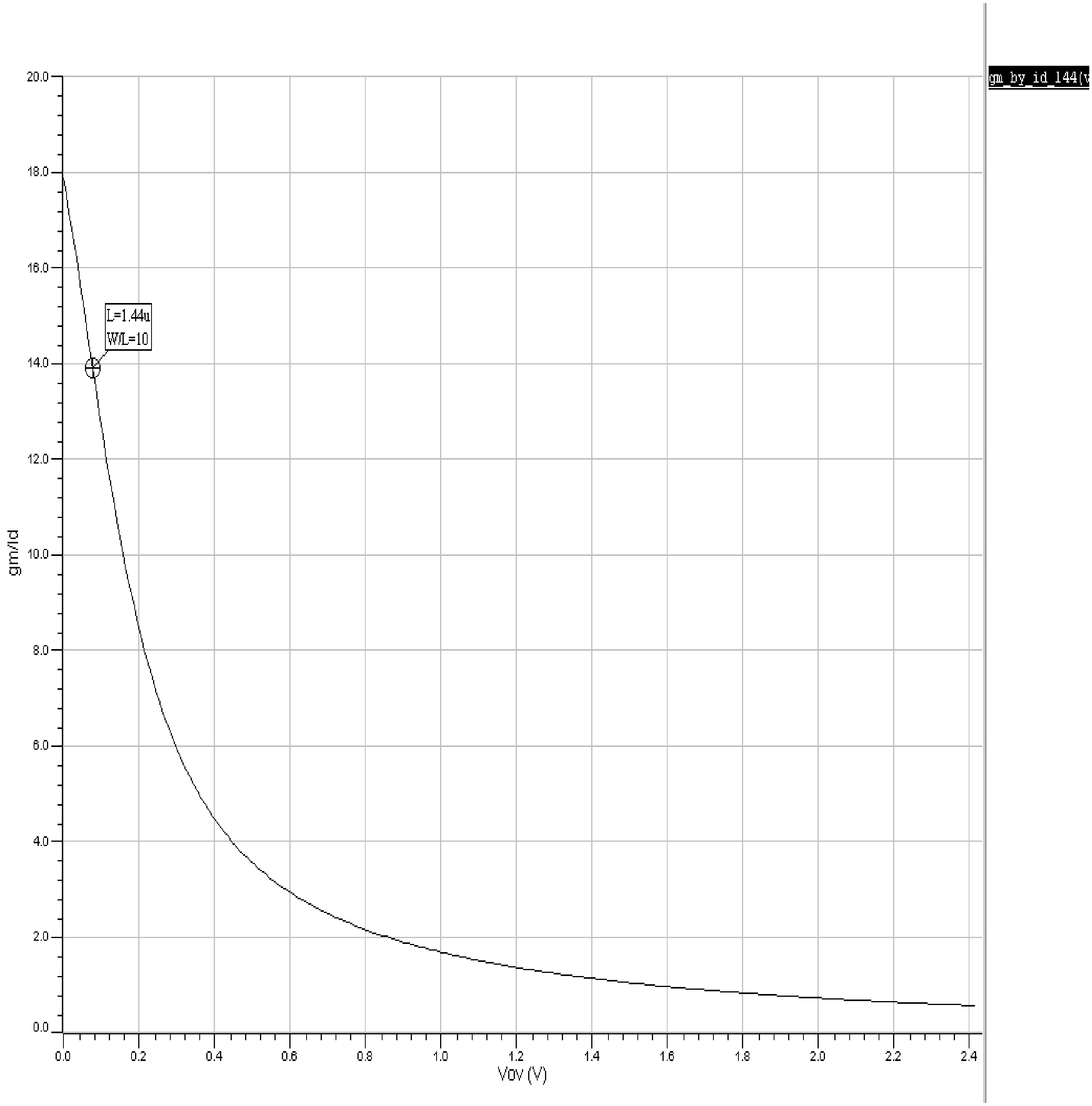
Since gm/Id Vs Vov plots are very important in the design procedure, Separate plots for each L have been generated.



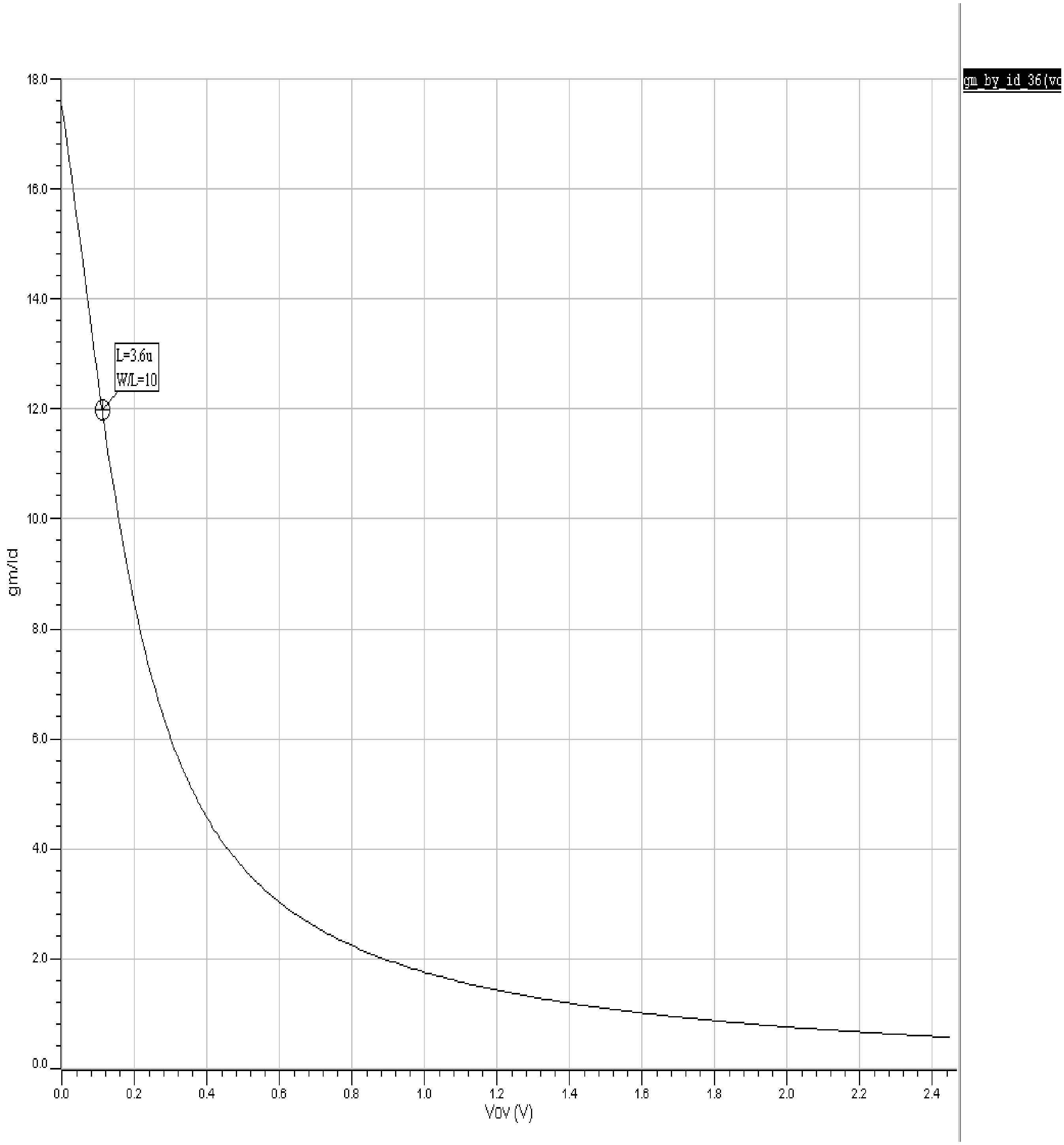
gm/Id Vs Vov (L=0.36 m)



gm/Id Vs Vov (L=0.72 m)



gm/Id Vs Vov (L=1.44 m)

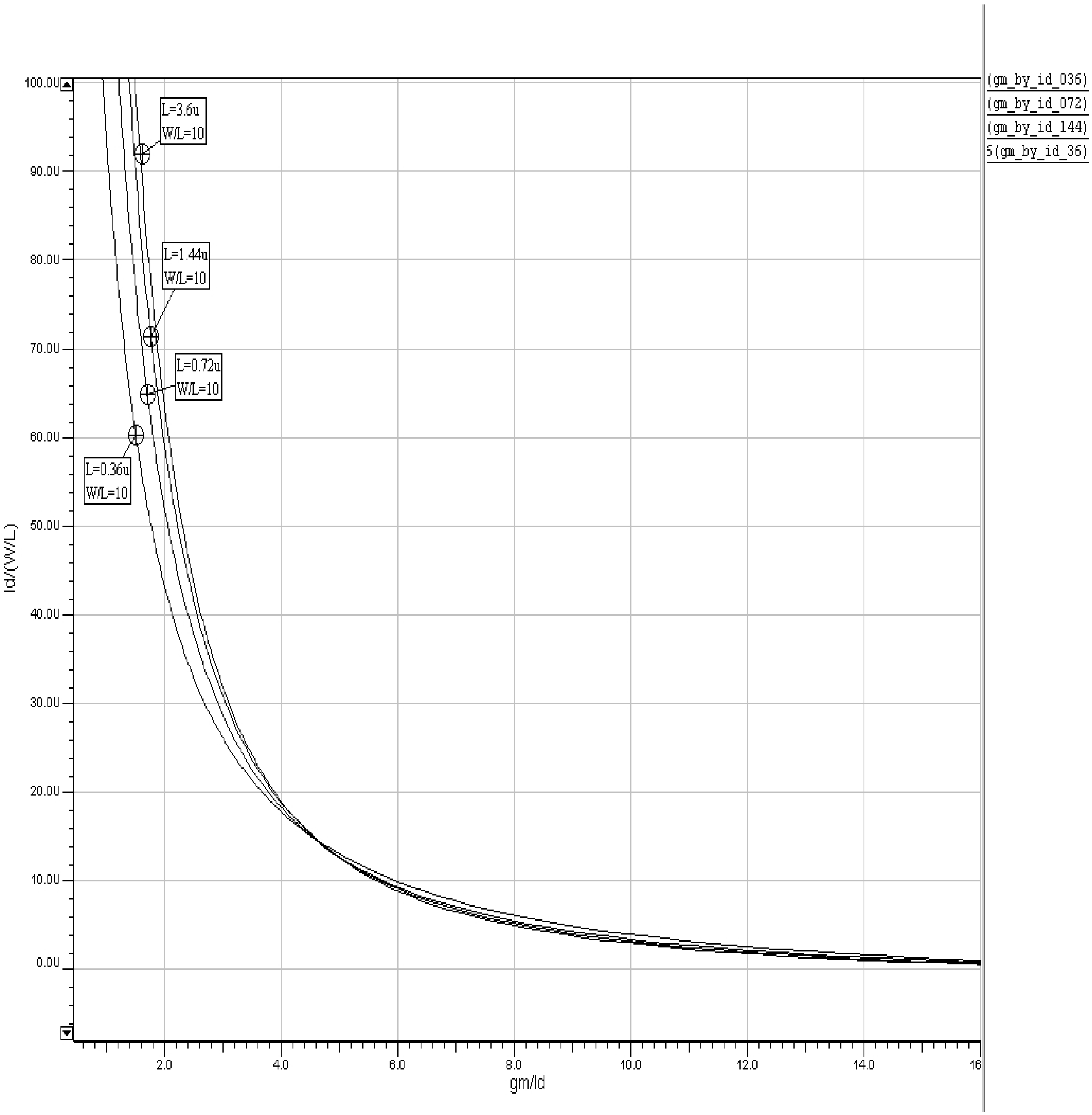


gm/Id Vs Vov (L=3.6 m)

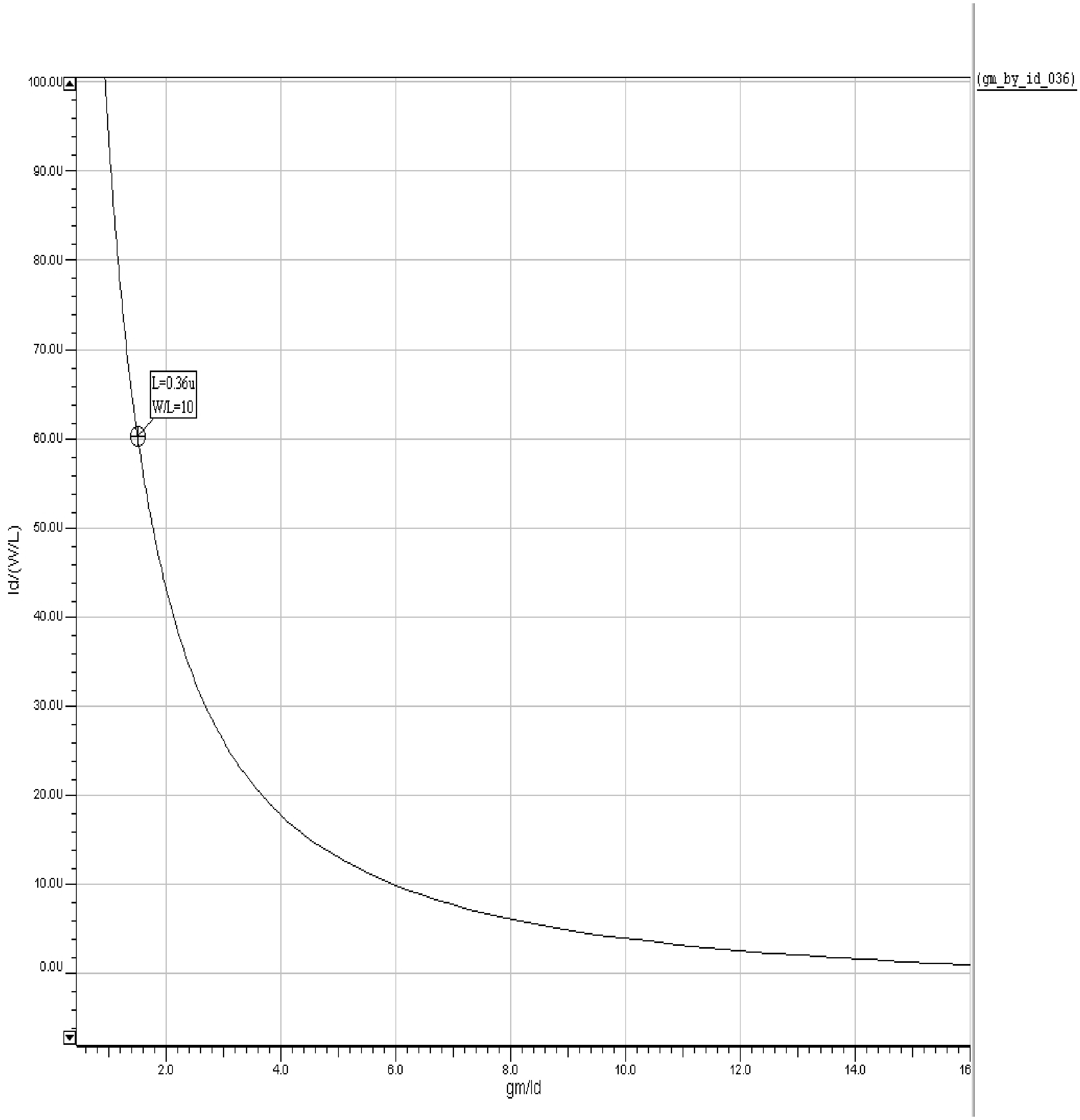
4. Id/ (W/L) Vs gm/Id Plots

These plots help in determining the required W/L for a given current. If we have chosen the gm/Id values, we can choose the aspect ration of the MOST from these plots.

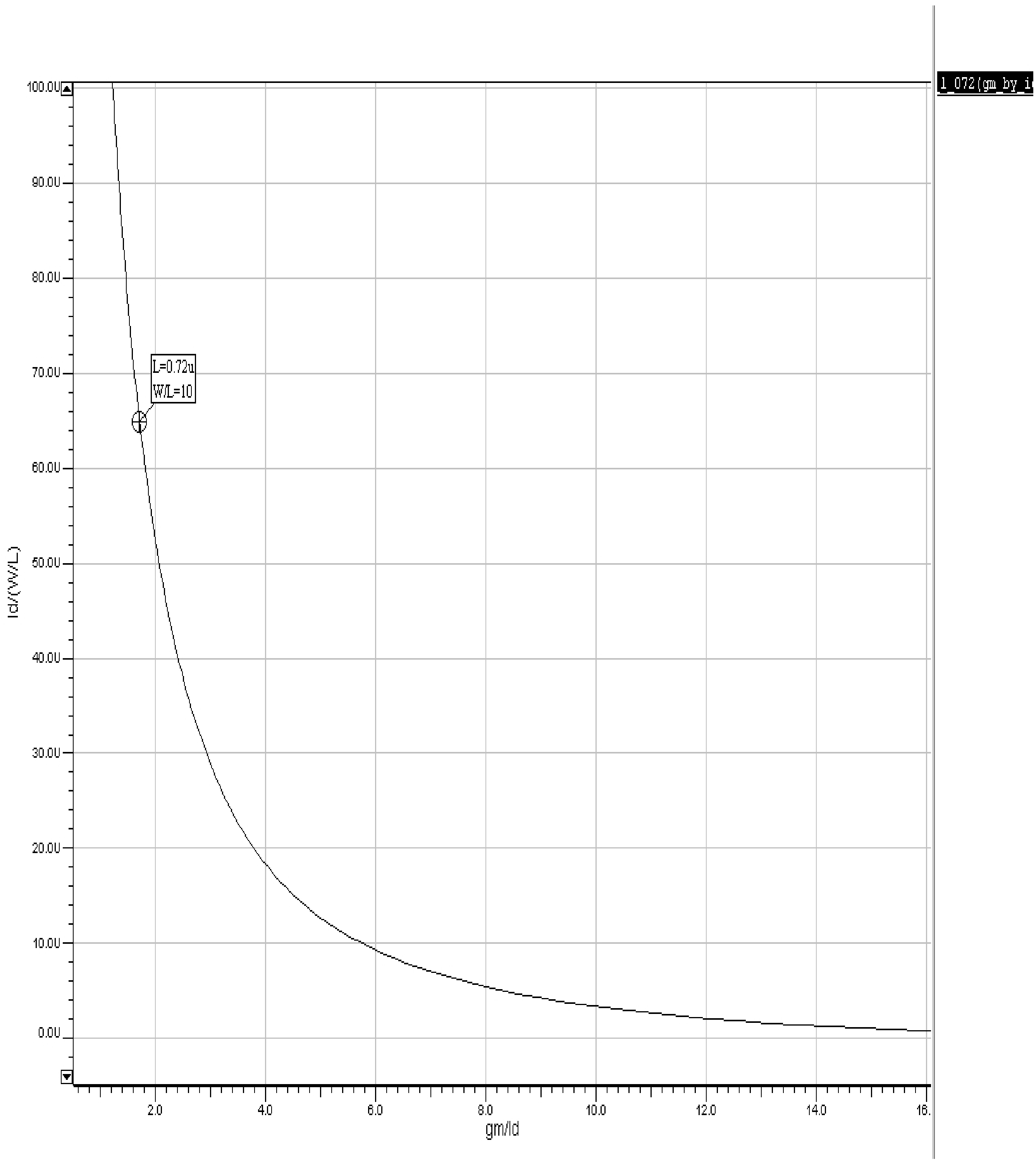
First, a comparative plot is shown. Here L varies from 0.36 m to 3.6 m.



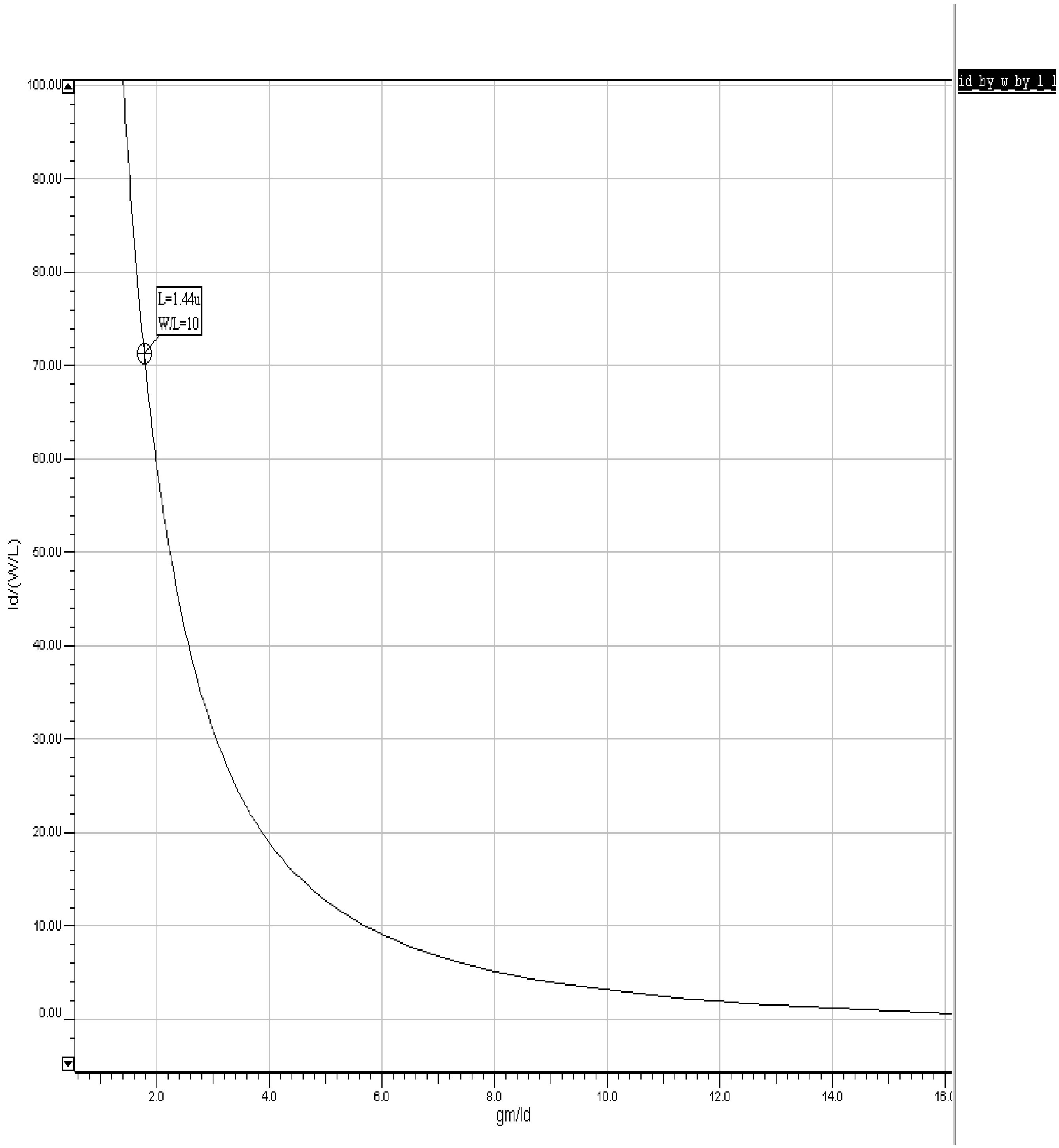
Separate Id/(W/L) Vs gm/Id plots have been generated for each L
(0.36 m,0.72 m,1.44 m,3.6 m)



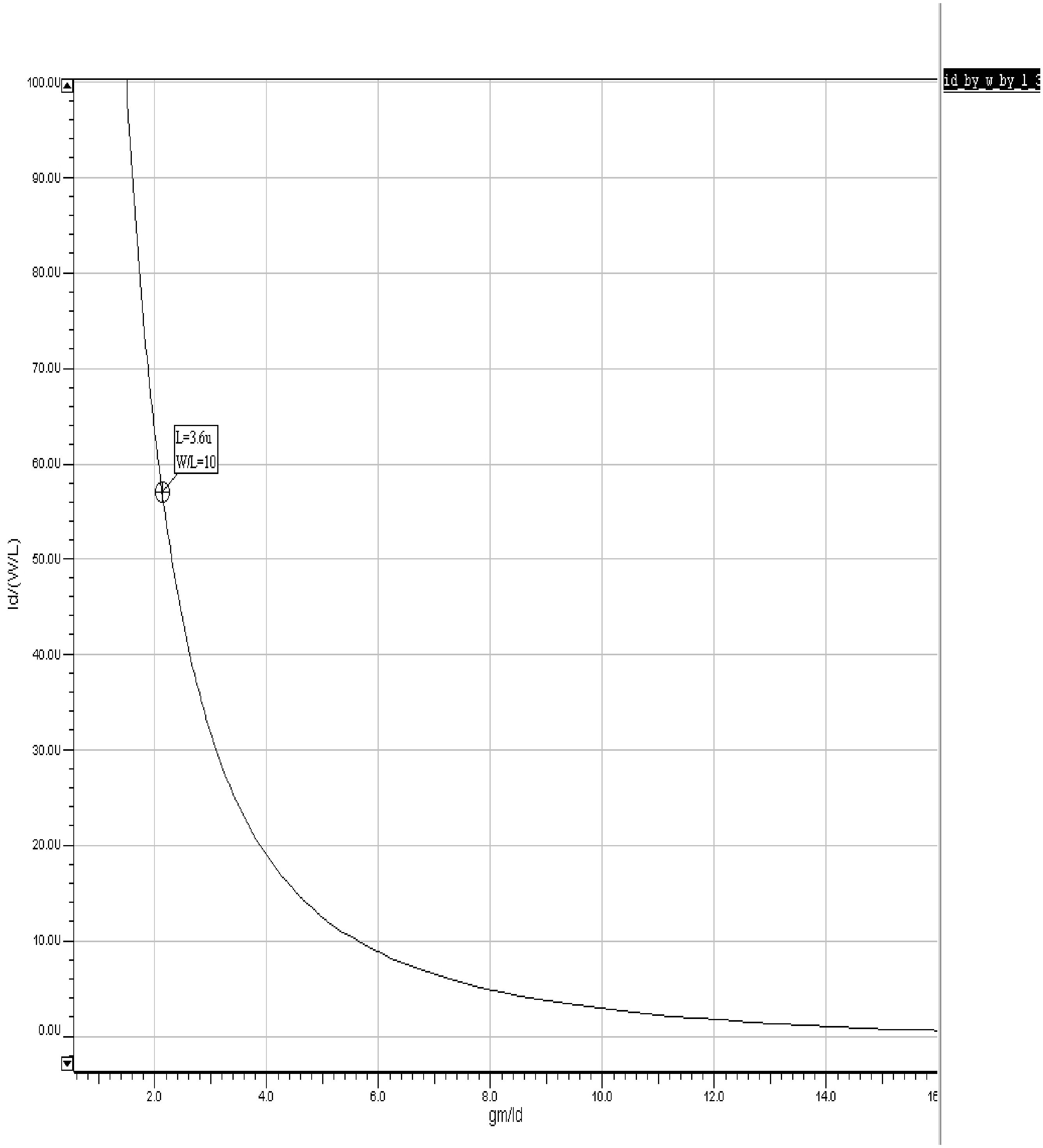
Id/(W/L) Vs gm/Id plot for L = 0.36 m



Id/(W/L) Vs gm/Id plot for L = 0.72 m



Id/(W/L) Vs gm/Id plot for L = 1.44 m



Id/(W/L) Vs gm/Id plot for L = 3.6 m

Design of Common Source and Differential amplifiers using Gm/Id method.

This part of the experiment was done using TSMC 0.25µm technology files.
So the Gm/Id plots given previously were not used.
Library used is:

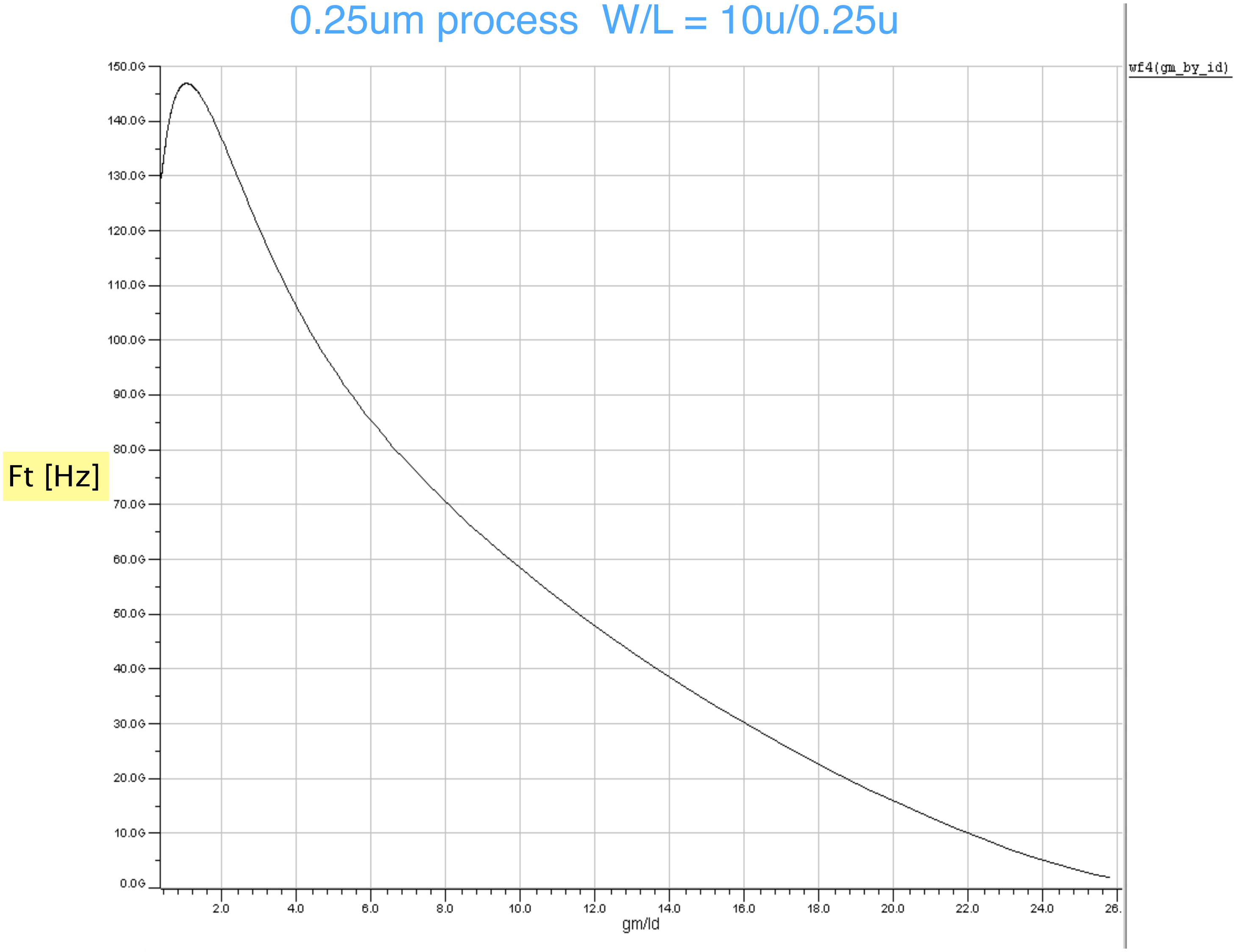
/edatools/dk/tsmc025/models/eldo/logic025.eldo

Gm/Id plots for this technology have been given below.
These plots will be used for designing the amplifiers in the subsequent stages.
W/L = 10µ/0.25µ

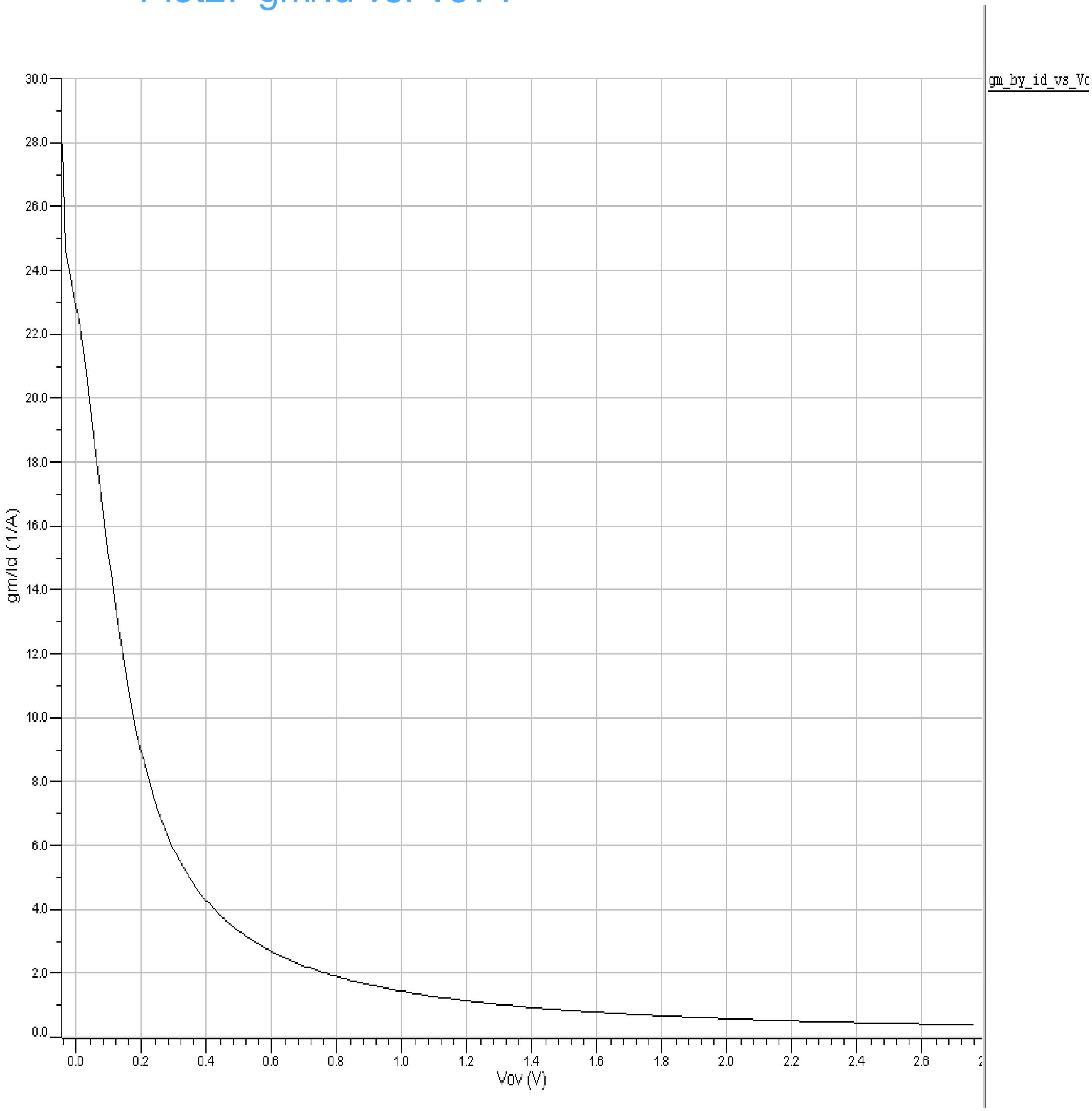
Plot 1:
F_T Vs gm/Id

GBW (Ft) vs. gm/Id

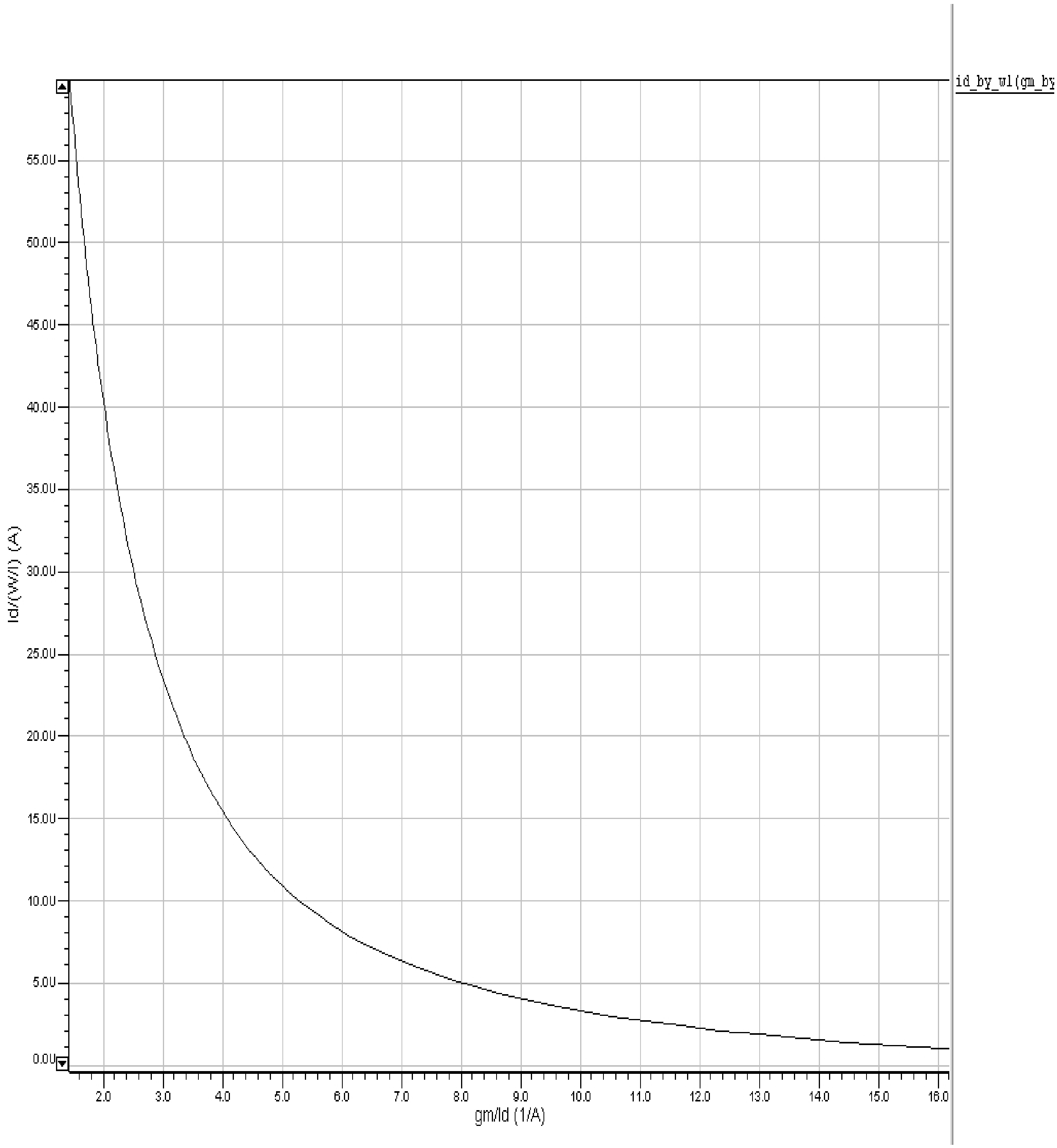
0.25um process W/L = 10u/0.25u



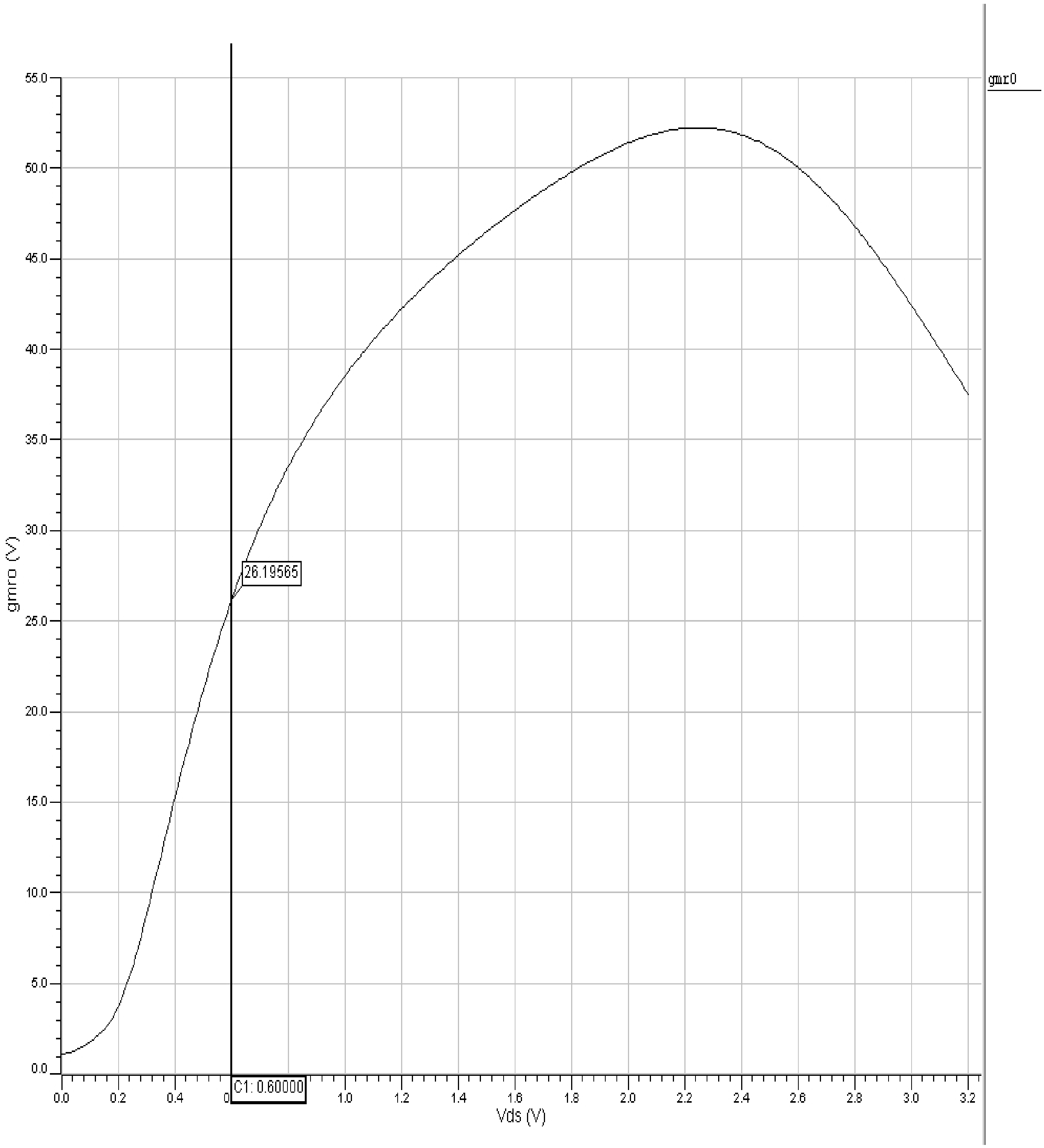
Plot2: gm/Id vs. Vov :



Plot 3:
Id/(W/l) Vs Gm/Id

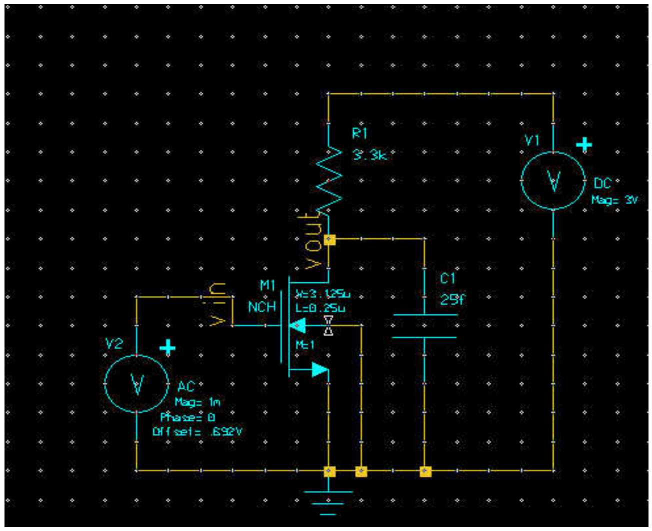


Plot 4:
$Gm*r_0$ Vs Vds



Design of Common Source Amplifier

The circuit diagram is given below.



Design for Maximum Gain

When designing for maximum gain, we need to get the maximum gm possible, since the gain of CS amplifier is simply -gm*R_L. Apart from increasing gm, R_L can also be increased, but in case of a resistive load, the resistance will be set be the output common mode voltage requirements.

From the gm/Id Vs Vov plot, we can see that to obtain higher transconductance efficiency, we need to work at lower overdrive voltages. At the same time, the overdrive voltage cannot be arbitrarily small otherwise the W/L of the transistor will be very large.

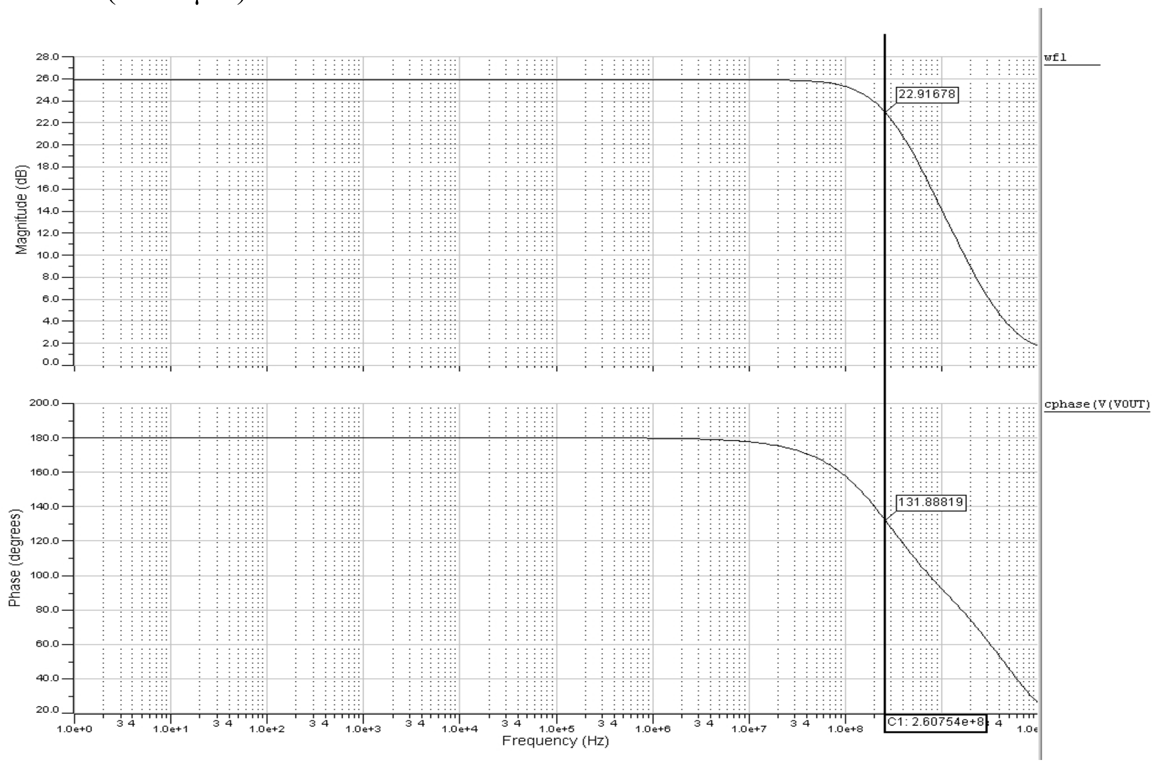
So we select a gm/Id value of 15 from this plot and read the corresponding Vov.

Next, we refer to the Id/(W/L) Vs gm/Id plot and read the Id/(W/L) value from it.
Id/(W/L) = 1.6µ (approximate value)

Setting Id= 100µA,
we get W/L = 60
If L= 0.5µm, W= 30µm
To get a 1.0v as output common mode voltage,
R_L = (3-1)/100µA = 20K

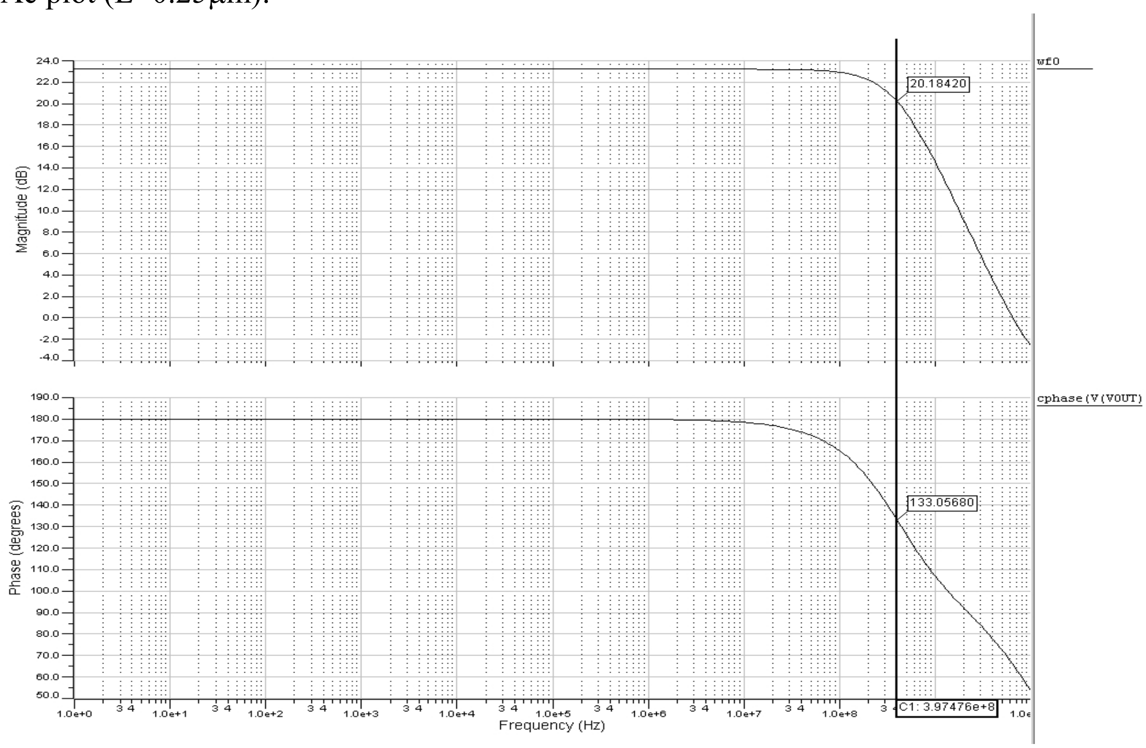
The simulation results using these values are shown below:
Note that, according to the gm*r_0 plot, the maximum gain achievable is around 50 v/v but we are getting only about 20 v/v. This is because R_L is much smaller compared to r_0.

Ac Plot (L=0.5µm):



Gain = 19.95 v/v -3dB frequency = 260MHz

Ac plot (L=0.25µm):



Gain = 14.1 v/v -3dB frequency = 397MH