Board Design Guidelines for PCI Express™ Architecture

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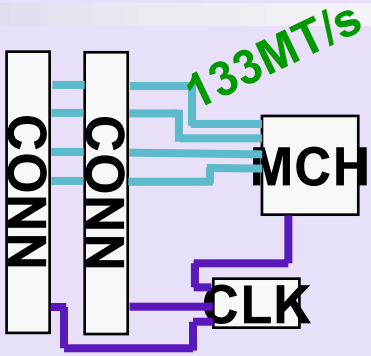
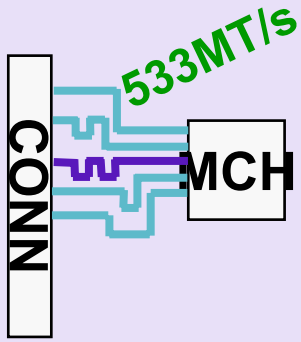
Agenda

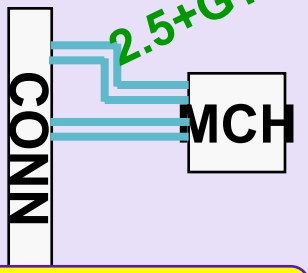
- Background
- Layout considerations
- System board requirements
- Add-in card designs
- Signal validations
- Summary

Bus Topology Evolution

- PCI common clock
  - ✓Meet setup/hold timing
  - ✓Multi-drop parallel I/O
- AGP source synchronous
  - ✓Single strobe, multiple data
  - ✓Match all data to strobes
- PCI Express* serial differential
  - ✓Embedded clock
  - ✓Point-to-point, match per data pair only
  - ✓Longer route, creative device placement

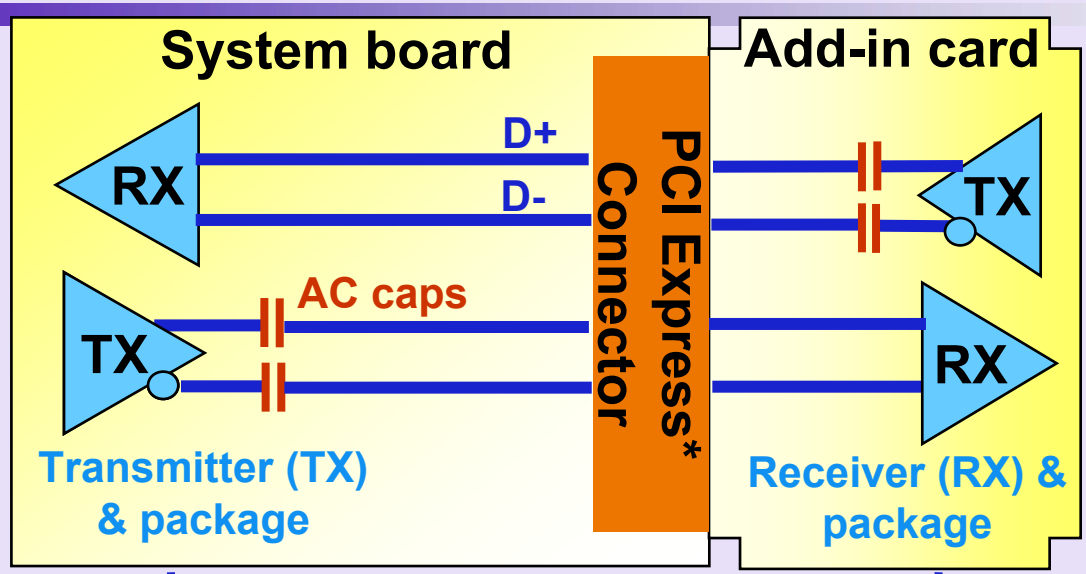




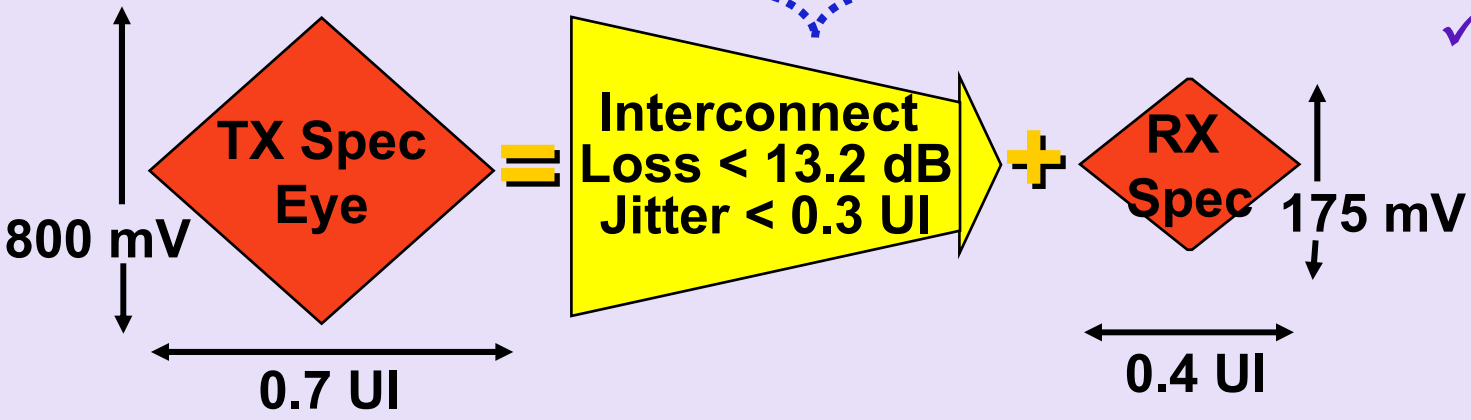


PCI Express* pt-to-pt routing is straightforward

Serial Differential



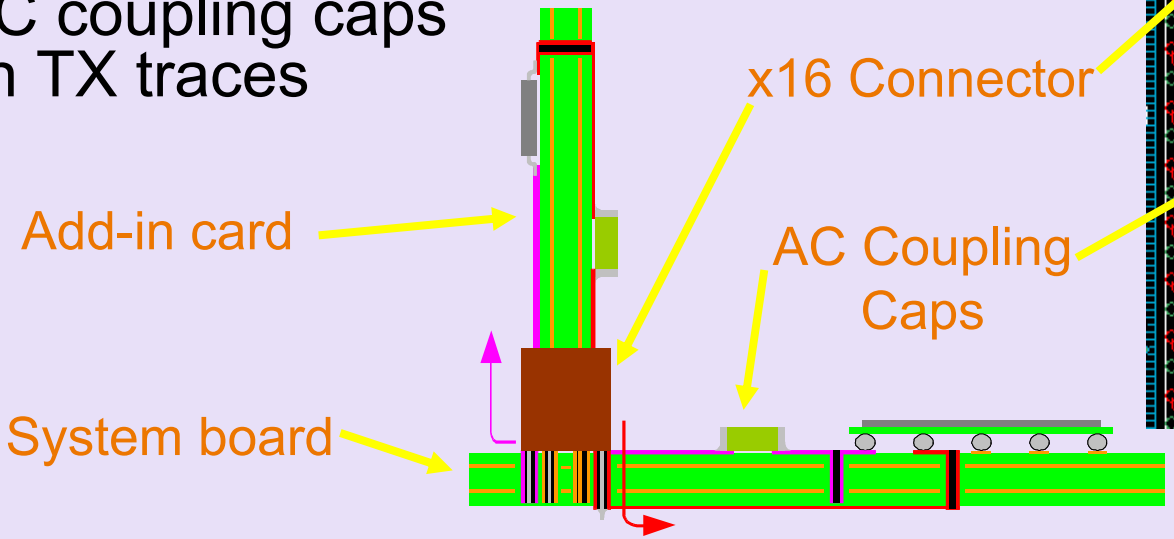
- ✓Diff. pairs
- ✓AC coupled
- ✓Lane-to-lane de-skew
- ✓Polarity inversion
- ✓On-chip equalization
- ✓On-chip terminations

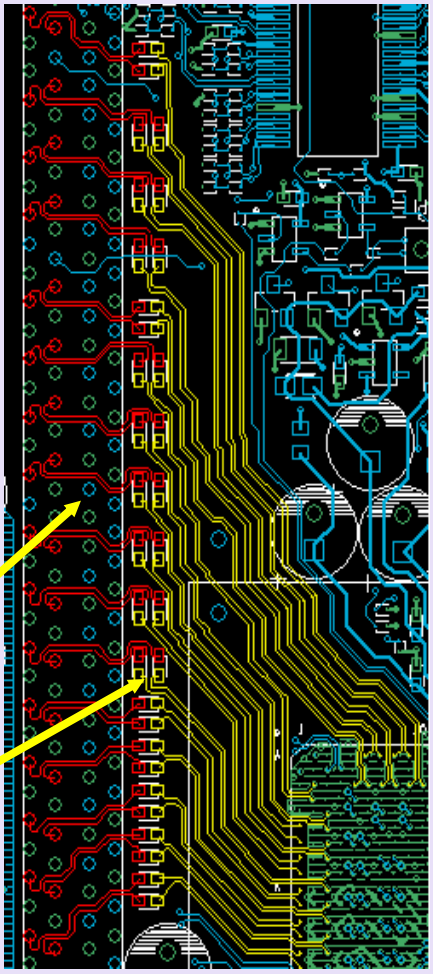


UI = Unit Interval as defined in PCI Express* Base Spec

PCI Express* Routing

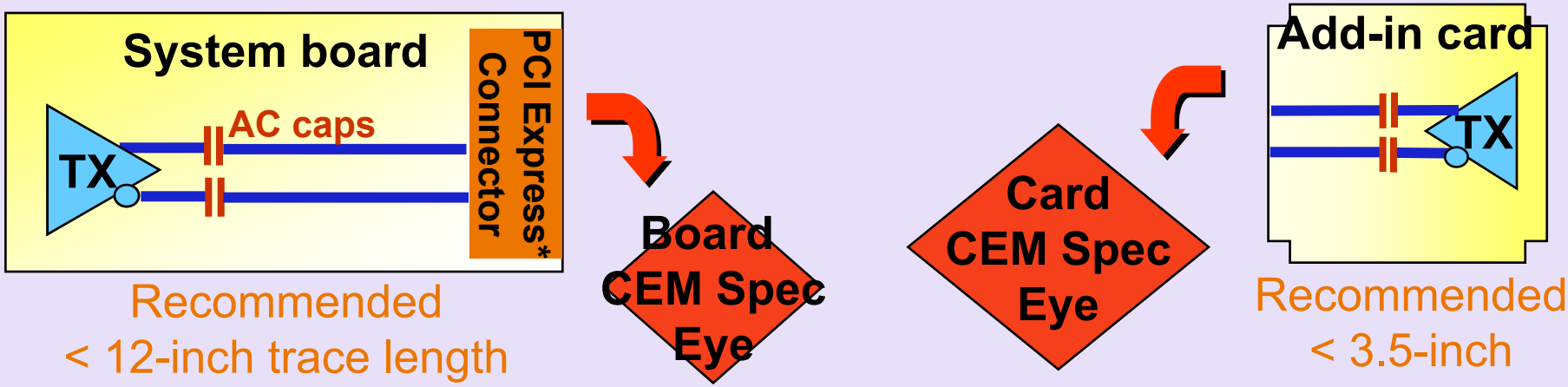
- Trace length matching between pairs is not required
  - ✓Embedded clock & lane-to-lane de-skew simplifies routing rules
- Longer system board traces possible
- TX usually route on top layer
  - ✓AC coupling caps on TX traces





CEM* Interconnect Budget

- CEM* (Card ElectroMechanical) Spec defines budget allocation
  - ✓*Loss* and *jitter* are key parameters
  - ✓Target impedance not as critical
  - ✓Maintain differential pair symmetry
  - ✓Design tradeoffs: loss vs. trace length, etc.



Manage loss and jitter to meet budget

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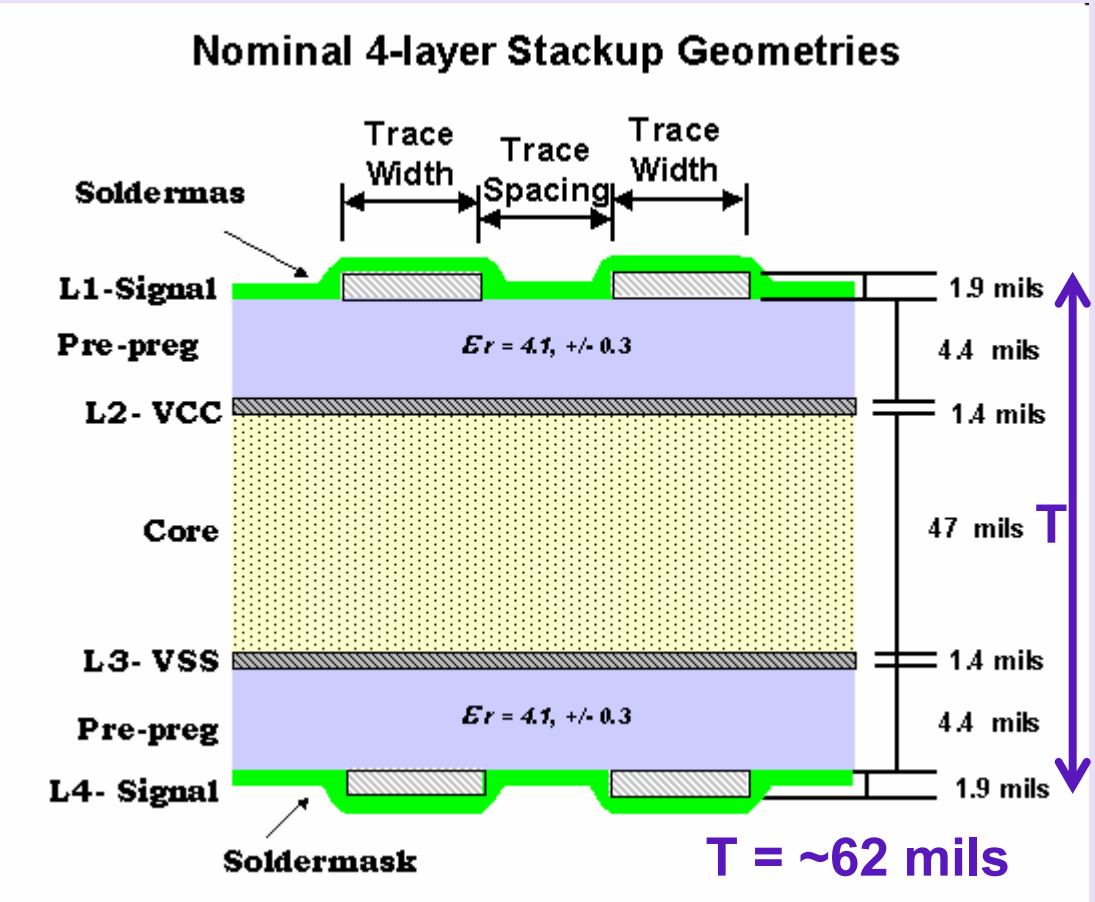
Stackup Design

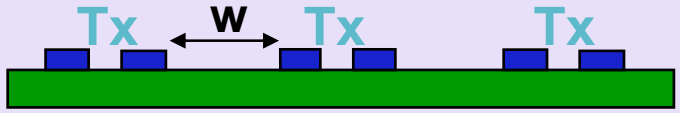
- No new PCB technology required
- Standard 4-layer stackup 0.062-inch thick PCB
- Microstrip ½ oz Cu plated or,
- Stripline 1 oz Cu (6+ layers)



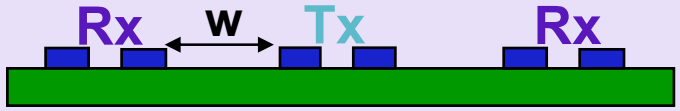
Follow simple layout rules & design tradeoffs

Trace Geometry & Impedance

- Wide pair-to-pair spacing ⇒ minimize crosstalk
  - ✓"Close" intra-pair spacing
- Same geometry for interleaved/non-interleaved
- Example impedance targets:
  - ✓Single-end Z_o of 60 Ω ±15%
  - ✓Differential Impedance of ~100 Ω ±20%

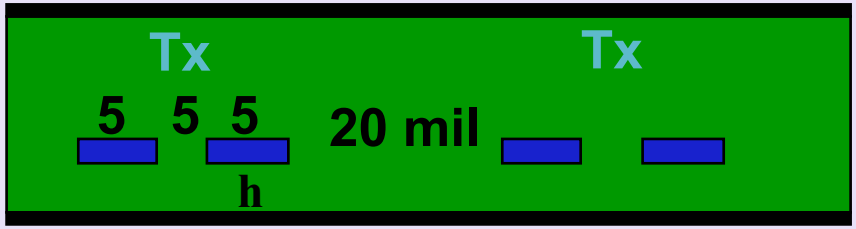


Non-interleaved topology example



Interleaved topology example

Microstrip



Stripline

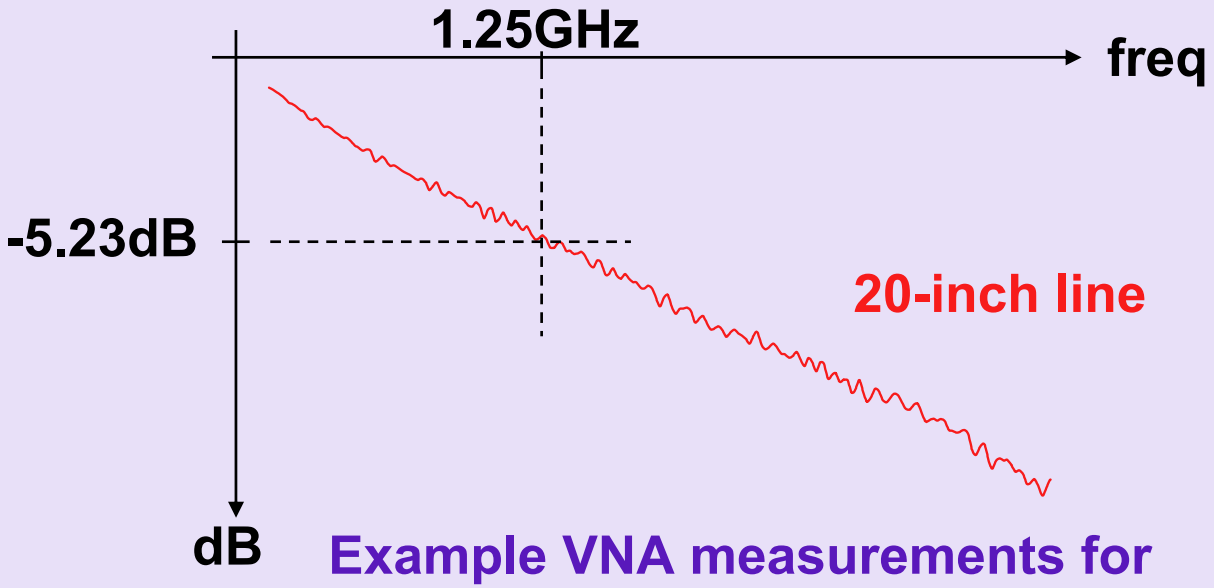
FR4 Loss Considerations

- Loss ↑ with …
- Stackup: FR4 material
  - ✓Narrow traces
  - ✓Copper roughness
  - ✓Dielectrics with more resin material
- Non-homogeneous dielectrics
  - ✓Localized Zo variation due to material weave
- Wide differential impedance variation on μstrip traces
  - ✓Etching and plating process

FR4 cross-section

Trace Length

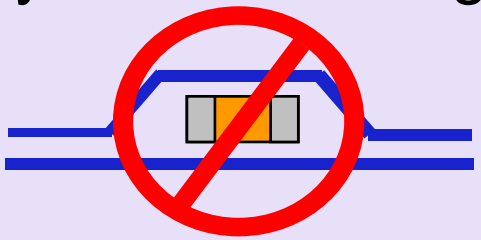
- Longer trace length ⇒ loss ↑
  - ✓~0.25 to 0.35 dB inherent loss per inch for FR4 microstrip traces at 1.25GHz
- Manage trace lengths to minimize loss
  - ✓Example: 12-inch board, 3.5-inch card lengths max

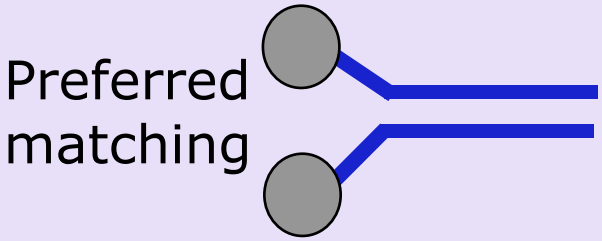


Example VNA measurements for differential μstrip trace insertion loss

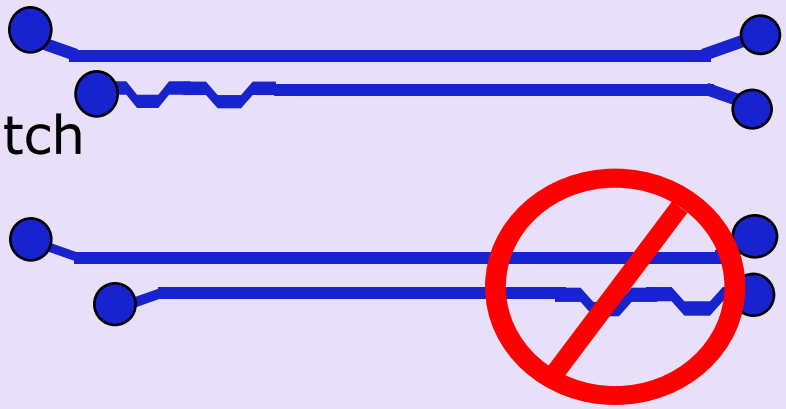
Trace Symmetry & Matching

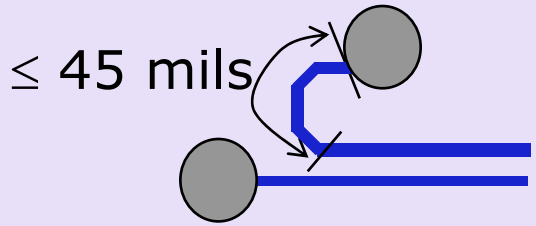
- No matching needed pair-to-pair
- Match within each differential pair per segment
  - ✓Match overall length ≤ 5 mils (recommended)
  - ✓Symmetric routing for each pair





Match
near
mismatch

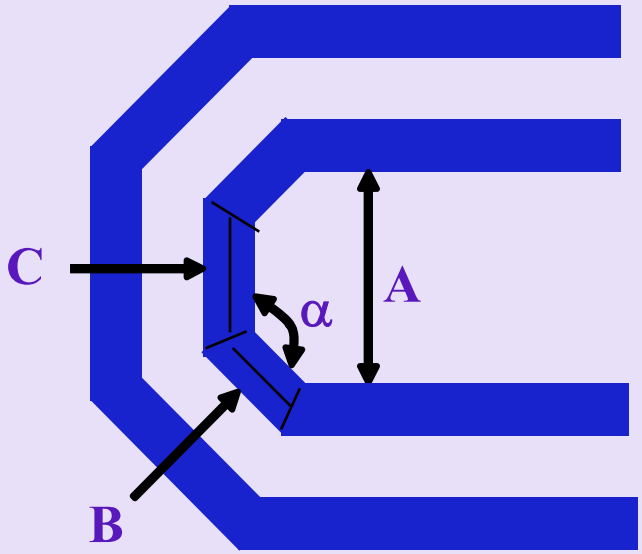


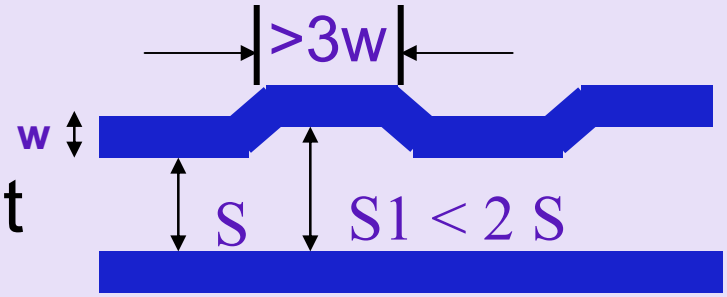


Alternative
matching

Bends and Small Serpentines

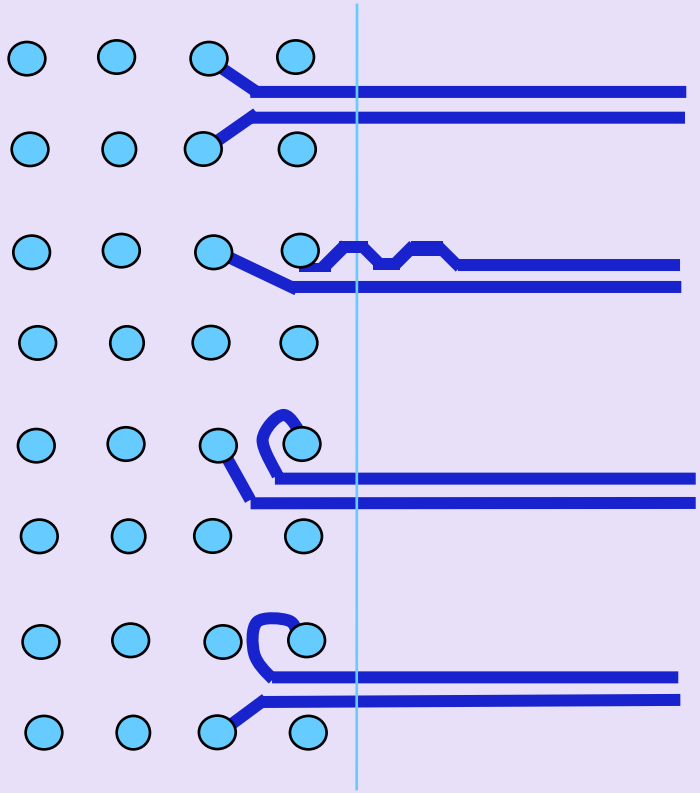
- Avoid tight bends
  - ✓No 90° bends; impact to loss and jitter budgets
- Keep angles >= 135° (α)
- Maintain adequate air gap
  - ✓ A >= 4x the trace width
- Lengths of B, C >= 1.5x the width of the trace
- Serpentines length is at least 3w for jog





Package Pin Field Breakout

- Use side-by-side breakout for package to maintain symmetry
- Avoid tight bends



Side-by-side **Best**

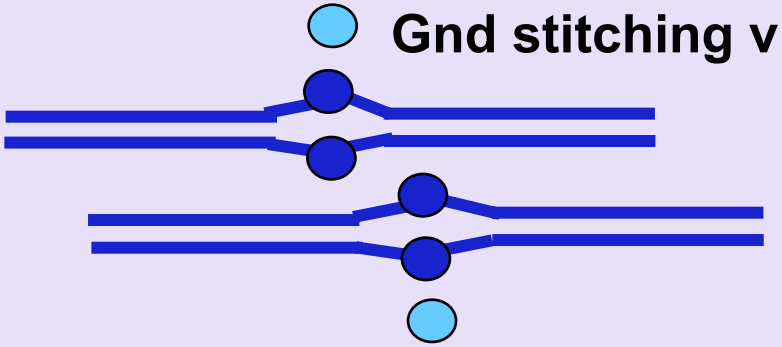
Adjacent w/ small serpentine **OK**

Adjacent w/ bend **Fair**

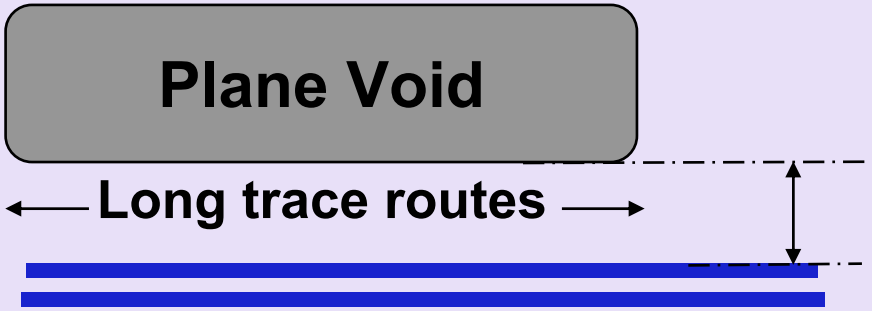
Diagonal routing **Fair**

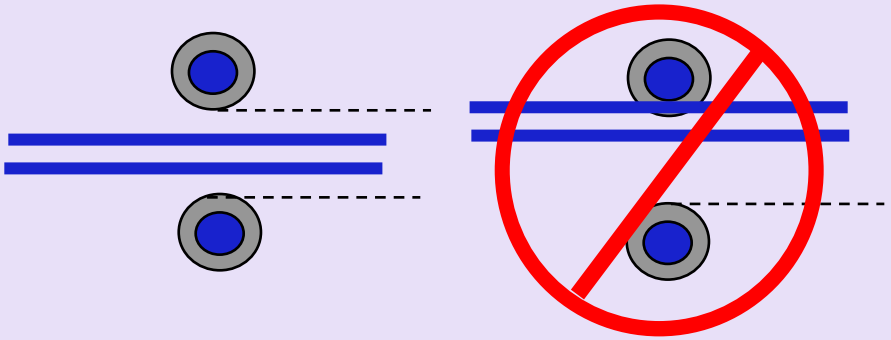
Reference Plane

- Full GND plane reference recommended
- Stitching vias required for layer transition



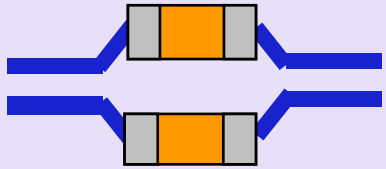
- Keep clearance from plane voids
- Avoid plane splits
- Avoid trace over anti-pad

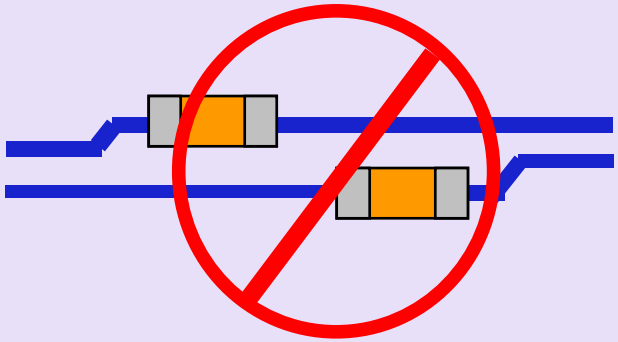




AC Coupling Capacitors

- Size: 0402 best, 0603 ok
- No 0805 size or C-packs
- Symmetric placement best

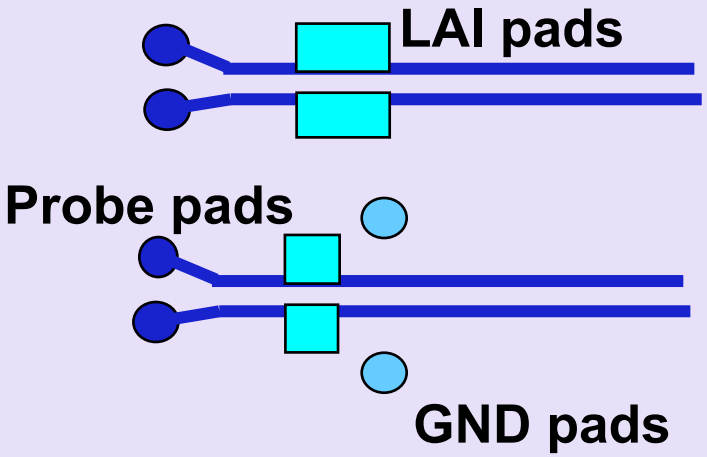


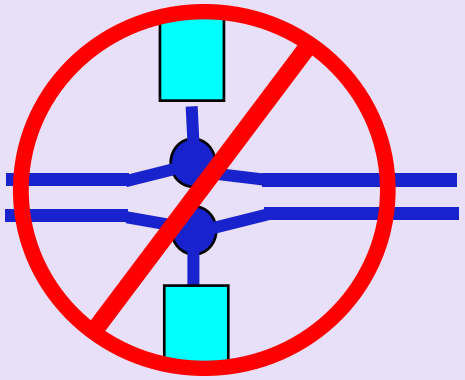


- Cap size: 0.1uF best
- Same sizes for both D+/D-
- Cap location:
  - ✓Along Tx pairs on system board
  - ✓Along Tx pairs on add-in card

Test Points & Vias

- Minimize via usage
  - ✓Up to 0.25 dB loss per via
  - ✓Use via pad size ≤ 25 mil, hole size ≤ 14 mil; standard anti-pad size of 35 mil
- Put test points or LAI pads in series (if used)
  - ✓No stubs
  - ✓Place symmetrically
  - ✓Provide GND pads for single-ended probing





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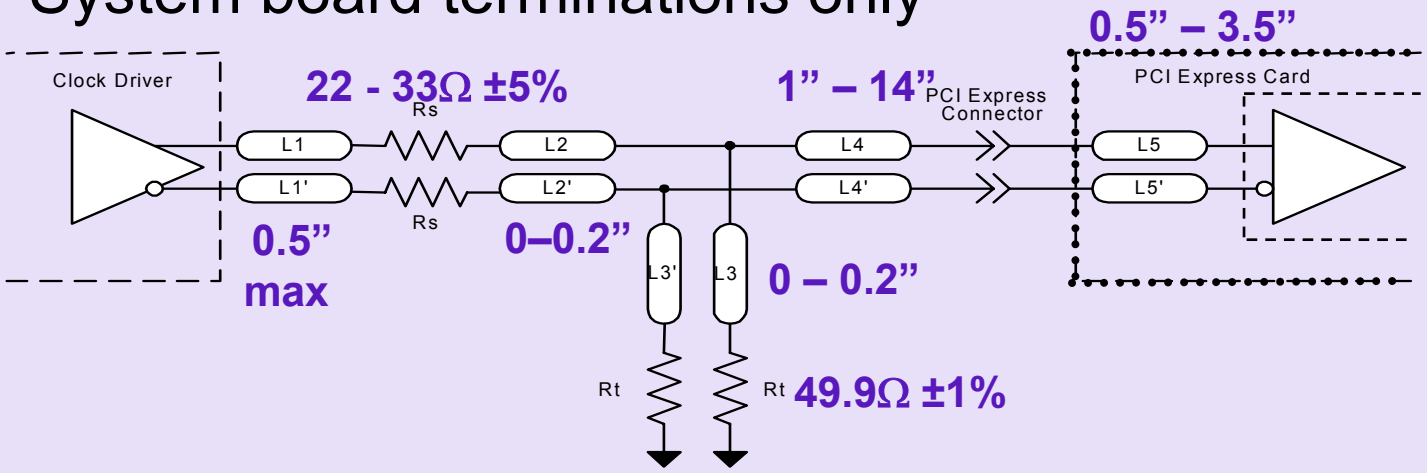
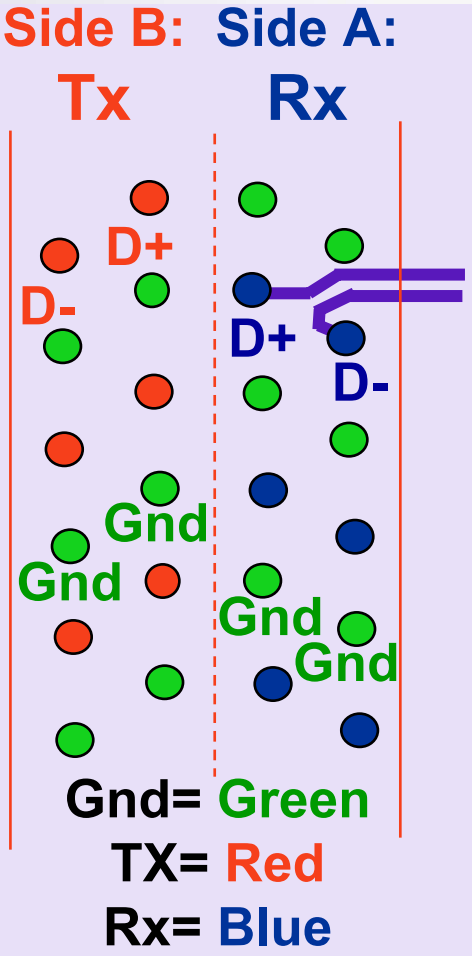
Reference Clock Routing

- Differential clock routing to each device and connector
  - ✓Use the same differential trace geometries
  - ✓Length matching to different devices *NOT* required!
- Clock driver requirements:
  - ✓100MHz with SSC support (e.g. CK410)
  - ✓Choose low jitter components
  - ✓System board terminations only



Connector Layout

- Connector with standard PTH
  - ✓Connector sizes: x1, x4, x8, x16
  - ✓Pinout optimized for differential routing & crosstalk reduction
  - ✓Polarity inversion allowed
- Loss & crosstalk part of system board budget



Improved PTH connector for PCI Express*

Power Rails

- Increased current capability for x16 connector
  - ✓Additional +12V pin; 1.1 Amp per pin capability
- Helpful grouping of power supply pins
  - ✓Eases power delivery routing
- ATX power supply connector
  - ✓ 2x12 (recommended)

Power Rail	75W Slot
+3.3V Voltage Tolerance Current	 ± 9% (max) 3.0 A (max)
+12V Voltage Tolerance Current	 ± 8% (max) 5.5A (max)
+3.3Vaux Voltage Tolerance Current: Wake Non-Wake	 ± 9% (max) 375 mA (max) 20 mA (max)

Power Consumption

- CEM* Spec 1.1 allows for 75W cards
  - ✓Available for x16 connectors
  - ✓Allows for performance graphics cards
  - ✓75W can be fully drawn thru x16 connector
  - ✓Note: ≤ 25W at initial power-up
    (75W after configuration as a high power device)
- Up to 25W allowed for x1, x4, x8 cards

Connector Sizes	X1		x4/x8	x16	
Standard height	10 W[1] (max)	25 W (max)	25 W (max)	25 W[1] (max)	75 W (max)
Low profile card	10 W (max)		10 W (max)	25 W (max)	

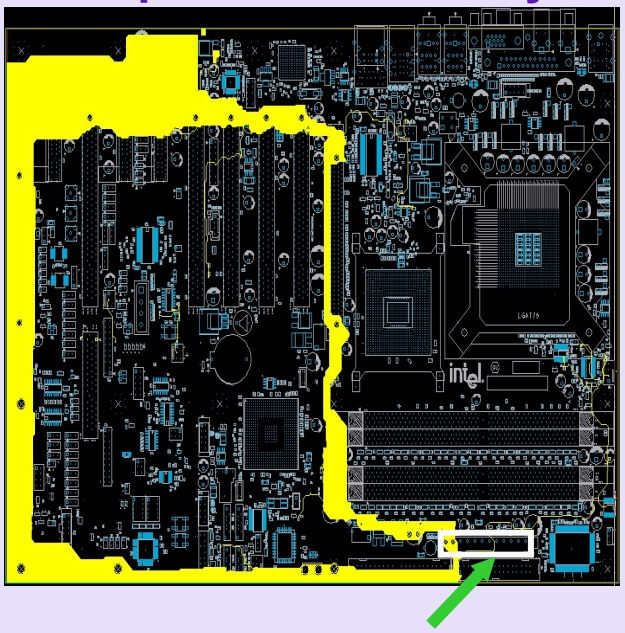
1. Max at initial power-up only.

PCI Express* spec support for 75W cards

Power Delivery

- Ensure +3.3V & +12V tolerances at add-in card
- Max of 2%~3% MB +12V voltage drop (e.g. 360mV)
  - ✓Typical power supply = ± 5% drop
  - ✓Balance trace width vs. length
  - ✓Example: 100 mils min trace width, ≤ 12” length for +12V with 1oz Cu
- Proper power decoupling
  - ✓Max current slew rate of 0.1A/μs
  - ✓Suppress high freq coupling noise
  - ✓Tune capacitor type/location to board needs

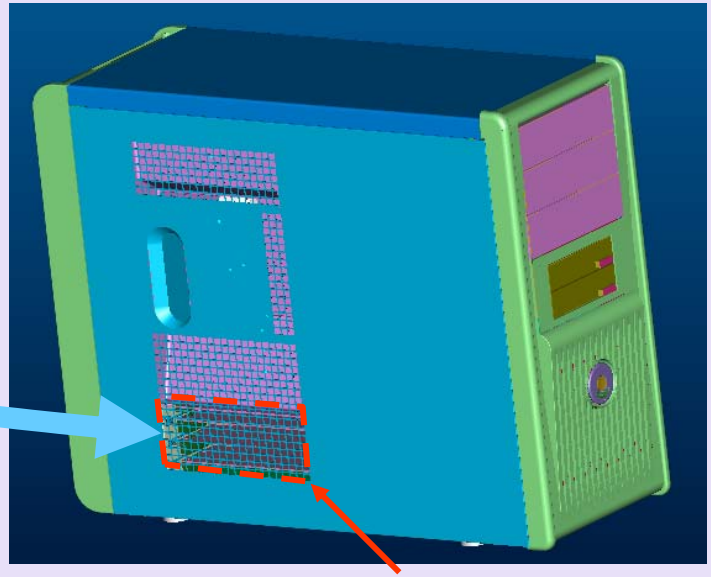
Example uATX +12V layout



2x12 Power Supply Connector

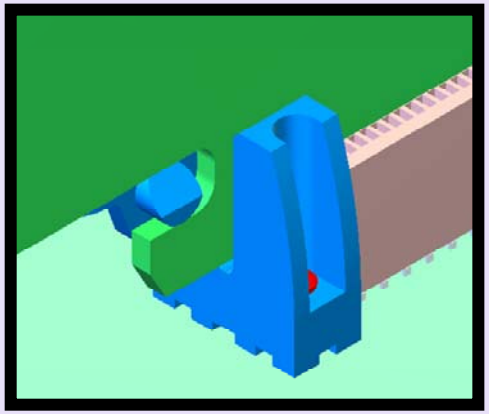
Thermal & Acoustic

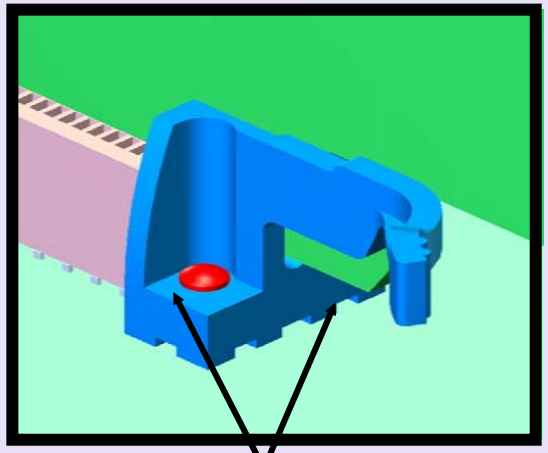
- Platforms need to deliver cool air to x16 slot
  - ✓Use side panel vents, ducting
  - ✓75W card recommendation: ≤ 55°C air temp at graphics card fan intake
  - ✓Use larger fans for better acoustics

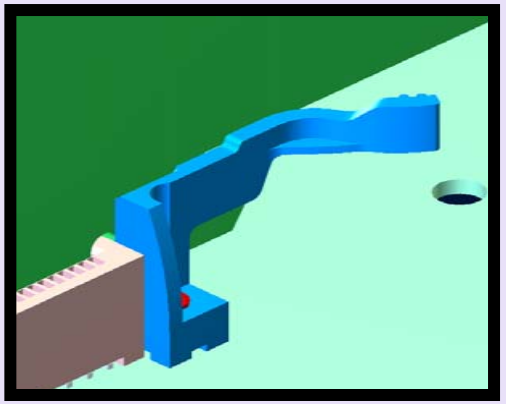


Card Retention

- Card allows for chassis & system board retention
  - ✓ Fixed card height & keep outs
  - ✓ "Hockey-stick" near edge fingers
- 75W Gfx design guideline for retention solution
  - ✓ Clip for system board, card "hockey-stick"
  - ✓ Supports up to 350g for 75W cards
- OEMs free to innovate independent solutions







Requires two, 80-mil diameter holes

Power Delivery - 150W support

- Additional 2x3 power supply connector on graphics card for +12V
  - ✓Separate power planes from x16 connector's +12V planes on the graphics card
- Graphics card should meet safety certifications
- Features still being reviewed:
  - ✓Recommended current limiting at input of Voltage Regulators (VR) on graphics card
  - ✓Card tolerance to nominal input voltage variations between +12V rails
- Refer to PCI Express* High-End Graphics CEM Specifications

Card Retention - 150W support

- Card may use the space of adjacent slot
- Additional retention required for cards > 350 grams
- Hockey Stick feature on card is required on 75W cards but optional for High End Graphic cards.
  - ✓Ergonomic issue with double wide card. Limited access to release lever

High End Graphics Spec support 150W cards

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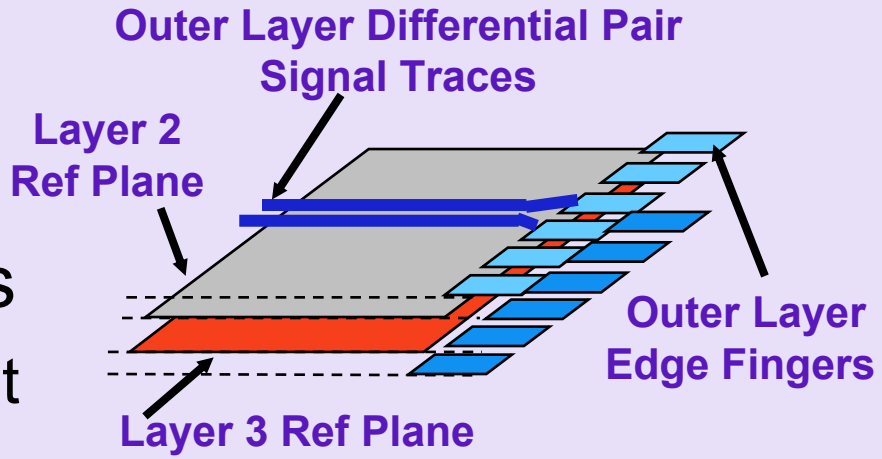
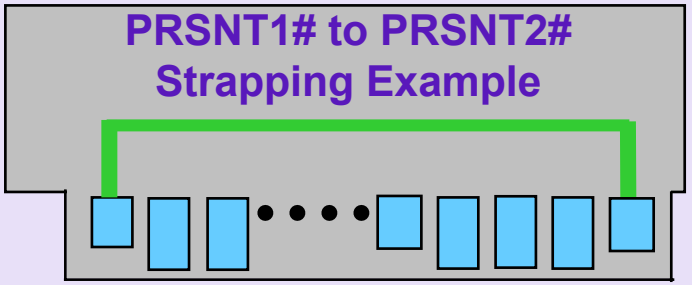
Card Edge Fingers

- Remove ref plane under edge finger pads
  - ✓Better impedance match
- PRSNT1#, PRSNT2# Pins
  - ✓1mm shorter: last-mate, first break Hot-Plug support
  - ✓Multiple PRSNT2# pins (x4,x8,x16 cards)
  - ✓Cards must strap PRSNT1# with furthest PRSNT2# signal
  - ✓*System board Hot-Plug support optional*

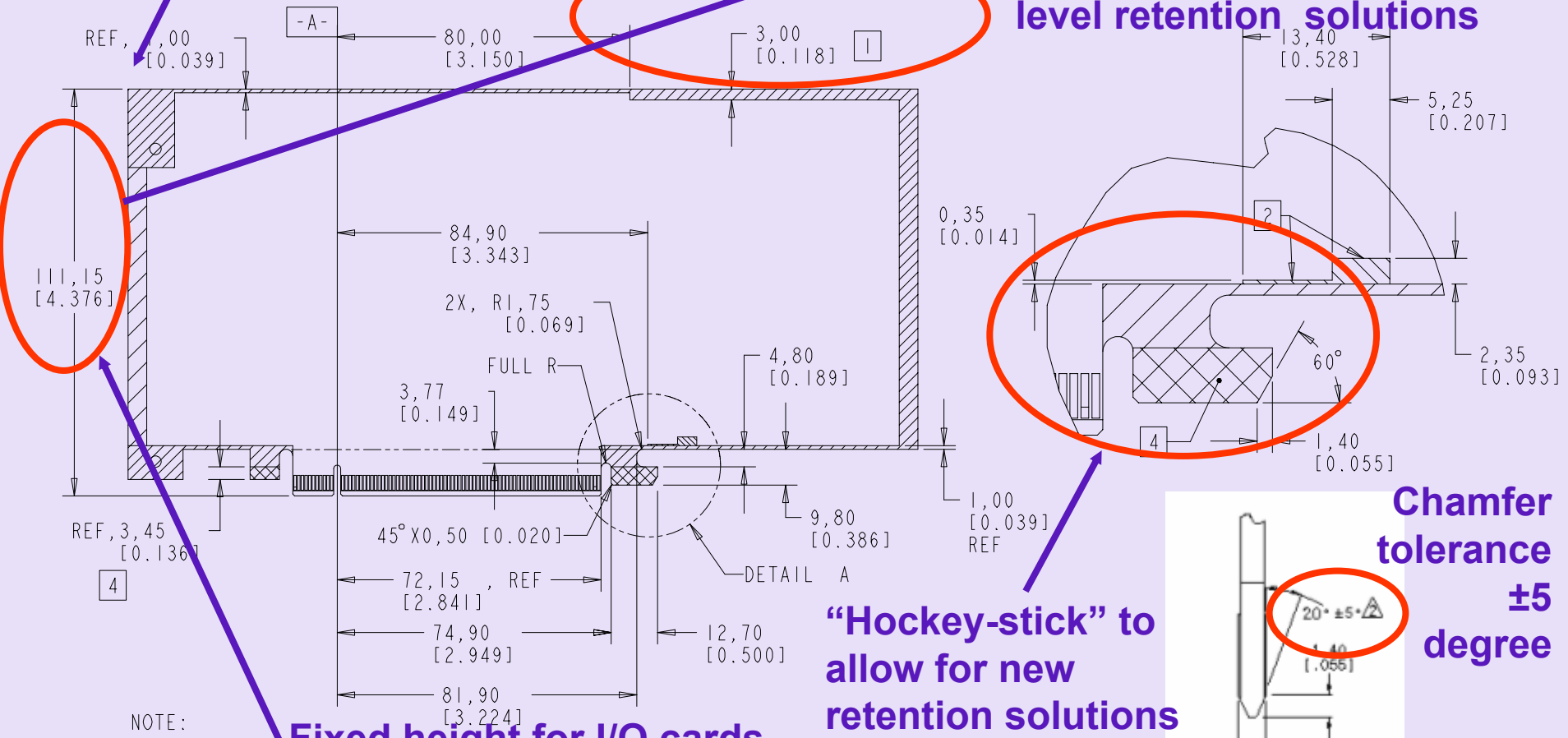




Card Physical Dimensions

End bracket

Top edge keep out and fixed height to enable chassis level retention solutions



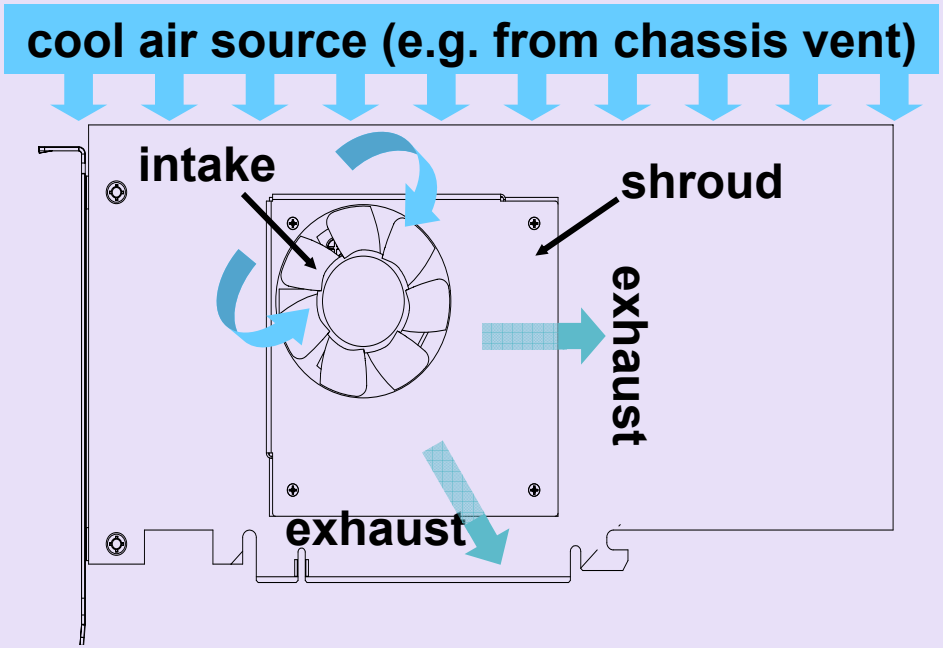
"Hockey-stick" to allow for new retention solutions

Chamfer tolerance ±5 degree

Fixed height for I/O cards (allowance for low profile compliance)

Card Thermal & Acoustic

- *Limit* heat re-circulated thru Gfx card heat sink
  - ✓Use shroud to separate fan intake and heat sink *exhaust*
  - ✓Place fan intake near air source- direct away the exhaust
  - ✓Reduce fan noise and low speed chatter
  - ✓Use diode and/or thermister for fan speed control



Card Thermal - 150W support

- Exhaust flow of graphic card needs to be managed
- Recommended that exhaust from graphic card exit to outside of typical ATX Chassis
- Recommended that graphic card manufacturer and system integrator work together to insure overall system performance

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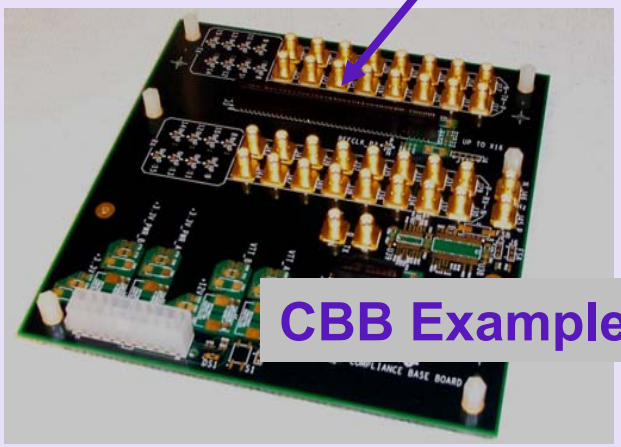
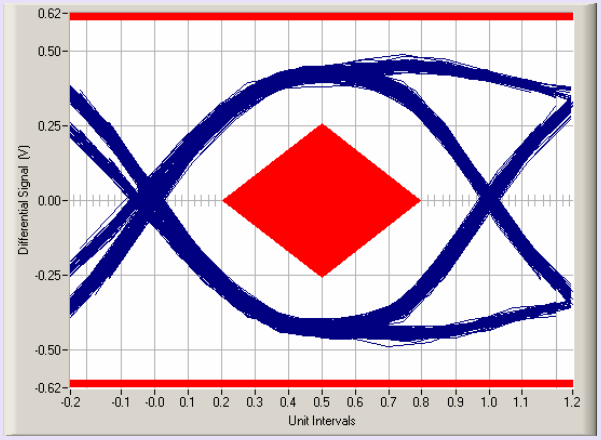
Compliance Measurements

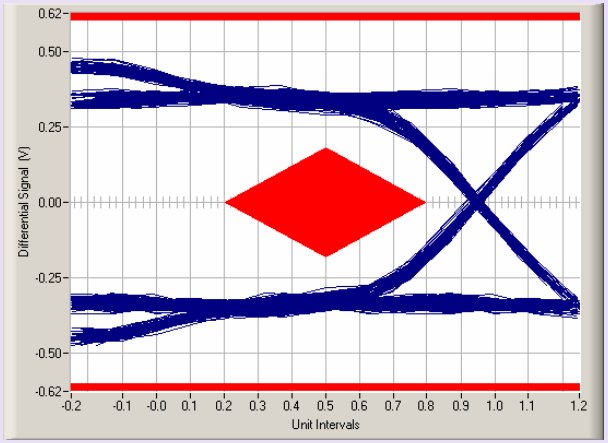
- PCI Express* devices generate compliance pattern per spec
- Signal validation using:
  - ✓ Compliance Base Board (CBB) for add-in cards
  - ✓ Compliance Load Board (CLB) for system boards
- Eye diagrams w/ real-time scope
  - ✓ 6+ GHz analog bandwidth
  - ✓ 20+ Gs sampling bandwidth
  - ✓ SIGTEST analysis software



Results Analysis

- Probe locations
  - ✓TX outputs w/ SMA cables (50Ω terminations at scope)
- SIGTEST software
  - ✓Create transition bit eye
  - ✓Create de-emphasized eye
- Pass/Fail:
  - ✓Max median-to-peak jitter
  - ✓Min eye voltage margin (high/low)





Validate eye diagrams using real time scope

Agenda

- ✓Background
- ✓Layout considerations
- ✓System board requirements
- ✓Add-in card designs
- ✓Signal validations
- Summary

Summary

- PCI Express* point-to-point layout is straightforward
- Manage loss and jitter from PCB to meet CEM* interconnect budget
- Follow basic layout rules and design tradeoffs to implement typical topologies
- Improved system & add-in card features for 75W & 150W cards support
- Validate compliance eye diagrams using compliance boards and real-time scope

Collateral

- Intel Developer Network for PCI Express*
  - ✓http://www.express-lane.org/
- Where attendees may get additional and updated information on PCI Express*
  - ✓http://www.pcisig.org

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