The Flipped Voltage Follower (FVF)

A useful cell for low-voltage, low-power circuit design

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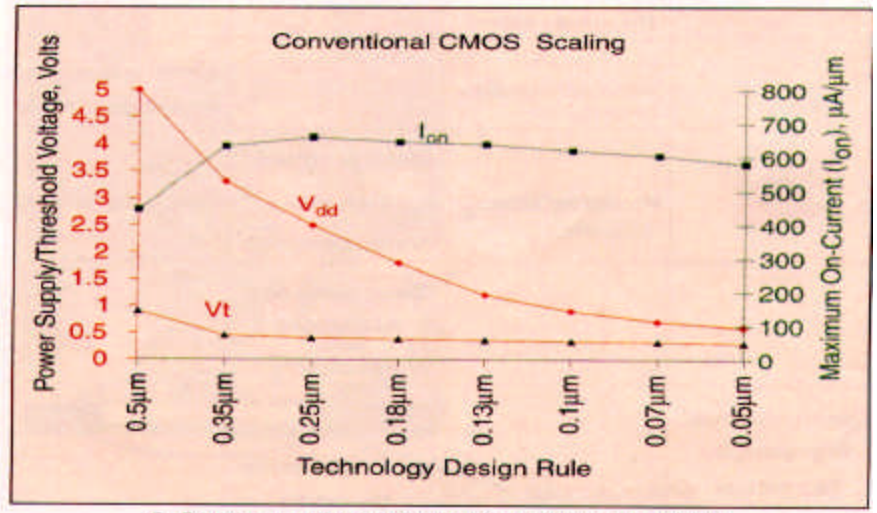
1. Introduction

- Portable and mobile, battery-operated devices.
- Power consumption in digital blocks is highly dependent on the supply voltage ($P \sim V_{DD}^2$). This forces to decrease the supply voltage in mixed-signals ASIC's.

- Downscaling of technology forces V_{DD} to decrease but V_T does not scale in the same way.



3. Power supply scaling and performance limits

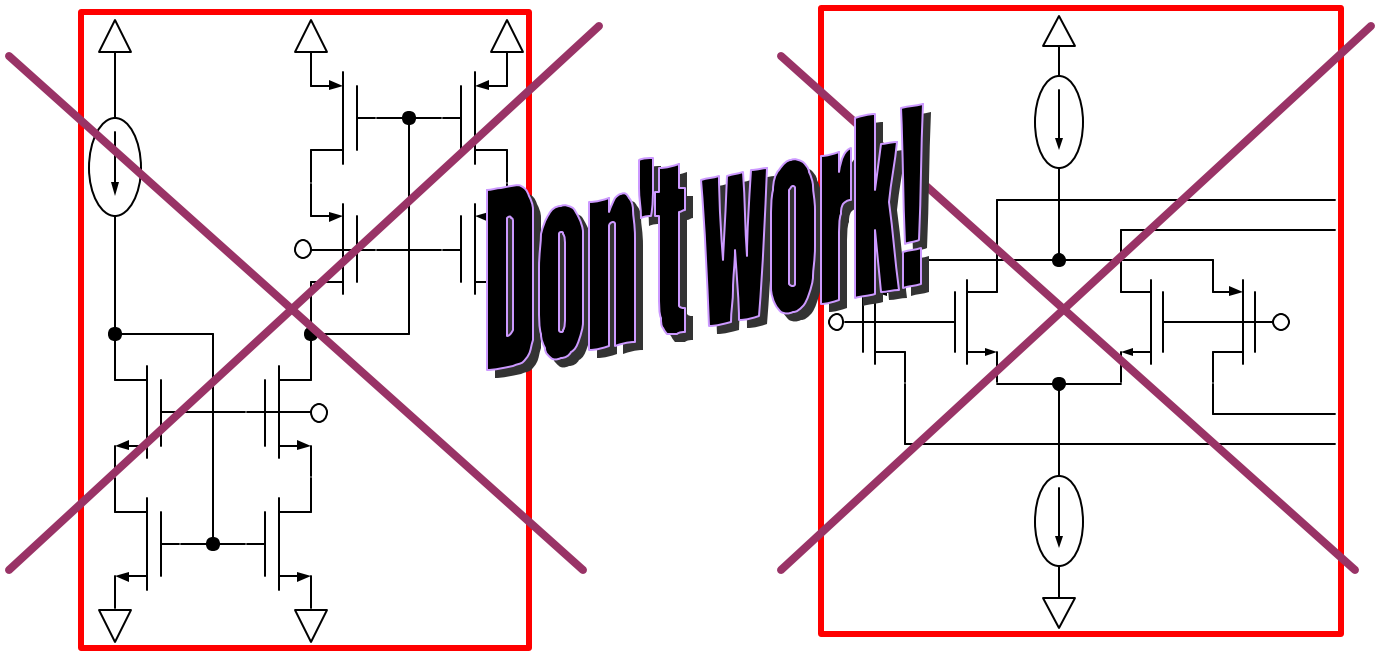
- In the near future

$$V_{DD} < V_{Tn} + |V_{Tp}|$$

1. Introduction

- Even very simple circuits do not work under this condition

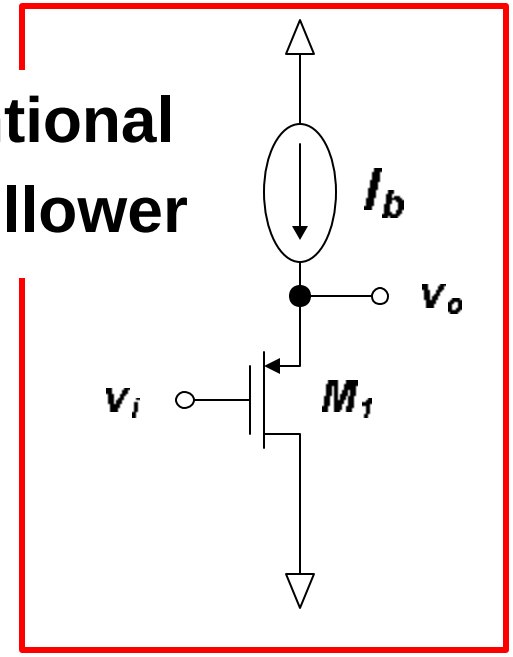
$$V_{DD} < V_{Tn} + |V_{Tp}|$$



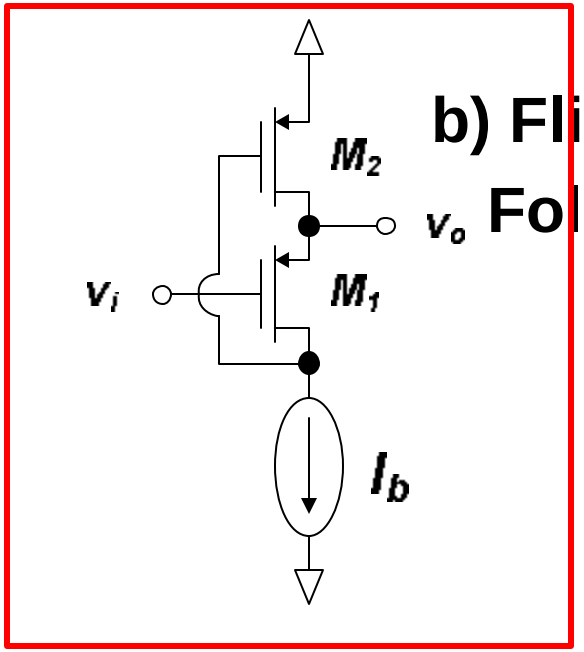
- New design techniques and new circuit structures are required for low voltage, low power design

2. The Basic FVF

a) Conventional Voltage Follower



b) Flipped-Voltage Follower (FVF)

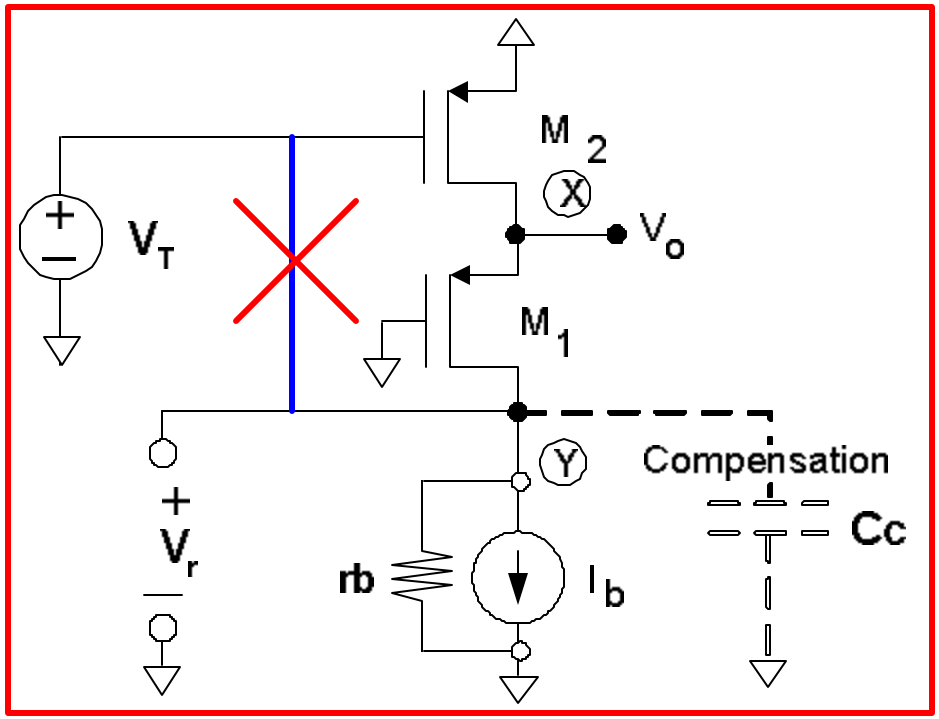


	Sourcing	Sinking	A_v	g_{out}
a) Conventional	I_b	HIGH	< 1	gm_1
b) FVF	HIGH	I_b	= 1	$gm_1\, gm_2\, ro_1$

[Ramirez-Angulo'92] J.Ramírez-Angulo, R.G.Carvajal, A.Torralba, J.Galán, A.P.VegaLeal, and J.Tombs. "The Flipped Voltage Follower: a useful cell for low-voltage low power circuit design," Proc. ISCAS'02, vol. 3, pp. 615-618, 2002.

2. The Basic FVF

Open Loop Analysis



C_X *parasitics at node X (incl. LOAD)*
C_Y *parasitics at node Y (incl. Cc if any)*

Dc gain

$A_{OL} = V_r / V_T = - gm_2 R_{OLY}$
$R_{OLY} = r_b \,||\, gm_1 ro_1 ro_2$,
$R_{OLX} \sim (1+r_b/ro_1)/gm_1 \,||\, ro_2$

Dominant Pole

At Y: $w_{pY} = 1 / C_Y R_{OLY}$

Non-Dominant Pole

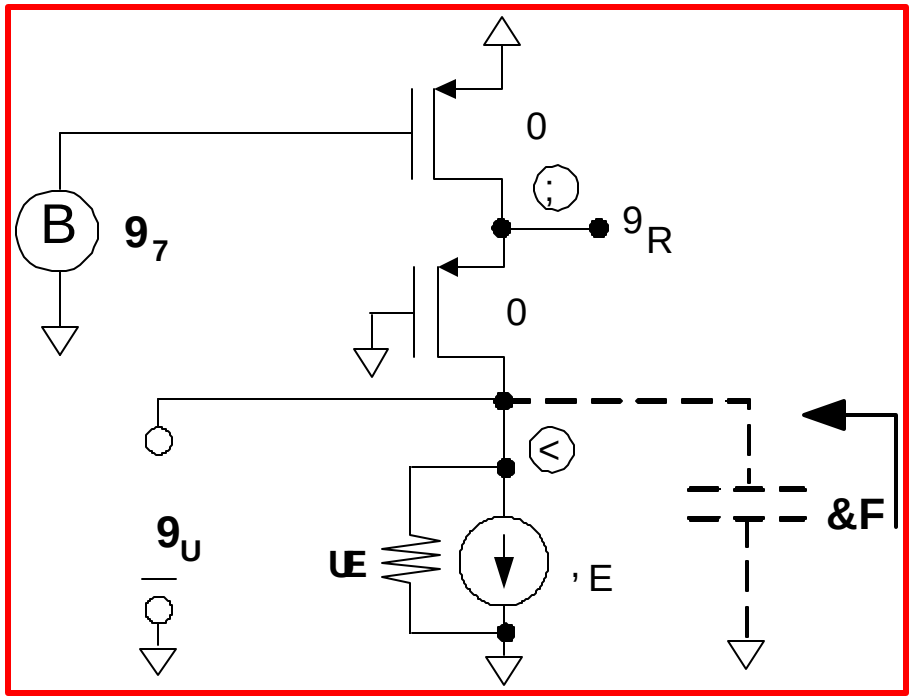
At X: $w_{pX} = 1 / C_X R_{OLX}$

Gain-Bandwidth Product

$GB = gm_2 / C_Y$

2. The Basic FVF

Stability Analysis



C_X *parasitics at node X (incl. LOAD)*
C_Y *parasitics at node Y (incl. Cc if any)*

Stability Criterion: $w_{pX} > 2\ GB$

- For I_b a simple current mirror ($r_b \sim ro_1$)

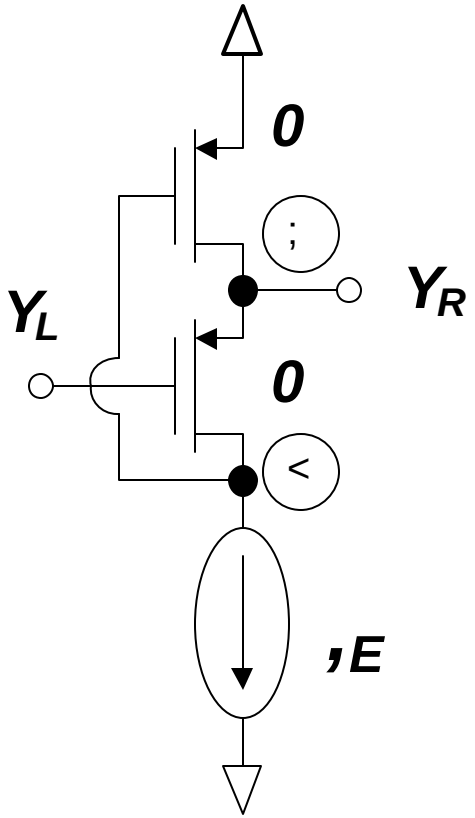
$$\frac{C_X}{C_Y} < \frac{gm_1}{4gm_2}$$

- For I_b a cascode current mirror ($r_b \sim gm_1\, ro_1\, ro_2$)

$$\frac{C_X}{C_Y} < \frac{1}{gm_2 ro_2}$$

usually requires compensation

2. The Basic FVF



Closed Loop Output Resistance

$$R_{CLX} = \frac{R_{OX}}{1+|A_{OL}|} \approx \frac{\frac{1}{gm_1}\left(1+\frac{r_b}{ro_1}\right) \| ro_2}{gm_2\left(r_b \| gm_1 ro_1 ro_2\right)}$$

- For I_b a simple current mirror (rb ~ ro1)

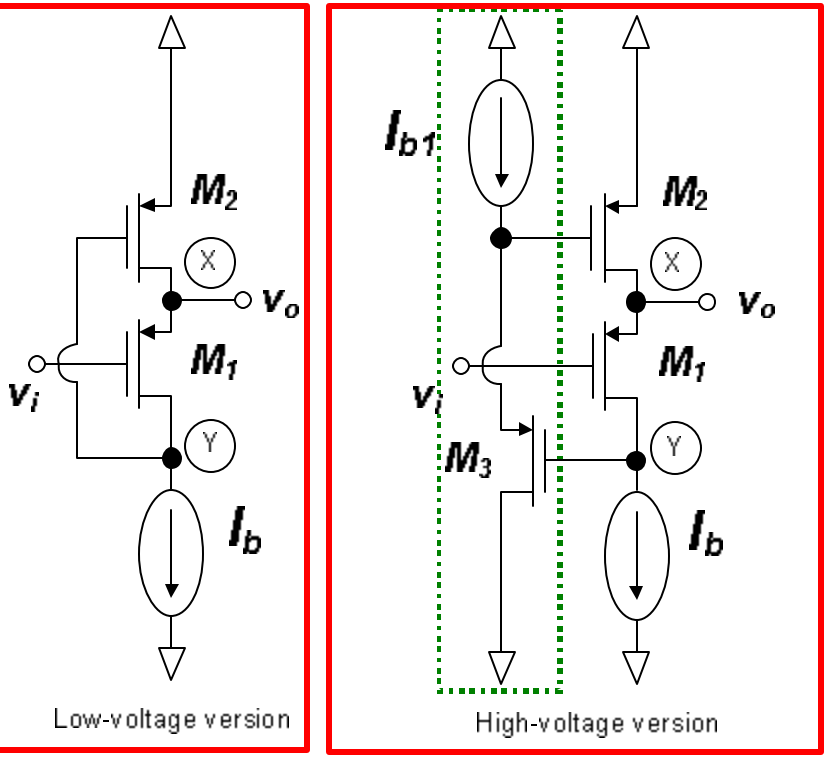
$$R_{CLX} \rightarrow \frac{2}{gm_1 gm_2 ro_1}$$

- For I_b a cascode current mirror (r_b ~ gm_1 ro_1 ro_2)

$$R_{CLX} \rightarrow \frac{1}{gm_1 gm_2 ro_1}$$

A_{CL} ~ 1 and R_{CLX} is only a few Ohms (20 – 100) in all cases

2. The Basic FVF

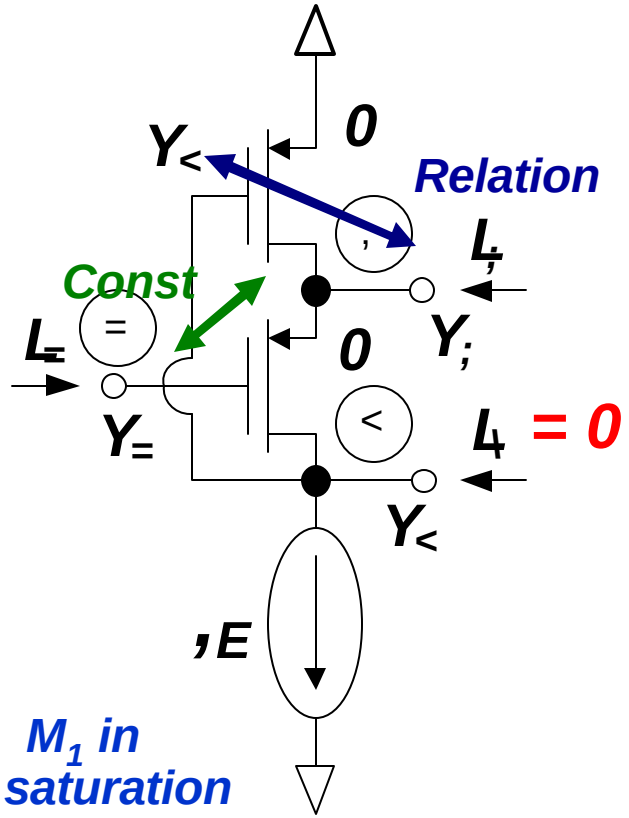


DC considerations

- $V_{DD}^{MIN} = V_{GS}^{MIN} + V_{DS}^{sat} \sim$ 0.8 V for 0.6µm CMOS technology. It is a low-voltage cell.
- But, for large V_{DD}, biasing M_2 in saturation is difficult for low v_i. A high-voltage version includes a voltage shifter in the feedback loop [Chung-Chih'95]

[Chung-Chih'95] H.Chung-Chih, H.Changku, M. Ismail, "CMOS low-voltage rail-to-rail V-I converter," Proc. 38th MWSCAS, vol.2, pp. 1337-1340, 1995.

2. The Basic FVF



3-terminal cell (strong inv.)

$$v_X = v_Z + f(I_b, i_Y)$$

$$v_Y = g(I_b, i_X, i_Y, v_Z) \quad ; \quad f(I_b, i_Y) = |V_{Tp}| + \sqrt{\frac{2(I_b - i_Y)}{k_p (W/L)_{M_1}}}$$

$$i_Z = 0$$

- **For M_2 in saturation**

$$g(I_b, i_X, i_Y, v_Z) = V_{DD} - |V_{Tp}| - \sqrt{\frac{2(I_b - i_Y - i_X)}{k_p (W/L)_{M_2}}}$$

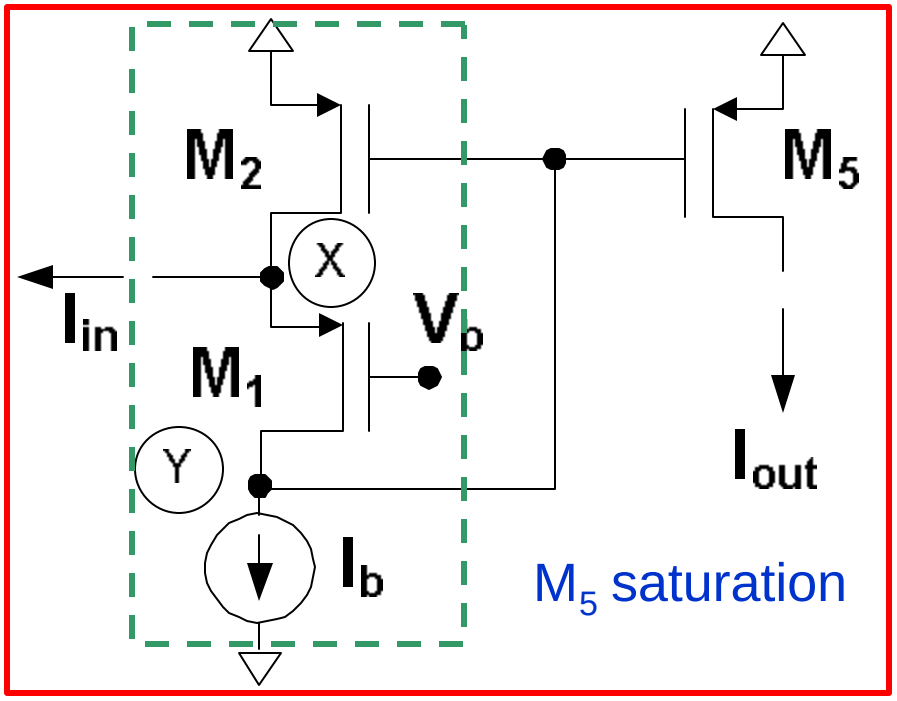
- **For M_2 in ohmic**

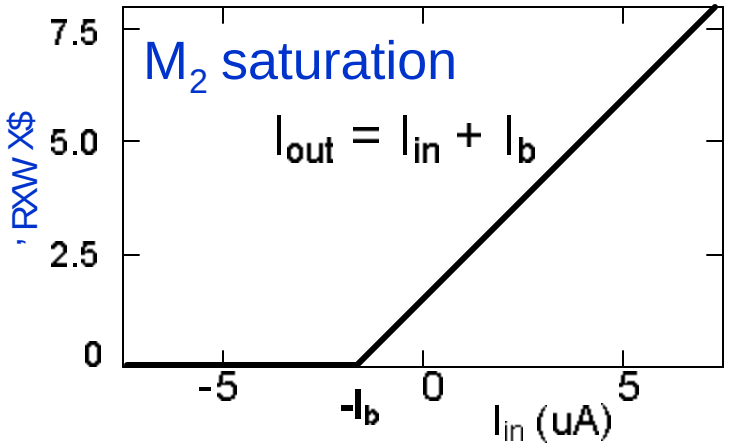
$$g(I_b, i_X, i_Y, v_Z) = V_{DD} - |V_{Tp}| - \frac{v_X}{2} - \frac{I_b - i_Y - i_X}{k_p (W/L)_{M_2}} \cdot \frac{1}{v_X}$$

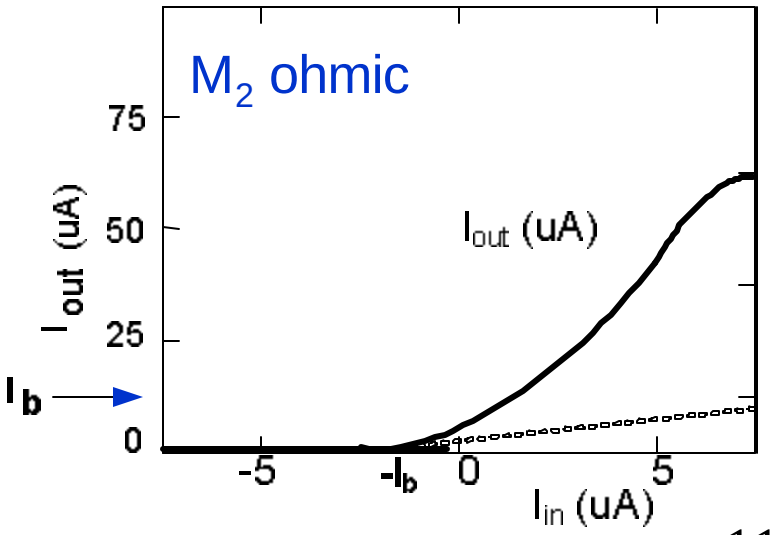
The most interesting case is for $i_Y = 0$

3.FVF Structures

Current sensor (FVF-CS)

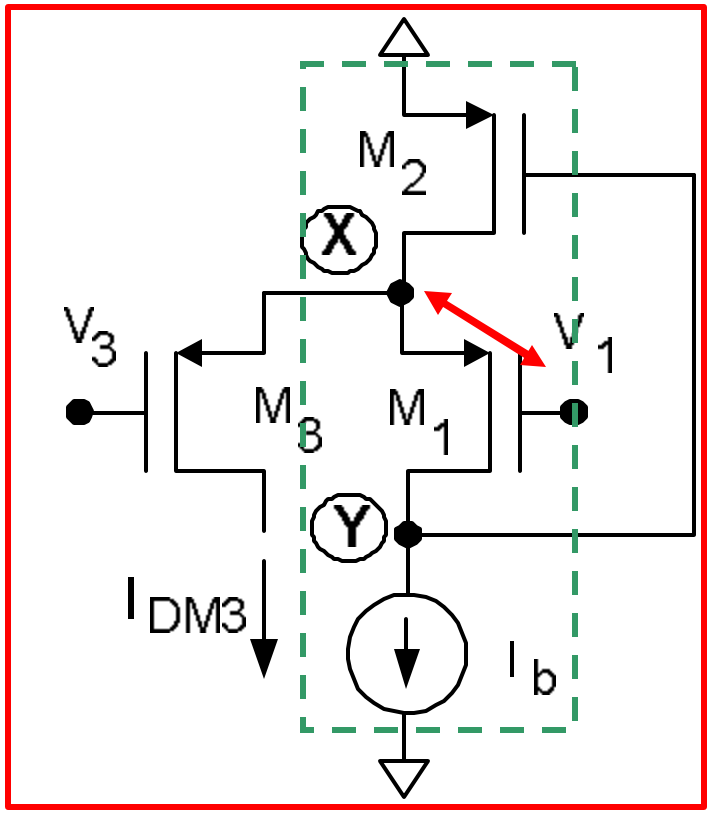


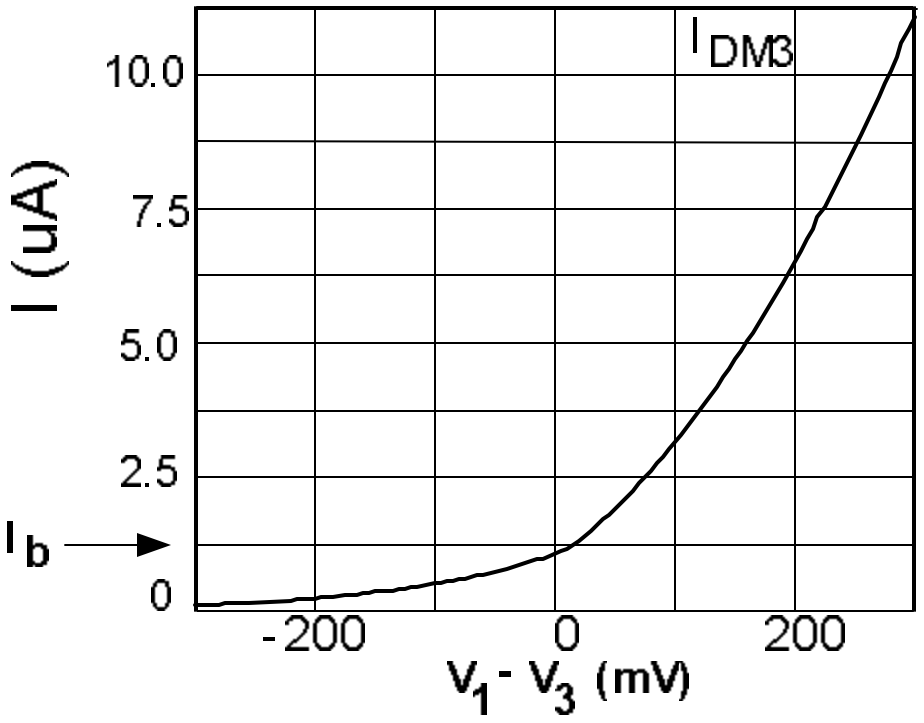




3.FVF Structures

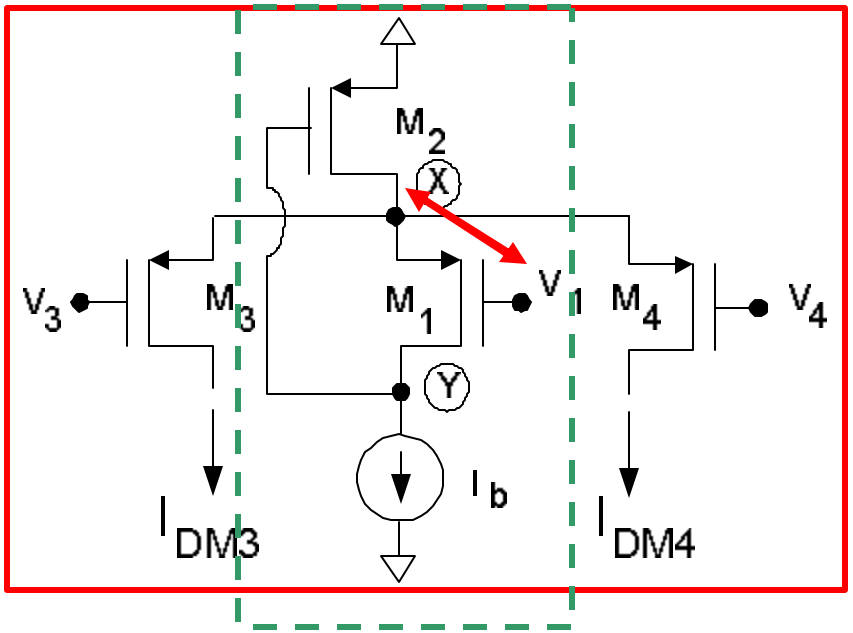
Non-Symmetrical Class-AB Differential Pair (FVF-NDP)

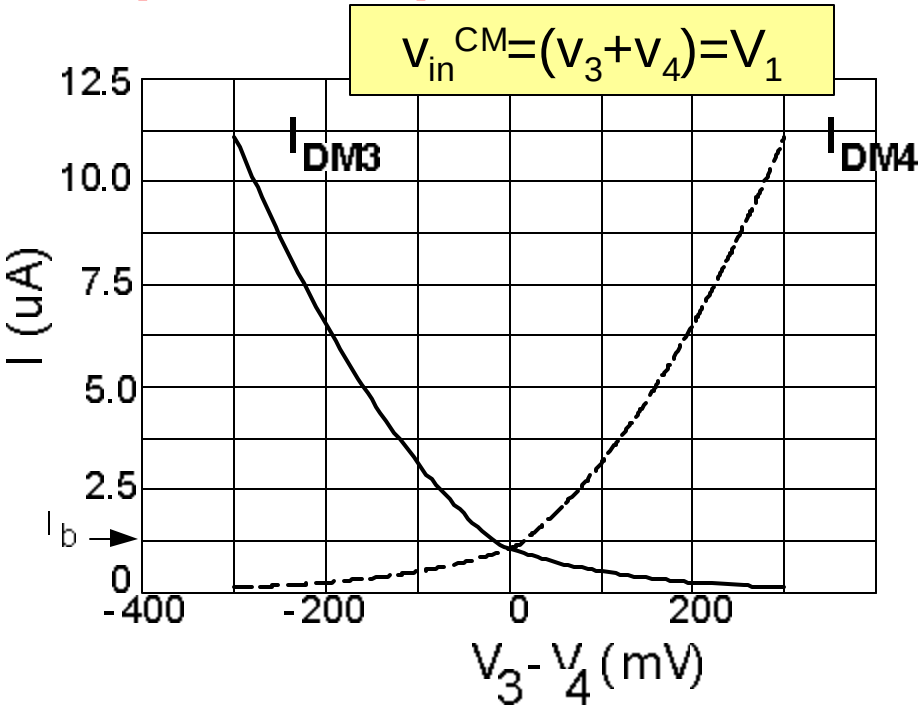




3.FVF Structures

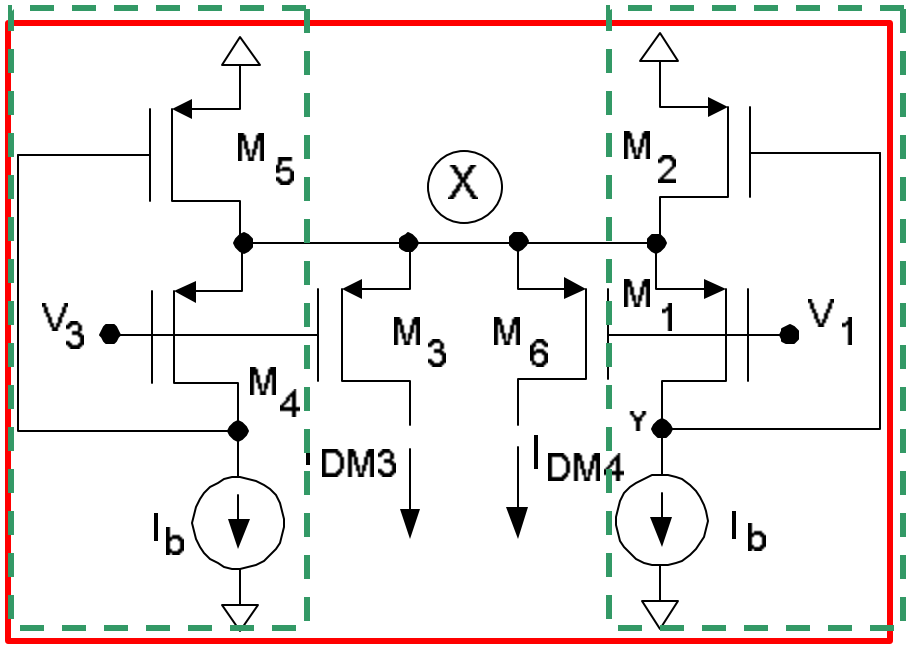
Symmetrical Class-AB Pseudo Differential Pair (FVF-PDP)

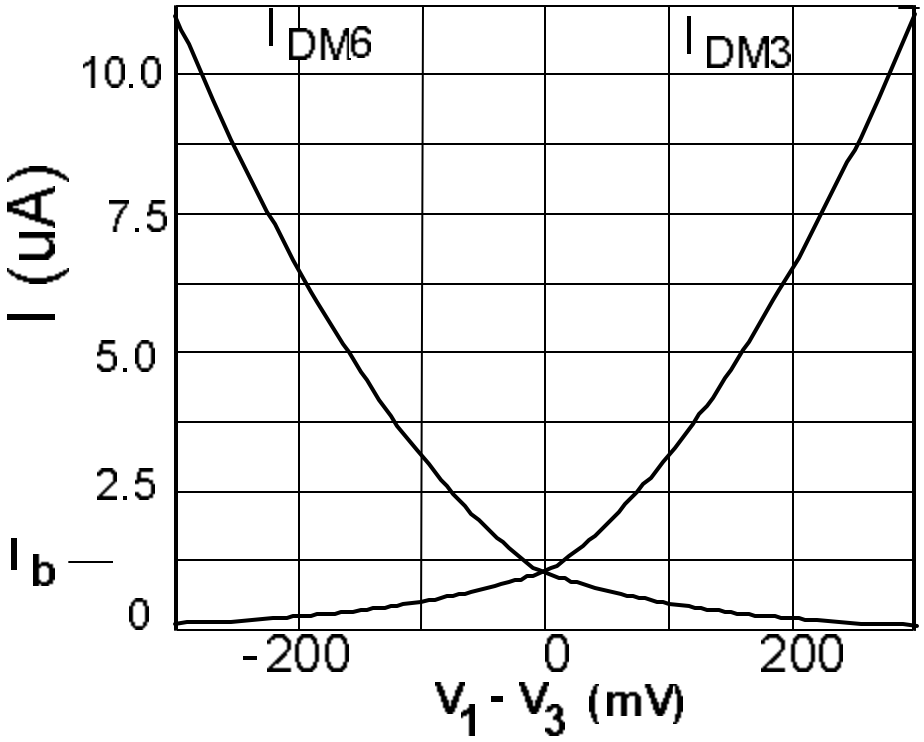




3.FVF Structures

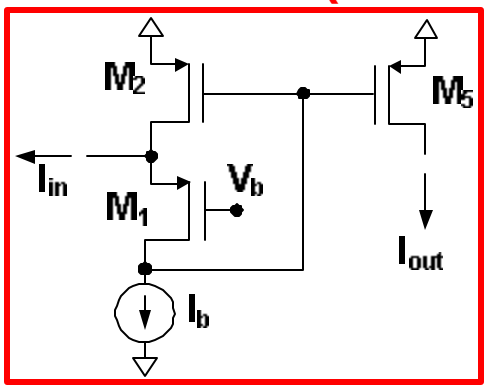
Symmetrical Class-AB Differential Pair (FVF-SDP)

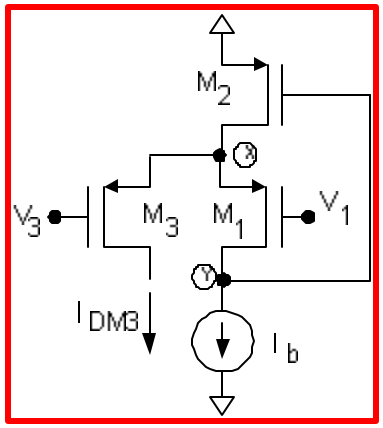




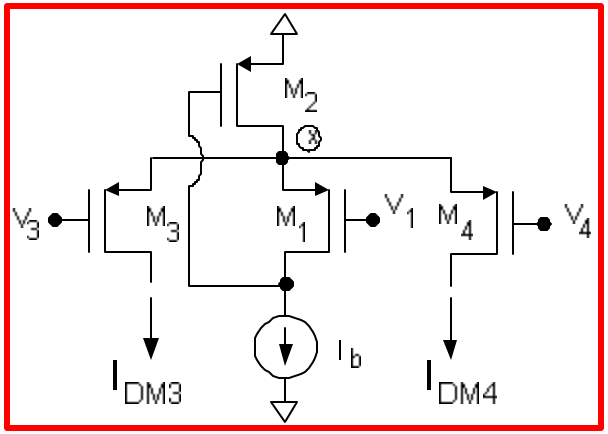
3.FVF Structures. Summary

Current sensor (FVF-CS)

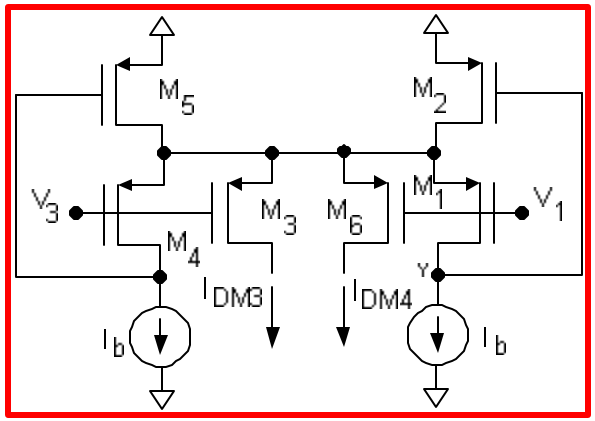




Non-Symmetrical Class-AB Differential Pair (FVF-NDP)



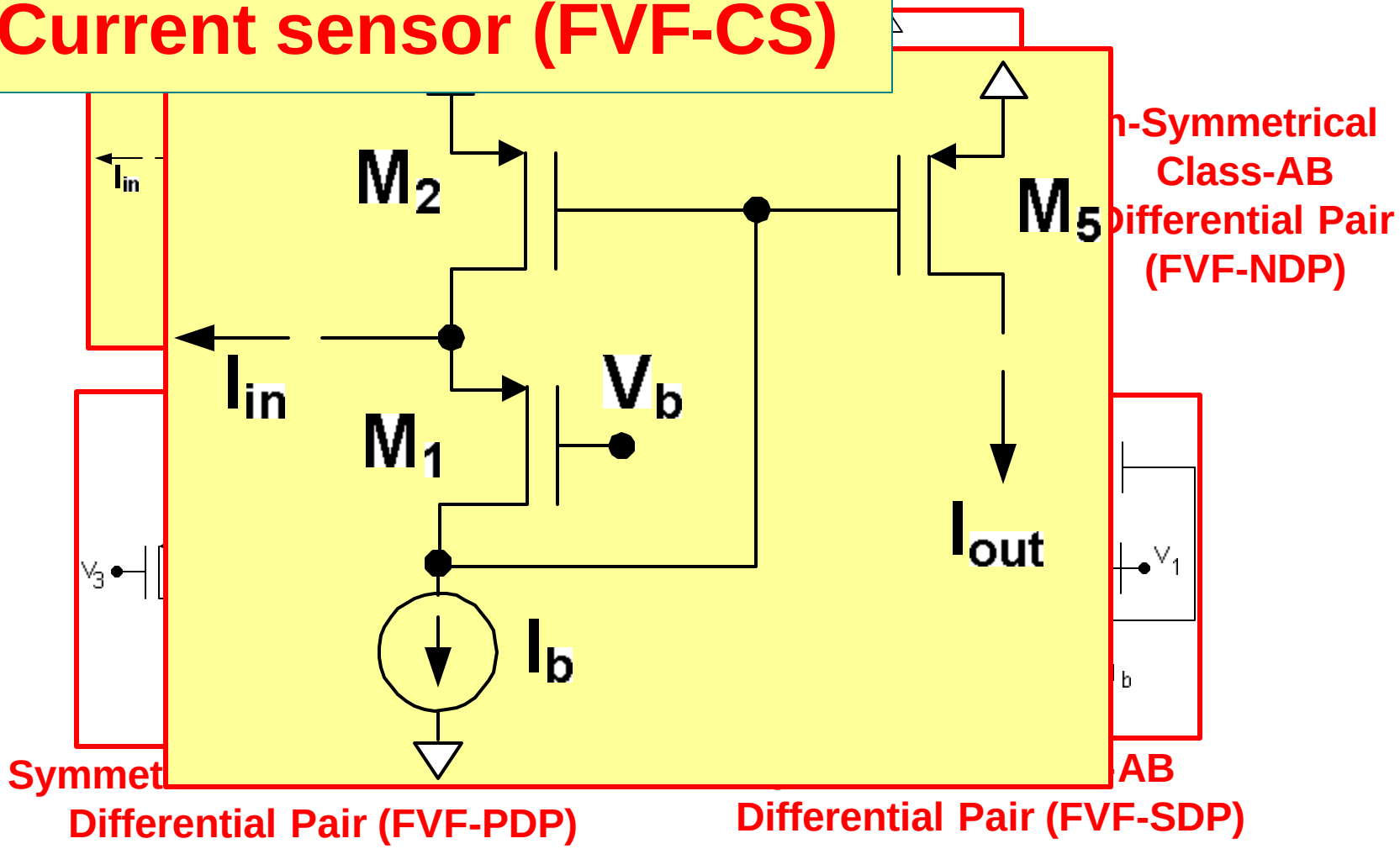
Symmetrical Class-AB Pseudo Differential Pair (FVF-PDP)



Symmetrical Class-AB Differential Pair (FVF-SDP)

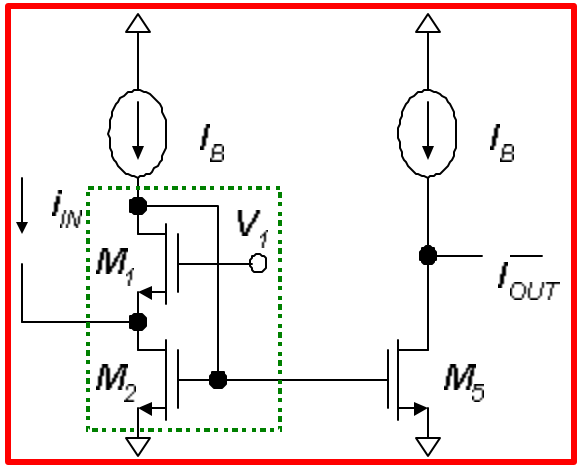
3.FVF Structures. Summary

Current sensor (FVF-CS)

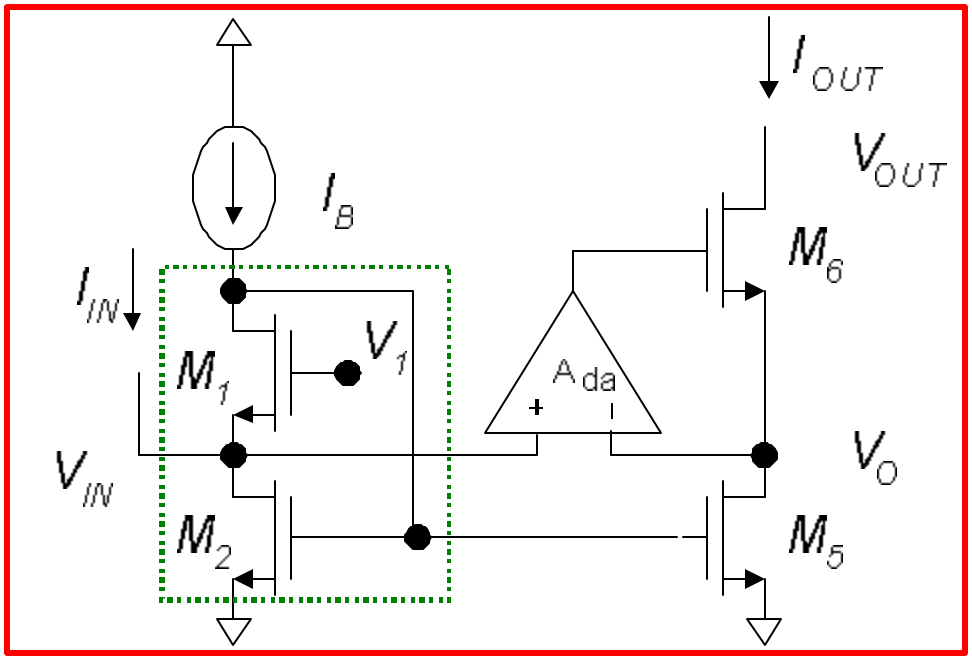


4.FVF-CS Applications

Current sensor (FVF-CS)
Low voltage current mirrors



[Rijns'93] J.J.F. Rijns, "54 MHz switched-capacitor video channel equalizer" *Electr.Lett.*, vol. 29, no. 25, pp. 2181-2182, Dec. 1993

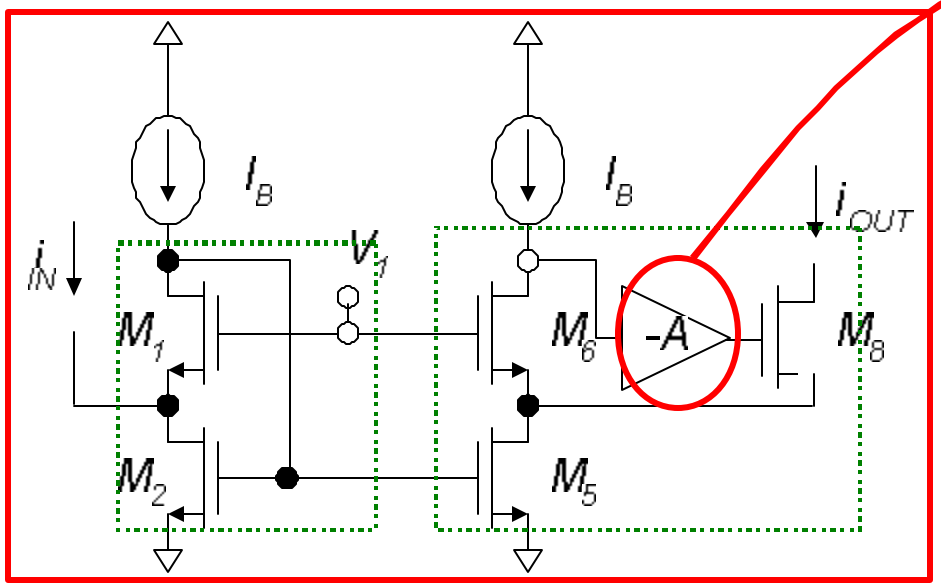


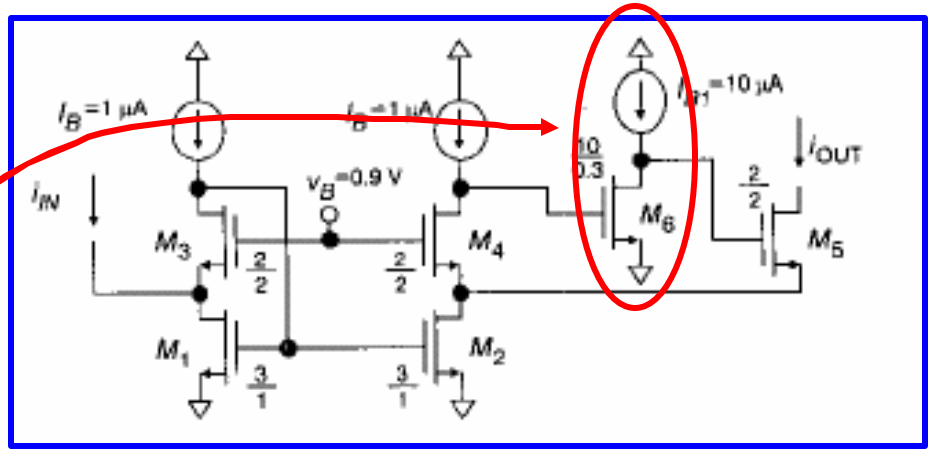
[Ramirez-Angulo'04] J. Ramírez-Angulo, R.G.Carvajal, A.Torralba, "Low-supply voltage high-performance CMOS current mirror with low input and output voltage requirements," *IEEE TCAS-II*, vol.51, no. 3, pp. 124-129, March 2004.

- $V_{in}^{MIN} = V_{DSsat}$
- **Very low input resistance (a few Ohms)**

4.FVF-CS Applications

Current sensor (FVF-CS)
Low voltage current mirrors





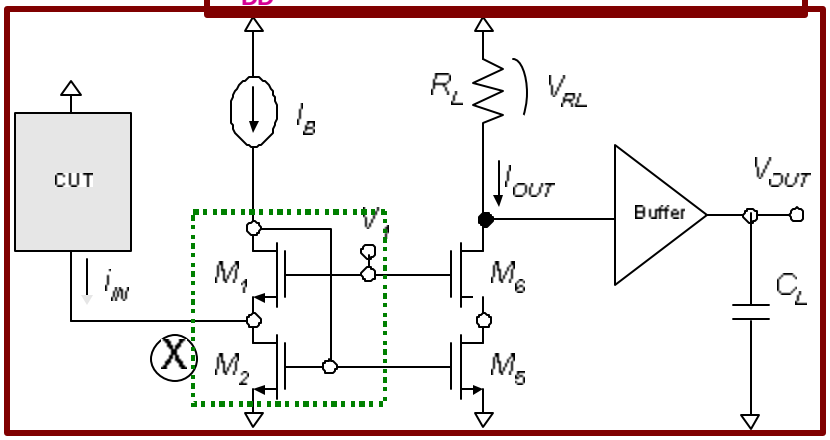
Technology	0,35µm CMOS AMS
Minimum supply voltage	1 V
Load resistor	10 KOhm
Bandwidth	120 MHz
Input impedance	A few Ohms
Output impedance	˜ 1 GOhm
Input referred noise (@10MHz)	1.5 pA/vHz
Settling time (1%, 4 µA step)	20ns
THD (10 µA pp, @10KHz)	-66dB

[Torralba'02] A. Torralba, R.G.Carvajal, J.Ramírez-Angulo, "Output stage for low supply voltage CMOS current mirrors" *Electr.Lett.*, vol. 38, no. 24, pp. 1528-1529, Nov. 2002

4.FVF-CS Applications

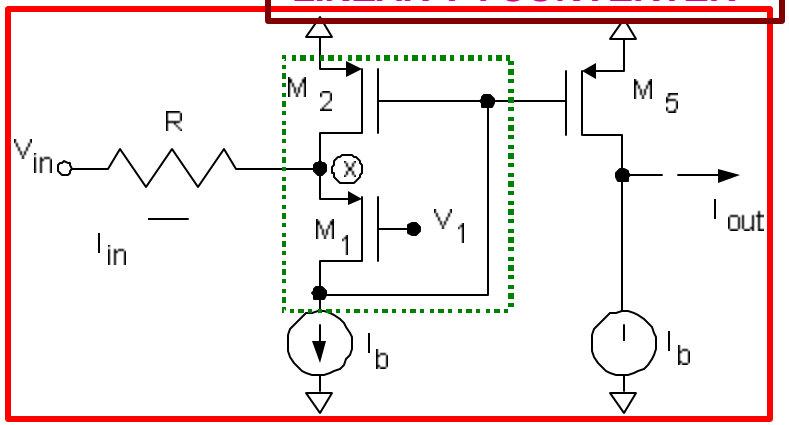
Current sensor (FVF-CS)
Other applications

I_{DD} TEST CURRENT SENSOR

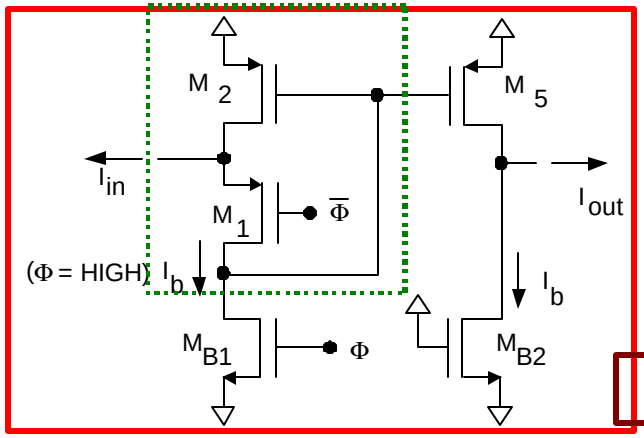


[Docudray'03] G.O.Ducodray, R.G.Carvajal, J.Ramírez-Angulo, "A high-speed dynamic current sensor scheme for I_{DD} test using a FVF" *Proc. SSMSD*, pp. 50-53, 2003

LINEAR V-I CONVERTER



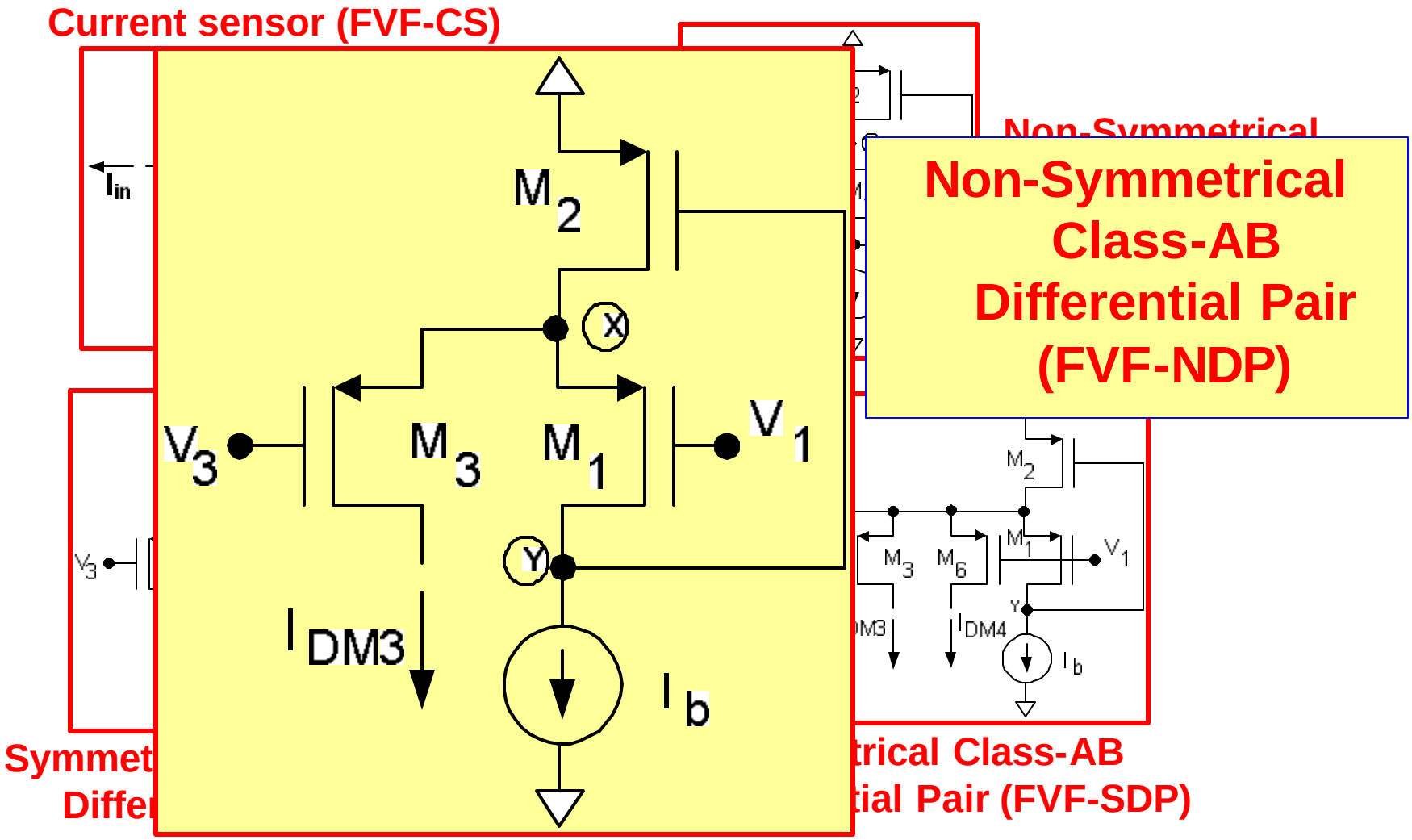
[Karthikeyan'01] S. Karthikeyan, A. Tamminneedi, E.K.F.Lee, "Design of low-voltage front-end interfaces for switched-opamp circuits," *IEEE TCAS-II*, vol.48, no. 7, pp. 722-726, July 2001.



[Rout'00] S. Rout, E.K.F.Lee, "Design of 1 V switched-current cells in standard CMOS process," *Proc. ISCAS*, vol.2, pp. 421-424, 2000

SI Circuits

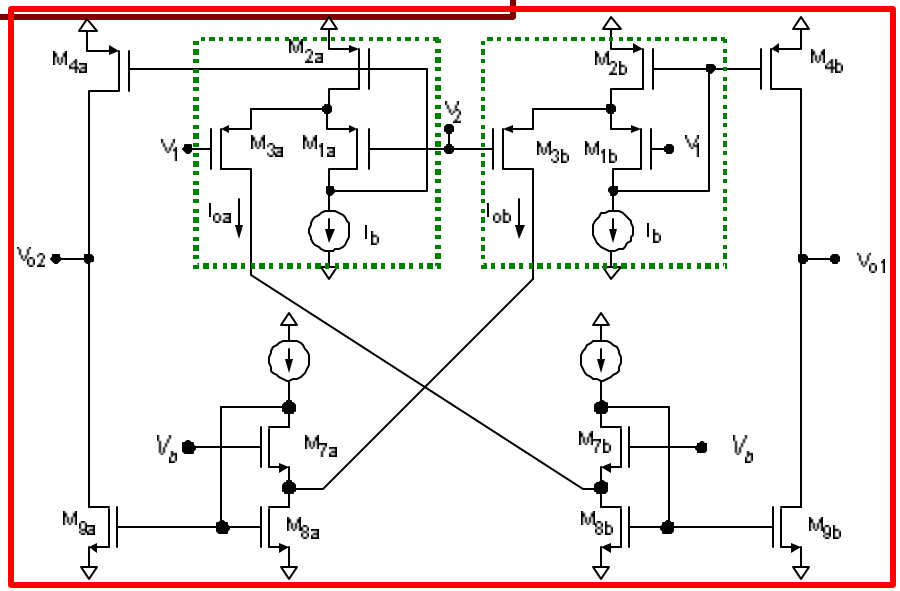
3.FVF Structures. Summary



4.FVF-NDP Applications

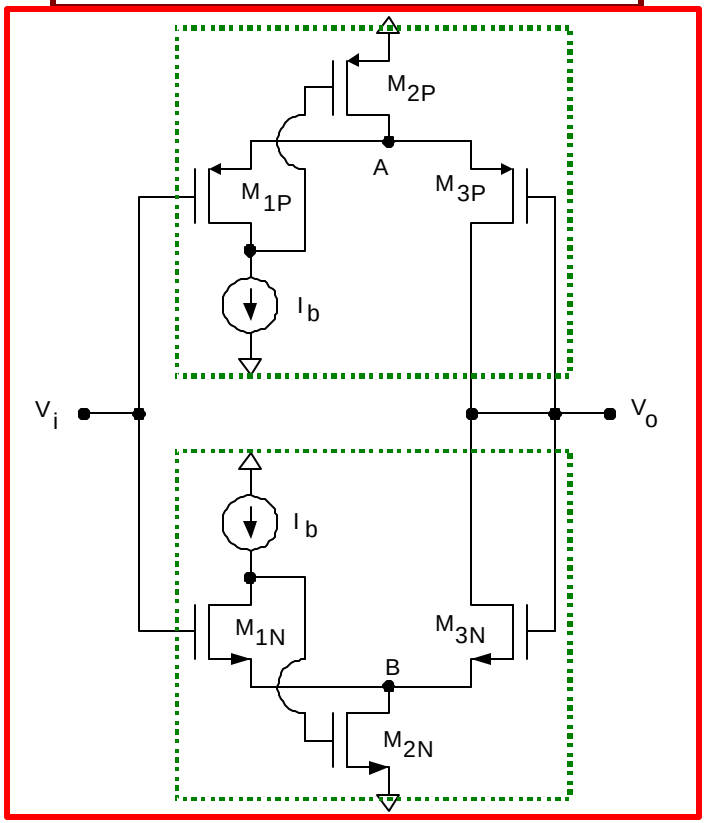
Non-Symmetrical Class-AB Differential Pair (FVF-NDP)

NON-LINEAR CLASS_AB TRANSCONDUCTOR



[Peluso'00] V.Peluso, P. Vancorenland, A.M.Marques, M.S.J.Steyaert, W.Sansen, "A 900mV low-power ΔΣ A/D converter with 77dB dynamic range," *IEEE J.Solid-State Circuits*, vol. 35, no. 4, pp. 632-636, April 2000.

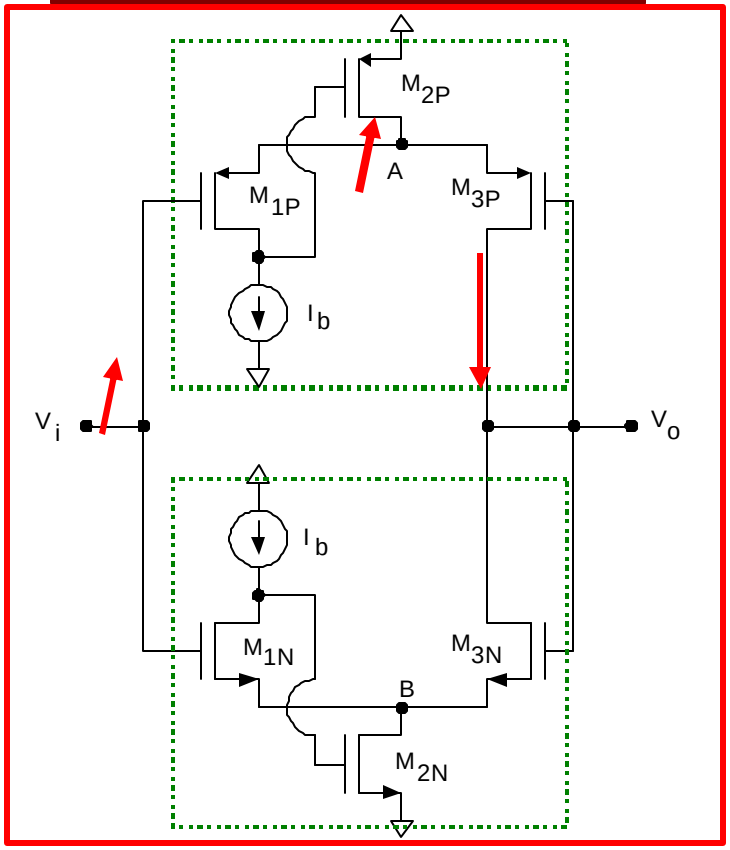
CLASS-AB OUTPUT BUFFER



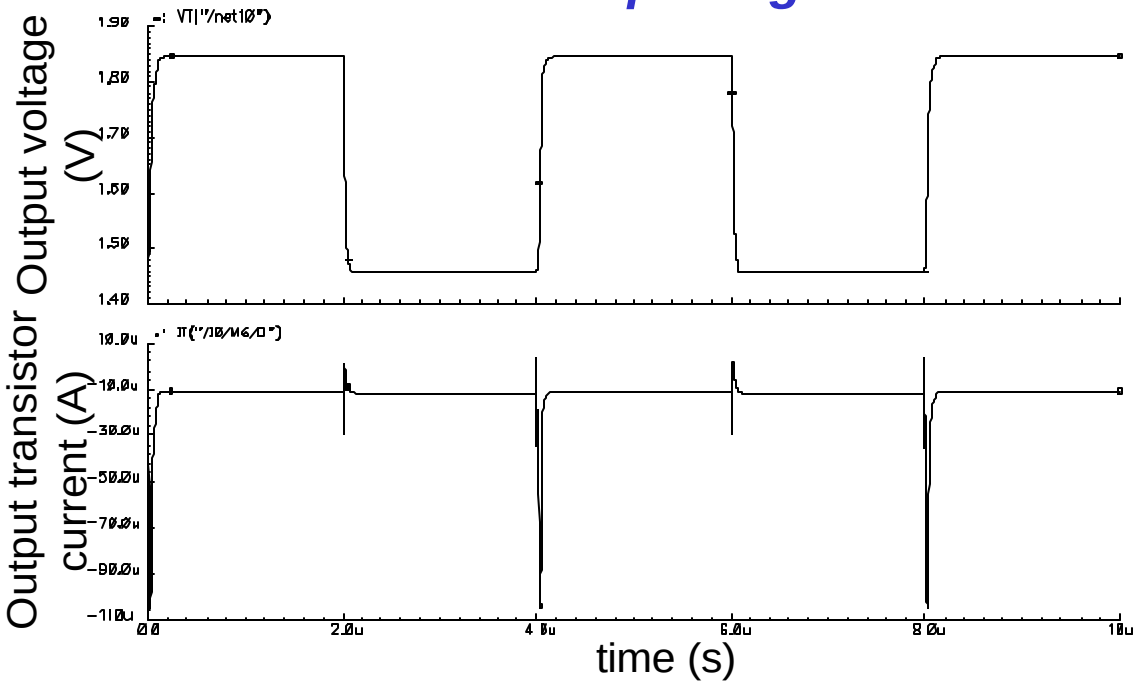
[Carvajal'02] R.G.Carvajal, A. Torralba, J.Ramírez-Angulo, J.Tombs, F. Muñoz, "Compact low-power high slew-rate CMOS buffer for large capacitive loads," *Electron. Lett.*, vol.38, no. 32, pp. 1348-1349, Oct. 2002.

4. FVF-NPD Applications

CLASS-AB OUTPUT BUFFER



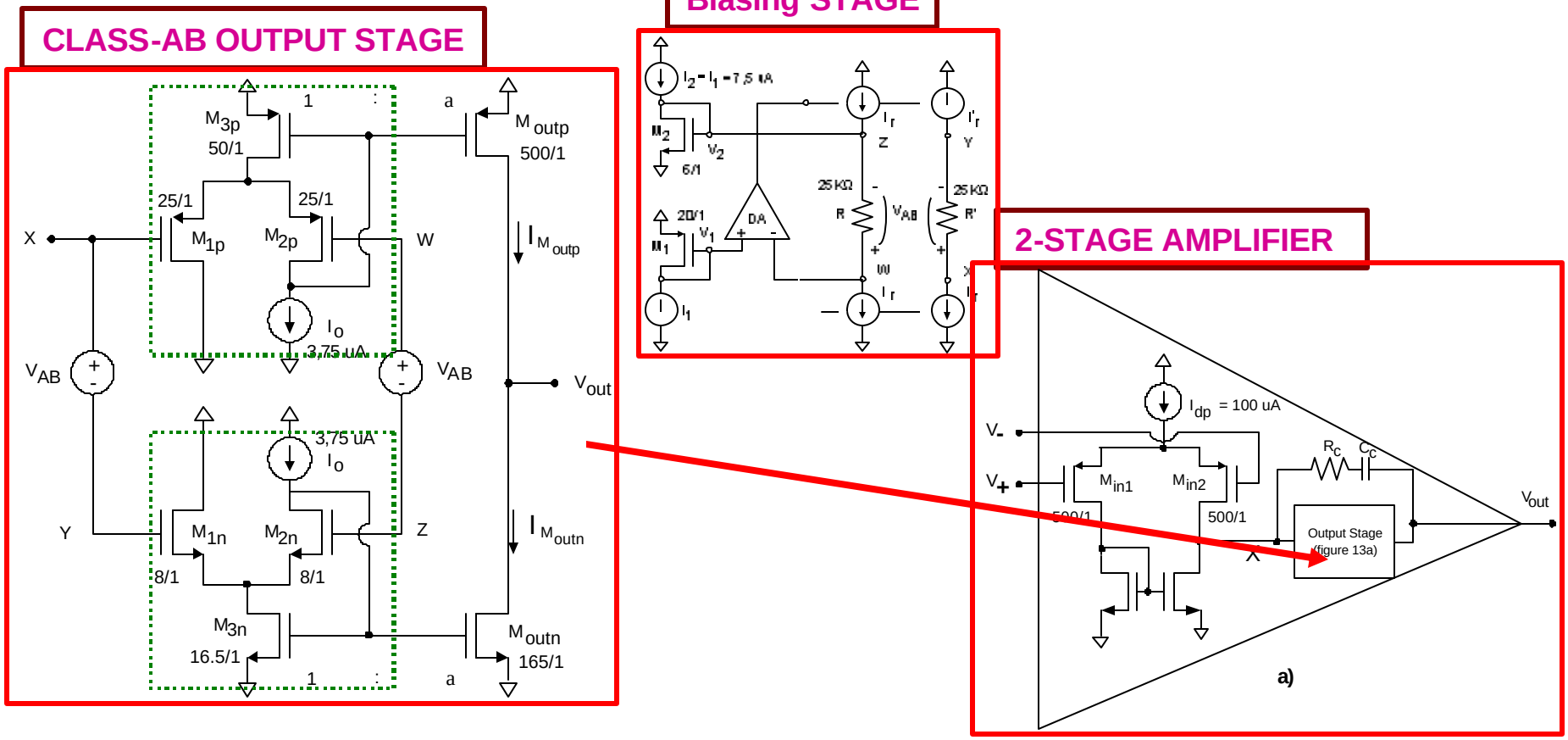
2 V supply, 10pF capacitor load, 250 KHz input signal



[Carrillo'04] J.M.Carrilo R.G.Carvajal,, A. Torralba, J.Duque-Carrillo, "Rail-to-rail, low-power high slew-rate CMOS analog buffer," *Electron. Lett.*, vol.40, no. 14, July 2004.

More than 100uA max. output current with 30uA total quiescent current !

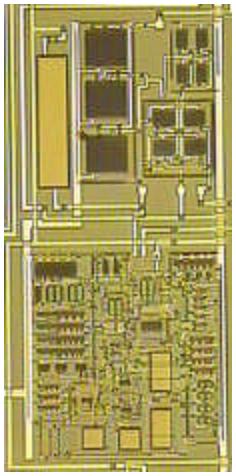
4.FVF-NPD Applications

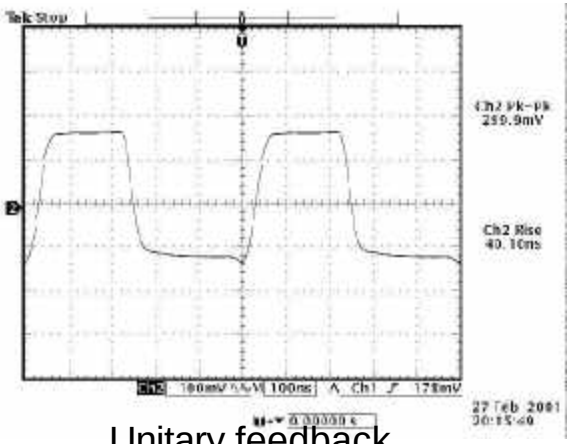


[Torralba'00] A. Torralba, R.G.Carvajal, J. Martínez-Heredia, J.Ramírez-Angulo, "Class-AB output stage for low voltage CMOS op-amps with accurate quiescent current control," *Electron. Lett.*, vol.36, no. 21, pp. 1753-1754, Oct. 2000.

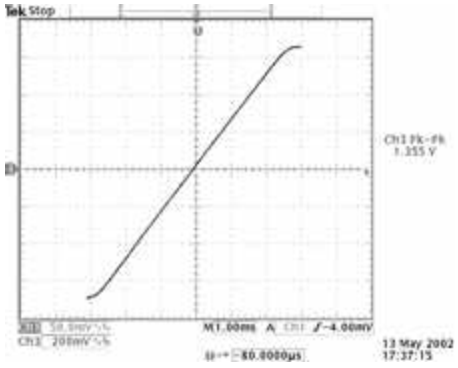
4.FVF Applications

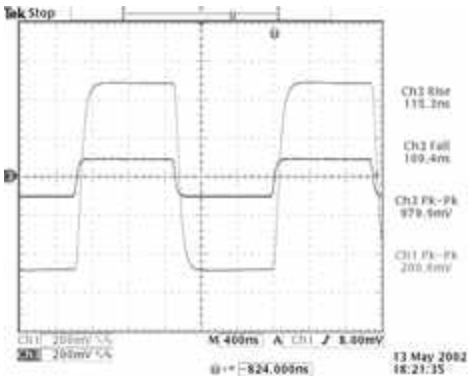
CLASS-AB OUTPUT STAGE in a 2-STAGE OP-AMP





Unitary feedback





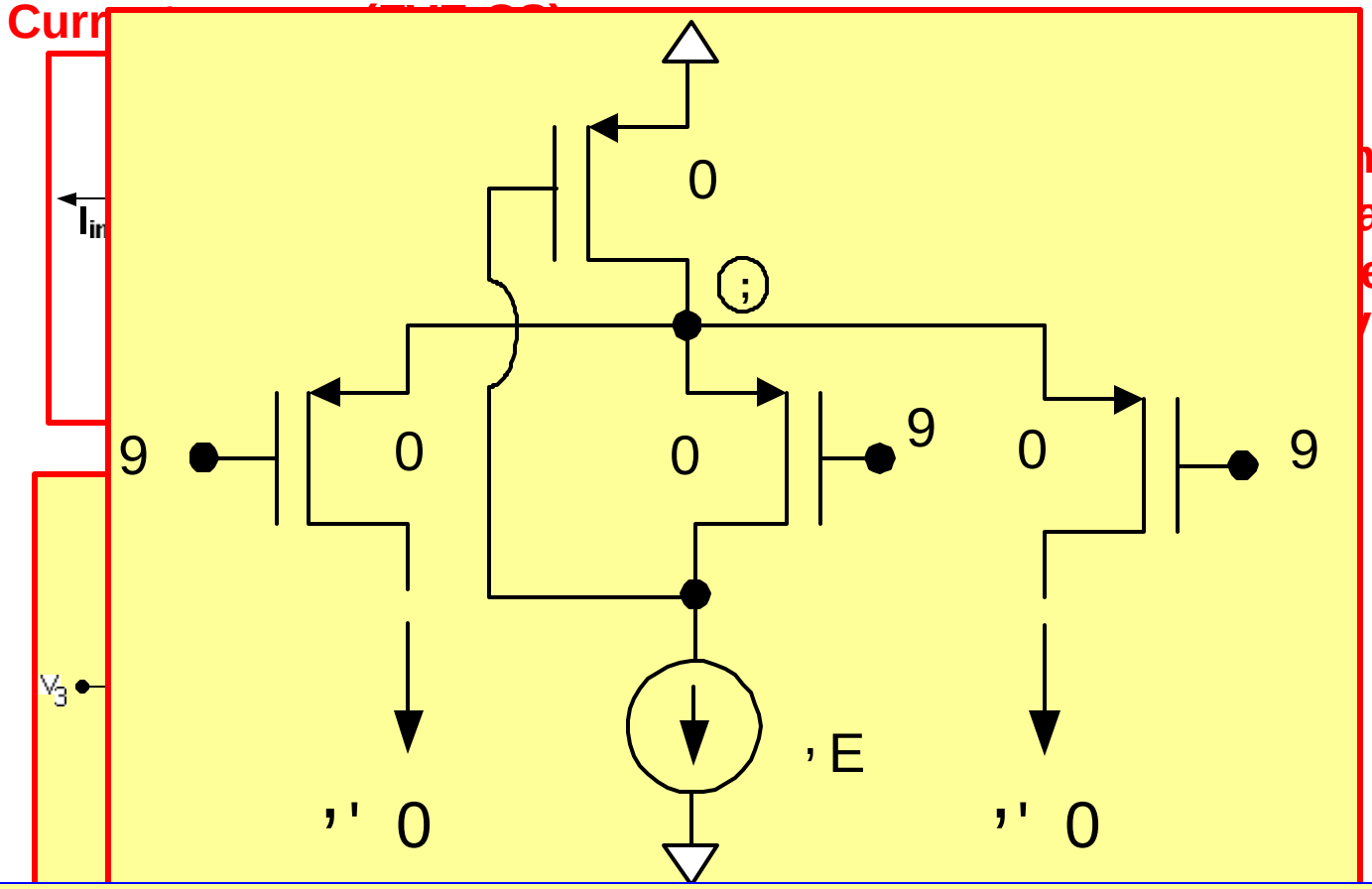
Non-inverting Gain= 5 with 2 internal resistors

DC Gain	dB	65
Phase Margin	deg (°)	75°
Unity Gain frequency	MHz	15
Quiescent output current	(µA)	76
Minimum current through output transistors	(µA)	38
Supply current	(µA)	218
PSRR	dB	38
CMRR	dB	45
THD (1kHz)	dB	65
Input referred noise (100kHz)	nV^2/Hz	21
Slew Rate * (@ 0.3 V peak)	V/µs	10
Peak output current * (@ 0.3 V peak)	µA	500

V_{DD}=1.5 V, C_L=10pF, 0.8 µm CMOS (Vt ˜ 0.85 V)

Op-amp comp. C_C=10pF, R_C=500Ω

3.FVF Structures. Summary



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/F-NDP)

Symmetrical Class-AB Pseudo Differential Pair (FVF-PDP)

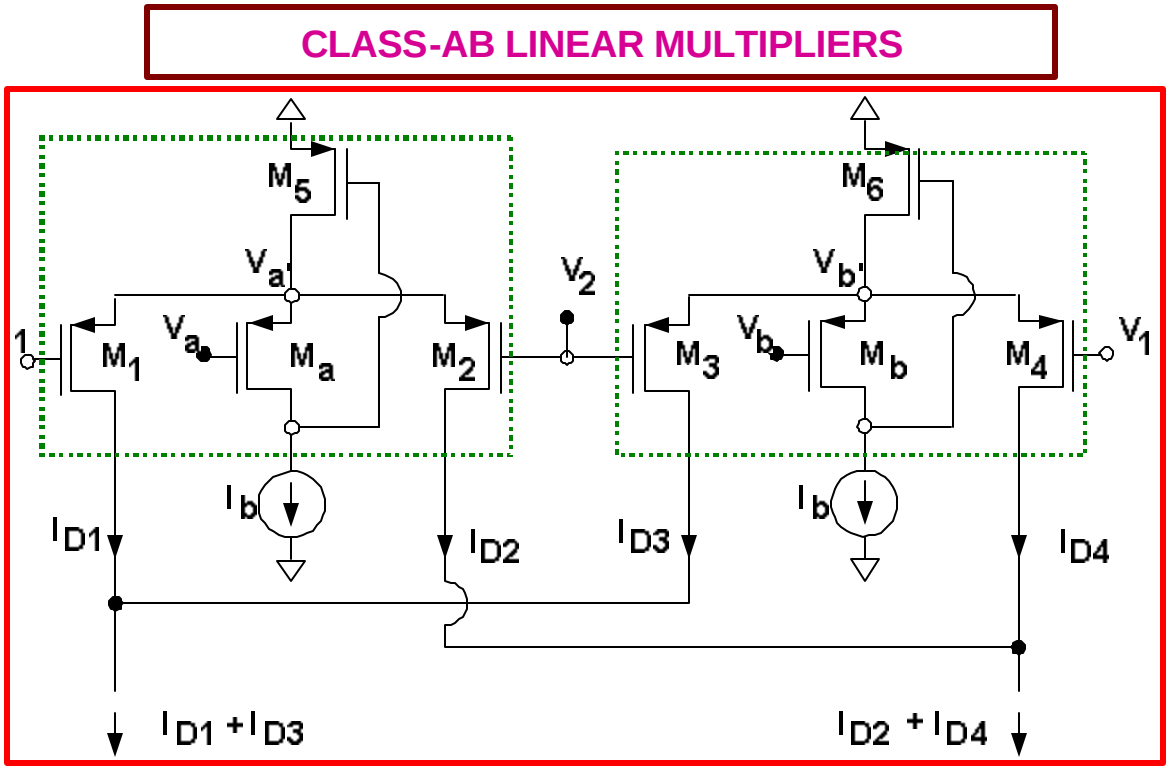
S

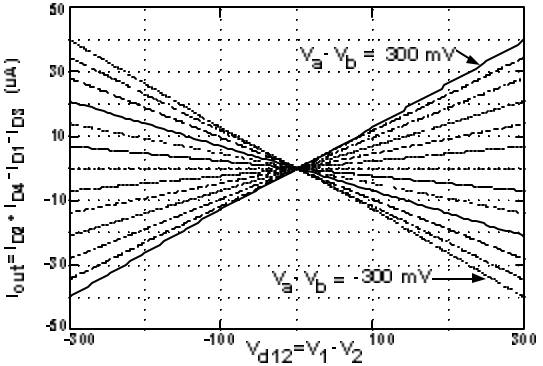
Differential Pair (FVF-PDP)

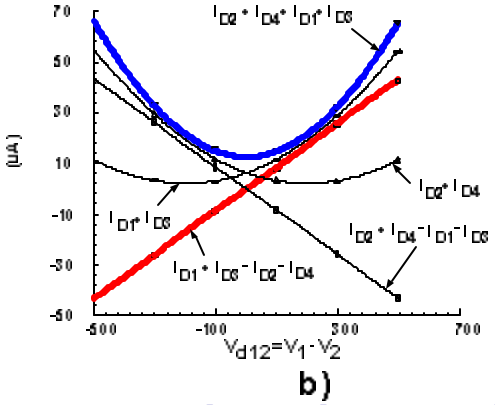
Differential Pair (FVF-SDP)

4.FVF-PDP Applications

Symmetrical Class-AB Pesudo-Differential Pair (FVF-PDP)





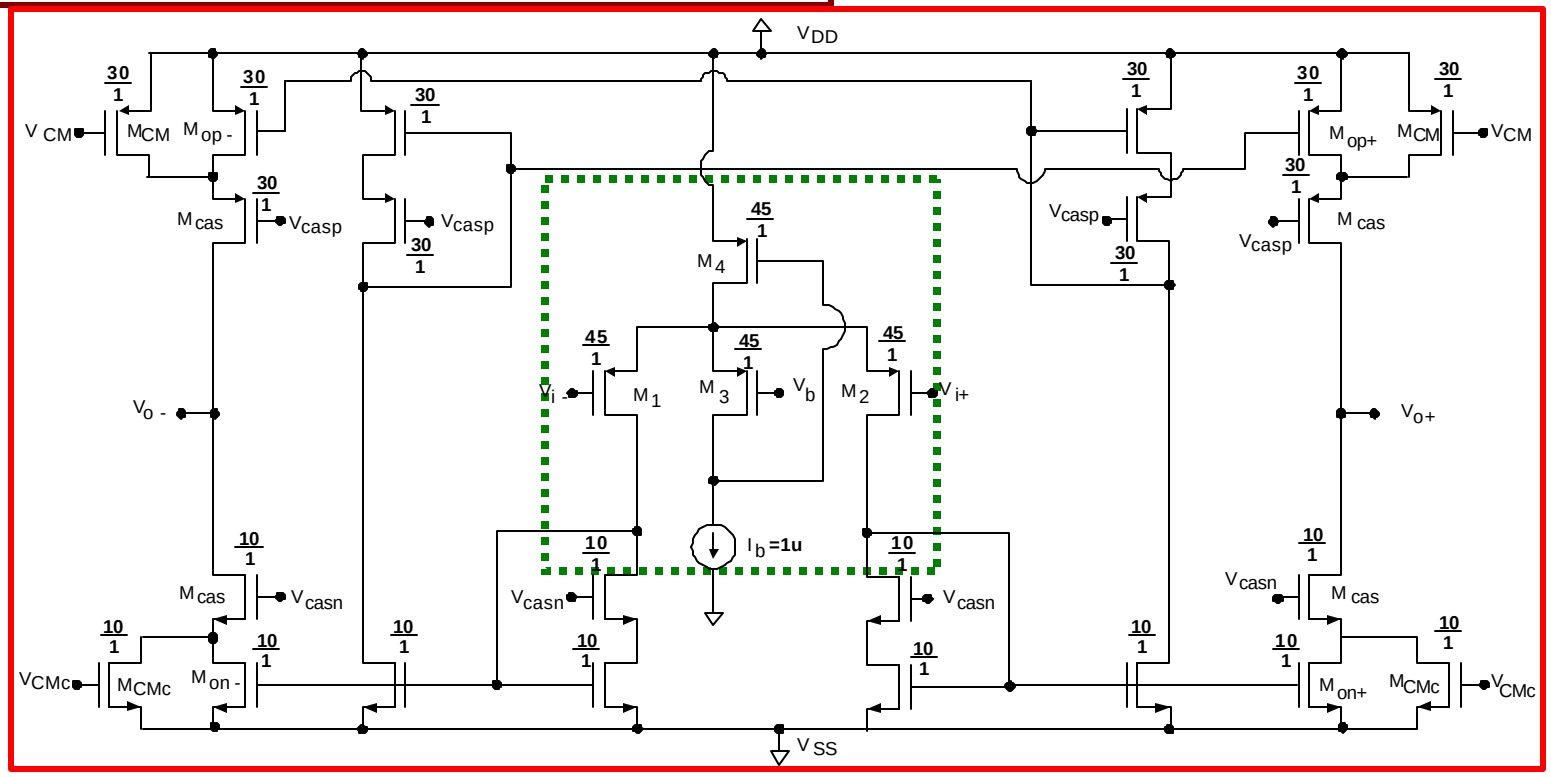


[Ramirez-Angulo'00] J.Ramírez-Angulo, R.G.Carvajal, J.M.Martínez-Heredia, "1.4V supply, wide swing, high frequency CMOS analogue multiplier with high current efficiency," *Proc. ISCAS*, vol. 5, pp. 533-536, 2000

[Ramirez-Angulo'03] J.Ramírez-Angulo, S.Thoutam, A.López-Martín, R.G.Carvajal, "Low voltage CMOS analogue four quadrant multiplier based on Flipped-Voltage-Followers," *Electron. Lett.*, vol.39, no. 25, Dec. 2003.

4.FVF-PDP Applications

NON-LINEAR CLASS_AB TRANSCONDUCTORS

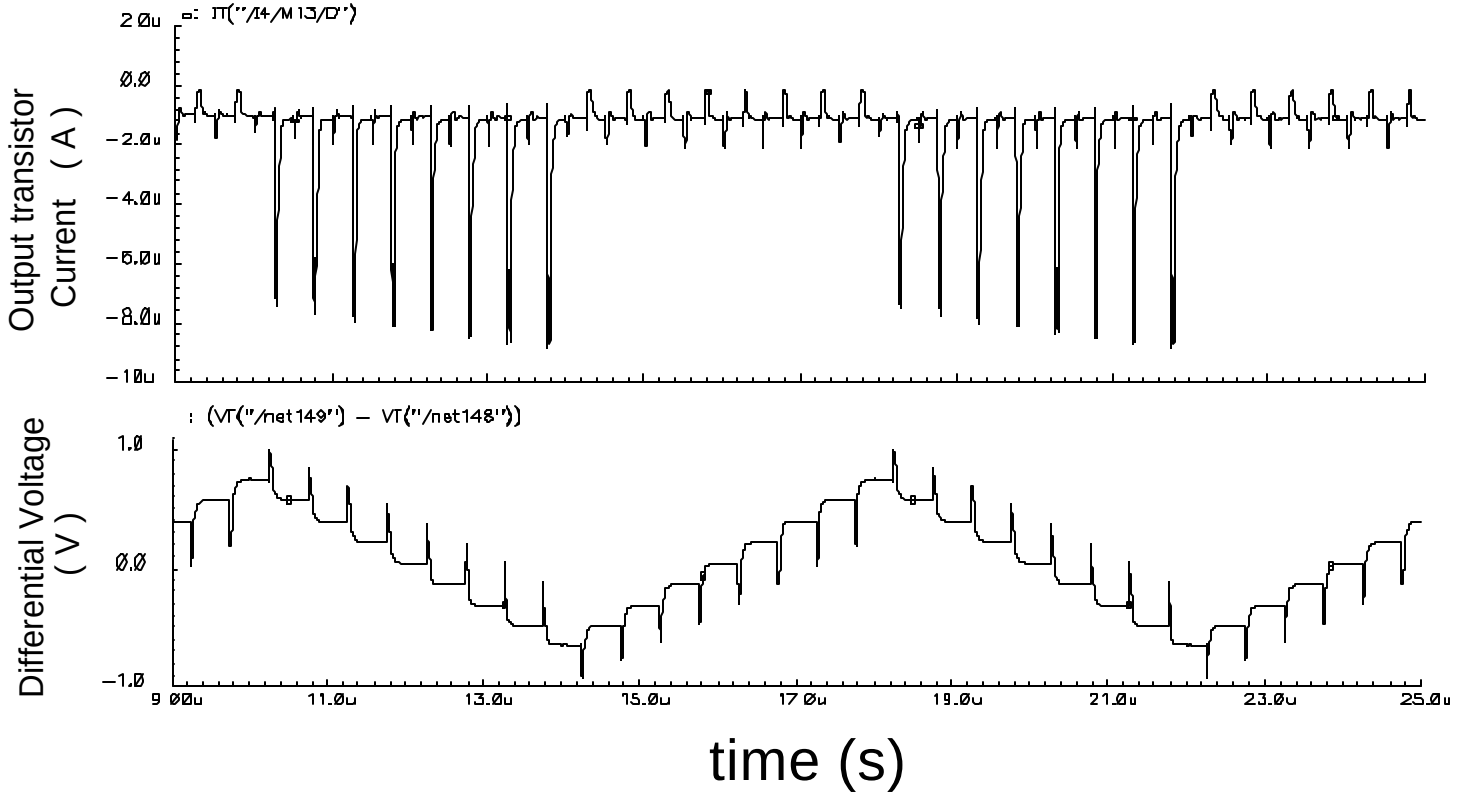


• [Carvajal'02] R.G.Carvajal, J.Galán, J.Ramírez-Angulo, A. Torralba, "Low-power, low voltage differential class-AB OTAs for SC circuits," *Electron. Lett.*, vol.38, no. 22, pp. 1304-1305, Oct. 2002.

• [Galan'02] J.Galán, A.P. VegaLeal, F. Muñoz, R.G.Carvajal, A.Torralba, J.Tombs, J. Ramírez-Angulo, "A 1.1V very low-power SD modulator for 14-b 16 KHz A/D conversion using a novel class AB transconductance amplifier," *Proc. ISCAS*, vol. 2, pp. 616-619, 2002.

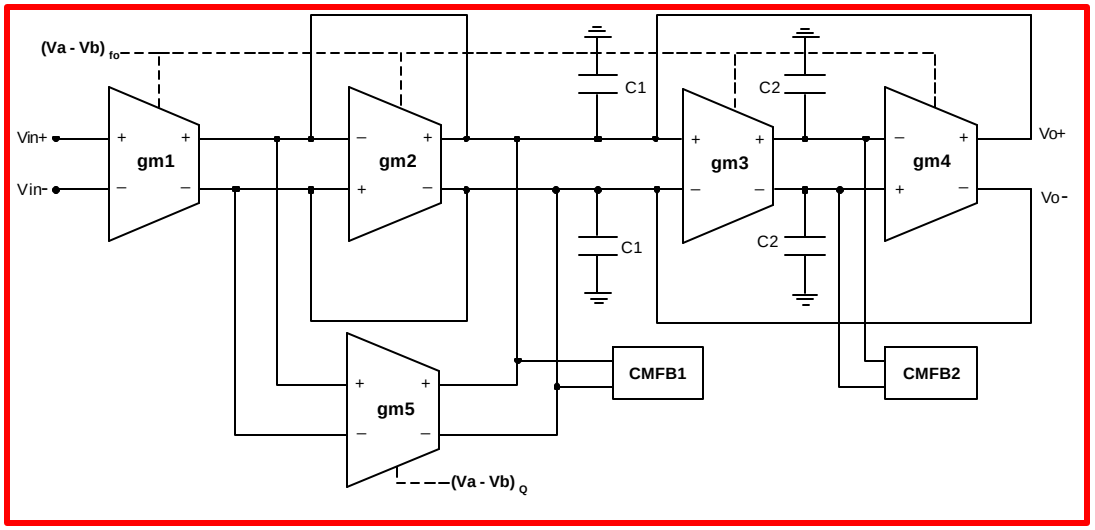
4. FVF-PDP Applications

1.1 V, SC Integrator. 1pF capacitor load, 2MHz switching frequency

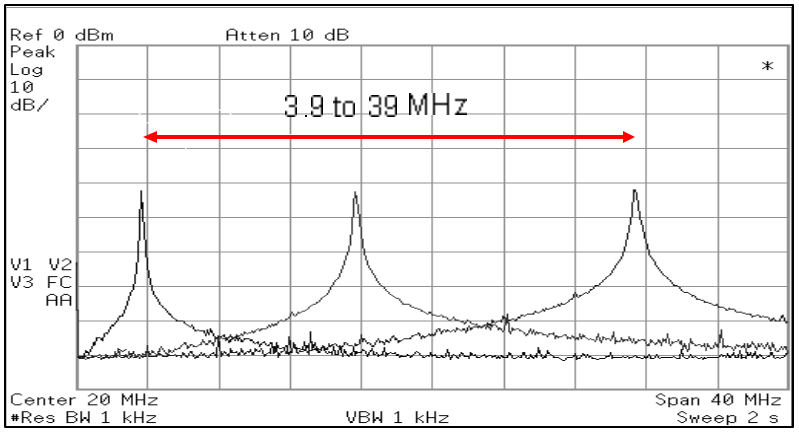


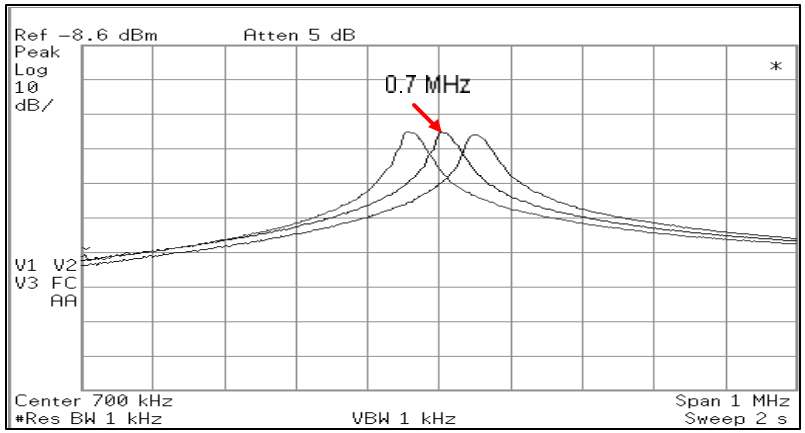
10 V/usec SR with only 11 uA total quiescent current !
(0.35 µm CMOS)

4.FVF-PDP Applications

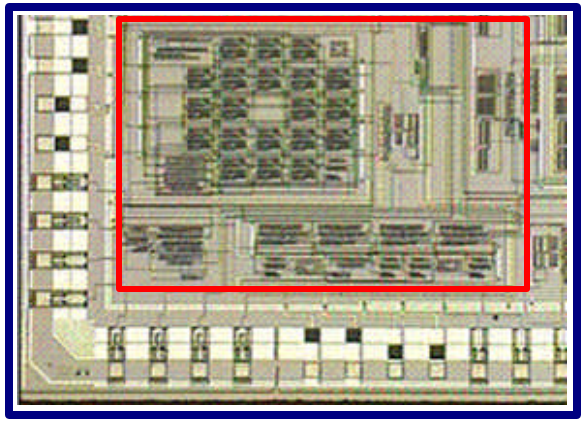


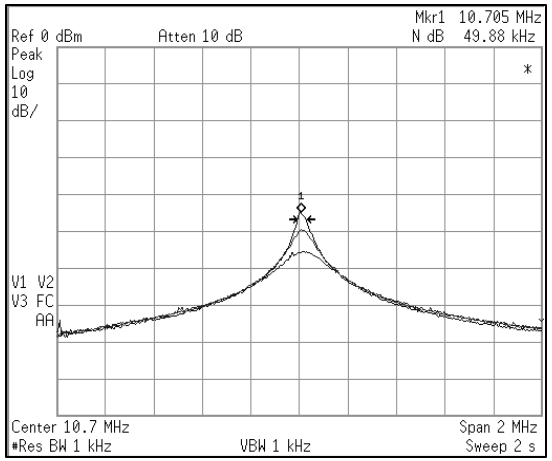
gm-C Filter





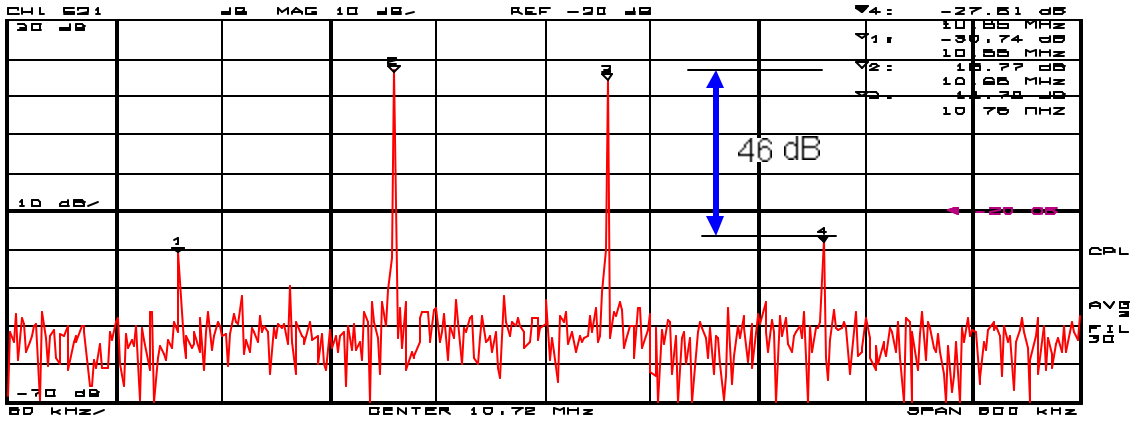
4.FVF-PDP Applications



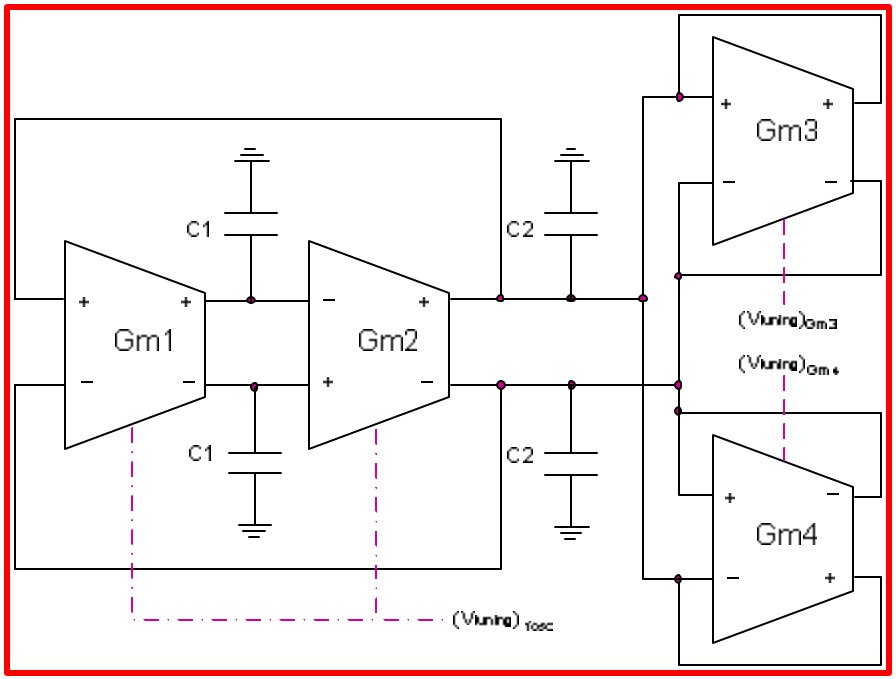


gm-C Filter

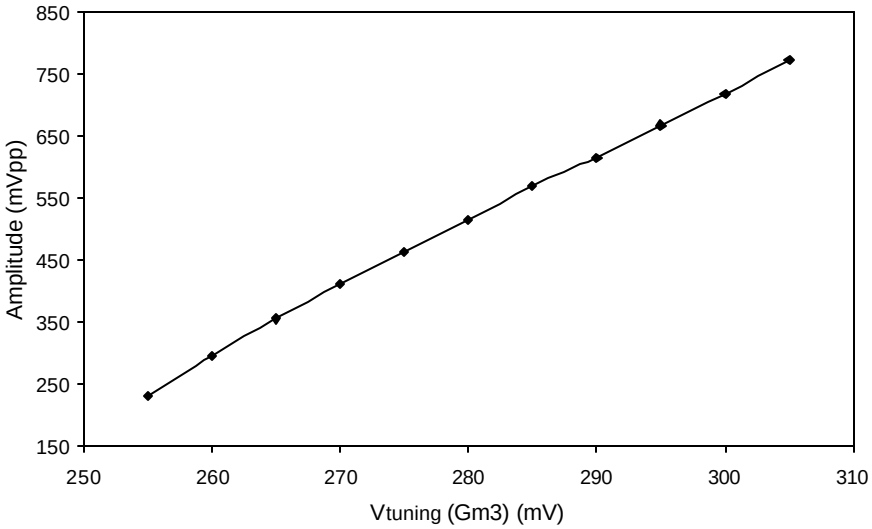
Power supply	2 V
Technology	0.8 μm CMOS
Chip area	1.44 mm^2
Frequency tuning range	300 kHz - 32 MHz
Q range (@10.7MHz)	4 - 501
$V_{o,CM}$ variation in the entire tuning range	14 mV
Power consumption range	**1.18 - 1.8 mW**
THD (@10.7MHz)	- 40dB@200 mV_{pp}
SNR	45 dB
IM3 (@10.7MHz)	46 dB
IIP3	8 dBm
PSRR (@ 10.7 MHz)	39 dB
CMRR (@ 10.7 MHz)	42 dB



4.FVF-PDP Applications



gm-C VCO



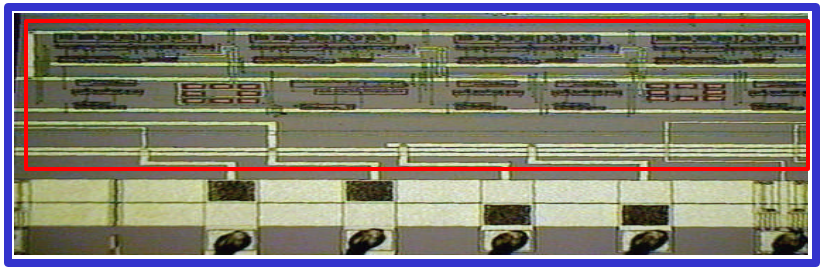
• [Galan'03] J.Galán, R.G.Carvajal, F. Muñoz, A.Torralba, J. Ramírez-Angulo, "A low-power low-voltage OTA-C sinusoidal oscillator with more than two decades of linear tuning range," *Proc. ISCAS*, vol. 1, pp. 677-680, 2003.

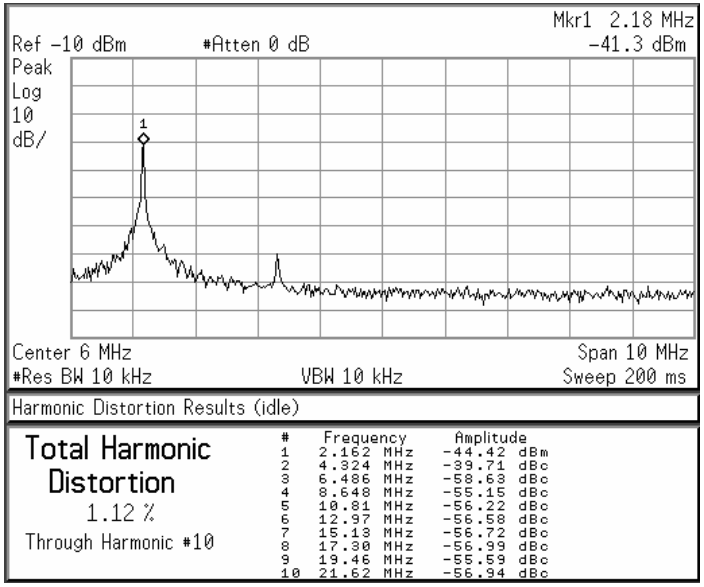
• [Galán'04] J. Galan, R. G. Carvajal, A. Torralba, F. Muñoz, and J. Ramirez-Angulo, A low-power, low-voltage OTA-C simusoidal oscillator with a large tuning range. *IEEE Trans. On CAS-II. (to appear)*

4.FVF Applications

Symmetrical Class-AB Pseudo-Differential Pair (FVF-PDP)

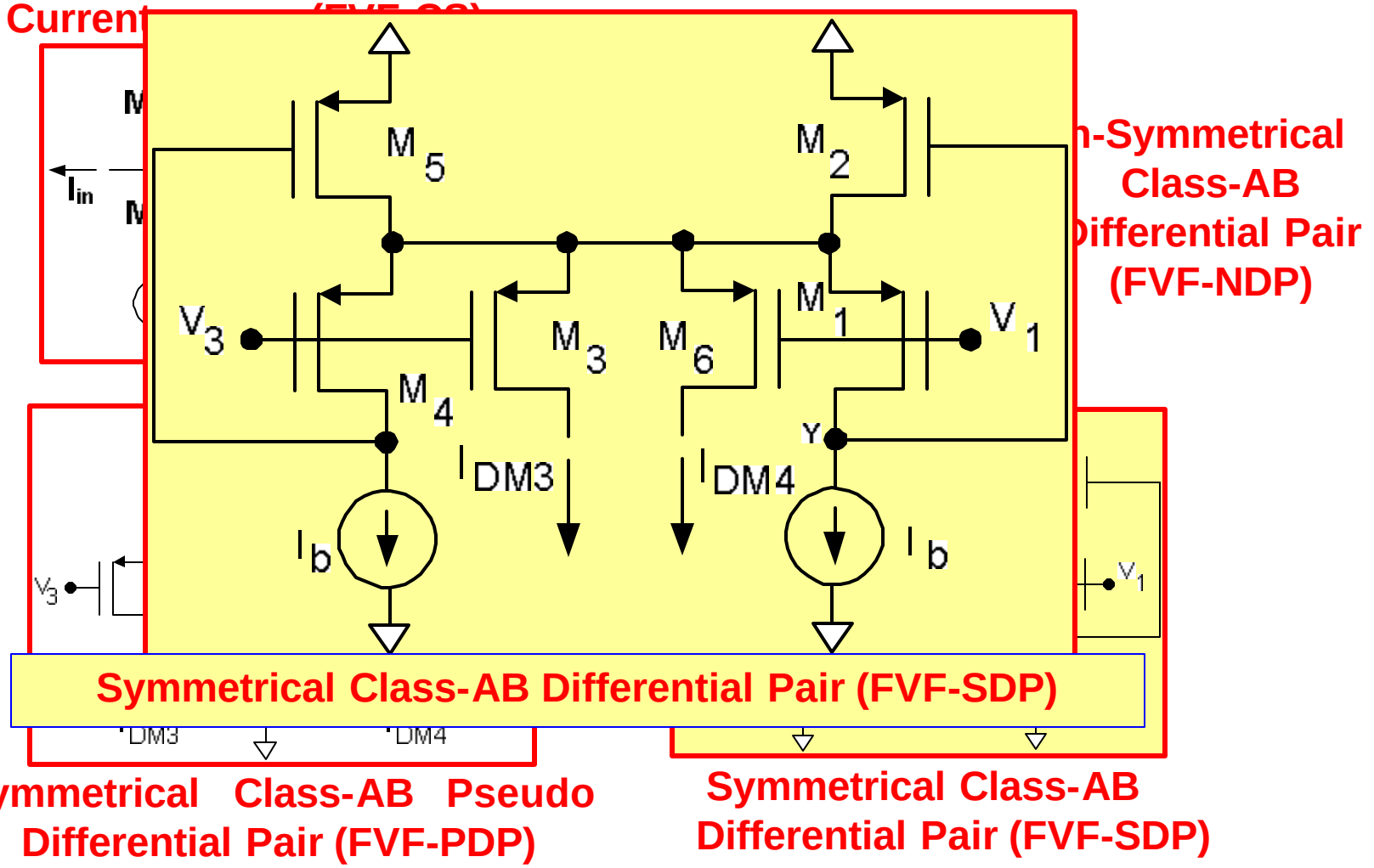
gm-C VCO





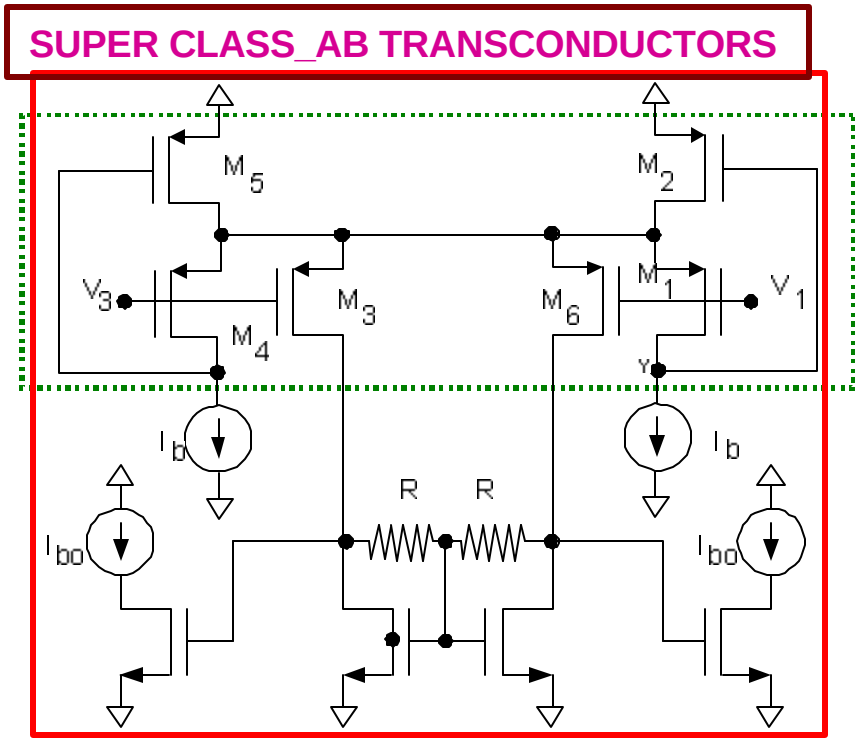
Power supply	2 V
Chip area	0.63 mm^2
Technology	0.8 μm
V_{tuning} control	25 mV- 500 mV
Frequency tuning range	1 MHz- 25 MHz
Power consumption range	**1.05- 1.58 mW**
THD (2 / 25 MHz) @200 mV_{pp}	1.12% / 0.66%
Phase Noise at 10kHz offset	- 67 dBc/Hz

3.FVF Structures. Summary

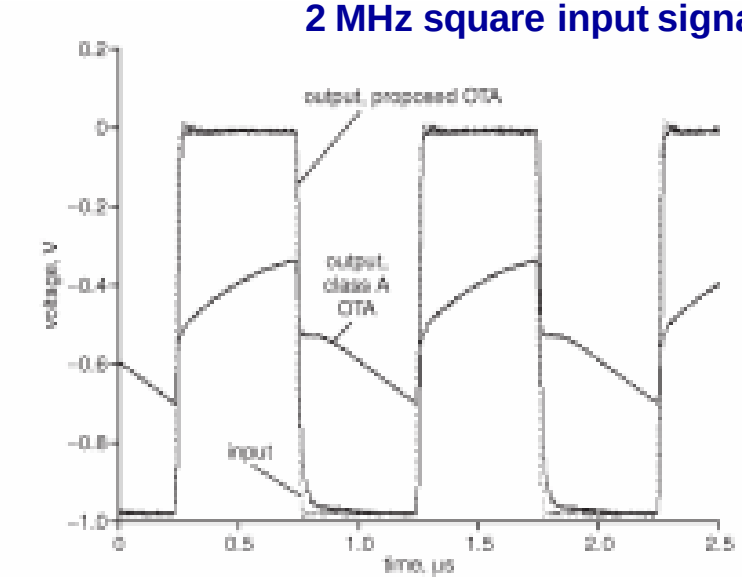


4.FVF-SDP Applications

Symmetrical Class-AB Differential Pair (FVF-SDP)



0.5 µCMOS, V_{DD} = 2 V, C_L = 80pF
2 MHz square input signal

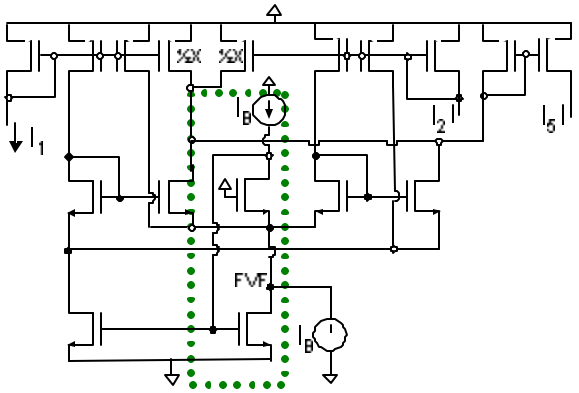


Quiescent power consumption = 120 uW
SR = 78 V/us, 1% settling time = 110 ns
THD (@100 kHz) = 0.15 %

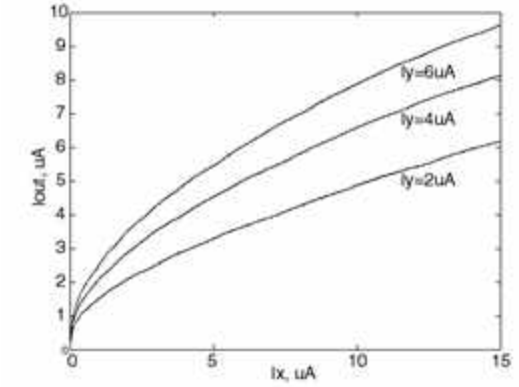
[Baswa'04] S. Baswa, A. López-Martín, R.G.Carvajal, J.Ramírez-Angulo, "Low voltage micro-power super class-AB CMOS OTA," *Electron. Lett.*, vol.40, no. 4, Feb. 2004.

4.Other Applications

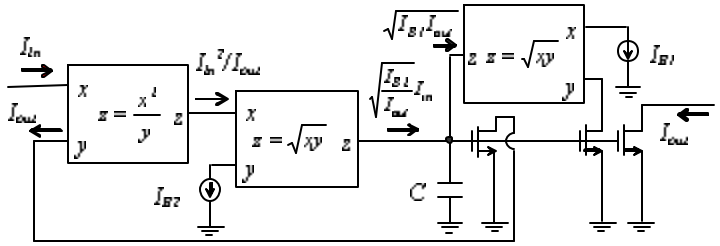
Translinear loops, Geometric Mean, Square-Root Domain Filters, etc.



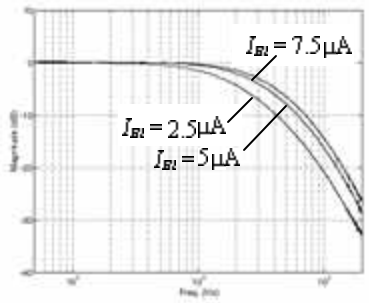
(a)



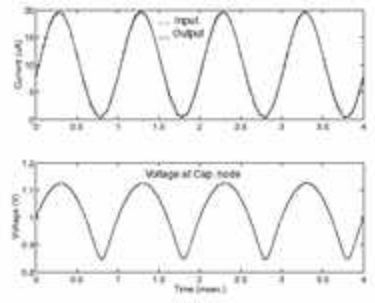
(b)



(a)



(b)



(c)

• A.J. López-Martín and A. Carlosena, "Current-mode multiplier/divider circuits based on the MOS translinear principle", *Analog Integrated Circuits and Signal Processing*, vol. 28, no. 3, pp. 265-278, 2001.

• A.J. López-Martín and A. Carlosena, "Systematic design of companding systems by component substitution", *Analog Integrated Circuits and Signal Processing*, vol. 28, no. 1, pp. 91-106, 2001.

• A.J. López-Martín and A. Carlosena, "A 3.3V CMOS RMS-DC converter based on the MOS Translinear principle", *VLSI Design, 2002*

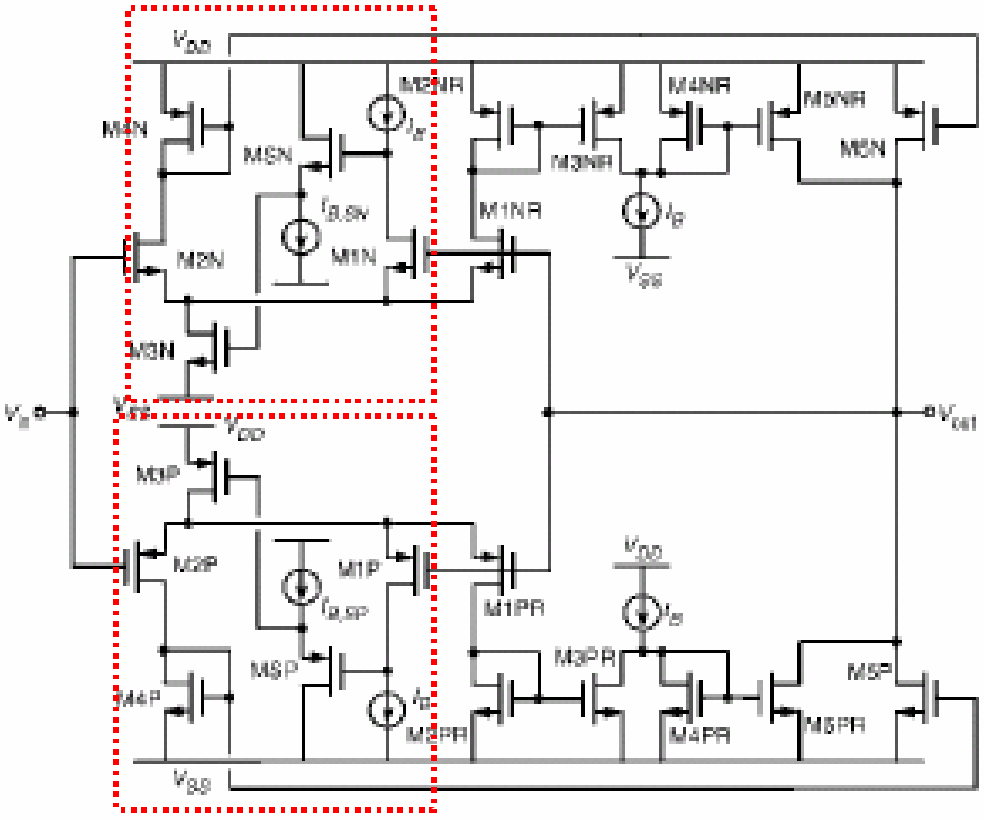
Conclusions

1. A new cell, called *Flipped Voltage Follower (FVF)* has been identified.
2. For low-voltage, low power, class AB operation.
3. Different applications have been reviewed (current mirror, voltage buffer, mixer, OTA, transconductance multiplier and op-amp output stage, filters, VCO, SD modulators…).
4. Simulation and experimental results have been presented that show the potential of the so-called FVF structure.

The End

4. FVF-NPD Applications

CLASS-AB OUTPUT BUFFER



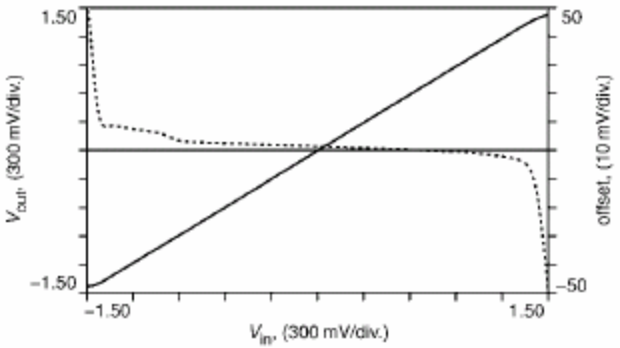


Fig. 3 *DC transfer characteristic of analogue buffer in Fig. 2*
——— output voltage -------- offset voltage

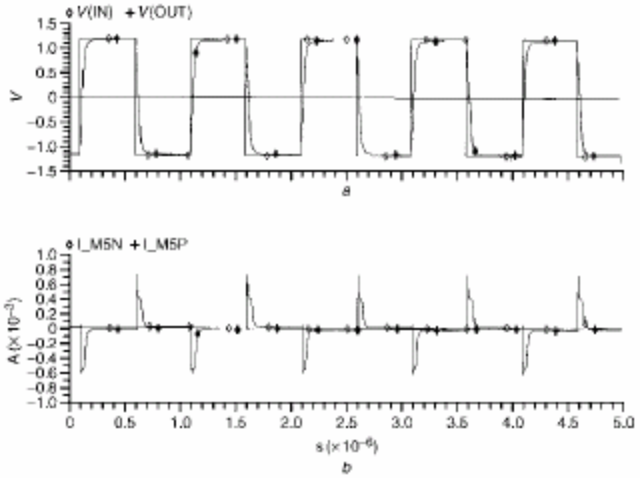


Fig. 4 *Large-signal transient response of buffer in Fig. 2 for 2.4 V_{pp}, 1 MHz square input signal with 10 pF load*
a Input and output voltages *b* Currents through output transistors

[Carrillo'04] J.M.Carrilo R.G.Carvajal,, A. Torralba, J.Duque-Carrillo, "Rail-to-rail, low-power high slew-rate CMOS analog buffer," *Electron. Lett.*, vol.40, no. 14, July 2004.