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Design of two Low-Power full adder cells using GDI structure and hybrid CMOS logic style

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ABSTRACT

Full adder is one of the most important digital components for which many improvements have been made to improve its architecture. In this paper, we present two new symmetric designs for Low-Power full adder cells featuring GDI (Gate-Diffusion Input) structure and hybrid CMOS logic style. The main design objectives for these adder modules are not only providing Low-Power dissipation and high speed but also full-voltage swing.

In the first design, hybrid logic style is employed. The hybrid logic style utilizes different logic styles in order to create new full adders with desired performance. This provides the designer with a higher degree of design freedom to target a wide range of applications, hence reducing design efforts. The second design is based on a different new approach which eliminates the need of XOR/XNOR gates for designing full adder cell and also by utilizing GDI (Gate-Diffusion-Input) technique in its structure, it provides Ultra Low-Power and high speed digital component as well as a full voltage swing circuit.

Many of the previously reported adders in literature suffered from the problems of low-swing and high noise when operated at low supply voltages. These two new designs successfully operate at low voltages with tremendous signal integrity and driving capability. In order to evaluate the performance of the two new full adders in a real environment, we incorporated two 16-bit ripple carry adders (RCA). The studied circuits are optimized for energy efficiency at 0.13 μm and 90 nm PD SOI CMOS process technology. The comparison between these two novel circuits with standard full adder cells shows excessive improvement in terms of Power, Area, Delay and Power-Delay-Product (PDP).

1. Introduction

Addition is a very basic operation in arithmetic. Subtraction, multiplication, division and address calculation are some of the well-known operations based on addition. These operations are widely used in many VLSI applications, since the full adder cell is the building block of the binary adder, enhancing the performance of the 1-bit full adder is a significant goal and has attracted much attention. A variety of full adders using different logic styles and technologies have been reported in literature [1–5] and they commonly aim at reducing power consumption and increasing speed.

Adder performance affects the arithmetic system as a whole. There are two main ways to improve adder's performance in the literature. One is 'System Level viewpoint' approach which is finding the longest critical path in the ripple adders and then shortens the path in order to reduce the total critical path delay. In most situations, the longest signal path is in the propagation of carry out signals to generate the carry out signal of the most significant bit. Another approach is 'Circuit Design viewpoint' in transistor level, that is, design of high-performance full adder core based on transistor level design skills. At the circuit level, an optimized design is required to prevent any reduction in the output signal, consume less power, have less delay in critical path and be reliable even at low supply voltage as we scale towards nano-meter. Good driving capability under different load conditions and balanced output to avoid glitches is also an important point. Since the full adder cells are duplicated in large numbers, layout regularity, and interconnect complexity are also of importance.

By scaling down the feature size of MOSFET devices in nano-meter, the supply voltage should be scaled down to avoid hot-carrier effects in CMOS circuits. In order to keep and increase the speed of CMOS circuits, the threshold voltage has to be scaled down. However, threshold voltage scaling causes an increase in the standby current. As a result, static power becomes a real contributor to total power in nano-scale circuits and needs an efficient power control [6].

Several different static CMOS logic styles have been proposed to implement Low-Power adder cells [7,8]. Generally they are divided

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into two main categories: classical designs which use only one logic style for the whole full adder design and the hybrid CMOS logic styles that use more than one logic style in their structure.

Complementary CMOS (C-CMOS) full adder [8–11] is an example of classical approach. This full adder is based on the regular CMOS structure with PMOS pull-up and NMOS pull-down transistors. One of its merits is its robust structure against voltage scaling and transistor sizing. This circuit provides full-swing which is essential when utilized in a more complex structure. The layout of the C-CMOS full adder is simple, symmetric and efficient due to the complementary transistor pairs however due to employing number of large PMOS transistors in its structure, the input capacitance is large and also the existence of sized up PMOS transistors has a direct impact on its area.

The complementary pass transistor logic (CPL) [8,9,11,12] full adder with swing restoration is another classical circuit. It has a dual-rail structure with 32 transistors. It provides high-speed, full-swing output and good driving capability due to the output static inverters and the fast differential stage of cross-coupled PMOS transistors. The main drawback of CPL is large power consumption due to existence of a number of internal nodes and static inverters which are the primary source of the leakage and static power dissipation.

The other two full adder designs contain transmission function full adder (TFA) [8,9,13] and transmission gate full adder (TGA) [13,14,20]. These designs are based on transmission function theory and transmission gates. Transmission gate [14,15] consists of a PMOS transistor and an NMOS transistor that are connected in parallel which is a particular type of pass-transistor logic circuit. There is no voltage drop problem but it requires double the number of transistors to design a similar function. TFA and TGA are low power consuming and they are suitable for designing XOR or XNOR gates [8–10,16]. The main disadvantage of these logic styles is that they lack driving capability. When TGA or TFA are cascaded, their performance degrades significantly. Hence, in order to improve its weak driving capability additional buffers are needed. These additional buffers increase the power consumption and chip area [8].

The rest of this paper is organized as follows. Section 2 discusses two previously reported full adder designs in hybrid CMOS logic styles. In Section 3, two new approaches in designing Ultra Low-Power full adder cells using GDI technique [17] and hybrid CMOS logic style are proposed. The proposed full adder cells exhibits low PDP, full-swing operation and excellent driving capabilities. Quantitative evaluation and comparisons of two proposed full adders versus four well known state-of-the-art designs is carried out in a real environment which is a two 16-bit ripple carry adders (RCA) in Section 4 and the new adders displayed better performance as compared to the standard full adders. Finally, Section 5 concludes the paper.

2. Review of two well-known hybrid full adder cells

The hybrid logic style uses different logic styles in order to create new full adders with desired performance. As an example, Hybrid-CMOS full adder [7], shown in Fig. 1, could be mentioned. This circuit utilizes a novel XOR-XNOR design to produce internal signals (Module.1). Module.1 is based on complementary pass transistor logic (CPL) and one inverter. The first half uses only NMOS pass transistors for generating the output. This circuit is inherently fast due the use of high mobility NMOS transistors and fast differential cross-coupled PMOS transistors. The main drawback of this circuit is large power consumption due to the use of CPL structure [8,11] and also an inverter which is the primary source of static power dissipation in nano-scale circuits. In order to implement module.3 (Cout output) this circuit uses four transistors XOR gate [18] and one inverter. As discussed in [7], the first part of module.3 is inherently Low-Power due to its pass transistor structure, but as mentioned in [7], they suffer from lack of driving capability. The output inverter is added in order to improve driving capability in a cascaded situation which simultaneously increases the power consumption and the area. Finally this design uses a new hybrid circuit for implementing module.2 (SUM output). Module.2 uses the Low-Power consuming Transmission Gates and the robust static-CMOS logic style to create a new SUM output. It utilizes ten transistors and possesses the properties of both static-CMOS and Transmission gates logic styles. As discussed in [8], because of employing large PMOS transistors in static-CMOS logic style, the input capacitance is large and also

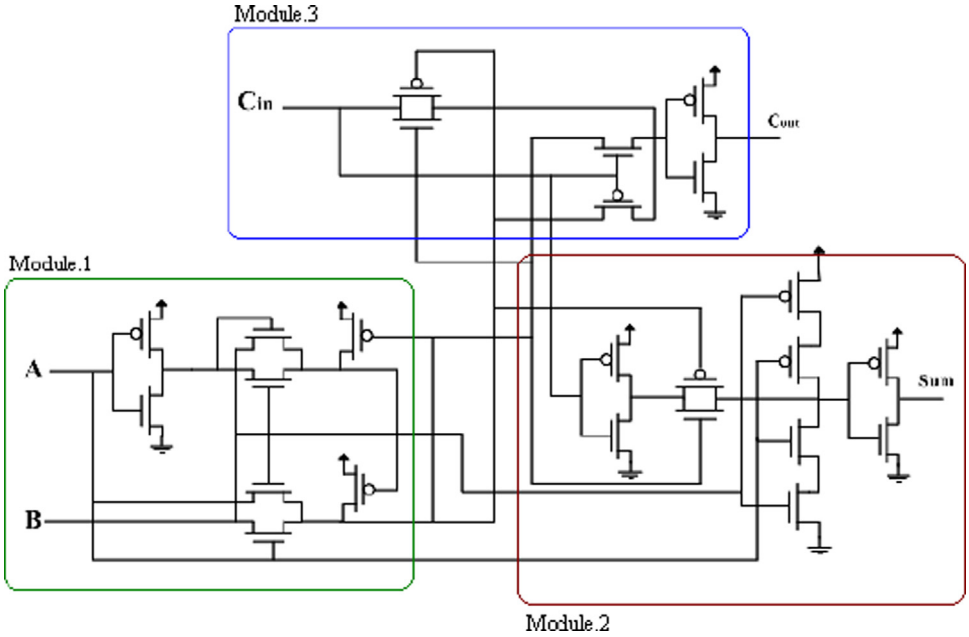

Fig. 1. Hybrid-CMOS full adder.

the existence of sized up PMOS transistors has a direct impact on its area. Moreover the series transistors in the output create a weak driver. Hence, additional inverter at the last stage is required to provide the necessary driving power [8], which results in higher power consumption.

Another hybrid adder is ULPFA (Ultra Low-Power Full Adder) [19]. Fig. 2 shows the hybrid structure of this full adder which is a combination of Pass Transistor Logic and static-CMOS Logic style. This adder utilizes special voltage restorer called ULPD (Ultra Low-Power Diode) that eliminates the speed problem of the conventional voltage restorer in order to create full swing voltage output. ULPD is illustrated in Fig. 3. The ULPD is discussed in [20,21]. It has a strongly reduced leakage current when compared to a standard MOS diode.

The ULPD is created by the combination of a NMOS and a PMOS transistor, as shown in Fig. 3. It has low leakage current in a reverse biased situation due to operation of both NMOS and PMOS with negative voltages V_{GS}.

As studied in [19], by increasing the reverse bias voltage, the reverse current of ULPD is increased because of increasing in V_{DS} of PMOS and NMOS transistors but after reaching a maximum value it will largely decreases due to V_{GS} of both transistors becoming more negative. This results in a negative resistance region that could be used in level restoration. [19,22] shows that in order to have higher reverse current peak in the negative resistance region, Depletion-Mode NMOS and Depletion-Mode PMOS must be used to ensure sufficient level of restoration in a timely fashion. In this paper, MOSFETs in depletion mode with an absolute threshold voltage of 0.23 V are used for 0.13 μm and with an absolute threshold voltage of 0.18 V for 90 nm.

Fig. 4 illustrates the use of ULPD level restorer in low logic and high logic levels. It takes advantage of capabilities of MOSFET in depletion mode. C_{node} shows the input parasitic capacitance at the non full-swing node. The operation of low logic restoration is depicted in Fig. 4(a). When V_{node} is between 0 and $V_{dd}/2$, ULPD is

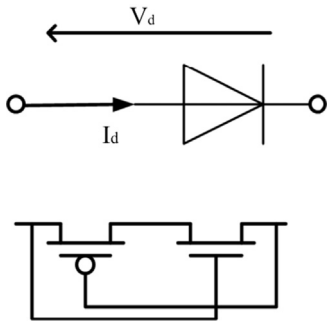

Fig. 3. ULPD (Ultra Low-Power Diode).

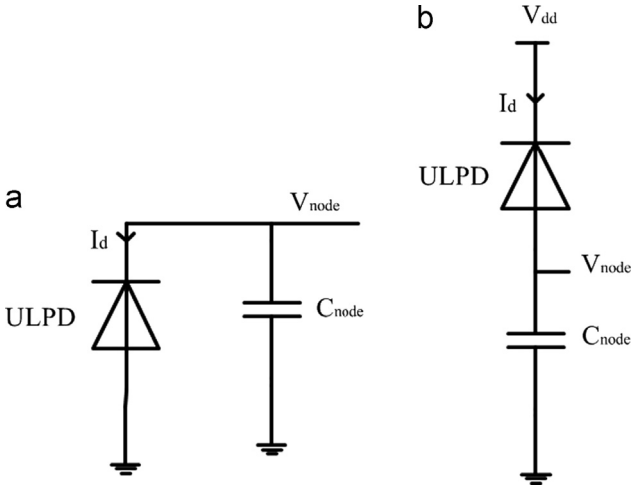

Fig. 4. (a) ULPD low-logic-level restorer and (b) ULPD high-logic-level restorer.

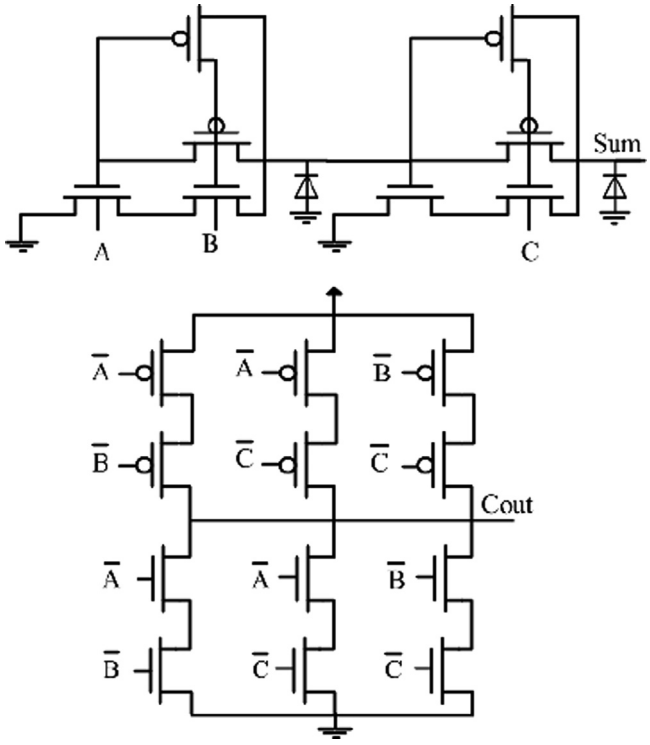

Fig. 2. ULPFA using the ULPDs.

in its negative resistance region and because of the reverse biased situation, the ULPD current I_d is positive and discharges C_{node}. For V_{node} comprised between $V_{dd}/2$ and V_{dd}, both NMOS and PMOS transistors are turned off due to operation with negative voltages V_{GS}. Hence there is no current in ULPD. On the other hand Fig. 4 (b) shows the operation of high logic level restoration. When V_{node} is between $V_{dd}/2$ and V_{dd}, ULPD is in its negative resistance and due to its reverse biased state; I_d is positive and charges C_{node} to V_{dd}.

ULPFA uses Low-Power XOR-XNOR gates [23] which are implemented with Pass Transistor Logic style in order to produce the SUM output and by utilizing ULPD voltage level restorer, the drawbacks of previously reported level restorers such as delay, noise and power consumption are eliminated. For designing the C_{out} circuit, static-CMOS logic style is employed in order to obtain the properties of static-CMOS logic style. This circuit is robust against voltage scaling and transistor sizing but, the disadvantages of this circuit are high input capacitance and high area consumption due to the use of low-mobility large PMOS in its structure and also the series transistors in the output create a weak driver. Moreover this design needs the inputs to be inverted (complemented inputs) in order to eliminate the additional inverter at the output node which could be consider as another drawback of this design. Non-symmetrical and non-regular layout due to the combination of two different logic styles for designing SUM and C_{out}, is another negative point of this full adder cell.

In the next section we present two novel Low-Power full adder cells using GDI and hybrid techniques.

3. Hybrid and GDI FULL adders

3.1. Hybrid full adder

In this section we introduce a novel Low-Power full adder, which has good characteristic in terms of speed and power. Our design is based on SEMI XOR-XNOR gates (Lack of ability to generate all of the possible outputs in conventional XOR-XNOR gates). Fig. 5 demonstrates the circuits of these gates and Table 1 depicts the Truth-Table of these two gates.

In [2] SEMI XOR-XNOR gates have been employed, however in this paper a new C_{out} circuit structure is proposed, which results in having a modular, flexible, robust and Low-Power circuit.

Table 2 demonstrates the Truth-Table of SUM and C_{out} of the full adder cell. As can be seen in Table 2, the SEMI XOR gate has the ability to generate the first four states of the sum output, with the remaining states produced with the SEMI XNOR gate. As depicted in Table 1, in order to design the SUM circuit, these SEMI XOR-XNOR gates could be employed with C_{in} input used as a selector. When C_{in} is equal to '0', the SEMI XOR gate is similar to the SUM, and when C_{in} is equal to '1', the SEMI XNOR gate is more like the remaining states of the SUM. Hence the proposed structure for SUM circuit is illustrated in Fig. 6. As mentioned before, SEMI XOR and SEMI XNOR circuit cannot generate all the possible outputs of the SUM and the depicted high impedance states would cause a malfunction in the circuit. One of these two situations occurs when 'A' and 'B' inputs are equal to '1' and C_{in} input is '0'. In order to have the correct value at the output node, we have to add one more transistor to compensate for the inability of the presented circuit in this specific state. If we connect the output of the SEMI XNOR gate to the gate of one NMOS transistor, where the source/drain of this transistor is connected to SUM output and its drain/source is connected to the C_{in}, the high impedance states in the output will be set to the correct value. It is significant to know that this new added NMOS transistor is turned on in two situations when the output of SEMI XNOR gate is equal to '1', where the output of the SUM in these two states is equal to the C_{in}. Therefore by connecting the C_{in} to the drain/source of this NMOS, there would be no adverse effect to the circuit functionality.

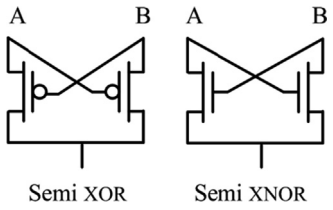

Fig. 5. Schematic of SEMI XOR and SEMI XNOR gate.

Table 1
Truth-Table of SEMI XOR and SEMI XNOR gate.

A	B	SEMI-XOR	SEMI-XNOR
0	0	0	HZ
0	1	1	0
1	0	1	0
1	1	HZ	1

Table 2
Truth Table of SUM and C_{OUT}.

C_{in}	B	A	SUM	C_{out}	SEMI-XOR	SEMI-XNOR
0	0	0	0	0	0	HZ
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	HZ	1
1	0	0	1	0	0	HZ
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	HZ	1

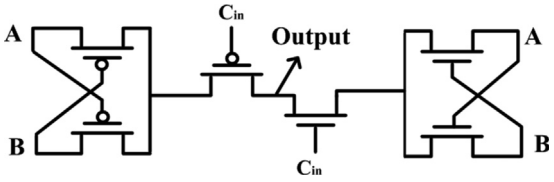

Fig. 6. Incomplete SUM generator cell.

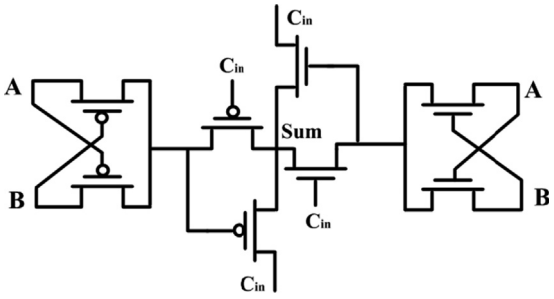

Fig. 7. Complete SUM generator cell circuit.

Finally in order to eliminate the other high impedance situation, for properly operating as a SUM generator, one more transistor must be added to the circuit. As Table 2 shows this situation occurs when 'A' and 'B' are equal to zero and C_{in} is 1. If we connect the SEMI XOR output to the gate of one PMOS while the source/drain of this transistor is connected to the SUM output and its drain/source is connected to the C_{in}, the last undesirable behavior of the circuit would be eliminated. It is notable that the new added PMOS transistor is only turned on in two states when the SEMI XOR gate output is equal to '0'. In these two states the output of the sum generator is equal to C_{in}, which results in a new design for the SUM generation part of a full adder. Final schematic of SUM generator is shown in Fig. 7.

In the next step, the C_{out} generator is constructed with a different outlook in comparison with the previous circuits. Table 2 illustrates the Truth-Table of C_{out} function and as can be seen the first four outputs of the SEMI XNOR gate are similar to the C_{out} and also the remaining states of the C_{out} are equal to the output of the SEMI XOR gate. If the C_{in} input is utilized as a controller, a new C_{out} generator circuit will be implemented. This circuit is shown in Fig. 8. Due to the inability of the SEMI XOR-XNOR gates in producing all the states of the real XOR-XNOR gates, two undesired high impedance situations are created in the proposed design. In order to eliminate this problem, two more transistors are added to the C_{out} generator part to generate the desired value of the output. According to Table 2, one of these situations occurs when all of the full adder inputs are equal to zero, so by connecting the output of SEMI XOR to the gate of one PMOS connecting its source to the output and its drain to the GND, one of the high impedance states is eliminated resulting in creating the correct value of logic '0' at the output. Finally for eliminating the last high impedance situation, which arises when all of the inputs are equal to logic '1', a new NMOS, with its gate connected to the output of the SEMI XNOR gate, its drain connected to V_{dd} and the source linked to the C_{out} output, is attached to the circuit. Fig. 9 depicts the proposed full adder.

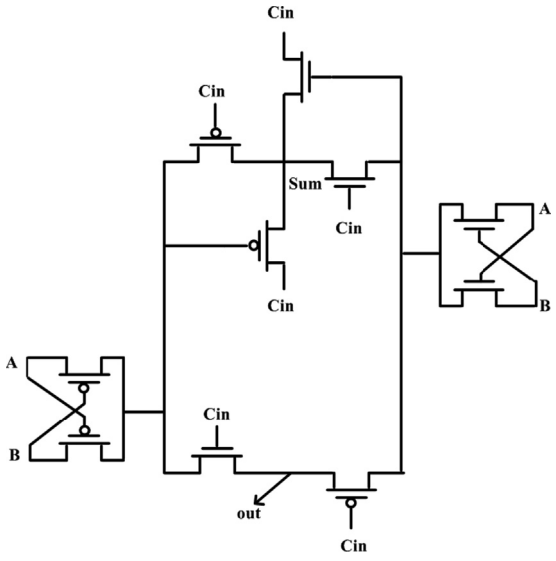

Fig. 8. Incomplete full adder cell.

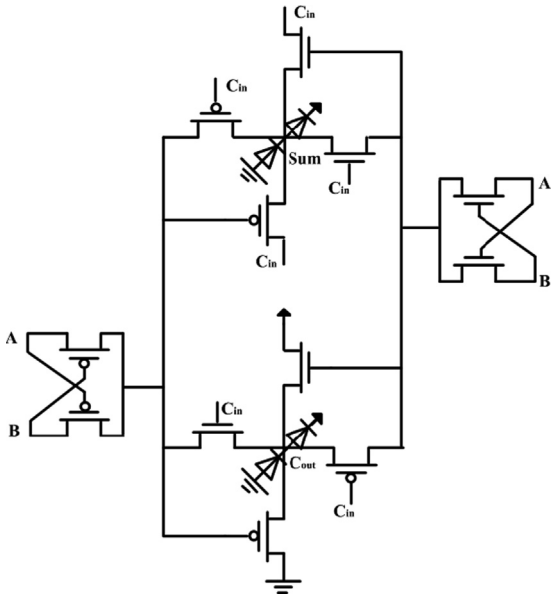

Fig. 9. Proposed hybrid full adder cell.

As shown in Fig. 9, in order to provide full-swing voltage at SUM and C_{out}, we take advantage of using ULPD level restorer [19,20] in the structure of the proposed hybrid full adder cell. As it is apparent, this novel hybrid adder cell minimizes the static power consumption by eliminating any possible direct path between V_{dd} and the ground due to the use of NMOSs and PMOSs in a complementary manner. By utilizing this technique, when each part of the circuit is in the conducting mode, the other part is in the off situation, so there is no short-circuit current. Moreover, by utilizing ULPD level restorer not only the leakage current is eliminated but also this capable device provides good driving capability which is essential when this circuit is used in a cascaded or a more complex situation. Using ULPD as level restorer eliminates the need of output buffers which are the main source of static power consumption. This design uses 20 transistors and because of its low transistor count in comparison with its counterparts, our proposed hybrid design has low dynamic power dissipation due to its low switching capacitance. In terms of the speed, this circuit is superior to the previously reported full adder cells. As it is apparent it has just two transistors in the critical path for driving the output.

3.2. GDI-MUX full adder

In this section a new approach for designing full adder cell eliminating the need for complicated XOR-XNOR gates is introduced. In the second step the implementation of this Ultra Low-Power circuit using GDI technique [17] is discussed.

By considering the full adder's Truth-Table in Table 2, it can be seen that C_{out} is equal to (A AND B) when C_{in}='0', and C_{out} is equal to (A OR B) when C_{in}='1'. Thus, a multiplexer can be used to obtain the C_{out} output. Following the same criteria, the SUM output is equal to (A OR B OR C_{in}) when C_{out}='0', and SUM is (A AND B AND C_{in}) when C_{out}='1'. Again, C_{out} can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full adder cell can be formed by AND, OR and MUX logic blocks as shown in Fig. 10.

In order to have an implementation of this alternative logic scheme, GDI technique is used. The basic GDI cell is shown in Fig. 11 while the Truth-Table is shown in Table 3. The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are linked to N or P, so it can arbitrarily be biased at contrast to a CMOS inverter. These features give the GDI cell two extra input pins to use, which makes the GDI design more flexible than usual CMOS design. The GDI scheme requires silicon on insulator (SOI) process in order to be implemented. As stated in [17], GDI is suitable for designing

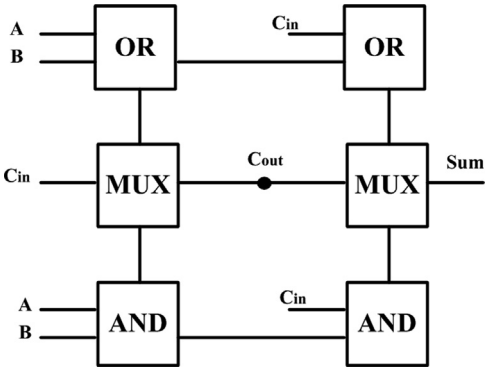

Fig. 10. Novel and alternative logic scheme for designing full adder cell.

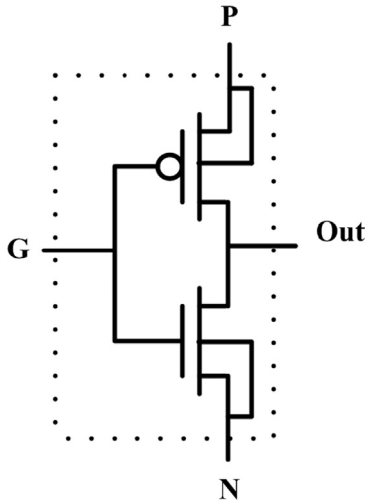

Fig. 11. Basic Gate-Diffusion Input (GDI) cell.

fast, Low-Power circuits, using a reduced number of transistors (as compared to CMOS and Pass Transistor Logic techniques), while improving logic level swing and static power characteristics. Moreover GDI solves the problem of Top-Down design complexity of Pass Transistor Logic which has no simple and universal cell library preventing them from having a major role in real VLSIs [24], by providing small cell library.

The proposed GDI-MUX full adder is shown in Fig. 12. In order to implement (A OR B), N input is connected to V_{dd}, P is connected to B and G is connected to A, hence as shown in Fig. 12, Module.1 is GDI implementation of (A OR B). In the next step (A AND B) is designed by connecting G, N and P to A, B and GND respectively. Module.2 in Fig. 12, illustrates the implementation of (A AND B). For producing C_{out}, C_{in} is connected to G input of GDI as selector and N is connected to (A OR B) and P is connected to (A AND B). Fig. 12 shows the implementation of multiplexer (module. 3). Following the same criteria, (A OR B OR C_{in}) is implemented in Module. 4 by connecting G input to (A OR B), P to C_{in} and N to V_{dd}. Module.5 shows (A AND B AND C_{in}) by connecting G input to (A AND B), P to GND and N to C_{in}. Finally in order to produce the SUM, GDI is used as a multiplexer with its G input connected to C_{out} and finally its P and N inputs are linked to (A OR B OR C_{in}) and (A AND B AND C_{in}) respectively.

Table 3
Truth table of the basic GDI cell.

N	P	G	Out	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
0	1	A	$\overline{A}$	NOT

As can be seen ULPD level restorer is used to provide full swing output. This novel design takes advantage of using GDI technique which is proved [17] as one of the effective structures in designing Low-Power circuits. As stated in [17], this new approach minimizes both static and dynamic power consumption. This design uses ULPD level restorer to eliminate the leakage current and also providing good driving capability which is necessary in a cascaded situation. Using ULPD as level restorer eliminates the need for output buffers which are the main source of static power consumption. This design also uses 20 transistors and has low dynamic power dissipation due to its low switching capacitance.

4. Simulation results and analysis

In this section, the two proposed full adder cells shown in Figs. 9 and 12 are evaluated and compared to the ones chosen from the literature. All the circuits are implemented using Cadence layout editor and extracted using 0.13 μm and 90 nm PD SOI CMOS technology. Simulations are carried out using HSPICE, with the capacitances extracted from the layout. The full adder cells are simulated with 100 MHz frequency and at 27 °C and the supply voltages varying from 0.8 to 1.4 V for 0.13 μm and 0.6 to 1.2 V for 90 nm. The threshold voltages of the PMOS and NMOS transistors are around 0.34 V for 0.13 μm and 0.27 V for 90 nm, respectively. Different loading conditions are also considered to evaluate the performance of the test circuits. Loading conditions are varying from 5 to 100 fF for 0.13 μm and 1 to 70 fF for 90 nm.

It has been a common practice to treat the full adder cell as a standalone cell in simulation [16,25-27]. It is also not unusual that the full adder cells that perform well in such simulation still fail upon actual deployment because of the lack of driving power. This is because full adder cells are normally cascaded to form a useful arithmetic circuit. Therefore, the full adder cells must possess sufficient drivability to provide the next cell with clean inputs [9].

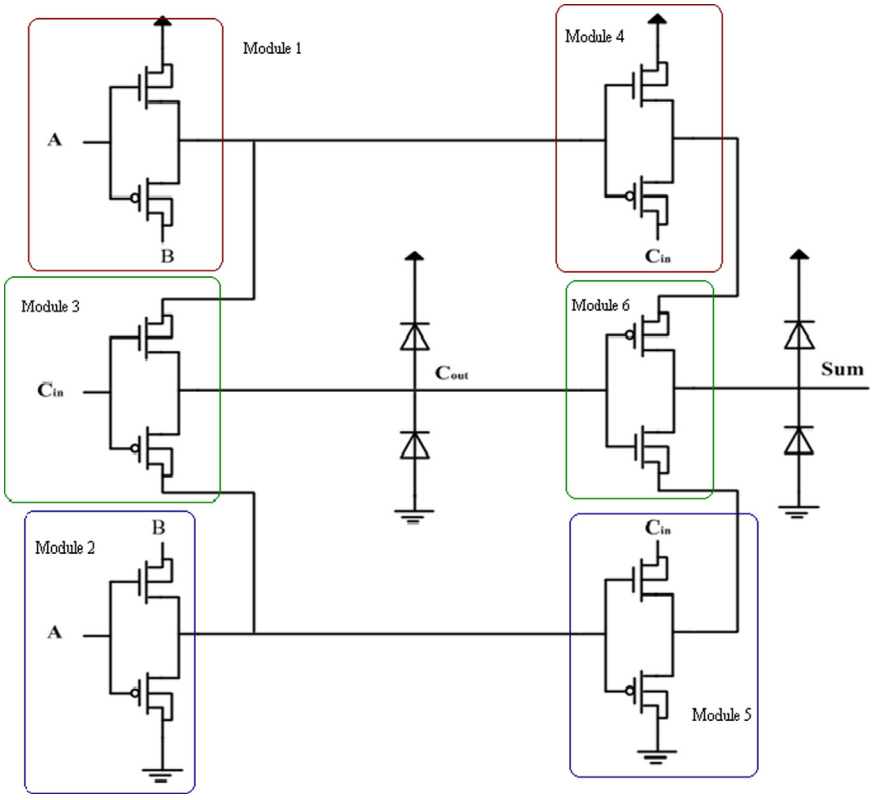

Fig. 12. Proposed GDI-MUX full adder.

Otherwise, the performance of the circuit will be degraded dramatically or become non-operative at low supply voltage.

In order to have a practical application for the proposed circuit, the suggested structure for simulation, which is made of 16 cascaded full adder cells, is shown in Fig. 13. This structure simulates the circuits like regular multipliers and binary adders that use full adder cells as the building block. The inputs are fed from the buffers to give more realistic input signals and the outputs are loaded with buffers to give proper loading condition.

An input transition may or may not result in change at the output node. Even if there is no switching at the output node, some internal node may be switching which results in power consumption. For an accurate result, all the required input-pattern-to-input-pattern transitions are included in the test patterns. The power consumption value and delay are measured for the whole 16 bit adder. The input and output waveforms of the ninth cell are shown in Fig. 14.

Comparison of full adder cells is discussed below in five subsections referred to Delay, Power, PDP, Area and Immunity to noise.

4.1. Delay

The values of delay obtained based on post layout simulation for considered values of (0.8–1.4 V) and load (5–100 fF) in 0.13 μm

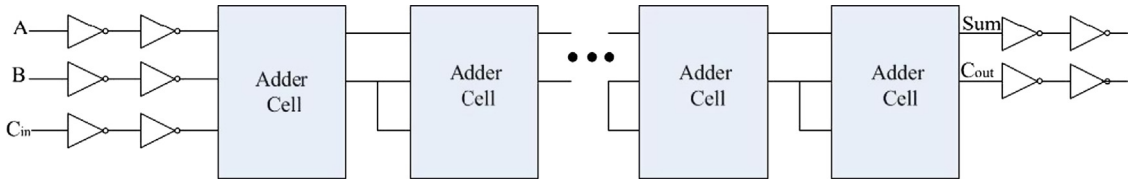

Fig. 13. 16 bit test-bench structure.

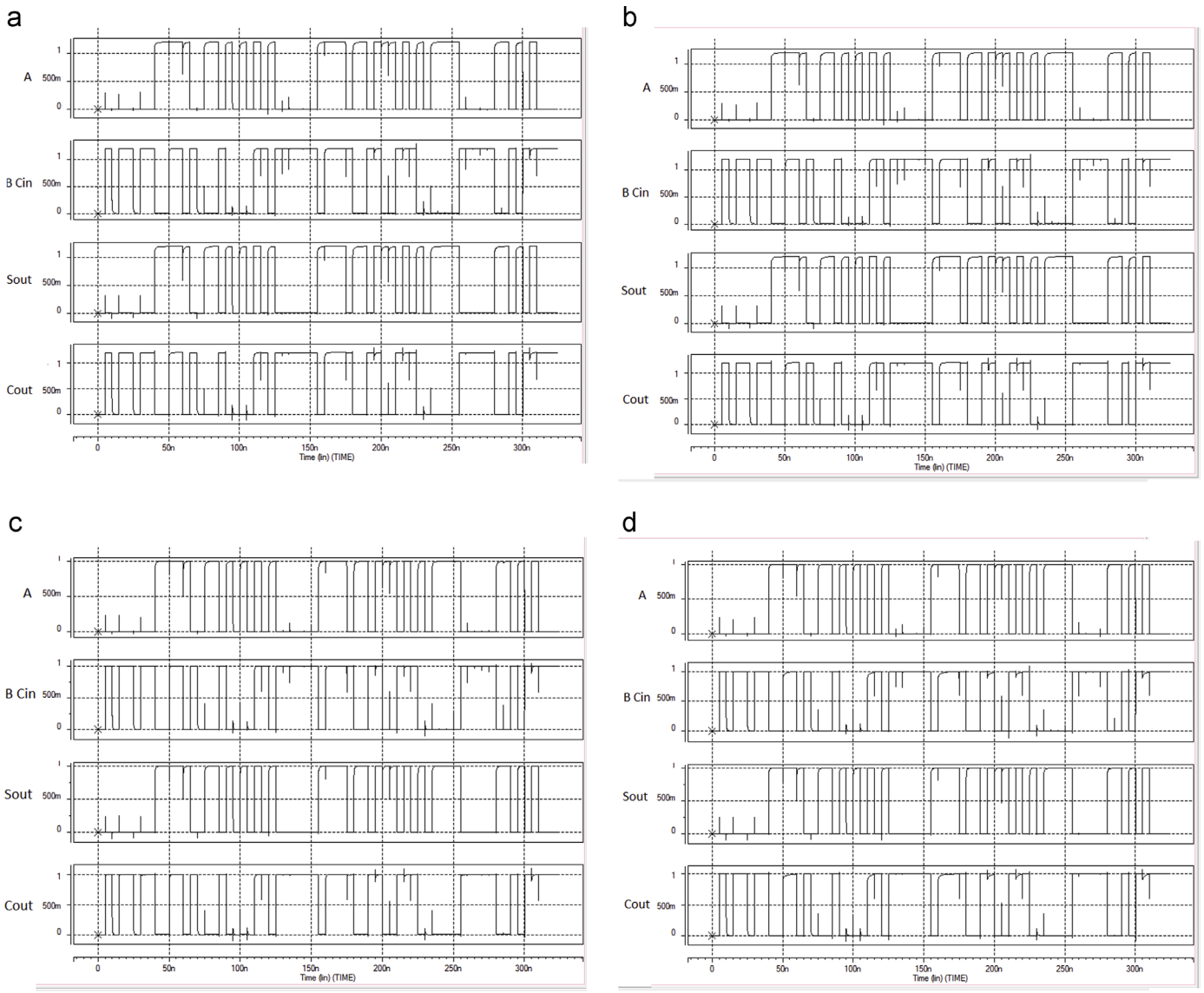

Fig. 14. The input and output waveforms of the ninth full adder cell. (a) Proposed hybrid full adder in 0.13 μm, (b) GDI-MUX full adder in 0.13 μm, (c) proposed hybrid full adder in 90 nm and (d) GDI-MUX full adder in 90 nm.

and (0.6–1.2 V) and load (1 to 70 fF) in 90 nm for C-CMOS, CPL, Hybrid full adder in Fig. 1, ULPFA and the two new full adder cells are shown in Figs. 15–18(a). Likewise in Figs. 22 and 23(a), delay value of the 16-bit adder based on each full adder cells is illustrated. Tables 4 and 5 show the delay values at 1.2 V for 0.13 μm and 1 V for 90 nm respectively.

For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. It is apparent that among the existing full adders, the proposed hybrid full adder cell has the smallest delay because of just having two transistors in the critical path for driving the output. The GDI-MUX full adder follows the hybrid adder in outperforming the other four full adder cells in delay. These two novel full adder cells could be considered as the fastest ones because of their different and symmetrical structure which reduces the critical inputs and outputs path to 3 transistors in the worst case and also because of using ULPD for their voltage restoration. When output load is increased, the proposed hybrid full adder and the GDI-MUX full adder show the best performance. The proposed hybrid full adder shows minimum delay at all supply voltages when compared to the C-CMOS, CPL, Hybrid full adder in Fig. 1 and ULPFA full adders. At 1.2 V in 0.13 μm, the proposed hybrid adder is 55%, 46%, 44%, and 21% faster than C-CMOS, CPL, Hybrid full adder in Fig. 1 and ULPFA full adders, respectively. At 1 V in 90 nm, the proposed hybrid adder is 58%, 53%, 34%, and 17% faster than C-CMOS, CPL, Hybrid full adder in Fig. 1 and ULPFA full adders.

After the two proposed novel full adders, ULPFA outperforms the others because of using ULPD in its design.

Among the remaining previously reported full adders, Hybrid full adder in Fig. 1 shows the least delay because of utilizing a novel XOR-XNOR design to produce internal signals, which is based on complementary pass transistor logic (CPL). The first half of the circuit utilizes only NMOS pass transistors for generating the output and because of using high mobility NMOS transistors and fast differential cross-coupled PMOS transistors, this circuit is fast. Overall, the proposed full adders have good speed response at different voltages owing to their novel structure and taking advantage of ULPD.

4.2. Power

The average power consumption for C-CMOS, CPL, Hybrid full adder in Fig. 1, ULPFA and the two new full adder cells are determined under different supply voltages (0.8–1.4 V) and load (5–100 fF) in 0.13 μm and (0.6–1.2 V) and load (1 to 70 fF) in 90 nm and are shown in Figs. 15–18(b) respectively. Figs. 22 and 23 (b) illustrate the values of power consumption of the 16-bit adder based on each full adder cells. Tables 4 and 5 illustrate the values at 1.2 V for 0.13 μm and 1 V for 90 nm.

Among the conventional full adders, CPL consumes the most power because of its dual-rail structure, high number of internal nodes in its design and utilizing static inverters which are the primary source of leakage and static power dissipation.

The proposed GDI-MUX full adder shows the best performance among the above mentioned full adders under varying supply voltages. The GDI-MUX full adder utilizes GDI structure as its main cell which is proved in [17] to be one of the lowest power consumer cells that not only is suitable for designing fast, Low-Power circuits but also improves logic level swing and static power characteristics. The GDI-MUX full adder cell also takes advantage of using ULPD in its structure as its output voltage restorer. The ULPD has a strongly reduced leakage current when compared to a standard MOS diode. Employing ULPD resolves the drawbacks of conventional feedback voltage restorer transistors which are low

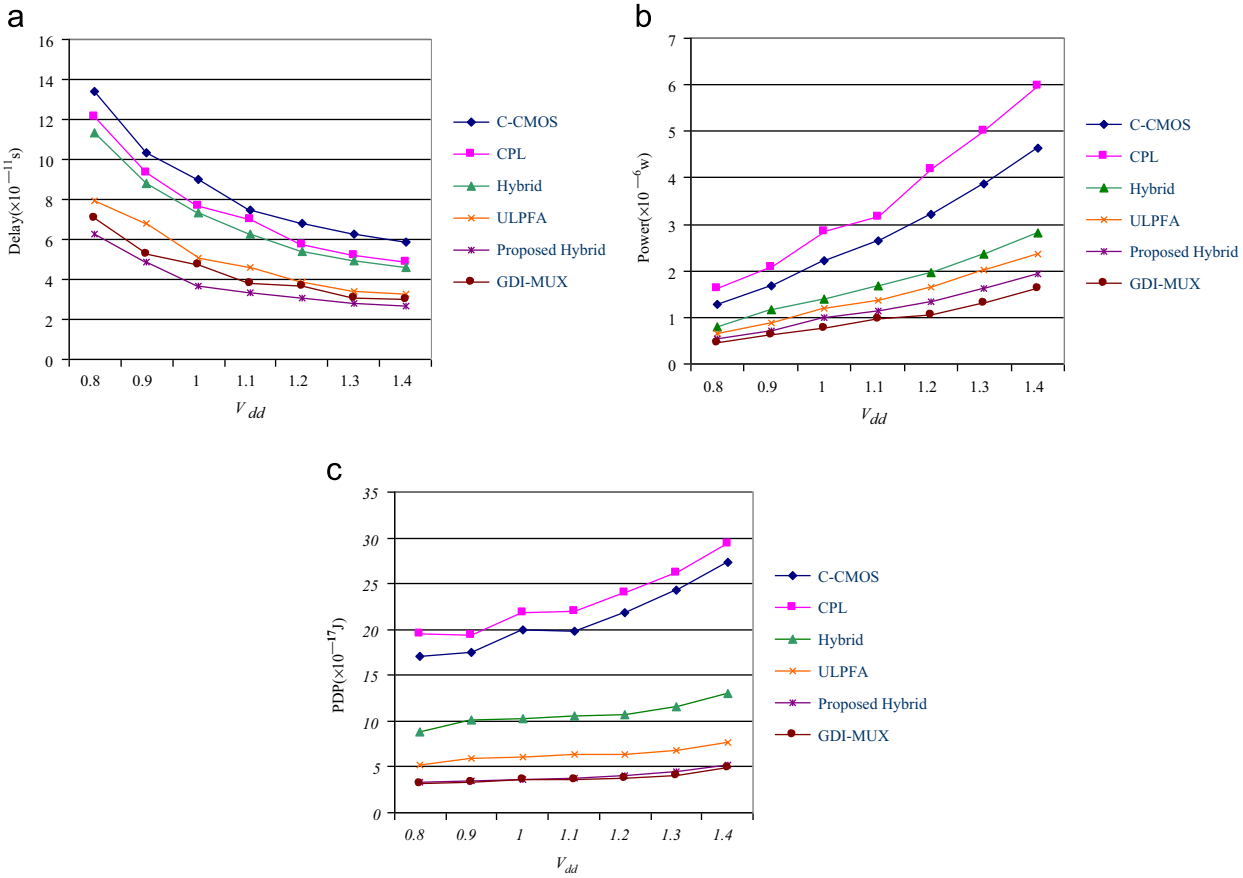

Fig. 15. Power, delay, and PDP results for different supply voltages in 0.13 μm.

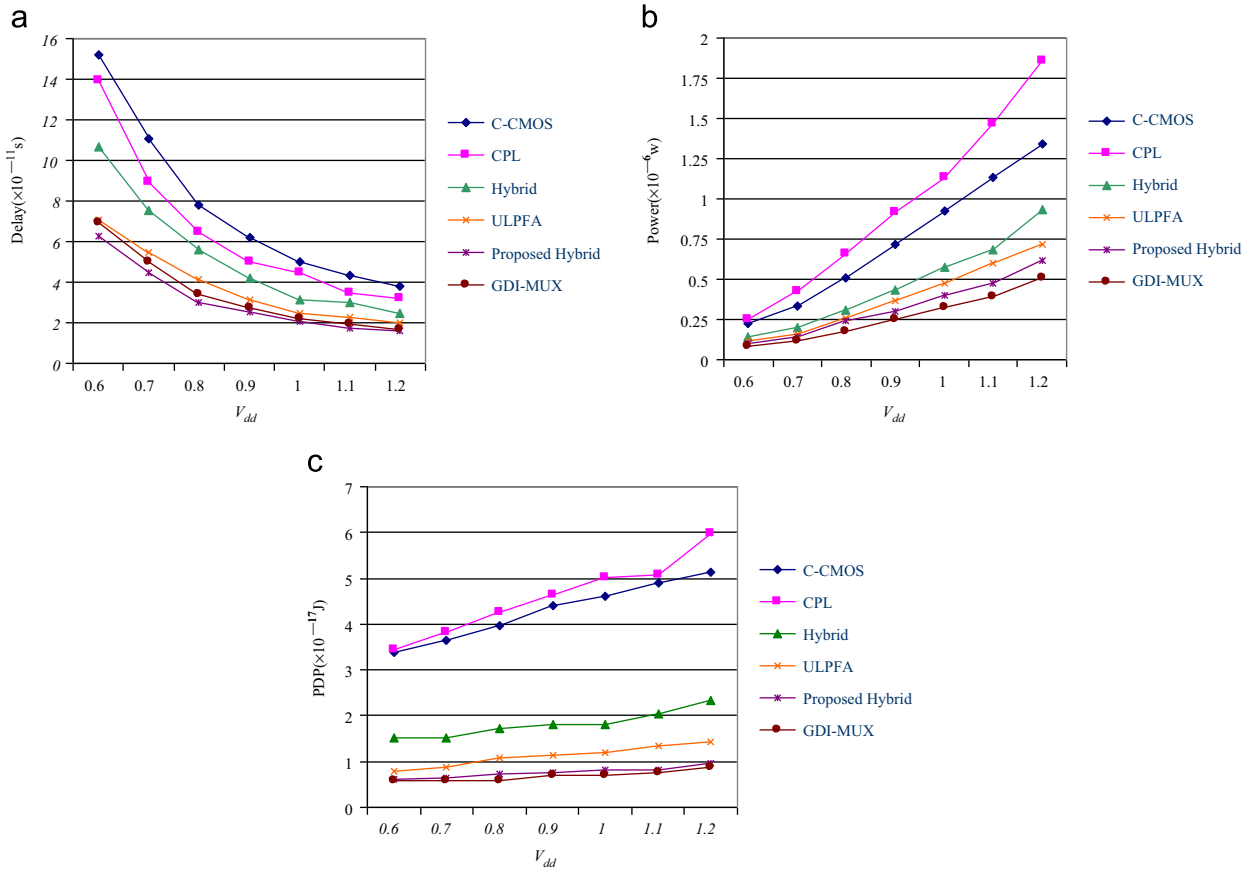

Fig. 16. Power, delay, and PDP results for different supply voltages in 90 nm.

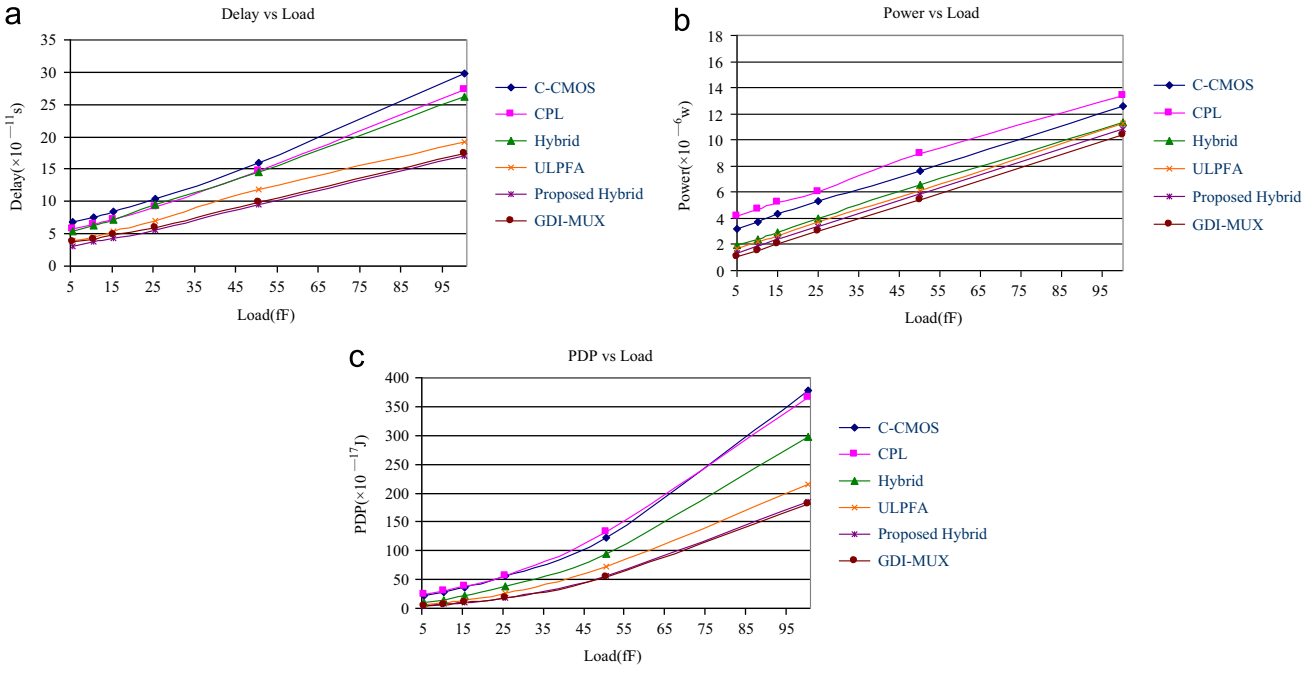

Fig. 17. Power, delay, and PDP results under different load conditions 0.13 μm.

noise immunity and delay that result in step voltage in output. It is notable that GDI-MUX full adder uses 20 transistors in its structure and because of its low transistor count in comparison with its counterparts; our proposed GDI-MUX full adder has low switching capacitance and low dynamic power dissipation. The proposed Hybrid full adder cell follows GDI-MUX full adder in outperforming the other four full adder cells in power consumption. The proposed Hybrid full adder cell consumes low static power due to removal of any direct path between V_{dd} and the ground by employing NMOSs and PMOSs in a complementary manner. Using

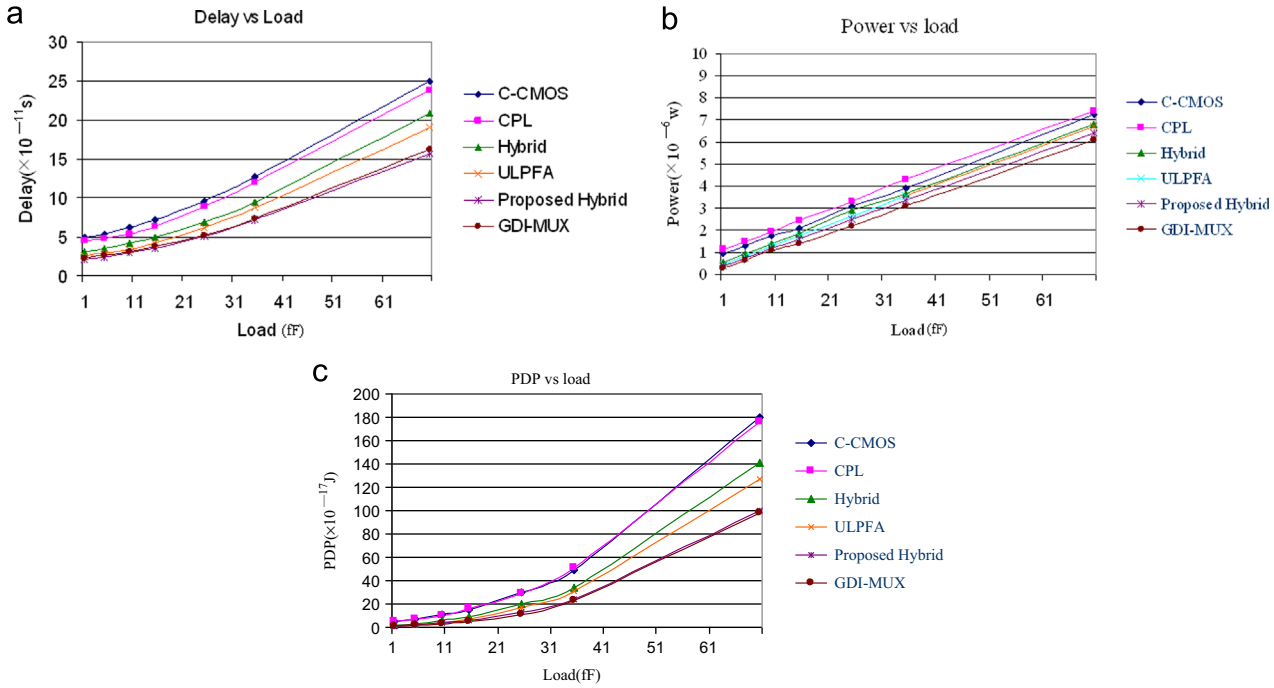

Fig. 18. Power, delay, and PDP results under different load conditions in 90 nm.

Table 4
Simulation results for full adders in 0.13 μM with $f=100$ MHZ and 1.2 V V_{dd}.

Design	Delay ($\times 10^{-11}$ s)	Power ($\times 10^{-6}$ w)	PDP ($\times 10^{-17}$ J)	Device count
C-CMOS	6.7893	3.2199	21.8609	28
CPL	5.7385	4.1831	24.0047	32
Hybrid	5.4134	1.972	10.6752	24
ULPFA	3.861	1.6542	6.3869	24
Proposed hybrid	3.0493	1.3483	4.1114	20
GDI-MUX	3.6724	1.0398	3.8186	20

Table 5
Simulation results for full adders in 90 NM with $f=100$ MHZ and 1 V V_{dd}.

Design	Delay ($\times 10^{-11}$ s)	Power ($\times 10^{-6}$ w)	PDP ($\times 10^{-17}$ J)	Device count
C-CMOS	4.9806	0.9256	4.6100	28
CPL	4.4389	1.1317	5.0235	32
Hybrid	3.1634	0.5724	1.8107	24
ULPFA	2.4946	0.4749	1.1847	24
Proposed hybrid	2.0802	0.3964	0.8246	20
GDI-MUX	2.2159	0.3223	0.7142	20

ULPD as level restorer eliminates the need of output buffers which are the main source of static power consumption. Utilizing low transistor count in comparison with its counterparts minimizes the switching capacitance which results in low dynamic power dissipation. The GDI-MUX full adder shows minimum power consumption at all supply voltages when compared to the C-CMOS, CPL, Hybrid full adder of Fig. 1and ULPFA full adders.

4.3. Power-Delay-Product (PDP)

The PDP is a quantitative measure of the efficiency and a compromise between power dissipation and speed. PDP is particularly important when low power operation is needed. The Power-Delay-Product for C-CMOS, CPL, Hybrid full adder in Fig. 1, ULPFA and the two new full adder cells are evaluated under different supply voltages (0.8–1.4 V) and load (5–100 fF) in 0.13 μm and (0.6–1.2 V) and load (1 to 70 fF) in 90 nm and are depicted in Figs. 15–18(c) respectively. Figs. 22 and 23(c) illustrate the values of PDP of the 16-bit adder based on each full adder cells. Tables 4 and 5 illustrate the values at 1.2 V for 0.13 μm and 1 V for 90 nm. As shown the GDI-MUX full adder has the best PDP in comparison with its counterpart.

4.4. Area

Table 6 shows the area of each full adder. The transistors are sized to have best PDP. Fig. 19 shows exact layout of the proposed Hybrid and GDI-MUX full adder in PD SOI CMOS. Among the mentioned full adders, the CPL has the highest area. This is because of irregular structure of the CPL adder and high number of transistors which results in an irregular layout and increased layout complexity. The static-CMOS full adder has less number of transistors as compared to the CPL adder and occupies lesser area because of its regular structure.

Hybrid full adder in Fig. 1 and ULPFA are consuming roughly the same area owing to the use of Pass Transistor and static-CMOS Logic styles. Because of their low transistor count in comparison with CPL and static-CMOS logic style, they have lesser area.

Among the mentioned full adders, proposed hybrid full adder and GDI-MUX full adder with 20 transistors have the smallest area. This is Because of the highly symmetric arrangement and low number of transistors of their design.

4.5. Immunity to noise

Noise Immunity Curve (NIC), which is proposed in [27], is used to measure the noise-tolerance performance of the mentioned full adder cells. In particular, noise pulses must have sufficiently high amplitude and long duration to cause unrecoverable logic errors in digital circuits. The NIC is a locus of points (T_n, V_n), where T_n is the noise pulse width and V_n is the noise pulse amplitude, for which the gate just makes a logic error. Since each point on Noise

Immunity Curve (NIC) represents an amplitude V_n and width T_n of the input noise pulse that causes logic errors, all points below the NIC are in a safe zone. Hence, the higher the NIC of a gate, the higher immunity to noise is to gate.

Fig. 20 shows the noise injection circuit [28]. This circuit is capable to provide a noise of the desired width and amplitude in order to create a glitch in the output. The amplitude and the width of the noise pulse are controlled by V_P, and V_t respectively. The NIC is plotted by considering the width of the noise pulse, for a given noise pulse amplitude, that is sufficient to make a glitch in the output. This glitch must be sufficient to cause unrecoverable logic errors in the circuit under test.

The noise immunity curves (NIC) results for the full adders are shown in Fig. 21. All the hybrid designs show good noise immunity as compared to the conventional full adders. The GDI-MUX full adder has the highest noise immunity curves (NIC) followed by the proposed hybrid full adder. After the hybrid adder the ULPFA shows the best noise immunity curves (NIC) in comparison to the others.

For considering another aspect of noise immunity, the values of delay and power consumption for the two proposed and the mentioned adder cells including C-CMOS, CPL Hybrid full adder in Fig. 1 and ULPFA in different temperatures in 0.13 μm with 1.2 V supply voltage are shown in Table 7. Simulation results in Table 4 measured in room temperature around 27 °C but values in Table 7 are in 0 °C and 70 °C with 1.2 V supply voltage. As Table 7 shows lowering temperature decreases the power consumption and speed of circuits but any increase in temperature enlarges these parameters. It is also obvious from Table 7 that the new design can perform reliable in these temperatures and increasing or

Table 6
Area comparison of the full-adders.

Design	C-CMOS	CPL	Hybrid	ULPFA	Proposed hybrid	GDI-MUX
Length (μm)	12.20	9.34	10.23	9.95	9.67	9.18
Width (μm)	10.45	18.32	10.45	10.62	9.23	10.23
Area (μm^2)	127.49	171.1	106.9	105.66	89.25	93.91

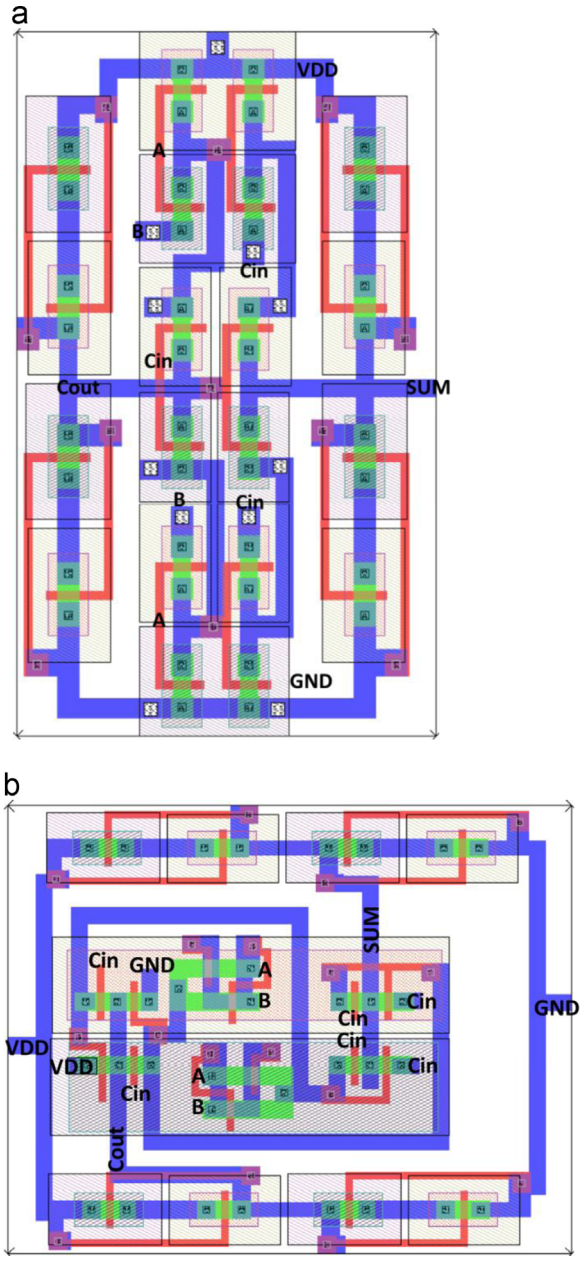

Fig. 19. (a) GDI-MUX full adder layout and (b) proposed hybrid full adder layout.

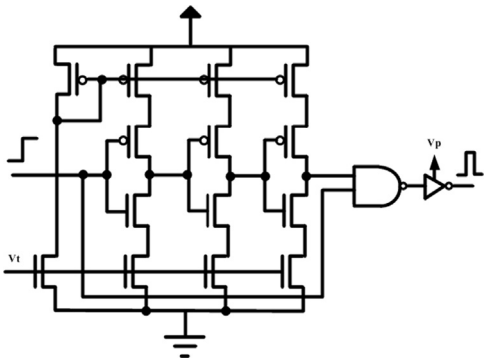

Fig. 20. Noise injection circuit.

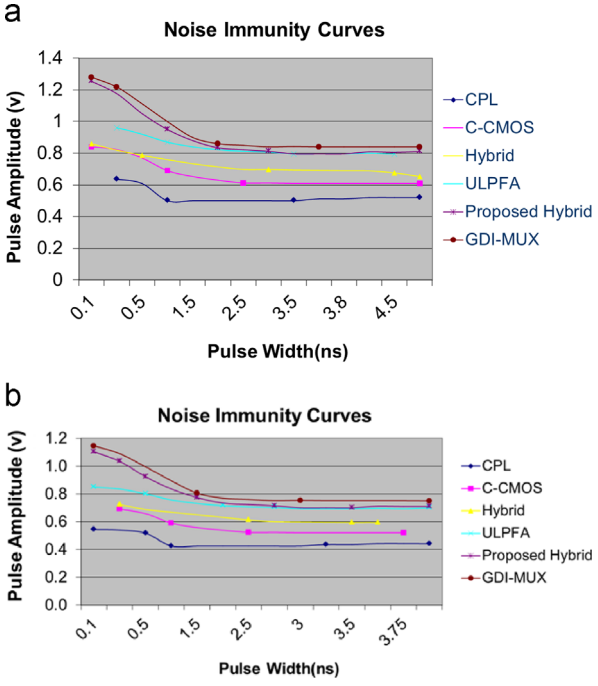

Fig. 21. Noise Immunity Curves (NIC) for the full adders in (a) 0.13 μm and (b) 90 nm technology.

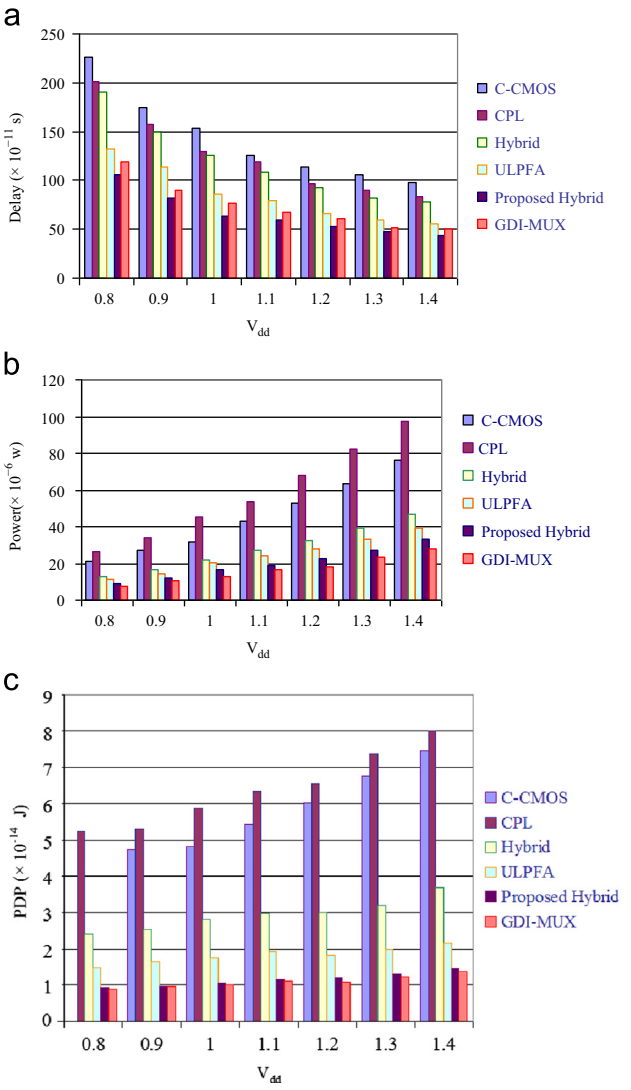

Fig. 22. Power, delay, and PDP results for different supply voltages in 0.13 μm for 16-bit adder.

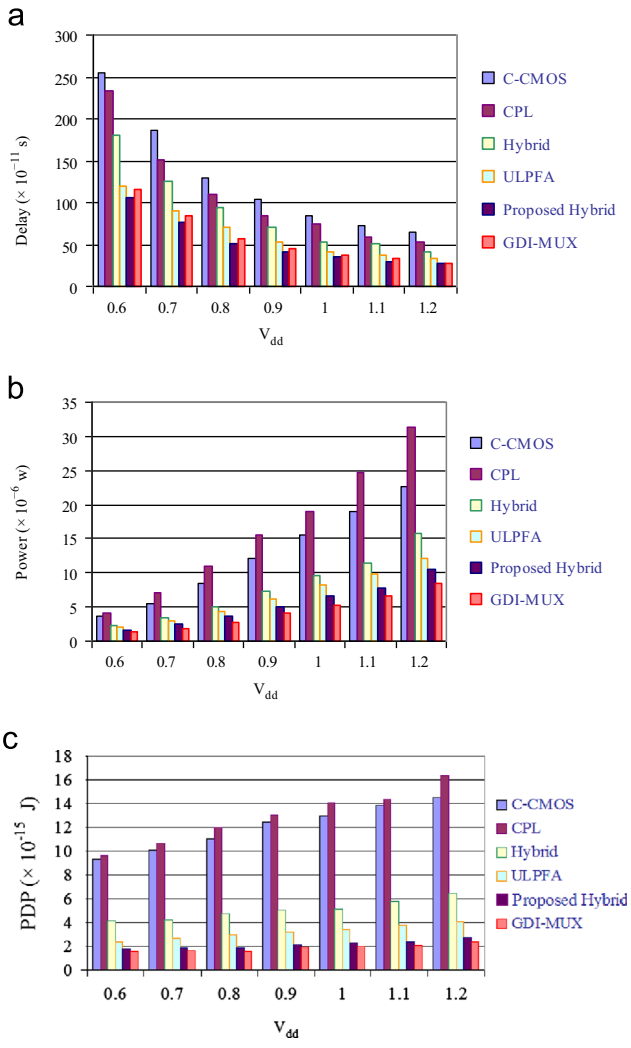

Fig. 23. Power, delay, and PDP results under different load conditions in 90 nm for 16-bit adder

decreasing of delay and power consumption in 0 and 70 °C toward 27 °C is acceptable.

Another exploited metric is unity noise gain (UNG) [29,30]. It is defined as the amplitude of the input noise that causes a glitch with the same amplitude at the output node. Identical noise pulses are applied to all inputs and the amplitude of the noise at the outputs are measured. The effective noise depends on both the amplitude and duration of the noise pulse. The input noise level can be increased by increasing either the noise pulse duration or amplitude. In our experiment, we change the input noise level by changing its amplitude. Tables 8 and 9 illustrate the unity noise gain (UNG) at 1.2 V for 0.13 μm and 1 V for 90 nm.

Table 7
Values of delay and power consumption in different temperatures in 0.13 μM technology.

Design	Temp. (0 °C)		Temp. (70 °C)	
	Delay ($\times 10^{-11}$ s)	Power ($\times 10^{-6}$ w)	Delay ($\times 10^{-11}$ s)	Power ($\times 10^{-6}$ w)
C-CMOS	6.8321	3.1947	6.7311	3.2318
CPL	5.8342	4.1211	5.7097	4.153
Hybrid	5.4145	1.914	5.3248	1.9412
ULPFA	3.961	1.6249	3.7864	1.6981
Proposed hybrid	3.1274	1.3266	2.913	1.3506
GDI-MUX	3.7349	1.0196	3.4914	1.0477

5. Conclusion

In this paper two novel full adder cells using GDI (Gate-Diffusion Input) structure and hybrid CMOS logic style for Low-Power application are proposed. These two new designs successfully operate at low voltages with tremendous signal integrity and driving capability. The circuits being studied are optimized for energy efficiency at 0.13 μm and 90 nm PD SOI CMOS process technology. Simulations have been performed on HSPICE to evaluate the new designs as well as four other adders, including C-CMOS, CPL, Hybrid full adder in Fig. 1 and ULPFA. A broad comparison to the state of the art designs cited in the VLSI literature illustrates a significant improvement in terms of power dissipation and Power-Delay product (PDP) parameter. The number of transistors used is significantly reduced resulting in a great reduction in switching activity and area. This considerable reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

Table 8
Unity noise gain (V) in 0.13 μM technology for $V_{dd}=1.2$ V.

Design	Unity noise gain
C-CMOS	1.0258
CPL	0.9804
Hybrid	1.0012
ULPFA	1.1252
Proposed hybrid	1.1549
GDI-MUX	1.1732

Table 9
Unity noise gain (V) in 90 nm technology for $V_{dd}=1$ V.

Design	Unity noise gain
C-CMOS	0.8491
CPL	0.817
Hybrid	0.8242
ULPFA	0.9313
Proposed hybrid	0.9595
GDI-MUX	0.9769

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