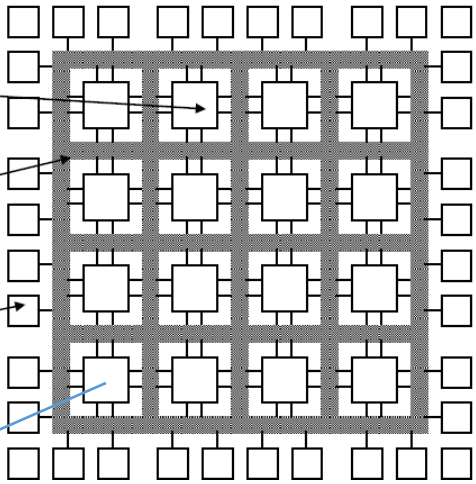
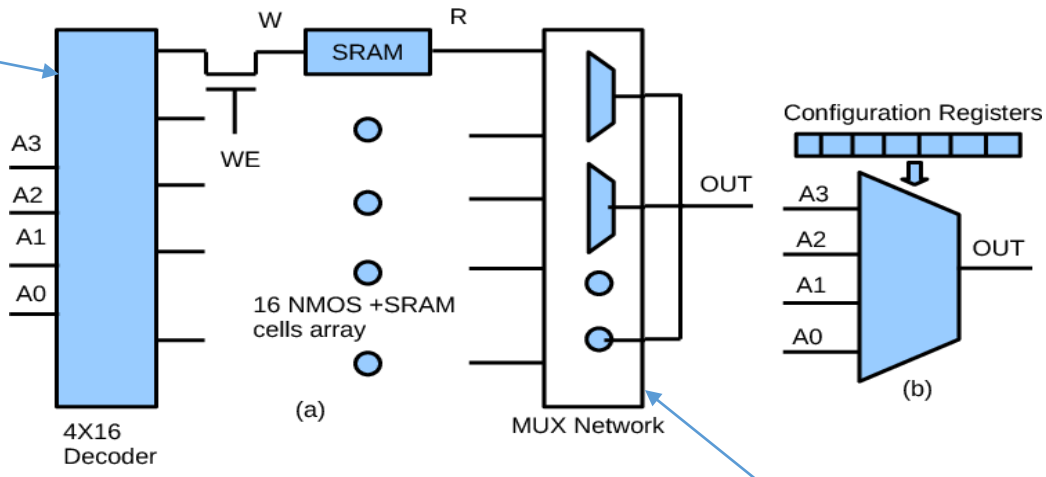
- **Logic blocks**
  - To implement combinational and sequential logic
- **Interconnect**
  - Wires to connect inputs and outputs to logic blocks
- **I/O blocks**
  - Special logic blocks at periphery of device for external connections



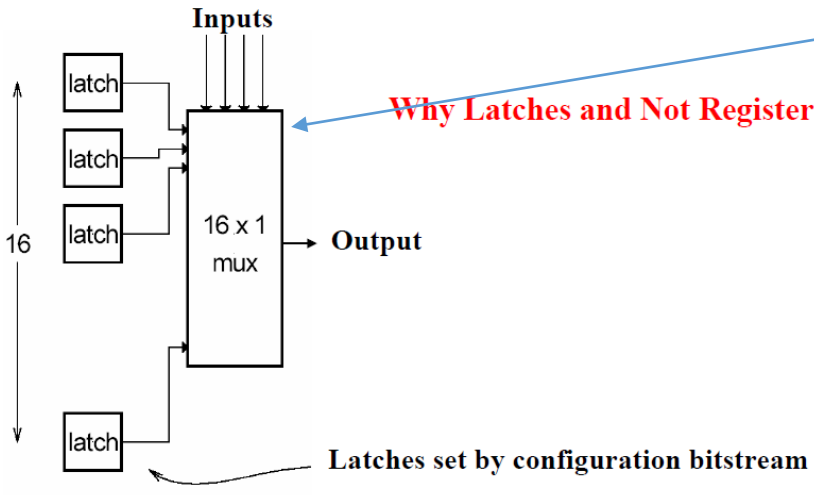
FPGA Resources

Decoder for configuring the SRAM



CLB Design

MUX used during computation; accessing the RAM



Why Latches and Not Registers?