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To understand the operation of the folded cascode OTA, this last has a differential stage consisting of NMOS transistors  $M_9$  and  $M_{10}$ . Mosfets  $M_{11}$  and  $M_{12}$  provide the DC bias voltages to  $M_1$ - $M_2$ - $M_7$ - $M_8$  transistors. The open-loop voltage gain and gain bandwidth are given by (1) and (2) below:

$$A_v = \frac{g_{m9} \cdot g_{m6} \cdot g_{m4}}{I_D^2 (g_{m4} \lambda_N^2 + g_{m6} \lambda_P^2)} \quad (1)$$

$$GBW = \frac{g_{m9}}{I_D} \cdot \frac{I_D}{C_L} \quad (2)$$

Where,  $g_{m4}$ ,  $g_{m6}$  and  $g_{m9}$  are respectively the transconductances of transistors  $M_4$ ,  $M_6$  and  $M_9$ .  $I_D$  is the bias current flowing in Mosfets  $M_4$ ,  $M_6$ , and  $M_9$ .  $C_L$  is the capacitance at the output node,  $\lambda_N$  and  $\lambda_P$  are the parameters related to channel length modulation respectively for NMOS and PMOS devices. Taking into account the complementarity between the transistors  $M_4$  and  $M_6$ :

$$g_{m4} = g_{m6} \quad (3)$$

The gain expression becomes:

$$A_v = \frac{g_{m9} \cdot g_{m6}}{I_D^2 (\lambda_N^2 + \lambda_P^2)} \quad (4)$$

### III. FOLDED CASCODE OTA DESIGN

The op-amp is characterized by various performances like open-loop voltage gain, unity-gain bandwidth, slew rate, noise and so on. These performances measures are fixed by the design parameters, e.g., transistor sizing, bias currents, and other component values [26].

The aim of this work is to determine values of the design parameters that optimize an objective feature whereas satisfying specifications or constraints. In this paper, we introduce the design of the folded cascode OTA amplifier in the three regions of operation. This design applies a synthesis procedure based on the  $g_m/I_D$  methodology introduced by Flandre and Silveira [27].

#### A Sizing Algorithm

The formulation of a design flow clarifies a top-down synthesis methodology for CMOS OTA architectures (Fig.2) [28]. In fact, this last starts by fixing the specifications to optimize for example: gain and unity gain frequency in order to determine the unknowns that are MOS device sizes and bias current:

- Equation (2) directly yields  $g_{m9}$  from the given transition frequency and capacitive load, whereas  $g_{m9}/I_D$  is derived from the specified DC open-loop gain and the chosen technology using equation (4).
- $g_{m9}$  and  $g_{m9}/I_D$  yield the bias current  $I_D$  and furthermore  $g_{m9}/I_D$  gives  $I'$  where  $I' = I_D/(W/L)_9$ .
- $W/L$  is finally given by  $I_D/I'$ .

The universal  $g_m/I_D$  as a function of  $I_D/(W/L)$  characteristic of the CMOS technology under consideration ( $0.35\mu\text{m}$  of AMS) is exploited in order to apply the method quoted previously and compute the design parameters (Fig.3). This characteristic is obtained by simulation and defined in the

three regions of operation of transistor.

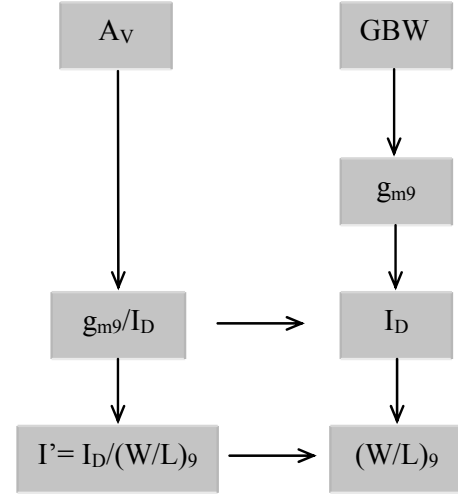


Fig.2 Design flow

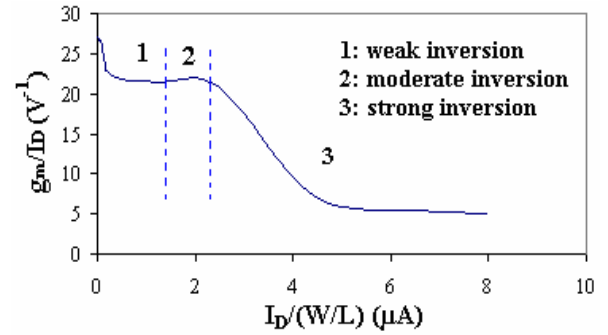


Fig.3  $g_m/I_D$  as a function of  $I_D/(W/L)$

#### B. Weak Inversion Region

The operating range of transistors can be entirely exploited: weak, moderate or strong inversion, linear or saturated mode, quasi-static or high-frequency operation [30].

The transistors are traditionally biased in the saturation mode in analogue circuits. But, they can be operated in strong inversion or weak inversion. Transistors biasing in weak inversion provide higher transconductance and supply a larger gain with a smaller current. These transistors present a low thermal noise. In our design, we will study the folded cascode OTA behaviour in the three regions of operation.

#### C. Design in Weak Inversion

As shown in Fig.4, we note that weak inversion presents higher  $g_m/I_D$  values with smaller current, so an increased gain is favorable for this operating mode.

We set specifications to the circuit of Fig.1 presented by table I.

TABLE I  
SPECIFICATIONS

Specifications	Values
$A_v$ (dB)	105
GBW (MHz)	21.5
$C_L$ (fF)	10
$V_{dd}/V_{ss}$ (V)	$\pm 1$
Channel length ( $\mu\text{m}$ )	1

After applying the design strategy clarified previously, we obtain the parameters computed and summarized in table II.

TABLE II  
DESIGN PARAMETERS IN WEAK INVERSION

Parameters	Values
$I_D$ (nA)	50
$W_{9,10}$ ( $\mu\text{m}$ )	3.5
$W_{3,4}$ ( $\mu\text{m}$ )	2.7
$W_{5,6,7,8}$ ( $\mu\text{m}$ )	1
$W_{1,2,12}$ ( $\mu\text{m}$ )	5.4
$W_{11}$ ( $\mu\text{m}$ )	2
$V_1 = V_2$ (mV)	-428

The designed folded cascode OTA is biased at  $\pm 1\text{V}$  power supply voltage using CMOS technology of  $0.35\text{ }\mu\text{m}$  of AMS with the BSIM3V3 MOSFET model. The circuit denotes an offset voltage of  $0.4\text{mV}$ , a Slew Rate of  $3.3\text{V}/\mu\text{s}$ , a wide input common-mode range of  $[-0.99\text{V}, 0.98\text{V}]$ , a wide output common-mode range between  $-0.96\text{V}$  and  $0.95\text{V}$ . It consumes  $0.6\mu\text{W}$ .

Moreover, our device is able to achieve a degrading gain of  $75.5\text{dB}$ , a bandwidth of  $19.14\text{MHz}$  with phase margin of  $67^\circ$  (Fig.4), a good common mode rejection ratio of  $126.8\text{dB}$  and a low transconductance of  $1.8\mu\text{S}$  kept constant for a wide range of frequency (Fig.5).

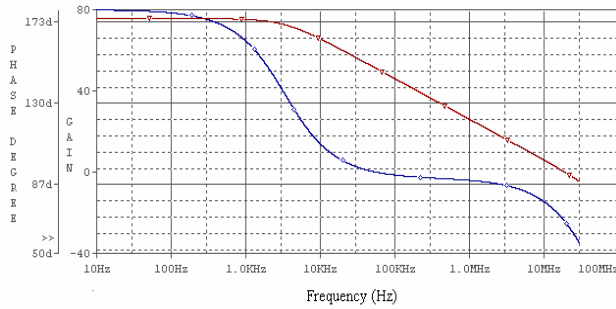


Fig.4 Gain and phase curve

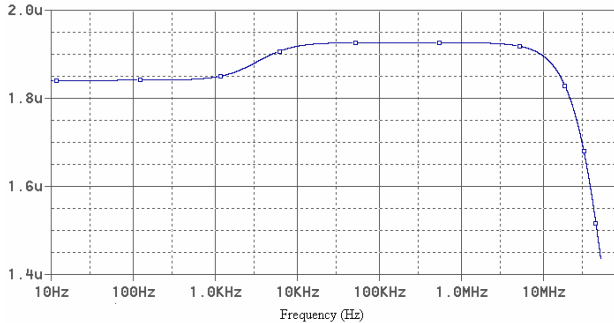


Fig.5 OTA's transconductance in weak inversion region

#### D. Design in Moderate Inversion

In weak inversion, we succeed in reaching good performances with very low consumption; hence, the gain bandwidth product isn't raised and necessary enough to satisfy wide band applications.

In order to improve this parameter, relatively with the same lower consumption, we will study the design of the OTA in moderate inversion region. Thus, we propose specifications illustrated by table III that put more constraints on OTA gain bandwidth product.

TABLE III  
SPECIFICATIONS

Specifications	Values
$A_v$ (dB)	100
GBW (MHz)	70
$C_L$ (pF)	0.1
$V_{dd}/V_{ss}$ (V)	$\pm 2$
Channel length ( $\mu\text{m}$ )	1

Likewise, the design strategy described in section A is adopted keeping small signals model invariant in different operation's regions of transistor. The design parameters found are collected in table IV. The voltages  $V_1$  and  $V_2$  are well fixed at  $-256\text{mV}$ .

TABLE IV  
DESIGN PARAMETERS IN MODERATE INVERSION

Parameters	Values
$I_D$ ( $\mu\text{A}$ )	2
$W_{9,10}$ ( $\mu\text{m}$ )	9
$W_{3,4}$ ( $\mu\text{m}$ )	2.7
$W_{5,6,7,8}$ ( $\mu\text{m}$ )	1
$W_{1,2,12}$ ( $\mu\text{m}$ )	5.4
$W_{11}$ ( $\mu\text{m}$ )	2
$V_1 = V_2$ (mV)	-256

The OTA circuit can reach a DC gain of  $92\text{dB}$ , a unity-gain frequency of  $69\text{MHz}$  with phase margin of  $74.5^\circ$  (Fig.6). Its transconductance is about  $65\mu\text{S}$  (Fig.7). It dissipates  $48\mu\text{W}$ .

In this behaviour mode, the gain and GBW characteristics are interesting, also a wide input and output swings are maintained.

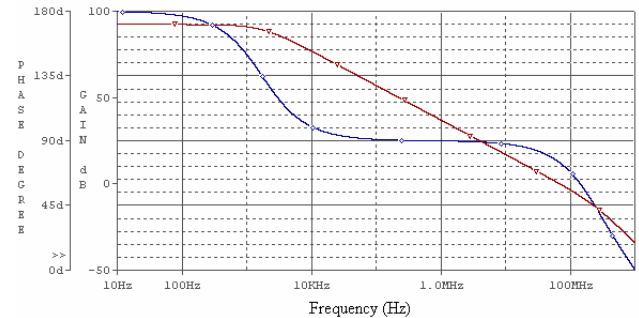


Fig.6 Gain and phase curve

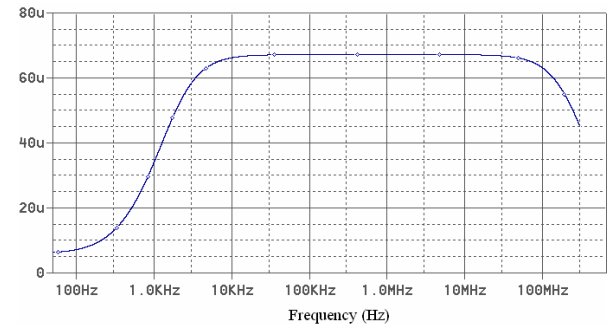


Fig.7 OTA's transconductance in moderate inversion region

#### E. Design in Strong Inversion

In weak inversion and for bias current relatively considerable, we estimate reaching bandwidths satisfying wide band applications requirements.

We remark that  $g_m/I_D$  ratio decreased as a function of current in this region of operation. Then, we fixed

specifications given by table V.

TABLE V SPECIFICATIONS	
Caractéristiques	Valeurs
$A_v$ (dB)	80
GBW (MHz)	450
$C_L$ (pF)	0.1
$V_{dd}/V_{ss}$ (V)	$\pm 2$
Channel length ( $\mu\text{m}$ )	1

The Mosfets sizes are computed as a result of the design flow (table VI). We conclude that the sizes found in strong inversion are more important than those obtained in weak and moderate inversion; this can be explained by the use of high current towards other regions.

TABLE VI DESIGN PARAMETERS IN STRONG INVERSION	
Parameters	Values
$I_D$ ( $\mu\text{A}$ )	27.5
$W_{9,10}$ ( $\mu\text{m}$ )	14
$W_{3,4}$ ( $\mu\text{m}$ )	5.4
$W_{5,6,7,8}$ ( $\mu\text{m}$ )	2
$W_{1,2,12}$ ( $\mu\text{m}$ )	10.8
$W_{11}$ ( $\mu\text{m}$ )	4
$V_1 = V_2$ (mV)	-318

The folded cascode OTA has a gain of 77.5dB, a large unity-gain frequency of 430MHz and a phase margin of 58.2degrees. Its transconductance is about 396 $\mu\text{S}$  (Fig.8).

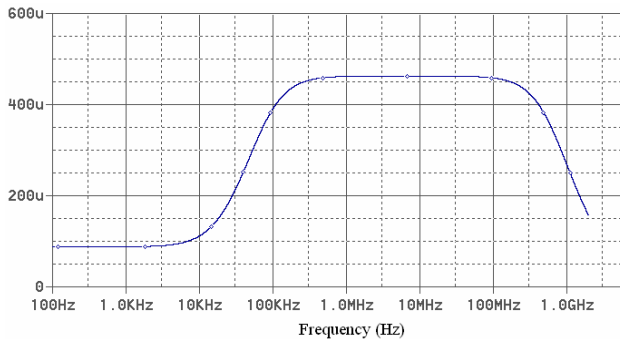


Fig.8 OTA's transconductance in strong inversion region

Several characteristics were depicted in folded cascode OTA designing step (table.VII). This topology works in various frequency ranges. According to the application and its constraints, we choose the mode of operation of transistors.

#### IV. DESIGN WINDOW

To verify some design parameters namely unity gain frequency and drain source current, we try to present a design window in different regions of operation that yields a different couple of ( $F_t$ ,  $I_D$ ) values, using MATLAB tool.

As illustrated in Fig.9 and Fig.10, in strong inversion, a drain current of 27.5 $\mu\text{A}$  leads to a unity-gain frequency of 460MHz. In moderate inversion, for a current fixed at 2 $\mu\text{A}$ , GBW value is around 90MHz.

We notice that unity gain frequency increases in moderate inversion region, so we have to take the change of small signals model in moderate inversion into account.

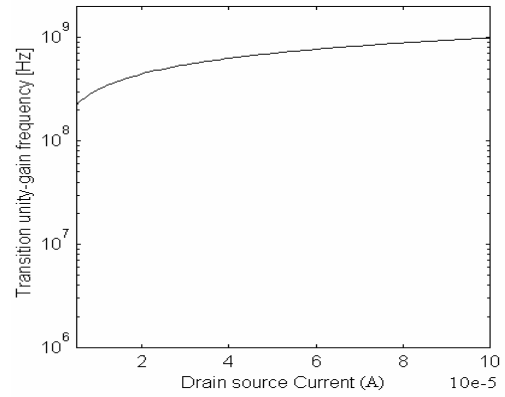


Fig.9 Unity gain frequency as a function of drain source current in strong inversion region

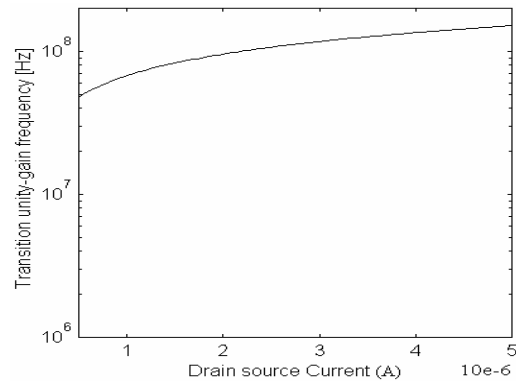


Fig.10 Unity gain frequency as a function of drain source current in moderate inversion region

#### V. COMPARISON OF RESULTS

After discussing the different parameters of OTA design we can evaluate our study toward other works. The performance of the folded cascode OTA from this work has been compared to two recent OTA circuits design. The first is a Class-AB OTA [29]. The second was a telescopic OTA architecture presented in [30]. This comparison is given in table VIII. It is clearly seen that with folded cascode OTA architecture, we reach low power low voltage topology with high static gain.

#### VI. CONCLUSIONS

Consequently, the synthesis of high-performance analog integrated circuits constitutes a complex activity requiring the command of many concepts. As a result, the analog designer remains a rare and highly-valued engineer worldwide.

This contribution presents the strategy design of folded cascode OTA in the three operation's modes of transistor: weak inversion, strong inversion and moderate inversion, so, the goal to reach high gain and large bandwidth has been fulfilled.

We estimate that  $g_m/I_D$  methodology is well adopted for sizing in different function modes to reach extremely performances offered by a given technology.

Future work would involve the exploitation of these results on folded cascode OTA for low consumption and wide band applications to use it in wide band analog-to-digital converters.

TABLE VII  
FOLDED CASCODE OTA SPECIFICATIONS

Specifications	Weak inversion	Moderate inversion	Strong inversion
DC Gain (dB)	75.57	92	77.53
GBW (MHz)	19.14	69	430
Transconductance ( $\mu$ S)	1.8	65	396
Phase margin (degrees)	67	74.5	58
Offset voltage ( $\mu$ V)	430.4	246	337
Output swing (V)	[-0.96 ; 0.95]	[-1.94 ; 1.84]	[-1.84 ; 1.72]
Input swing (V)	[-0.99 ; 0.98]	[-1.95 ; 1.87]	[-1.95 ; 1.87]
Slew Rate (V/ $\mu$ s)	3.3	16.5	196
CMRR (dB)	126.8	133	114
PSRR p, n (dB)	18	45.7	46.5
Supply voltage (V)	$\pm 1$	$\pm 2$	$\pm 2$
Bias current ( $\mu$ A)	0.1	4	55
Power consumption ( $\mu$ W)	0.6	48	660

TABLE VIII  
PERFORMANCES COMPARISON

Performance/Design	Yao & Steyaert [29]	Craig Brendan Keogh [30]	This work
OTA Architecture	Class-AB	Telescopic	Folded cascode
Technology ( $\mu$ m)	0.09	0.18	0.35
DC Gain (dB)	50	79	75.57
GBW (MHz)	57	8.5	19.14
Phase margin (degrees)	57	78	67
Supply voltage (V)	1	0.925	1
Power consumption ( $\mu$ W)	80	4.6	0.6

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